PI7C9X440SL

PCI EXPRESS TO USB 2.0 HOST CONTROLLER

DATASHEET

REVISION 3

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1545 Barber Lane Milpitas, CA 95035
Telephone: 408-232-9100
FAX: 408-434-1040
Internet: http://www.diodes.com

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REVISION HISTORY

Date	Revision Number	Description
06/30/09	0.2	Preliminary datasheet
10/20/09	0.3	Added Section 6 EEPROM Interface and System Management Bus Added Section 7 Register Description Updated Table 11-3 DC Electrical Characteristics
06/18/10	0.4	Updated Section 6.1.3 EEPROM Space Address Map and 6.1.4 Mapping EEPROM Contents to Configuration Registers (Offset – C0h Physical Layer Control 3) Updated Section 7.2 PCI Express Configuration Registers (Offset – C0h, C4h, C8h) Added Section 14 Recommended Components
06/23/10	0.5	Updated Section 3 Pin Definition and Section 4 Pin Assignments (VDDCAUX to ADDC, VAUX to VDDR) Updated Figure 12-1 Package outline drawing
08/27/10	0.6	Updated Section 1 Features (Industrial Temperature Range) Updated Section 3.3 USB Interface Signals (OCI and POE pins) Updated Section 3.5 Miscellaneous Signals (NC pins) Updated Section 13 Ordering Information (Industrial Temperature Range) Updated Table 11-1 (Ambient Temperature with power applied)
11/18/10	0.7	Updated Section 3.3 USB Interface Signals (PME_L pin) Updated Section 3.5 Miscellaneous Signals (MAIN_DETECT, GPIO and SMBCLK pins) Corrected Section 4.1 Pin List (Pin 30) Updated Section 6.1.4 Mapping EEPROM Contents to Configuration Registers (24h, 3Eh) Updated Section 7.3.17 Serial Bus Release Number Register and 7.3.18 Miscellaneous Register
12/23/10	0.8	Updated 7.3.10 Base Address Register 0, 7.3.11 Base Address Register 0, 7.3.17 Serial Bus Release Number Register, 7.3.18 Frame Length Adjustment Register, 7.3.19 Port Wake Capability Register, 7.3.22 Power Management Data Register, 7.3.27 Message Signaled Interrupt Capability ID Register, 7.3.29 Message Control Register, 7.3.30 Message Address Register, 7.3.31 Message Data Register, 7.3.40 Device Control Register, 7.3.42 Link Capabilities Register, 7.3.43 Link Control Register
04/29/11	1.0	Updated Table 9-3 JTAG boundary scan register definition Updated 7.3.24 Power Management Data Register (bit 15) Production PI7X9X440SL datasheet revision 1.0 released
06/10/11	1.1	Updated Section 8.2 USB Interface Updated Section 10.1 Express Power States Updated Section 11.3 DC Specification
07/15/11	1.2	Update Section 7.2.46, 7.2.53. 7.2.55. 7.2.57, 7.2.58 and 7.3.40.
11/07/11	1.3	Added Table 8.2 Input Clock Requirements for USB Interface
11/23/11	1.4	Added Table 11-4 DC electrical characteristics for Digital I/O Updated Table 11-7 USB Interface Characteristics
02/13/11	1.5	Updated Section 5.1.1.3 Receiver Equalization Updated Section 5.1.1.6 Driver Amplitude Updated Section 7.2.53 Physical Layer Control 0 - Offset B4h (Upstream Port) Updated Section 7.2.55 Physical Layer Control 0 - Offset B4h (Downstream Port)
08/13/13	1.6	Updated Section 1 Features (Power Dissipation) Updated Section 3.5 Miscellaneous Signals (GPIO) Updated Section 11.2 Power Consumption
09/25/13	1.7	Updated Section 3.6 Power Pins (Added pin 129 to VSS) Updated Section 4.1 Pin Assignments (Added pin 129)
01/05/16	1.8	Updated Section 13 Ordering Information
01/17/17	1.9	Updated Table 11-4 DC Electrical Characteristics for Digital I/O Updated Logo Updated Section 11.1 Absolute Maximum Ratings Added Section 11.2 Operating Ambient Temperature
03/22/17	2.0	Updated Section 3.4 JTAG Boundary Scan Signals Updated Figure 12-1 Package Outline Drawing Updated Section 11.1 Absolute Maximum Ratings Remove Section 14 Recommended Components
01/11/18	3	Revision numbering system changed to whole number Updated Section 13 Ordering Information Added Figure 12-2 Part Marking

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1 Features

General Features

- PCI Express to four USB 2.0 host controller ports
- Strapped pins configurable with optional EEPROM or SMBus
- SMBus interface support
- Low Power Dissipation at 432 mW typical in L0 normal mode
- Industrial Temperature Range -40°C to 85°C
- 128-pin LQFP 14mm x 14mm package

Industrial Compliance

- Compliant with PCI Express Base Specification Revision 1.1
- Compliant with PCI Express CEM Specification Revision 1.1
- Compliant with PCI-to-PCI Bridge Architecture Specification Revision 1.2
- Compliant with Advanced Configuration Power Interface (ACPI) Specification
- Compliant with Universal Serial Bus Specification Revision 2.0 (data rate 1.5/12/480 Mbps)
- Compliant with Open Host Controller Interface Specification for USB Rev 1.0a
- Compliant with Enhanced Host Controller Interface Specification for USB Rev 1.0
- Compliant with System Management (SM) Bus, Version 1.0

PCI Express Interface

- One x1 PCIe 1.1 port
- Advanced Power Saving
    - Link Power Management
    - Supports L0, L0s, L1, L2, L2/L3Ready and L3 link power state
    - Active state power management for L0s and L1 state
    - PME# support in L2 state
    - Device State Power Management
    - Supports D0, D3Hot and D3Cold device power state
    - 3.3V Aux Power support in D3Cold power state
- Supports up to 256-byte maximum payload size
- Programmable driver current and de-emphasis level at the PCIe port
- Reliability, Availability and Serviceability

USB Host Controller

- USB Root Hub with 4 downstream facing ports shared by OHCI and EHCI host controllers
- All USB downstream facing ports are able to handle high-speed (480 Mbps), full-speed (12 Mbps) and low-speed (1.5 Mbps) transactions
- PCI Express to USB bridging through PCI Express multi-functional core of PI7C9X440SL
- Two OHCI host controllers for full-speed and low-speed and one EHCI host controller for high-speed
- Programmable PHY parameters for each USB port
- Operational registers of the USB Host Controller are directly mapped to PCI memory space

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2 GENERAL DESCRIPTION

The PI7C9X440SL PCI Express-to-USB 2.0 Host Controller complies with PCI Express Base Specification Revision 1.1, Open Host Controller Interface Specification Revision 1.0a, and Enhanced Host Controller Interface Specification Revision 1.0. The high-performance architecture of the PI7C9X440SL is capable of bridging from one PCIe x1 upstream port to four USB 2.0 ports. The device allows simultaneous access to multiple USB devices from system host processor, and therefore expands the connectivity domain of the system. The USB ports of the device can support all the available speeds including High-Speed (HS), Full-Speed (FS) and Low-Speed (LS). The PCIe-to-USB2.0 bridge function of the device is implemented by two types of host controllers, the Enhanced Host Controller Interface (EHCI) and Open Host Controller Interface (OHCI). There are one EHCI controller and two OHCI controllers residing in PI7C9X440SL. The EHCI controller handles High-Speed USB transaction while the OHCI controllers handle Full-Speed or Low-Speed USB transaction.

From the perspective of system model, the device contains two cascaded virtual PCI-to-PCI bridges, where the upstream-port bridge sits upon the downstream-port bridge over a virtual PCI Bus, and three USB controllers are attached to the downstream PCI Express port. During enumeration, the internal PCIe upstream and downstream ports are given unique bus numbers, device number and function number that are logically formed as a destination ID. The USB host controllers are viewed as a multi-functional device by the bootstrapping procedures. The EHCI controller is assigned function #2 and the two OHCI controllers are assigned function #0 and #1, and all the controllers are assigned the same device number. The memory-map and IO address ranges are exclusively allocated to each port and USB host controller. After the software enumeration is completed, the transaction packets are routed to the dedicated PCIe port or USB host controller based on the embedded contents of address or destination ID.

For the PCIe-to-USB bridging function, the four USB ports are first served in a host-centric manner by EHCI or OHCI host controllers, which then interface with the PCIe port to transfer packets to/from the upstream port through switch fabric. At High-Speed mode, all the USB ports are handled by ECHI controller with function #2. At Full-Speed and Low-Speed modes, USB port #1 and port #2 are handled by OHCI controller with function #0 and USB port #3 and port #4 are handled by OHCI controller with function #1. The Root Hub resides between the USB ports and host controllers and handles connection sessions from the host controller cores to USB ports.

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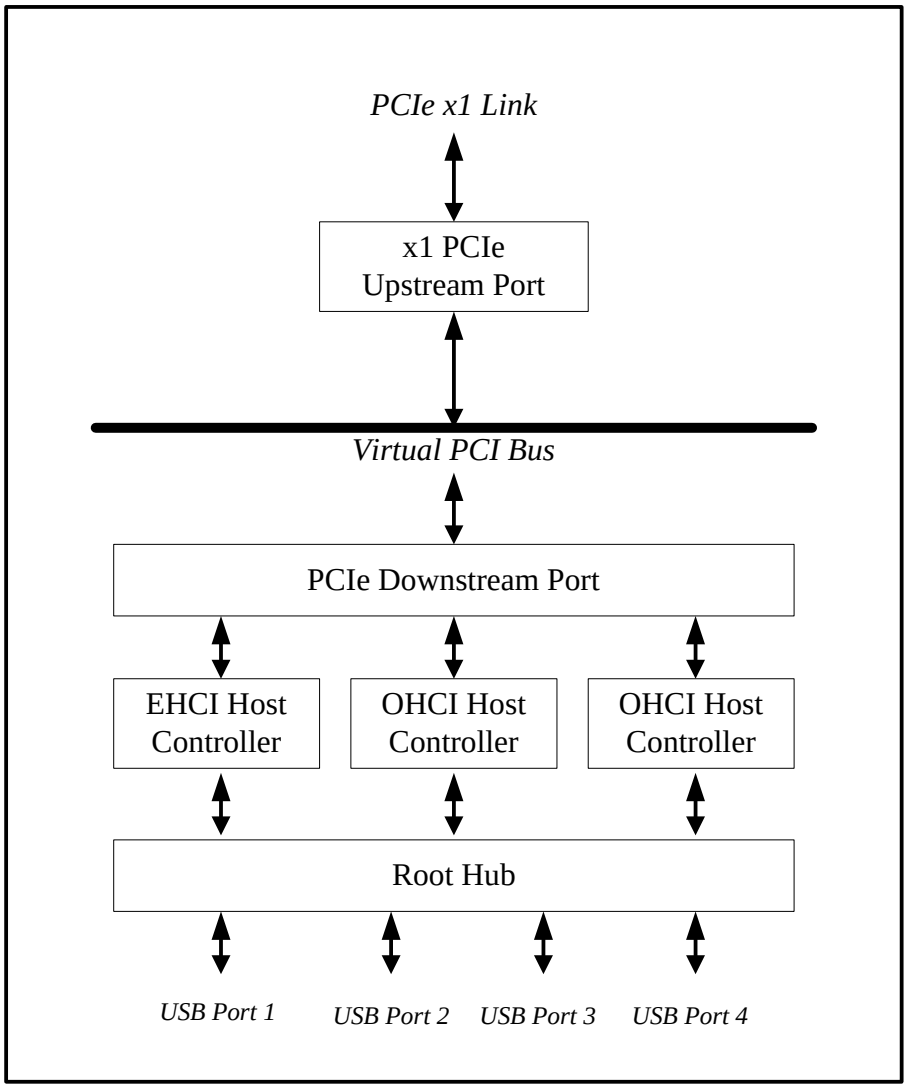

Figure 2-1 PI7C9X440SL Topology

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3 PIN DEFINITION

3.1 SIGNAL TYPES

TYPE OF SIGNAL	DESCRIPTION
I	Input
O	Output
P	Power

"_L" in signal name indicates Active LOW signal

3.2 PCI EXPRESS INTERFACE SIGNALS

NAME	PIN	TYPE	DESCRIPTION
REFCLKP REFCLKN	51, 52	I	**Reference Clock Input Pairs:** Connect to external 100MHz differential clock. The input clock signals must be delivered to the clock buffer cell through an AC-coupled interface so that only the AC information of the clock is received, converted, and buffered. It is recommended that a 0.1uF be used in the AC-coupling.
PERP	37	I	**PCI Express Data Serial Input Pair:** Differential data receive signals.
PERN	38	I	
PETP	41	O	**PCI Express Data Serial Output Pairs:** Differential data transmit signals.
PETN	42	O	
PERST_L	104	I	**System Reset (Active LOW):** When PERST_L is asserted, the internal states of whole chip except sticky logics are initialized.
REXT	57	I	**External Reference Resistor:** Connect an external resistor (1.43K Ohm +/- 1%) to REXT_GND to provide a reference to both the bias currents and impedance calibration circuitry.
REXT_GND	56	I	**External Reference Resistor Ground:** Connect to an external resistor to REXT.

3.3 USB INTERFACE SIGNALS

NAME	PIN	TYPE	DESCRIPTION
DP [4:1]	85, 93, 117, 124	I/O	**USB D+ Signal:** USB D+ analog signal covering HS/FS/LS. DP [x] is correspondent to Portx, where x=1,2,3,4.
DM [4:1]	84, 92, 116, 123	I/O	**USB D- Signal:** USB D- analog signal covering HS/FS/LS. DP [x] is correspondent to Portx, where x=1,2,3,4.
OCI [4:1]	7, 6, 5, 4	I	**Over Current Input (Active LOW):** These signals are asserted low to indicate that an over-current condition has occurred. OCI [x] is correspondent to Portx, where x=1,2,3,4.
POE [4:1]	13, 12, 11, 10	O	**Power Output Enable (Active LOW):** Power supply control output for USB Root Hub Port. When these signals are asserted low, they enable an external power switch to turn on the power supply. POE [x] is correspondent to Portx, where x=1,2,3,4.
RREF[4:1]	87, 95, 119, 126	I/O	**External Resistor Connection for Current Reference:** This analog signal is the connection to the external resistor. It sets the reference current. No external capacitor should be connected. The recommended value for the resistor is 6.04 kohm and accuracy of +/- 1%.
XI	102	I	**Crystal Oscillator Input:** A 12MHz crystal oscillator is required.
XO	103	O	**Crystal Oscillator Output**
PME_L	113	O	**Power Management Event (Low Active):** This signal is asserted whenever the USB power state is resumed to Operational State from Suspend State.
LEG_EMU_EN	20	O	**OHCI Legacy Emulation Enable:** This signal indicates that Legacy emulation support is enabled for the OHCI controller, and the application can read or write to I/O ports 60h/64h when I/O access for the OHCI controller is enabled. See section 5.2.1.1 for details of the Legacy Mode.

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NAME	PIN	TYPE	DESCRIPTION
SMI_O	14	O	**System Management Interrupt:** This signal is used to indicate that an interrupt condition has occurred. The signal is used only when OHCI Legacy support is enabled. See section 5.2.1.1 for details of the Legacy Mode.
IO_HIT_I	3	I	**Application I/O Hit:** This signal indicates a PCI I/O cycle strobe. See section 5.2.1.1 for details of the Legacy Mode.
IRQ1_I	16	I	**External Interrupt 1:** This external keyboard controller interrupt 1 causes an emulation interrupt. See section 5.2.1.1 for details of the Legacy Mode.
IRQ1_O	18	O	**OHCI Legacy IRQ1:** This signal is asserted when an emulation interrupt condition exists and OutputFull, IRQEn, and AuxOutputFull are asserted. See section 5.2.1.1 for details of the Legacy Mode.
IRQ12_I	17	I	**External Interrupt 12:** This external keyboard controller interrupt 12 causes an emulation interrupt. See section 5.2.1.1 for details of the Legacy Mode.
IRQ12_O	19	O	**OHCI Legacy IRQ12:** This signal is asserted when an emulation interrupt condition exists, OutputFull and IRQEn are asserted, and AuxOutputFull is de-asserted. See section 5.2.1.1 for details of the Legacy Mode.

3.4 JTAG BOUNDARY SCAN SIGNALS

NAME	PIN	TYPE	DESCRIPTION
TCK	26	I	**Test Clock:** TCK is the test clock to synchronize the state information and data during boundary scan operation. When JTAG boundary scan function is not implemented, this pin should be left open (NC).
TMS	27	I	**Test Mode Select:** TMS controls the state of the Test Access Port (TAP) controller. When JTAG boundary scan function is not implemented, this pin should be pulled low through a 5.1K pull-down resistor.
TDO	25	O	**Test Data Output:** TDO is the test data output and connects to the end of the JTAG scan chain. When JTAG boundary scan function is not implemented, this pin should be left open (NC).
TDI	28	I	**Test Data Input:** TDI is the test data input and connects to the beginning of the JTAG scan chain. It allows the test instructions and data to be serially shifted into the Test Access Port. When JTAG boundary scan function is not implemented, this pin should be left open (NC).
TRST_L	29	I	**Test Reset (Active LOW):** TRST_L is the test reset to initialize the Test Access Port (TAP) controller. When JTAG boundary scan function is not implemented, this pin should be pulled low through a 5.1K pull-down resistor.

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3.5 MISCELLANEOUS SIGNALS

NAME	PIN	TYPE	DESCRIPTION
EECLK	99	O	**EEPROM Clock:** Clock signal to the EEPROM interface.
EEPD	98	I/O	**EEPROM Data:** Bi-directional serial data interface to and from the EEPROM. The pin is set to 1 by default.
SMBCLK	21	I	**SMBus Clock:** System management Bus Clock.
SMBDATA	64	I/O	**SMBus Data:** Bi-Directional System Management Bus Data.
SCAN_EN	15	I/O	**Full-Scan Enable Control:** For normal operation, SCAN_EN is an output with a value of "0". SCAN_EN becomes an input during manufacturing testing.
GPIO[7:0]	76, 75, 74, 73, 72, 71, 70, 69	I/O	**General Purpose input and output:** These eight general-purpose pins are programmed as either input-only or bi-directional pins by writing the GPIO output enable control register.
MAIN_DETECT	24	I	**Main Power Detect:** MAIN_DETECT should be tied to the Aux Power of the system through a 4.7K ohm pull-up resistor if the USB remote wakeup function is to be supported. Otherwise, this signal should be tied to the Main Power of the system through a 4.7K ohm pull-up resistor.
TEST1/3/4/5/6	1, 65, 77, 114, 66	I	**Test Pins:** For testing purposes only. TEST1 and TEST4 should be tied to ground, and TEST3, TEST5, and TEST6 should be tied to high for normal operation. The suggested value for the pull-up and pull-down resistor is 5.1K.
NC	2, 30, 31, 32, 43, 44, 47, 48, 55, 58, 59, 62, 63, 78, 79, 80, 88, 107, 108		**Not Connected:** These pins can be left floating.

3.6 POWER PINS

NAME	PIN	TYPE	DESCRIPTION
VDDC	22, 35, 81, 100, 109, 111	P	**VDDC Supply (1.0V):** Used as digital core power pins.
VDDR	8, 33, 67, 105, 112	P	**VDDR Supply (3.3V):** Used as digital I/O power pins.
VDDA	83, 90, 91, 97, 115, 121, 122, 128	P	**VDDA Supply (3.3V):** Used as USB analog power pins.
AVDD	40, 46, 49, 60,	P	**AVDD Supply (1.0V):** Used as PCI Express analog power pins.
AVDDH	54	P	**AVDDH Supply (3.3V):** Used as PCI Express analog high voltage power pins.
VSS	9, 23, 34, 36, 39, 45, 50, 53, 61, 68, 82, 86, 89, 94, 96, 101, 106, 110, 118, 120, 125, 127, 129	P	**VSS Ground:** Used as ground pins. **GND:** The central thermal pad underneath the package should be connected to ground.

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4 PIN ASSIGNMENTS

4.1 PIN LIST of 128-PIN LQFP

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	TEST1	33	VDDR	65	TEST3	97	VDDA
2	NC	34	VSS	66	TEST6	98	EEPD
3	IO_HIT_I	35	VDDC	67	VDDR	99	EECLK
4	OCI[1]	36	VSS	68	VSS	100	VDDC
5	OCI[2]	37	PERP	69	GPIO[0]	101	VSS
6	OCI[3]	38	PERN	70	GPIO[1]	102	XI
7	OCI[4]	39	VSS	71	GPIO[2]	103	XO
8	VDDR	40	AVDD	72	GPIO[3]	104	PERST_L
9	VSS	41	PETP	73	GPIO[4]	105	VDDR
10	POE[1]	42	PETN	74	GPIO[5]	106	VSS
11	POE[2]	43	NC	75	GPIO[6]	107	NC
12	POE[3]	44	NC	76	GPIO[7]	108	NC
13	POE[4]	45	VSS	77	TEST4	109	VDDC
14	SMI_O	46	AVDD	78	NC	110	VSS
15	SCAN_EN	47	NC	79	NC	111	VDDC
16	IRQ1_I	48	NC	80	NC	112	VDDR
17	IRQ12_I	49	AVDD	81	VDDC	113	PME_L
18	IRQ1_O	50	VSS	82	VSS	114	TEST5
19	IRQ12_O	51	REFCLKP	83	VDDA	115	VDDA
20	LEG_EMU_EN	52	REFCLKN	84	DM[4]	116	DM[2]
21	SMBCLK	53	VSS	85	DP[4]	117	DP[2]
22	VDDC	54	AVDDH	86	VSS	118	VSS
23	VSS	55	NC	87	RREF[4]	119	RREF[2]
24	MAIN_DETECT	56	REXT_GND	88	NC	120	VSS
25	TDO	57	REXT	89	VSS	121	VDDA
26	TCK	58	NC	90	VDDA	122	VDDA
27	TMS	59	NC	91	VDDA	123	DM[1]
28	TDI	60	AVDD	92	DM[3]	124	DP[1]
29	TRST_L	61	VSS	93	DP[3]	125	VSS
30	NC	62	NC	94	VSS	126	RREF[1]
31	NC	63	NC	95	RREF[3]	127	VSS
32	NC	64	SMBDATA	96	VSS	128	VDDA
						129	E_PAD

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5 FUNCTIONAL DESCRIPTION

The PCI Express-to-USB Bridge contains two virtual PCI-to-PCI Bridges (VPPB) connected by a virtual PCI bus. One of the VPPB is implemented as the upstream port, and the other VPPB is implemented as the downstream port to connect to the USB Host Controllers (OHCI and EHCI). The upstream PCIe port encompasses complete PCIe architecture with the physical, data link, and transaction layers. One VPPB represents a single PCIe Port, which handles the transmission and reception of PCIe packets. The USB Host Controller is able to handle operational registers and descriptor link list, which provide a communication channel for Host Controller Driver (HCD) to initiate USB packet transactions to and from USB devices.

The operation of the PCIe to USB bridging functions are depicted as follows. The HCD first prepares the data structure of the USB commands or data. Then, the host controllers are notified to fetch the commands or data, which are eventually converted from PCIe into USB packet format. Depending on the direction of transfer, the host controller moves and converts the packet to/from USB devices. When the transfer is complete, an interrupt message will notify the HCD to process the data stored in the system memory the descriptor points to.

5.1 PCI EXPRESS INTERFACE FUNCTIONALITIES

5.1.1 PHYSICAL LAYER CIRCUIT

The physical layer circuit design is based on the **P**HY **I**nterface for **P**CI **E**xpress Architecture (PIPE). It contains Physical Media Attachment (PMA) and Physical Coding Sub-layer (PCS) blocks. PMA includes Serializer/ Deserializer (SERDES), PLL[1], Clock Recovery module, receiver detection circuits, beacon transmitter, electrical idle detector, and input/output buffers. PCS consists of framer, 8B/10B encoder/decoder, receiver elastic buffer, and PIPE PHY control/status circuitries. To provide the flexibility for port configuration, each lane has its own control and status signals for MAC to access individually. In addition, a pair of PRBS generator and checker is included for PHY built-in self test. The main functions of physical layer circuits include the conversion between serial-link and parallel bus, provision of clock source for the interface, resolving clock difference in receiver end, and detection of physical layer errors.

In order to meet the needs of different application, the drive amplitude, de-emphasis and equalization of each transmitting channels can be adjusted using EEPROM individually. De-emphasis of -3.5 db is implemented by the transmitters when full swing signaling is used, while an offset can be individually applied to each channel.

[1] Multiple lanes could share the PLL.

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5.1.1.1 RECEIVER DETECTION

The physical layer circuits implement receiver detection, which detects the presence of an attached 50 ohm to ground termination as per PCI Express Specification. The detect circuits determine if the voltage levels of the receiver have crossed the internal threshold after a configurable time determined by the Receiver Detection Threshold field in the Physical Layer Control Register 2 (offset BCh, bit[6:4]) as listed in Table 5-1.

Table 5-1 Receiver Detection Threshold Settings

Receiver Detection Threshold	Threshold
000	1.0 us
001	2.0 us
010	4.0 us (Recommended)
011	5.0 us
100	7.0 us
101	Reserved
110	Reserved
111	Reserved

5.1.1.2 RECEIVER SIGNAL DETECTION

Receiver signal idling is detected with levels above a programmable threshold specified by Receiver Signal Detect field in the Physical Layer Control Register 2 (Offset BCh, bit[22:21]) as listed in Table 5-2, and can be configured on a per-port basis via EEPROM settings.

Table 5-2 Receiver Signal Detect Threshold

Receiver Signal Detect	Min (mV ppd)	Max (mV ppd)
00	50	150
01 (Recommended)	65	175
10	75	200
11	120	240

5.1.1.3 RECEIVER EQUALIZATION

The receiver implements programmable equalizer via the Receiver Equalization field in the Physical Layer Control Register 2 (Offset BCh, bit[25:22]). There are 16 possible settings. It is recommended that customers determine the optimal equalization settings based on their environment to and their application.

5.1.1.4 TRANSMITTER SWING

The PCI Express transmitters support implementations of both full voltage swing and half (low) voltage swing. In full swing signaling mode, the transmitters implement de-emphasis, while in half swing mode, the transmitters do not. The Transmitter Swing field in the Physical Layer Control Register 2 (offset BCh, Bit[30]) is used for the selection of full swing signaling or half swing signaling.

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Table 5-3 Transmitter Swing Settings

Transmitter Swing	Mode	De-emphasis
0	Full Voltage Swing	Implemented
1	Half Voltage Swing	Not implemented

5.1.1.5 DRIVE AMPLITUDE AND DE-EMPHASIS SETTINGS

Depending on the operation condition (voltage swing and de-emphasis condition), one of the Drive Amplitude Base Level fields in the Physical Layer Control Register 0 (offset B4h) and one of the Drive De-Emphasis Base Level fields in the Physical Layer Control Register 1 (offset B8h) are active for configuration of the amplitude and de-emphasis.

In addition, optional offset values can be added to the drive amplitude and drive de-emphasis on a per-port basis via EEPROM settings (EEPROM offset 70h, bit[3:0]). The final drive amplitude and drive de-emphasis are the summation of the base level value and the offset value. The offset value for drive amplitude is 25 mV pd, and 6.25 mV pd for drive de-emphasis.

The driver output waveform is the synthesis of amplitude and de-emphasis as shown in Figure 5-1. The driver amplitude without de-emphasis is specified as a peak differential voltage level (mVpd), and the driver de-emphasis modifies the driver amplitude.

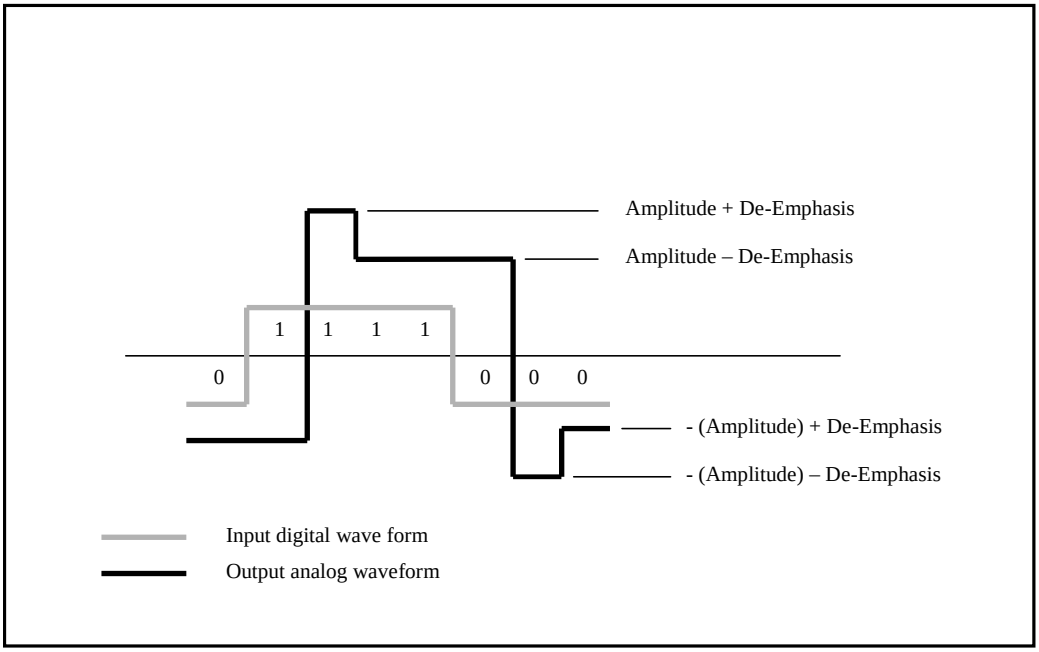

Figure 5-1 Driver Output Waveform

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5.1.1.6 DRIVE AMPLITUDE

Only one of the Drive Amplitude Level field in the Physical Control Register 0 (offset B4h, bit[20:16], bit[25:21] and bit[30:26]) listed in Table 5-4 is active depending on the de-emphasis and swing condition. The settings and the corresponding values of the amplitude level are listed in Table 5-5

Table 5-4 Drive Amplitude Base Level Registers

Active Register	De-Emphasis Condition	Swing Condition
Drive Amplitude Level (3P5 Nom)	-3.5 db	Full

Table 5-5 Drive Amplitude Base Level Settings

Setting	Amplitude (mV pd)	Setting	Amplitude (mV pd)	Setting	Amplitude (mV pd)
00000	0	00111	175	01110	350
00001	25	01000	200	01111	375
00010	50	01001	225	10000	400
00011	75	01010	250	10001	425
00100	100	01011	275	10010	450
00101	125	01100	300	10011	475
00110	150	01101	325	Others	Reserved

Note:
1. Nominal levels. Actual levels will vary with temperature, voltage and board effects.
2. The maximum nominal amplitude of the output driver is 475 mV pd. Combined values of driver amplitude and de-emphasis greater than 475 mV pd should be avoided.

5.1.1.7 DRIVE DE-EMPHASIS

The Drive De-Emphasis Level field in the Physical Control Register 1 (Offset B8h, bit[20:16]) listed in Table 5-6 controls the de-emphasis base level. The settings and the corresponding values of the de-emphasis level are listed in Table 5-7

Table 5-6 Drive De-Emphasis Base Level Register

Register	De-Emphasis Condition
Drive De-Emphasis Level	-3.5 db

Table 5-7 Drive De-Emphasis Base Level Settings

Setting	De-Emphasis (mV pd)	Setting	De-Emphasis (mV pd)	Setting	De-Emphasis (mV pd)
00000	0.0	01011	68.75	10110	137.5
00001	6.25	01100	75.0	10111	143.75
00010	12.5	01101	81.25	11000	150.0
00011	18.75	01110	87.5	11001	156.25
00100	25.0	01111	93.75	11010	162.5
00101	31.25	10000	100.0	11011	168.75
00110	37.5	10001	106.25	11100	175.0
00111	43.75	10010	112.5	11101	181.25
01000	50.0	10011	118.75	11110	187.5
01001	56.25	10100	125.0	11111	194.75
01010	62.5	10101	131.25	-	-

Note:
1. Nominal levels. Actual levels will vary with temperature, voltage and board effects.
2. The maximum nominal amplitude of the output driver is 475 mV pd. Combined values of driver amplitude and de-emphasis greater than 475 mV pd should be avoided.

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5.1.1.8 TRANSMITTER ELECTRICAL IDLE LATENCY

After the last character of the PCI Express transmission, the output current is reduced, and a differential voltage of less than 20 mV with common mode of VTX-CM-DC is established within 20 UI. This delay time is programmable via Transmitter PHY Latency field in the Physical Layer Control Register 2 (Offset BCh, bit[3:0]).

5.1.2 DATA LINK LAYER (DLL)

The Data Link Layer (DLL) provides a reliable data transmission between two PCI Express points. An ACK/NACK protocol is employed to guarantee the integrity of the packets delivered. Each Transaction Layer Packet (TLP) is protected by a 32-bit LCRC for error detection. The DLL receiver performs LCRC calculation to determine if the incoming packet is corrupted in the serial link. If an LCRC error is found, the DLL transmitter would issue a NACK data link layer packet (DLLP) to the opposite end to request a re-transmission, otherwise an ACK DLLP would be sent out to acknowledge on reception of a good TLP.

In the transmitter, a retry buffer is implemented to store the transmitted TLPs whose corresponding ACK/NACK DLLP have not been received yet. When an ACK is received, the TLPs with sequence number equals to and smaller than that carried in the ACK would be flushed out from the buffer. If a NACK is received or no ACK/NACK is returned from the link partner after the replay timer expires, then a replay mechanism built in DLL transmitter is triggered to re-transmit the corresponding packet that receives NACK or time-out and any other TLP transmitted after that packet.

Meanwhile, the DLL is also responsible for the initialization, updating, and monitoring of the flow-control credit. All of the flow control information is carried by DLLP to the other end of the link. Unlike TLP, DLLP is guarded by 16-bit CRC to detect if data corruption occurs.

In addition, the Media Access Control (MAC) block, which is consisted of LTSSM, multiple lanes deskew, scrambler/de-scrambler, clock correction from inserting skip order-set, and PIPE-related control/status circuits, is implemented to interface physical layer with data link layer.

5.1.3 TRANSACTION LAYER RECEIVE BLOCK (TLP DECAPSULATION)

The receiving end of the transaction layer performs header information retrieval and TC/VC mapping, and it validates the correctness of the transaction type and format. If the TLP is found to contain illegal header or the indicated packet length mismatches with the actual packet length, then a Malformed TLP is reported as an error associated with the receiving port. To ensure end-to-end data integrity, a 32-bit ECRC is checked against the TLP at the receiver if the digest bit is set in header.

5.1.4 ROUTING

The transaction layer implements three types of routing protocols: ID-based, address-based, and implicit routing. For configuration reads, configuration writes, transaction completion, and user-defined messages, the packets are routed by their destination ID constituted of bus number, device number, and function number. Address routing is employed to forward I/O or memory transactions to the destination port, which is located within the address range indicated by the address field carried in the packet header. The packet header indicates the packet types including memory read, memory write, IO read, IO write, Message Signaling Interrupt (MSI) and user-defined message. Implicit routing is mainly used to forward system message transactions such as virtual interrupt line, power management, and so on. The message type embedded in the packet header determines the routing mechanism.

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If the incoming packet can not be forwarded to any other port due to a miss to hit the defined address range or targeted ID, this is considered as Unsupported Request (UR) packet, which is similar to a master abort event in PCI protocol.

5.1.5 TC/VC MAPPING

The 3-bit TC field defined in the header identifies the traffic class of the incoming packets. To enable the differential service, a TC/VC mapping table at destination port that is pre-programmed by system software or EEPROM pre-load is utilized to cast the TC labeled packets into the desired virtual channel. Note that all the traffic classes are mapped to VC0, since only VC0 is available on the interface. After the TC/VC mapping, the receive block dispatches the incoming request, completion, or data into the VC0 queues.

5.1.6 QUEUE

In PCI Express, it defines six different packet types to represent request, completion, and data. They are respectively Posted Request Header (PH), Posted Request Data payload (PD), Non-Posted Request Header (NPH), Non-Posted Data Payload (NPD), Completion Header (CPLH) and Completion Data payload (CPLD). Each packet with different type would be put into a separate queue in order to facilitate the following ordering processor. Since NPD usually contains one DW, it can be merged with the corresponding NPH into a common queue named NPHD.

5.1.6.1 PH

PH queue provides TLP header spaces for posted memory writes and various message request headers. Each header space occupies sixteen bytes to accommodate 3 DW or 4 DW headers.

5.1.6.2 PD

PD queue is used for storing posted request data. If the received TLP is of the posted request type and is determined to have payload coming with the header, the payload data would be put into PD queue.

5.1.6.3 NPHD

NPHD queue provides TLP header spaces for non-posted request packets, which include memory read, IO read, IO write, configuration read, and configuration write. Each header space takes twenty bytes to accommodate a 3-DW header, s 4-DW header, s 3-WD header with 1-DW data, and a 4-DW header with 1-DW data.

5.1.6.4 CPLH

CPLH queue provides TLP header space for completion packets. Each header space takes twelve bytes to accommodate a 3-DW header. Please note that there is no 4-DW completion headers.

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5.1.6.5 CPLD

CPLD queue is used for storing completion data. If the received TLP is of the completion type and is determined to have payload coming with the header, the payload data would be put into CPLD queue.

5.1.7 TRANSACTION ORDERING

Within a VPPB, a set of ordering rules is defined to regulate the transactions on the PCI Express interface including Memory, IO, Configuration and Messages, in order to avoid deadlocks and to support the Producer-Consumer model. The ordering rules defined in table 5-4 apply within a single Traffic Class (TC). There is no ordering requirement among transactions within different TC labels.

Table 5-8 Summary of PCI Express Ordering Rules

Row Pass Column	Posted Request	Read Request	Non-posted Write Request	Read Completion	Non-posted Write Completion
Posted Request	Yes/No[1]	Yes[5]	Yes[5]	Yes[5]	Yes[5]
Read Request	No[2]	Yes	Yes	Yes	Yes
Non-posted Write Request	No[2]	Yes	Yes	Yes	Yes
Read Completion	Yes/No[3]	Yes	Yes	Yes	Yes
Non-Posted Write Completion	Yes[4]	Yes	Yes	Yes	Yes

1. When the Relaxed Ordering Attribute bit is cleared, the Posted Request transactions including memory write and message request must complete on the egress bus of VPPB in the order in which they are received on the ingress bus of VPPB. If the Relaxed Ordering Attribute bit is set, the Posted Request is permitted to pass over other Posted Requests occurring before it.

2. A Read Request transmitting in the same direction as a previously queued Posted Request transaction must push the posted write data ahead of it. The Posted Request transaction must complete on the egress bus before the Read Request can be attempted on the egress bus. The Read transaction can go to the same location as the Posted data. Therefore, if the Read transaction were to pass the Posted transaction, it would return stale data.

3. When the Relaxed Ordering Attribute bit is cleared, a Read completion must ‘‘pull’’ ahead of previously queued posted data transmitting in the same direction. In this case, the read data transmits in the same direction as the posted data, and the requestor of the read transaction is on the same side of the VPPB as the completer of the posted transaction. The posted transaction must deliver to the completer before the read data is returned to the requestor. If the Relaxed Ordering Attribute bit is set, then a read completion is permitted to pass a previously queued Memory Write or Message Request.

4. Non-Posted Write Completions are permitted to pass a previous Memory Write or Message Request transaction. Such transactions are actually transmitting in the opposite directions and hence have no ordering relationship.

5. Posted Request transactions must be given opportunities to pass Non-posted Read and Write Requests as well as Completions. Otherwise, deadlocks may occur when some older Bridges that do not support delayed transactions are mixed with PCIe interface in the same system. A fairness algorithm is used to arbitrate between the Posted Write queue and the Non-posted transaction queue.

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5.1.8 FLOW CONTROL

PCI Express employs Credit-Based Flow Control mechanism to make buffer utilization more efficient. The transaction layer transmitter ensures that it does not transmit a TLP to an opposite receiver unless the receiver has enough buffer space to accept the TLP. The transaction layer receiver has the responsibility to advertise the free buffer space to an opposite transmitter to avoid packet stale. In this device, each port has separate queues for different traffic types and the credits are on the fly sent to data link layer, which compares the current available credits with the monitored one and reports the updated credit to the counterpart. If no new credit is acquired, the credit reported is scheduled for every 30 us to prevent from link entering retrain. On the other hand, the receiver at each egress port gets the usable credits from the opposite end in a link. It would broadcast them to all the other ingress ports for gating the packet transmission.

5.1.9 TRANSATION LAYER TRANSMIT BLOCK (TLP ENCAPSULATION)

The transmit portion of transaction layer performs the following functions. They are to construct the all types of forwarded TLP generated from VC arbiter, respond with the completion packet when the local resource (i.e. configuration register) is accessed and regenerate the message that terminated at receiver to RC if acts as an upstream port.

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5.2 USB HOST CONTROLLER FUNCTIONALITIES

5.2.1 OHCI HOST CONTROLLER

The OHCI Host Controller (HC) is responsible for communications between Host Controller Driver (HCD) software and USB Full Speed/Low Speed devices. The OHCI/HC and HCD exchange the information via operational registers, bulk transfer descriptors, control transfer descriptors and Host Controller Communication Area (HCCA), which are for interrupt and isochronous transfer types.

When communicating with operational registers, the OHCI/HC acts as a PCI target device to accept the commands provided by HCD and reports the status requested by HCD. The operational register contains the pointers that indicate the locations of HCCA and descriptors for bulk and control within the system memory. The HCD receives the IO Request Packet (IRP) from USB driver software and prepares the data structure of Endpoint Descriptor (ED) and Transfer Descriptor (TD) in the format of linked list in the system memory. After ED and TD are prepared, the HC is notified and acts as a PCI master to fetch the ED and TD and move data between the USB devices and memory area by following the instructions described in the descriptors.

An ED is comprised of the information including endpoint address, speed, data flow direction and maximum packet size, etc. A TD contains the information of data toggle, buffer position in system memory, complete status code and data buffer size. The EDs are linked together based on their transfer type, and each ED points to a list of TD queue that is used to transfer the data or command associated with a specific endpoint.

5.2.1.1 OHCI LEGACY SUPPORT

The OHCI host controller implements legacy support for emulation of PS/2 mouse and/or keyboard in operating systems, applications, and drivers that do not support USB functions. The emulation code translates the standard USB compliant keyboard/mouse data and transfers the data to/from PS/2 compatible legacy keyboard interface at I/O addresses 60h and 64h.

The legacy support interface is consisted of 7 hardware pins, LEG_EN, SMI_O, IO_HIT_I, IRQ_1_I, IRQ1_O, IRQ12_I and IRQ12_O, and 4 operational registers, HceControl, HceInput, HceOutput and HceStatus (offset 100h, 104h, 108h and 10Ch). When EmulationEnable bit in HceControl register is set to 1, legacy emulation is enabled. The host controller decodes accesses to I/O registers 60h and 64h, and generates IRQ1 and/or IRQ12 when appropriate.

When legacy emulation is enabled, reads and writes of the I/O register 60h and 64h are captured in HceInput, HceOutput, and HceStatus operational registers.

For details, refer to OpenHCI Specification 1.0, Appendix B.

5.2.2 EHCI HOST CONTROLLER

The EHCI Host Controller (HC) is responsible for communications between HC Driver software and USB High Speed devices. Similar to OHCI/HC, the EHCI/HC and HCD exchange the information via operational registers as well as data structure arranged in periodic schedule and asynchronous schedule traversals in the system memory.

The periodic schedule traversal is used for time-sensitive isochronous and interrupts transfer types while the asynchronous schedule traversal is for less time-sensitive control and bulk transfer types. The handling of EHCI data structure is similar to that in OHCI. However, EHCI data is more complicated due to micro-frame scheduling and split transaction support. For isochronous and interrupt transactions, the data structure contains High Speed

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device isochronous transfer descriptors (iTD), Full Speed device split-transaction isochronous transfer descriptors (siTD) and queue head structure queue element descriptors (qTD) for interrupt devices. For bulk and control transactions, the HC utilizes the qTD to represent the asynchronous data transfer types for High Speed bulk and control devices.

5.2.3 PHYSICAL LAYER CIRCUIT

The USB physical layer circuit design is based on USB 2.0 Specification. The design contains PLL, bias current generator, voltage bandgap, clock and data recovery, sync detector, NRZI Encoder / Decoder, Serializer / De-Serializer, VBUS pulsing and discharge SRP circuit, and VBUS threshold comparators.

The USB physical layer parameters can be configured by setting the USB Physical Layer Control Register (Offset A0h for port 1, A4h for port 2, A8h for port 3, and ACh for port 4) and EEPROM. Each of the USB port has its own set of physical layer control parameters, and the configuration of the parameters is performed on a per-port basis.

5.2.3.1 HS DRIVER TIMING CONTROL

The timing of the HS Driver can be adjusted by changing the ratio of PMOS/NMOS strength. The PMOS Strength for HS Driver Timing and the PMOS Strength for HS Driver Timing fields (bit[0] and bit[2:1]) in the USB Physical Layer Control Register control the PMOS and NMOS strength respectively.

Table 5-9 HS Driver Timing Control for PMOS

PMOS Strength for HS Driver Timing	HS Driver Timing for PMOS
0 (default)	2x
1	8x

Table 5-10 HS Driver Timing Control for NMOS

NMOS Strength for HS Driver Timing	HS Driver Timing for NMOS
00 (default)	2x
01	4x
10	6x
11	8x

5.2.3.2 HS DRIVER AMPLITUDE

The amplitude of the HS driver current can be adjusted by setting the HS Driver Amplitude field (bit[4:3]) in the USB Physical Layer Control Register.

Table 5-11 HS Driver Amplitude Control

HS Driver Amplitude	HS Driver Current
00 (default)	I
01	I + 2.5%
10	I + 5%
11	I + 7.5%

Note: I=17.78mA

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5.2.3.3 HS DRIVER SLOPE CONTROL

The rise/fall times of the HS Driver can be adjusted by setting the HS Driver Slope Control field (bit[8:5]) in the USB Physical Layer Control Register. The field controls the injection of additional charge and changes the RC constant.

Table 5-12 HS Driver Slope Control

HS Driver Slope Control	Rise/Fall Time
0000 (default)	Actual values depend on boards, ambient temperatures, etc.
0001	
0010	
0011	
0100	
0101	
0110	
0111	
1000	
1001	
1010	
1011	
1100	
1101	
1110	
1111	

5.2.3.4 REFERENCE VOLTAGE FOR DISCONNECT CIRCUIT

The reference voltage of the disconnect circuit can be adjusted by setting the Reference Voltage for Disconnect Circuit field (bit[10:9]) in the USB Physical Layer Control Register.

Table 5-13 Reference Voltage for Disconnect Circuit

Reference Voltage for Disconnect Circuit	$V_{ref575m}$
00	(46 + 2) / 100 * vbg
01	(46 + 3) / 100 * vbg
10 (default)	(46 + 4) / 100 * vbg
11	(46 + 5) / 100 * vbg

5.2.3.5 REFERENCE VOLTAGE FOR SQUELCH CIRCUIT

The reference voltage of the squelch circuit can be adjusted by setting the Reference Voltage for Squelch Circuit field (bit[12:11]) in the USB Physical Layer Control Register.

Table 5-14 Reference Voltage for Squelch Circuit

Reference Voltage for Squelch Circuit	Differential Reference Voltage
00	9 / 100 * vbg
01	(9 + 1) / 100 * vbg
10 (default)	(9 + 2) / 100 * vbg
11	(9 + 3) / 100 * vbg

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5.2.3.6 REFERENCE VOLTAGE FOR CALIBRATION CIRCUIT

The reference voltage of the calibration circuit can be adjusted by setting the Reference Voltage for Calibration Circuit field (bit[15:13]) in the USB Physical Layer Control Register.

Table 5-15 Reference Voltage for Calibration Circuit

Reference Voltage for Calibration Circuit	$V_{ref575mtune}$
000	(46) / 100 * vbg
001	(46 + 1) / 100 * vbg
010	(46 + 2) / 100 * vbg
011	(46 + 3) / 100 * vbg
100 (default)	(46 + 4) / 100 * vbg
101	(46 + 5) / 100 * vbg
110	(46 + 6) / 100 * vbg
111	(46 + 7) / 100 * vbg

5.2.3.7 CHARGE PUMP CURRENT FOR PLL

The charge pump current can be adjusted by setting the Charge Pump Current for PLL field (bit[17:16]) in the USB Physical Layer Control Register.

Table 5-16 Charge Pump Current Control

Charge Pump Current for PLL	Charge Pump Current (mA)
00 (default)	Icp
01	Icp * 0.5
10	Icp * 1.5
11	Icp * 2

Note: Icp=40uA

5.2.3.8 FS RISE/FALL TIME CONTROL

The rise/fall times for FS can be adjusted by setting the FS Rise/Fall Time Control field (bit[19:18]) in the USB Physical Layer Control Register.

Table 5-17 FS Rise/Fall Time Control

FS Rise/Fall Time Control	Rise/Fall Time
00	Normal FS rise time - 30%
01 (default)	Normal FS rise time
10	Normal FS rise time
11	Normal FS rise time +30%

5.2.3.9 LS RISE/FALL TIME CONTROL

The rise/fall times for LS can be adjusted by setting the LS Rise/Fall Time Control field (bit[21:20]) in the USB Physical Layer Control Register.

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Table 5-18 LS Rise/Fall Time Control

LS Rise/Fall Time Control	Rise/Fall Time
00	Normal LS rise time - 30%
01 (default)	Normal LS rise time
10	Normal LS rise time
11	Normal LS rise time +30%

5.2.3.10 HS DRIVER PRE-EMPHASIS

The amplitude of the HS Driver can be adjusted by setting the HS Driver Pre-Emphasis field (bit[23:22]) in the USB Physical Layer Control Register.

Table 5-19 HS Driver Pre-Emphasis Control

HS Driver Pre-Emphasis	HS Drive Current
00 (default)	I
01	I + 10%
10	I
11	I + 20%

Note: I=17.78mA

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6 EEPROM INTERFACE AND SYSTEM MANAGEMENT BUS

The EEPROM interface consists of two pins: EECLK (EEPROM clock output) and EEPD (EEPROM bi-directional serial data). The Switch may control an ISSI IS24C04 or compatible parts using into 512x8 bits. The EEPROM is used to initialize a number of registers before enumeration. This is accomplished after PRST# is de-asserted, at which time the data from the EEPROM is loaded. The EEPROM interface is organized into a 16-bit base, and the Switch supplies a 7-bit EEPROM word address. The Switch does not control the EEPROM address input. It can only access the EEPROM with address input set to 0.

The System Management Bus interface consists of two pins: SMBCLK (System Management Bus Clock input) and SMBDATA (System Management Bus Data input/ output).

6.1 EEPROM INTERFACE

6.1.1 AUTO MODE EERPOM ACCESS

The Swidge may access the EEPROM in a WORD format by utilizing the auto mode through a hardware sequencer. The EEPROM start-control, address, and read/write commands can be accessed through the configuration register. Before each access, the software should check the Autoload Status bit before issuing the next start.

6.1.2 EEPROM MODE AT RESET

During a reset, the Switch will automatically load the information/data from the EEPROM if the automatic load condition is met. The first offset in the EEPROM contains a signature. If the signature is recognized, the autoload initiates right after the reset.

During the autoload, the Bridge will read sequential words from the EEPROM and write to the appropriate registers. Before the Bridge registers can be accessed through the host, the autoload condition should be verified by reading bit [3] offset DCh (EEPROM Autoload Status). The host access is allowed only after the status of this bit is set to '0' which indicates that the autoload initialization sequence is complete.

6.1.3 EEPROM SPACE ADDRESS MAP

15 – 8	7 – 0	BYTE OFFSET
EEPROM Signature (1516h)		00h
Vendor ID for Port 0 ~ 3		02h
Device ID for Port 0 ~ 3		04h
Extended VC Count / Link Capability / Switch Mode Operation / Interrupt pin for Port 1 ~ 2		06h
Subsystem Vender ID for Port 0 ~ 3		08h
Subsystem ID for Port 0 ~ 3		0Ah
Misc Configuration for Port 0 ~ 3		0Ch
Reserved	Revision ID for Port 0 ~ 3	0Eh
FTS / RefClk ppm Difference / Scramble Control for Port 0		10h
FTS / RefClk ppm Difference / Scramble Control for Port 1		12h
FTS / RefClk ppm Difference / Scramble Control for Port 2		14h
Reserved		16h
Physical Layer Control 0 for Port 0 ~ 2		18h
Physical Layer Control 1 for Port 0 ~ 2		1Ah
Physical Layer Control 2, Bit[6:0] for Port 0 ~ 2		1Ch

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15 – 8	7 – 0	BYTE OFFSET
Reserved		1Eh
TC/VC Map for Port 0 (VC0)	Slot Clock / LPVC Count / Port Num, Port 0	20h
TC/VC Map for Port 1(VC0)	Slot Implemented / Slot Clock / LPVC Count / Port Num, Port 1	22h
TC/VC Map for Port 2 (VC0)	Slot Implemented / Slot Clock / LPVC Count / Port Num, Port 2	24h
Reserved		26h
Vendor ID for Func 0		28h
Vendor ID for Func 1		2Ah
Vendor ID for Func 2		2Ch
Device Control for Func 0		2Eh
Reserved		30h
Slot Capability 0 for Port 1		32h
Slot Capability 0 for Port 2		34h
Reserved		36h
Device ID for Func 0		38h
Device ID for Func 1		3Ah
Device ID for Func 2		3Ch
Miscellaneous Register for Func 2		3Eh
Reserved		40h
Slot Capability 1 for Port 1		42h
Slot Capability 1 for Port 2		44h
Reserved		46h
Revision ID / Programming Interface for Func 0		48h
Revision ID / Programming Interface for Func 1		4Ah
Revision ID / Programming Interface for Func 2		4Ch
USB Physical Layer Control Register (USB Port 1), Bit[15:0]		4Eh
PM Data for Port 0	PM Capability for Port 0	50h
PM Data for Port 1	PM Capability for Port 1	52h
PM Data for Port 2	PM Capability for Port 2	54h
PM Data for Port 3	PM Capability for Port 3	56h
Class Code for Func 0		58h
Class Code for Func 1		5Ah
Class Code for Func 2		5Ch
USB Physical Layer Control Register (USB Port 2), Bit[15:0]		5Eh
Power Budgeting Capability Register for Port 0		60h
Power Budgeting Capability Register for Port 1		62h
Power Budgeting Capability Register for Port 2		64h
Reserved		66h
Subsystem Vendor ID for Func 0		68h
Subsystem Vendor ID for Func 1		6Ah
Subsystem Vendor ID for Func 2		6Ch
Device Control for Func 1		6Eh
Physical Layer Control 2, Bit[30:16] for Port 0		70h
Physical Layer Control 2, Bit[30:16] for Port 1		72h
Physical Layer Control 2, Bit[30:16] for Port 2		74h
Reserved		76h
Subsystem ID for Func 0		78h
Subsystem ID for Func 1		7Ah
Subsystem ID for Func 2		7Ch
Reserved		7Eh
Physical Layer Control 2, Bit[12:8] for Port 0		80h
Physical Layer Control 2, Bit[12:8] for Port 1		82h
Physical Layer Control 2, Bit[12:8] for Port 2		84h
Reserved		86h
Reserved	Capability Pointer for Func 0	88h
Reserved	Capability Pointer for Func 1	8Ah
Reserved	Capability Pointer for Func 2	8Ch
USB Physical Layer Control Register (USB Port 3), Bit[15:0]		8Eh
PM Control Parameter / Rx Polarity for Port 0		90h
PM Control Parameter / Rx Polarity for Port 1		92h
PM Control Parameter / Rx Polarity for Port 2		94h
Reserved		96h
PM Capability for Func 0	Next Pointer Item for Func 0	98h

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15 – 8	7 – 0	BYTE OFFSET
PM Capability for Func 1	Next Pointer Item for Func 1	9Ah
PM Capability for Func 2	Next Pointer Item for Func 2	9Ch
USB Physical Layer Control Register (USB Port 4), Bit[15:0]		9Eh
Replay Time-out Counter for Port 0		A0h
Replay Time-out Counter for Port 1		A2h
Replay Time-out Counter for Port 2		A4h
Reserved		A6h
PM Capability / PM Data / Next Pointer Item for Func 0		A8h
PM Capability / PM Data / Next Pointer Item for Func 1		AAh
PM Capability / PM Data / Next Pointer Item for Func 2		ACh
Device Control for Func 0		AEh
Acknowledge Latency Timer for Port 0		B0h
Acknowledge Latency Timer for Port 1		B2h
Acknowledge Latency Timer for Port 2		B4h
Reserved		B6h
Next Pointer Item for Func 0	Capability ID for Func 0	B8h
Next Pointer Item for Func 1	Capability ID for Func 1	BAh
Next Pointer Item for Func 2	Capability ID for Func 2	BCh
Reserved		BEh
Physical Layer Control 3 for Port 0		C0h
Reserved		C2h
Reserved		C4h
Reserved		C6h
PCI Express Capability for Func 0		C8h
PCI Express Capability for Func 1		CAh
PCI Express Capability for Func 2		CCh
USB Physical Layer Control Register (USB Port 2), Bit[23:16]	USB Physical Layer Control Register (USB Port 1), Bit[23:16]	CEh
Reserved		D0h
Reserved		D2h
Reserved		D4h
Reserved		D6h
Device Capability 0 for Func 0		D8h
Device Capability 0 for Func 1		DAh
Device Capability 0 for Func 2		DCh
USB Physical Layer Control Register (USB Port 4), Bit[23:16]	USB Physical Layer Control Register (USB Port 3), Bit[23:16]	DEh
Reserved		E0h
Reserved		E2h
Reserved		E4h
Reserved		E6h
Device Capability 1 for Func 0		E8h
Device Capability 1 for Func 1		EAh
Device Capability 1 for Func 2		ECh

6.1.4 MAPPING EEPROM CONTENTS TO CONFIGURATION REGISTERS

ADDRESS	PCI CFG OFFSET	DESCRIPTION
00h		**EEPROM signature** – 1516h
02h	00h ~ 01h	**Vendor ID for Port 0~3**
04h	02h ~ 03h	**Device ID for Port 0~3**

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ADDRESS	PCI CFG OFFSET	DESCRIPTION
06h	ECh (Port 0~2) ECh – Bit[14:12] ECh – Bit[17:15] B4h (Port 0~2) B4h – Bit[5] Bit[6] Bit[0] Bit[2:1] Bit[3] Bit[4] 3Ch (Port 1~2) 3Ch – Bit[8]	**Link Capability for Port 0~2** ▪ Bit[3:1]: It represents L0s Exit Latency for all ports ▪ Bit[6:4]: It represents L1 Exit Latency for all ports **Switch Mode Operation for Port 0~2** ▪ Bit[8]: Ordering on Different Egress Port Mode ▪ Bit[9]: Ordering on Different Tag of Completion Mode ▪ Bit[10]: Store and Forward ▪ Bit[12:11]: Cut-through Threshold ▪ Bit[13]: Port Arbitration Mode ▪ Bit[14]: Credit Update Mode **Interrupt pin for Port 1~2** ▪ Bit[15]: Set when INTA is requested for interrupt resource
08h	C4h ~ C5h	**Subsystem Vender ID**
0Ah	C6h ~ C7h	**Subsystem ID**
0Ch	E4h (Port 0~3) E4h – Bit[0] ECh (Port 0~3) ECh – Bit[11 :10] E4h (Port 0~3) E4h – Bit[15] B0h (Port 0~3) B0h – Bit[14] B0h – Bit[15] B4h (Port 0~3) B4h – Bit[15] B0h (Port 0~3) B0h – Bit[13] B4h (Port 0~3) B4h – Bit[7] B8h (Port 0~3) B8h – Bit[12] ECh (Port 1~3) ECh – Bit[19] B8h (Port 0~3) B8h – Bit[13] B8h (Port 0~3) B8h – Bit[14] B8h (Port 0~3) B8h – Bit[15]	**Max_Payload_Size Support for Port 0~3** ▪ Bit[0]: Indicated the maximum payload size that the device can support for the TLP **ASPM Support for Port 0~3** ▪ Bit[2:1]: Indicate the level of ASPM supported on the PCIe link **Role_Base Error Reporting for Port 0~3** ▪ Bit[3]: Indicate implement the role-base error reporting **MSI/AER Capability Disable for Port 0~3** ▪ Bit[4]: Disable MSI capability ▪ Bit[5]: Disable AER capability **Compliance Pattern Parity Control Disable for Port 0~3** ▪ Bit[6]: Compliance Pattern Parity Control Disable **Power Management Capability Disable for Port 0~3** ▪ Bit[7]: Disable Power Management Capability **Ordering Frozen for Port 0~3** ▪ Bit[10]: Freeze the ordering feature **TX SOF Latency Mode for Port 0~3** ▪ Bit[11]: Set to zero to shorten latency **Surprise Down Capability Enable for for Port 1~3** ▪ Bit[12]: Enable Surprise Down Capability **Power Management's Data Select Register R/W Capability for Port 0~3** ▪ Bit[13]: Enable Data Select Register R/W **Flow Control Update Type for Port 0~3** ▪ Bit[14]: Select Flow Control Update Type **4KB Boundary Check Enable for Port 0~3** ▪ Bit[15]: Enable 4KB Boundary Check
0Eh	08h (Port 0~3) 08h – Bit[7:0]	**Revision ID for Port 0~3** ▪ Bit [7:0]: Indicates the Revision ID of chip.
10h	B8h (Port 0) B8h – Bit[7 :0] A8h (Port 0) A8h – Bit[14:13] B8h (Port 0)	**FTS Number for Port 0** ▪ Bit[7:0]: FTS number at receiver side **RefClk ppm Difference for Port 0** ▪ Bit[9:8]: It represents RefClk ppm difference between the two ends in one link; 00: 0 ppm, 01: 100 ppm, 10: 200 ppm, 11: 300 ppm **Scrambler Control for Port 0**

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ADDRESS	PCI CFG OFFSET	DESCRIPTION
	B8h – Bit[11:10] B8h – Bit[12]	▪ Bit[11:10]: Scrambler Control ▪ Bit[12]: L0s
12h	B8h (Port 1) B8h – Bit[7 :0] A8h (Port 1) A8h – Bit[14:13] B8h (Port 1) B8h – Bit[9:8] B8h – Bit[10]	**FTS Number for Port 1** ▪ Bit[7:0]: FTS number at receiver side **RefClk ppm Difference for Port 1** ▪ Bit[9:8]: It represents RefClk ppm difference between the two ends in one link; 00: 0 ppm, 01: 100 ppm, 10: 200 ppm, 11: 300 ppm **Scrambler Control for Port 1** ▪ Bit[11:10]: Scrambler Control ▪ Bit[12]: L0s
14h	B8h (Port 2) B8h – Bit[7:0] A8h (Port 2) A8h – Bit [14:13] B8h (Port 2) B8h – Bit[9:8] B8h – Bit[10]	**FTS Number for Port 2** ▪ Bit[7:0]: FTS number at receiver side **RefClk ppm Difference for Port 2** ▪ Bit[9:8]: It represents RefClk ppm difference between the two ends in one link; 00: 0 ppm, 01: 100 ppm, 10: 200 ppm, 11: 300 ppm **Scrambler Control for Port 2** ▪ Bit[11:10]: Scrambler Control ▪ Bit[12]: L0s
18h	B4h (Port 0~2) B4h – Bit[20 :16] B4h – Bit[25 :21] B4h – Bit[30 :26]	**Physical Layer Control 0 for Port 0~2** ▪ Bit[4:0]: Drive Amplitude Level (3P5 Nom) ▪ Bit[9:5]: Drive Amplitude Level (6P0 Nom) ▪ Bit[14:10]: Drive Amplitude Level (Half)
1Ah	B8h (Port 0~2) B8h – Bit[20 :16] B8h – Bit[25 :21] B8h – Bit[30 :26]	**Physical Layer Control 1 for Port 0~2** ▪ Bit[4:0]: Drive De-Emphasis Level ▪ Bit[9:5]: Reserved ▪ Bit[14:10]: Reserved
1Ch	BCh (Port 0~2) BCh – Bit[3 :0] BCh – Bit[6 :4]	**Physical Layer Control 2 for Port 0~2** ▪ Bit[3:0]: Transmitter PHY Latency ▪ Bit[6:4]: Receiver Detection Threshold
20h	F0h (Port 0) F0h – Bit[28] 80h (Port 0) 80h – Bit[21] ECh (Port 0) ECh – Bit[25:24] 84h (Port 0) 84h – Bit[14:13]	**Slot Clock Configuration for Port 0** ▪ Bit[1]: When set, the component uses the clock provided on the connector **Device specific Initialization for Port 0** ▪ Bit[2]: When set, the DSI is required **Port Number for Port 0** ▪ Bit[5:4]: It represents the logic port numbering for physical port 0 **PMCSR Data Scale for Port 0** Bit[7:6]: It represents the PMCSR Data Scale for physical port 0
	154h (Port 0) 154h – Bit[7:1]	**VC0 TC/VC Map for Port 0** ▪ Bit[15:9]: When set, it indicates the corresponding TC is mapped into VC0
22h	E0h (Port1) E0h – Bit[24] F0h (Port 1) F0h – Bit[28] 80h (Port 1) 80h – Bit[21] ECh (Port 1) ECh – Bit[25:24] 84h (Port 1) 84h – Bit[14:13]	**PCIe Capability Slot Implemented for Port 1** ▪ Bit[0]: When set, the slot is implemented for Port 1 **Slot Clock Configuration for Port 1** ▪ Bit[1]: When set, the component uses the clock provided on the connector **Device specific Initialization for Port 1** ▪ Bit[2]: When set, the DSI is required **Port Number for Port 1** ▪ Bit[5:4]: It represents the logic port numbering for physical port 1 **PMCSR Data Scale for Port 1** Bit[7:6]: It represents the PMCSR Data Scale for physical port 1

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ADDRESS	PCI CFG OFFSET	DESCRIPTION
	154h (Port 1) 154h – Bit[7:1]	**VC0 TC/VC Map for Port 1** ▪ Bit[15:9]: When set, it indicates the corresponding TC is mapped into VC0
24h	E0h (Port 2) E0h – Bit[24] F0h (Port 2) F0h – Bit[28] 80h (Port 2) 80h – Bit[21] ECh (Port 2) ECh – Bit[25:24] 84h (Port 2) 84h – Bit[14:13]	**PCIe Capability Slot Implemented for Port 2** ▪ Bit[0]: When set, the slot is implemented for Port 2 **Slot Clock Configuration for Port 2** ▪ Bit[1]: When set, the component uses the clock provided on the connector **Device specific Initialization for Port 2** ▪ Bit[2]: When set, the DSI is required **Port Number for Port 2** ▪ Bit[5:4]: It represents the logic port numbering for physical port 2 **PMCSR Data Scale for Port 2** Bit[7:6]: It represents the PMCSR Data Scale for physical port 2
	154h (Port 2) 154h – Bit[7:1]	**VC0 TC/VC Map for Port 2** ▪ Bit[15:9]: When set, it indicates the corresponding TC is mapped into VC0
28h	00h ~ 01h (Func 0)	**Vendor ID for Func 0**
2Ah	00h ~ 01h (Func 1)	**Vendor ID for Func 1**
2Ch	00h ~ 01h (Func 2)	**Vendor ID for Func 2**
2Eh	E8h (Func 0) E8h – Bit[0] E8h – Bit[1] E8h – Bit[2] E8h – Bit[3] E8h – Bit[4] E8h – Bit[7 :5] E8h – Bit[8] E8h – Bit[9] E8h – Bit[10] E8h – Bit[11] E8h – Bit[14 :12]	**PCI Express Capability for Func 0** ▪ Bit[0]: Correctable Error Reporting Enable ▪ Bit[1]: Non-Fatal Error Reporting Enable ▪ Bit[2]: Fatal Error Reporting Enable ▪ Bit[3]: Unsupported Request Reporting Enable ▪ Bit[4]: Enable Relaxed Ordering ▪ Bit[7:5]: Max_Payload_Size ▪ Bit[8]: Extended Tag Field Enable ▪ Bit[9]: Phantom Function Enable ▪ Bit[10]: Auxiliary (AUX) Power PM Enable ▪ Bit[11]: Enable No Snoop ▪ Bit[14:12]: Max_Read_ Request_Size
32h	F4h (Port 1) F4h – Bit[15:0]	**Slot Capability 0 of Port 1** ▪ Bit[15:0]: Mapping to the low word of slot capability register
34h	F4h (Port 2) F4h – Bit[15:0]	**Slot Capability 0 of Port 2** ▪ Bit[15:0]: Mapping to the low word of slot capability register
38h	02h ~ 03h (Func 0)	**Device ID for Func 0**
3Ah	02h ~ 03h (Func 1)	**Device ID for Func 1**
3Ch	02h ~ 03h (Func 2)	**Device ID for Func 2**
3Eh	68h (Func 2) 68h – Bit[0] 68h – Bit[1] 68h – Bit[2] 68h – Bit[3] 68h – Bit[4] 68h – Bit[6:5] 68h – Bit[14:8]	**Miscellaneous Register for Func 2** ▪ Bit[0]: Enable Basic Mode ▪ Bit[1]: Enable Boundary 64-byte ▪ Bit[2]: Enable EHCI Prefetch ▪ Bit[3]: Reserved. Must to be 0b. ▪ Bit[4]: Enable User Max_Read_Request_Size ▪ Bit[6:5]: User Max_Read_Request_Size ▪ Bit[14:8]: Prefetch DW Size (Unit: DW)
42h	F4h (Port 1) F4h – Bit[31:16]	**Slot Capability 1 of Port 1** ▪ Bit[15:0]: Mapping to the high word of slot capability register
44h	F4h (Port 2) F4h – Bit[31:16]	**Slot Capability 1 of Port 2** ▪ Bit[15:0]: Mapping to the high word of slot capability register
48h	08h (Func 0) 08h – Bit[7:0] 08h – Bit[15:8]	**Revision ID and Class Code for Func 0** ▪ Bit[7:0]: Revision ID ▪ Bit[15:8]: Programming Interface
4Ah	08h (Func 1) 08h – Bit[7:0] 08h – Bit[15:8]	**Revision ID and Class Code for Func 1** ▪ Bit[7:0]: Revision ID ▪ Bit[15:8]: Programming Interface

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ADDRESS	PCI CFG OFFSET	DESCRIPTION
4Ch	08h (Func 2) 08h – Bit[7:0] 08h – Bit[15:8]	**Revision ID and Class Code for Func 2** ▪ Bit[7:0]: Revision ID ▪ Bit[15:8]: Programming Interface
4Eh	A0h (Func 0~2) A0h – Bit[15 :0]	**USB Physical Layer Control Register (USB Port 1), Bit[15:0]** ▪ Bit[15:0]: USB Physical Layer Control Register (USB Port 1), Bit[15:0]
50h	84h (Port 0) 84h – Bit[3] 80h (Port 0) 80h – Bit[24:22] 80h – Bit[25] 80h – Bit[26] 80h – Bit[29:28]	**No_Soft_Reset for Port 0** ▪ Bit[0]: No_Soft_Reset. **Power Management Capability for Port 0** ▪ Bit[3:1]: AUX Current ▪ Bit[4]: read only as 1 to indicate Bridge supports the D1 power management state ▪ Bit[5]: read only as 1 to indicate Bridge supports the D2 power management state ▪ Bit[7:6]: PME Support for D2 and D1 states
51h	84h (Port 0) 84h – Bit[31:24]	**Power Management Data for Port 0** ▪ Bit[15:8]: read only as Data register
52h	84h (Port 1) 84h – Bit[3] 80h (Port 1) 80h – Bit[24:22] 80h – Bit[25] 80h – Bit[26] 80h – Bit[29:28]	**No_Soft_Reset for Port 1** ▪ Bit[0]: No_Soft_Reset. **Power Management Capability for Port 1** ▪ Bit[3:1]: AUX Current ▪ Bit[4]: read only as 1 to indicate Bridge supports the D1 power management state ▪ Bit[5]: read only as 1 to indicate Bridge supports the D2 power management state ▪ Bit[7:6]: PME Support for D2 and D1 states
53h	84h (Port 1) 84h – Bit[31:24]	**Power Management Data for Port 1** ▪ Bit[15:8]: read only as Data register
54h	84h (Port 2) 84h – Bit[3] 80h (Port 2) 80h – Bit[24:22] 80h – Bit[25] 80h – Bit[26] 80h – Bit[29:28]	**No_Soft_Reset for Port 2** ▪ Bit[0]: No_Soft_Reset. **Power Management Capability for Port 2** ▪ Bit[3:1]: AUX Current ▪ Bit[4]: read only as 1 to indicate Bridge supports the D1 power management state ▪ Bit[5]: read only as 1 to indicate Bridge supports the D2 power management state ▪ Bit[7:6]: PME Support for D2 and D1 states
55h	84h (Port 2) 84h – Bit[31:24]	**Power Management Data for Port 2** ▪ Bit[15:8]: read only as Data register
56h	84h (Port 3) 84h – Bit[3] 80h (Port 3) 80h – Bit[24:22] 80h – Bit[25] 80h – Bit[26] 80h – Bit[29:28]	**No_Soft_Reset for Port 3** ▪ Bit[0]: No_Soft_Reset. **Power Management Capability for Port 3** ▪ Bit[3:1]: AUX Current ▪ Bit[4]: read only as 1 to indicate Bridge supports the D1 power management state ▪ Bit[5]: read only as 1 to indicate Bridge supports the D2 power management state ▪ Bit[7:6]: PME Support for D2 and D1 states
57h	84h (Port 3) 84h – Bit[31:24]	**Power Management Data for Port 3** ▪ Bit[15:8]: read only as Data register
58h	08h (Func 0) 08h – Bit[23:16] 08h – Bit[31:24]	**Class Code for Func 0** ▪ Bit[7:0]: Sub-Class Code ▪ Bit[15:8]: Base Class Code
5Ah	08h (Func 1) 08h – Bit[23:16] 08h – Bit[31:24]	**Class Code for Func 1** ▪ Bit[7:0]: Sub-Class Code ▪ Bit[15:8]: Base Class Code
5Ch	08h (Func 2) 08h – Bit[23:16] 08h – Bit[31:24]	**Class Code for Func 2** ▪ Bit[7:0]: Sub-Class Code ▪ Bit[15:8]: Base Class Code
5Eh	A4h (Func 0~2) A4h – Bit[15 :0]	**USB Physical Layer Control Register (USB Port 2), Bit[15:0]** ▪ Bit[15:0]: USB Physical Layer Control Register (USB Port 2), Bit[15:0]

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ADDRESS	PCI CFG OFFSET	DESCRIPTION
60h	214h (Port 0) 214h– Bit[7:0] 214h– Bit[9:8] 214h– Bit[12:10] 218h– Bit[0]	**Power Budget Register for Port 0** ▪ Bit[7:0]: Base Power ▪ Bit[9:8]: Data Scale ▪ Bit[12:10]: PM State ▪ Bit[15]: System Allocated
62h	214h (Port 1) 214h– Bit[7:0] 214h– Bit[9:8] 214h– Bit[12:10] 218h– Bit[0]	**Power Budget Register for Port 1** ▪ Bit[7:0]: Base Power ▪ Bit[9:8]: Data Scale ▪ Bit[12:10]: PM State ▪ Bit[15]: System Allocated
64h	214h (Port 2) 214h– Bit[7:0] 214h– Bit[9:8] 214h– Bit[12:10] 218h– Bit[0]	**Power Budget Register for Port 2** ▪ Bit[7:0]: Base Power ▪ Bit[9:8]: Data Scale ▪ Bit[12:10]: PM State ▪ Bit[15]: System Allocated
68h	2Ch ~ 2Dh (Func 0)	**Subsystem Vendor ID for Func 0**
6Ah	2Ch ~ 2Dh (Func 1)	**Subsystem Vendor ID for Func 1**
6Ch	2Ch ~ 2Dh (Func 2)	**Subsystem Vendor ID for Func 2**
6Eh	E8h (Func 1) E8h – Bit[0] E8h – Bit[1] E8h – Bit[2] E8h – Bit[3] E8h – Bit[7 :5] E8h – Bit[10]	**PCI Express Capability for Func 1** ▪ Bi[0]: Correctable Error Reporting Enable ▪ Bit[1]: Non-Fatal Error Reporting Enable ▪ Bit[2]: Fatal Error Reporting Enable ▪ Bit[3]: Unsupported Request Reporting Enable ▪ Bit[7:5]: Max_Payload_Size ▪ Bit[10]: Auxiliary (AUX) Power PM Enable
70h	BCh (Port 0) BCh – Bit[16] BCh – Bit[17] BCh – Bit[18] BCh – Bit[19] BCh – Bit[21:20] BCh – Bit[25:22] BCh – Bit[29:26] BCh – Bit[30]	**Physical Layer Control 2, Bit[30:16] for Port 0** ▪ Bit[0]: Per-Lane Main Drive Offset Enable (Margining) ▪ Bit[1]: Per-Lane Main Drive Offset Enable (Nominal) ▪ Bit[2]: Per-Lane De-Emphasis Drive Offset Enable (Margining) ▪ Bit[3]: Per-Lane De-Emphasis Drive Offset Enable (Nominal) ▪ Bit[5:4]: Receiver Signal Detection ▪ Bit[9:6]: Receiver Equalization ▪ Bit[13:10]: Reserved ▪ Bit[14] : Transmitter Swing
72h	BCh (Port 1) BCh – Bit[16] BCh – Bit[17] BCh – Bit[18] BCh – Bit[19] BCh – Bit[21:20] BCh – Bit[25:22] BCh – Bit[29:26] BCh – Bit[30]	**Physical Layer Control 2, Bit[30:16] for Port 1** ▪ Bit[0]: Per-Lane Main Drive Offset Enable (Margining) ▪ Bit[1]: Per-Lane Main Drive Offset Enable (Nominal) ▪ Bit[2]: Per-Lane De-Emphasis Drive Offset Enable (Margining) ▪ Bit[3]: Per-Lane De-Emphasis Drive Offset Enable (Nominal) ▪ Bit[5:4]: Receiver Signal Detection ▪ Bit[9:6]: Receiver Equalization ▪ Bit[13:10]: Reserved ▪ Bit[14] : Transmitter Swing
74h	BCh (Port 2) BCh – Bit[16] BCh – Bit[17] BCh – Bit[18] BCh – Bit[19] BCh – Bit[21:20] BCh – Bit[25:22] BCh – Bit[29:26] BCh – Bit[30]	**Physical Layer Control 2, Bit[30:16] for Port 2** ▪ Bit[0]: Per-Lane Main Drive Offset Enable (Margining) ▪ Bit[1]: Per-Lane Main Drive Offset Enable (Nominal) ▪ Bit[2]: Per-Lane De-Emphasis Drive Offset Enable (Margining) ▪ Bit[3]: Per-Lane De-Emphasis Drive Offset Enable (Nominal) ▪ Bit[5:4]: Receiver Signal Detection ▪ Bit[9:6]: Receiver Equalization ▪ Bit[13:10]: Reserved ▪ Bit[14] : Transmitter Swing
78h	2Eh ~ 2Fh (Func 0)	**Subsystem ID for Func 0**
7Ah	2Eh ~ 2Fh (Func 1)	**Subsystem ID for Func 1**
7Ch	2Eh ~ 2Fh (Func 2)	**Subsystem ID for Func 2**
80h	BCh (Port 0) BCh – Bit[8] BCh – Bit[10 :9] BCh – Bit[12 :11]	**Physical Layer Control 2, Bit[12:8] for Port 0** ▪ Bit [0]: CDR Loop Bandwidth Enable ▪ Bit [2:1]: CDR Threshold ▪ Bit [4:3]: CDR Loop Bandwidth Gain

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ADDRESS	PCI CFG OFFSET	DESCRIPTION
82h	BCh (Port 1) BCh – Bit[8] BCh – Bit[10 :9] BCh – Bit[12 :11]	**Physical Layer Control 2, Bit[12:8] for Port 1** ▪ Bit [0]: CDR Loop Bandwidth Enable ▪ Bit [2:1]: CDR Threshold ▪ Bit [4:3]: CDR Loop Bandwidth Gain
84h	BCh (Port 2) BCh – Bit[8] BCh – Bit[10 :9] BCh – Bit[12 :11]	**Physical Layer Control 2, Bit[12:8] for Port 2** ▪ Bit [0]: CDR Loop Bandwidth Enable ▪ Bit [2:1]: CDR Threshold ▪ Bit [4:3]: CDR Loop Bandwidth Gain
88h	34h (Func 0) 34h – Bit[7:0]	**Capabilities Pointer for Func 0** ▪ Bit[7:0]: Capabilities Pointer
8Ah	34h (Func 1) 34h – Bit[7:0]	**Capabilities Pointer for Func 1** ▪ Bit[7:0]: Capabilities Pointer
8Ch	34h (Func 2) 34h – Bit[7:0]	**Capabilities Pointer for Func 2** ▪ Bit[7:0]: Capabilities Pointer
8Eh	A8h (Func 0~2) A8h – Bit[15 :0]	**USB Physical Layer Control Register (USB Port 3), Bit[15:0]** ▪ Bit[15:0]: USB Physical Layer Control Register (USB Port 3), Bit[15:0]
90h	B4h (Port 0) B4h – Bit[9:8] B4h – Bit[11:10] B4h – Bit[13:12] B4h (Port 0) B4h – Bit[14] B0h (Port 0) B0h – Bit[31]	**PM Control Parameter for Port 0** ▪ Bit[1:0] : D3 enters L1 ▪ Bit[3:2] : L1 delay count select ▪ Bit[5:4] : L0s enable **Rx Polarity Inversion Disable for port 0** ▪ Bit[6] : RX Polarity Inversion Disable **Decode VGA for Port 0** ▪ Bit[7]
92h	B4h (Port 1) B4h – Bit[9:8] B4h – Bit[11:10] B4h – Bit[13:12] B4h (Port 1) B4h – Bit[14] B0h (Port 1) B0h – Bit[31]	**PM Control Parameter for Port 1** ▪ Bit[1:0] : D3 enters L1 ▪ Bit[3:2] : L1 delay count select ▪ Bit[5:4] : L0s enable **Rx Polarity Inversion Disable for port 1** ▪ Bit[6] : RX Polarity Inversion Disable **Decode VGA for Port 1** ▪ Bit[7]
94h	B4h (Port 2) B4h – Bit[9:8] B4h – Bit[11:10] B4h – Bit[13:12] B4h (Port 2) B4h – Bit[14] B0h (Port 2) B0h – Bit[31]	**PM Control Parameter for Port 2** ▪ Bit[1:0] : D3 enters L1 ▪ Bit[3:2] : L1 delay count select ▪ Bit[5:4] : L0s enable **Rx Polarity Inversion Disable for port 2** ▪ Bit[6] : RX Polarity Inversion Disable **Decode VGA for Port 2** ▪ Bit[7]
98h	80h (Func 0) 80h – Bit[15:8] 80h – Bit[21] 80h – Bit[24:22] 80h – Bit[25] 80h – Bit[26]	**Power Management Capability for Func 0** ▪ Bit[7:0]: Next Item Pointer ▪ Bit[8]: Device Specific Initialization ▪ Bit[11:9]: AUX Current ▪ Bit[12]: D1 Power State Support ▪ Bit[13]: D2 Power State Support
9Ah	80h (Func 1) 80h – Bit[15:8] 80h – Bit[21] 80h – Bit[24:22] 80h – Bit[25] 80h – Bit[26]	**Power Management Capability for Func 1** ▪ Bit[7:0]: Next Item Pointer ▪ Bit[8]: Device Specific Initialization ▪ Bit[11:9]: AUX Current ▪ Bit[12]: D1 Power State Support ▪ Bit[13]: D2 Power State Support
9Ch	80h (Func 2) 80h – Bit[15:8] 80h – Bit[21] 80h – Bit[24:22] 80h – Bit[25] 80h – Bit[26]	**Power Management Capability for Func 2** ▪ Bit[7:0]: Next Item Pointer ▪ Bit[8]: Device Specific Initialization ▪ Bit[11:9]: AUX Current ▪ Bit[12]: D1 Power State Support ▪ Bit[13]: D2 Power State Support

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ADDRESS	PCI CFG OFFSET	DESCRIPTION
9Eh	ACh (Func 0~2) ACh – Bit[15 :0]	**USB Physical Layer Control Register (USB Port 4), Bit[15:0]** ▪ Bit[15:0]: USB Physical Layer Control Register (USB Port 4), Bit[15:0]
A0h	B0h (Port 0) B0h – Bit[12 :0]	**Replay Time-out Counter for Port 0** ▪ Bit[12:0]: Replay Time-out Counter
A2h	B0h (Port 1) B0h – Bit[12 :0]	**Replay Time-out Counter for Port 1** ▪ Bit[12:0]: Replay Time-out Counter
A4h	B0h (Port 2) B0h – Bit[12 :0]	**Replay Time-out Counter for Port 2** ▪ Bit[12:0]: Replay Time-out Counter
A8h	80h (Func 0) 80h – Bit[31 :27] 84h (Func 0) 84h – Bit[3] 8Ch (Func 0) 8Ch – Bit[15 :8]	**Power Management Capability for Func 0** ▪ Bit[4:0]: PME# Support **Power Management Data for Func 0** ▪ Bit[5]: No_Soft_Reset **Next Item Pointer for Func 0** Bit[15:8]: Next Item Pointer
AAh	80h (Func 1) 80h – Bit[31 :27] 84h (Func 1) 84h – Bit[3] 8Ch (Func 1) 8Ch – Bit[15 :8]	**Power Management Capability for Func 1** ▪ Bit[4:0]: PME# Support **Power Management Data for Func 1** ▪ Bit[5]: No_Soft_Reset **Next Item Pointer for Func 1** Bit[15:8]: Next Item Pointer
ACh	80h (Func 2) 80h – Bit[31 :27] 84h (Func 2) 84h – Bit[3] 8Ch (Func 2) 8Ch – Bit[15 :8]	**Power Management Capability for Func 2** ▪ Bit[4:0]: PME# Support **Power Management Data for Func 2** ▪ Bit[5]: No_Soft_Reset **Next Item Pointer for Func 2** Bit[15:8]: Next Item Pointer
AEh	E8h (Func 2) E8h – Bit[0] E8h – Bit[1] E8h – Bit[2] E8h – Bit[3] E8h – Bit[7 :5] E8h – Bit[10]	**PCI Express Capability for Func 2** ▪ Bit[0]: Correctable Error Reporting Enable ▪ Bit[1]: Non-Fatal Error Reporting Enable ▪ Bit[2]: Fatal Error Reporting Enable ▪ Bit[3]: Unsupported Request Reporting Enable ▪ Bit[7:5]: Max_Payload_Size ▪ Bit[10]: Auxiliary (AUX) Power PM Enable
B0h	B0h (Port 0) B0h – Bit[30 :16]	**Acknowledge Latency Timer for Port 0** ▪ Bit[14:0]: Acknowledge Latency Timer
B2h	B0h (Port 1) B0h – Bit[30 :16]	**Acknowledge Latency Timer for Port 1** ▪ Bit[14:0]: Acknowledge Latency Timer
B4h	B0h (Port 2) B0h – Bit[30 :16]	**Acknowledge Latency Timer for Port 2** ▪ Bit[14:0]: Acknowledge Latency Timer
B8h	E0h (Func 0) E0h – Bit[7 :0] E0h – Bit[15 :8]	**PCI Express Capability for Func 0** ▪ Bit[7:0]: Enhanced Capabilities ID ▪ Bit[15:8]: Next Item Pointer
BAh	E0h (Func 1) E0h – Bit[7 :0] E0h – Bit[15 :8]	**PCI Express Capability for Func 1** ▪ Bit[7:0]: Enhanced Capabilities ID ▪ Bit[15:8]: Next Item Pointer
BCh	E0h (Func 2) E0h – Bit[7 :0] E0h – Bit[15 :8]	**PCI Express Capability for Func 2** ▪ Bit[7:0]: Enhanced Capabilities ID ▪ Bit[15:8]: Next Item Pointer
C0h	C0h – Bit[6 :0]	**Physical Layer Control 3 for Port 0** ▪ Bit [6:0]: Lane Mode
C8h	E0h (Func 0) E0h – Bit[19 :16] E0h – Bit[23 :20]	**PCI Express Capability for Func 0** ▪ Bit[3:0]: Capability Version ▪ Bit[7:4]: Device/Port Type
CAh	E0h (Func 1) E0h – Bit[19 :16] E0h – Bit[23 :20]	**PCI Express Capability for Func 1** ▪ Bit[3:0]: Capability Version ▪ Bit[7:4]: Device/Port Type
CCh	E0h (Func 2) E0h – Bit[19 :16] E0h – Bit[23 :20]	**PCI Express Capability for Func 2** ▪ Bit[3:0]: Capability Version ▪ Bit[7:4]: Device/Port Type

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ADDRESS	PCI CFG OFFSET	DESCRIPTION
CEh	A0h (Func 0~2) A0h – Bit[23 :16] A4h (Func 0~2) A4h – Bit[23 :16]	**USB Physical Control Register (USB Port 1), Bit[23:16]** ▪ Bit[7:0]: USB Physical Control Register (USB Port 1), Bit[23:16] **USB Physical Control Register (USB Port 2), Bit[23:16]** ▪ Bit[15:8]: USB Physical Control Register (USB Port 1), Bit[23:16]
D8h	E4h (Func 0) E4h – Bit[2 :0] E4h – Bit[8 :6] E4h – Bit[11 :9] E4h – Bit[15]	**Device Capability 0 for Func 0** ▪ Bit[2:0]: Max_Payload_Size Supported ▪ Bit[8:6]: Endpoint Los Acceptable Latency ▪ Bit[11:9]: Endpoint L1 Acceptable Latency ▪ Bit[15]: Role_Base Error Reporting
DAh	E4h (Func 1) E4h – Bit[2 :0] E4h – Bit[8 :6] E4h – Bit[11 :9] E4h – Bit[15]	**Device Capability 0 for Func 1** ▪ Bit[2:0]: Max_Payload_Size Supported ▪ Bit[8:6]: Endpoint Los Acceptable Latency ▪ Bit[11:9]: Endpoint L1 Acceptable Latency ▪ Bit[15]: Role_Base Error Reporting
DCh	E4h (Func 2) E4h – Bit[2 :0] E4h – Bit[8 :6] E4h – Bit[11 :9] E4h – Bit[15]	**Device Capability 0 for Func 2** ▪ Bit[2:0]: Max_Payload_Size Supported ▪ Bit[8:6]: Endpoint Los Acceptable Latency ▪ Bit[11:9]: Endpoint L1 Acceptable Latency ▪ Bit[15]: Role_Base Error Reporting
DEh	A8h (Func 0~2) A8h – Bit[23 :16] ACh (Func 0~2) ACh – Bit[23 :16]	**USB Physical Control Register (USB Port 3), Bit[23:16]** ▪ Bit[7:0]: USB Physical Control Register (USB Port 1), Bit[23:16] **USB Physical Control Register (USB Port 4), Bit[23:16]** ▪ Bit[15:8]: USB Physical Control Register (USB Port 1), Bit[23:16]
E8h	E4h (Func 0) E4h – Bit[25 :18] E4h – Bit[27 :26]	**PCI Express Capability 1 for Func 0** ▪ Bit[9:2]: Captured Slot Power Limit Value ▪ Bit[11:10]: Captured Slot Power Limit Scale
EAh	E4h (Func 1) E4h – Bit[25 :18] E4h – Bit[27 :26]	**PCI Express Capability 1 for Func 1** ▪ Bit[9:2]: Captured Slot Power Limit Value ▪ Bit[11:10]: Captured Slot Power Limit Scale
ECh	E4h (Func 2) E4h – Bit[25 :18] E4h – Bit[27 :26]	**PCI Express Capability 1 for Func 2** ▪ Bit[9:2]: Captured Slot Power Limit Value ▪ Bit[11:10]: Captured Slot Power Limit Scale

6.2 SMBus INTERFACE

The Swidge provides the System Management Bus (SMBus), a two-wire interface through which a simple device can communicate with the rest of the system. The SMBus interface on the Swidge is a bi-directional slave interface. It can receive data from the SMBus master or send data to the master. The interface allows full access to the configuration registers. A SMBus master, such as the processor or other SMBus devices, can read or write to every RW configuration register (read/write register). In addition, the RO and HwInt registers (read-only and hardware initialized registers) that can be auto-loaded by the EEPROM interface can also be read and written by the SMBus interface. This feature allows increases in the system expandability and flexibility in system implementation.

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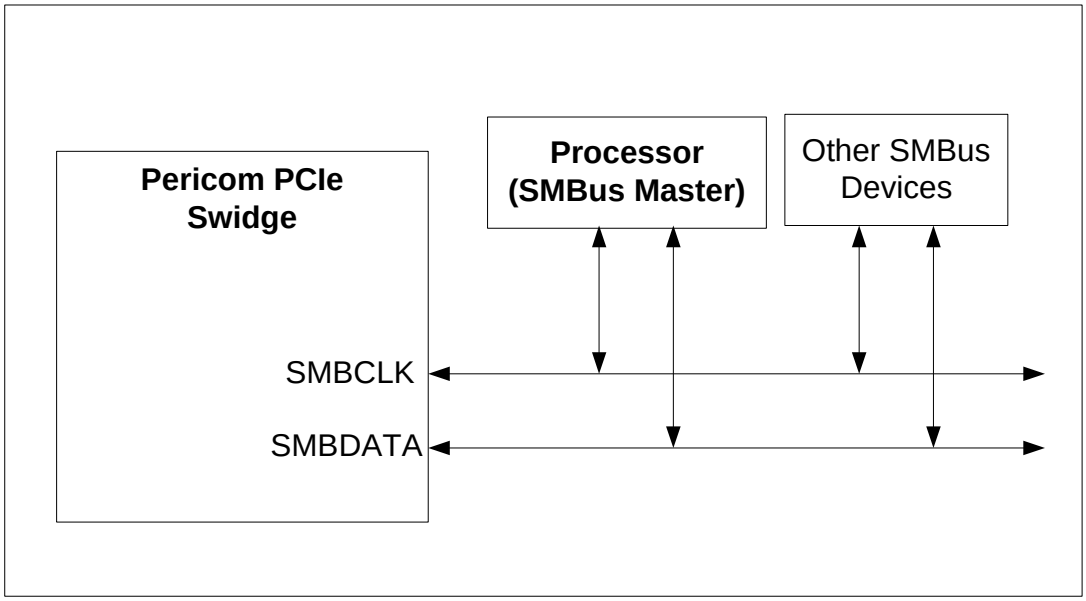

Figure 6-1 SMBus Architecture Implementation on PI7C9X440SL

The SMBus interface on the Swidge consists of one SMBus clock pin (SMBCLK), a SMBus data pin (SMBDATA), and 3 SMBus address pins (GPIO[5:7]). The SMBus clock pin provides or receives the clock signal. The SMBus data pin facilitates the data transmission and reception. Both of the clock and data pins are bi-directional. The SMBus address pins determine the address to which the Swidge responds to. The SMBus address pins generate addresses according to the following table:

Table 6-1 SMBus Address Pin Configuration

BIT	SMBus Address
0	GPIO[5]
1	GPIO[6]
2	GPIO[7]
3	1
4	0
5	1
6	1

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7 REGISTER DESCRIPTION

7.1 REGISTER TYPES

REGISTER TYPE	DEFINITION
HwInt	Hardware Initialization
RO	Read Only
RW	Read / Write
RWC	Read / Write 1 to Clear
RWCS	Sticky - Read Only / Write 1 to Clear
RWS	Sticky - Read / Write
ROS	Sticky – Read Only

7.2 PCI EXPRESS CONFIGURATION REGISTERS

When the PCI Express port of the Swidge is set to operate at the transparent mode, it is represented by a logical PCI-to-PCI bridge that implements type 1 configuration space header. The following table details the allocation of the register fields of the PCI 2.3 compatible type 1 configuration space header.

31 –24	23 – 16	15 - 8	7 –0	BYTE OFFSET
Device ID		Vendor ID		00h
Primary Status		Command		04h
Class Code			Revision ID	08h
Reserved	Header Type	Primary Latency Timer	Cache Line Size	0Ch
Reserved				10h – 17h
Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	18h
Secondary Status		I/O Limit Address	I/O Base Address	1Ch
Memory Limit Address		Memory Base Address		20h
Prefetchable Memory Limit Address		Prefetchable Memory Base Address		24h
Prefetchable Memory Base Address Upper 32-bit				28h
Prefetchable Memory Limit Address Upper 32-bit				2Ch
I/O Limit Address Upper 16-bit		I/O Base Address Upper 16-bit		30h
Reserved			Capability Pointer to 80h	34h
Reserved				38h
Bridge Control		Interrupt Pin	Interrupt Line	3Ch
Reserved				40h – 7Fh
Power Management Capabilities		Next Item Pointer=8C	Capability ID=01	80h
PM Data	PPB Support Extensions	Power Management Data		84h
Message Control		Next Item Pointer=9C	Capability ID=05	8Ch
Message Address				90h
Message Upper Address				94h
Reserved		Message Data		98h
VPD Register		Next Item Pointer=A4	Capability ID=03	9Ch
VPD Data Register				A0h
Length in Bytes (14h)		Next Item Pointer=C0	Capability ID=09	A4h
XPIP_CSR0				A8h
XPIP_CSR1				ACh
ACK Latency Timer		Replay Time-out Counter		B0h
Physical Layer Control 0		Switch Operation Mode		B4h
Physical Layer Control 1		XPIP CSR2 / TL CSR		B8h
Physical Layer Control 2				BCh
Reserved			Lane Mode	C0h
Reserved		Next Item Pointer=E0	SSID/SSVID Capability ID=0D	C4h
SSID		SSVID		C8h
Reserved				C8h – D7h

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31 –24	23 – 16	15 - 8	7 –0	BYTE OFFSET
GPIO Data and Control				D8h
EEPROM Data		EEPROM Address	EEPROM Control	DCh
PCI Express Capabilities Register		Next Item Pointer=00	Capability ID=10	E0h
Device Capabilities				E4h
Device Status		Device Control		E8h
Link Capabilities				ECh
Link Status		Link Control		F0h
Slot Capabilities				F4h
Slot Status		Slot Control		F8h
Reserved				FCh

Other than the PCI 2.3 compatible configuration space header, the Swidge also implements PCI express extended configuration space header, which includes advanced error reporting, virtual channel, and power budgeting capability registers. The following table details the allocation of the register fields of PCI express extended capability space header. The first extended capability always begins at offset 100h with a PCI Express Enhanced Capability header and the rest of capabilities are located at an offset greater than 0FFh relative to the beginning of PCI compatible configuration space.

31 –24	23 – 16	15 - 8	7 –0	BYTE OFFSET
Next Capability Offset	Cap. Version	PCI Express Extended Capability ID=0001h		100h
Uncorrectable Error Status Register				104h
Uncorrectable Error Mask Register				108h
Uncorrectable Error Severity Register				10Ch
Correctable Error Status Register				110h
Correctable Error Mask Register				114h
Advanced Error Capabilities and Control Register				118h
Header Log Register				11Ch – 128h
Reserved				12Ch – 13Fh
Next Capability Offset=20Ch	Cap. Version	PCI Express Extended Capability ID=0002h		140h
Port VC Capability Register 1				144h
VC Arbitration Table Offset=3	Port VC Capability Register 2			148h
Port VC Status Register		Port VC Control Register		14Ch
Port Arbitration Table Offset=4	VC Resource Capability Register (0)			150h
VC Resource Control Register (0)				154h
VC Resource Status Register (0)		Reserved		158h
Reserved				15Ch-17Ch
Port Arbitration Table with 128 Phases for VC0				180h – 1BCh
Reserved				1C0h – 1FCh
Reserved				200h – 20Bh
Next Capability Offset=000h	Cap. Version	PCI Express Extended Capability ID=0004h		20Ch
Reserved			Data Select Register	210h
Data Register				214h
Reserved			Power Budget Capability Register	218h

7.2.1 VENDOR ID REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Vendor ID	RO	Identifies Pericom as the vendor of this device. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 12D8h.

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7.2.2 DEVICE ID REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Device ID	RO	Identifies this device as the PI7C9X440. The default value may be changed by SMBus or auto-loading from EEPROM. Resets to 400Ch.

7.2.3 COMMAND REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
0	I/O Space Enable	RW	0b: Ignores I/O transactions on the primary interface 1b: Enables responses to I/O transactions on the primary interface Resets to 0b.
1	Memory Space Enable	RW	0b: Ignores memory transactions on the primary interface 1b: Enables responses to memory transactions on the primary interface Reset to 0b.
2	Bus Master Enable	RW	0b: Does not initiate memory or I/O transactions on the upstream port and handles as an Unsupported Request (UR) to memory and I/O transactions on the downstream port. For Non-Posted Requests, a completion with UR completion status must be returned 1b: Enables the Swidge Port to forward memory and I/O Read/Write transactions in the upstream direction Reset to 0b.
3	Special Cycle Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
4	Memory Write And Invalidate Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
5	VGA Palette Snoop Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
6	Parity Error Response Enable	RW	0b: Swidge may ignore any parity errors that it detects and continue normal operation 1b: Swidge must take its normal action when a parity error is detected Reset to 0b.
7	Wait Cycle Control	RO	Does not apply to PCI Express. Must be hardwired to 0.
8	SERR# enable	RW	0b: Disables the reporting of Non-fatal and Fatal errors detected by the Swidge to the Root Complex b1: Enables the Non-fatal and Fatal error reporting to Root Complex Reset to 0b.
9	Fast Back-to-Back Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
10	Interrupt Disable	RW	Controls the ability of a PCI Express device to generate INTx Interrupt Messages. In the Swidge, this bit does not affect the forwarding of INTx messages from the downstream ports. Reset to 0b.
15:11	Reserved	RO	Reset to 0b.

7.2.4 PRIMARY STATUS REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
18:16	Reserved	RO	Reset to 000b.
19	Interrupt Status	RO	Indicates that an INTx Interrupt Message is pending internally to the device. In the Swidge, the forwarding of INTx messages from the downstream device of the Swidge port is not reflected in this bit. Must be hardwired to 0b.
20	Capabilities List	RO	Set to 1 to enable support for the capability list (offset 34h is the pointer to the data structure).

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BIT	FUNCTION	TYPE	DESCRIPTION
			Reset to 1b.
21	66MHz Capable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
22	Reserved	RO	Reset to 0b.
23	Fast Back-to-Back Capable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
24	Master Data Parity Error	RWC	Set to 1 (by a requester) whenever a Parity error is detected or forwarded on the primary side of the port in a Swidge. If the Parity Error Response Enable bit is cleared, this bit is never set. Reset to 0b.
26:25	DEVSEL# timing	RO	Does not apply to PCI Express. Must be hardwired to 0b.
27	Signaled Target Abort	RO	Set to 1 (by a completer) whenever completing a request on the primary side using the Completer Abort Completion Status. Reset to 0b.
28	Received Target Abort	RO	Set to 1 (by a requestor) whenever receiving a Completion with Completer Abort Completion Status on the primary side. Reset to 0b.
29	Received Master Abort	RO	Set to 1 (by a requestor) whenever receiving a Completion with Unsupported Request Completion Status on primary side. Reset to 0b.
30	Signaled System Error	RWC	Set to 1 when the Swidge sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1. Reset to 0b.
31	Detected Parity Error	RWC	Set to 1 whenever the primary side of the port in a Swidge receives a Poisoned TLP. Reset to 0b.

7.2.5 REVISION ID REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Revision	RO	Indicates revision number of device. Hardwired to 00h.

7.2.6 CLASS CODE REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Programming Interface	RO	Read as 00h to indicate no programming interfaces have been defined for PCI-to-PCI Bridges.
23:16	Sub-Class Code	RO	Read as 04h to indicate device is a PCI-to-PCI Bridge.
31:24	Base Class Code	RO	Read as 06h to indicate device is a Bridge device.

7.2.7 CACHE LINE REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Cache Line Size	RW	The cache line size register is set by the system firmware and the operating system cache line size. This field is implemented by PCI Express devices as a RW field for legacy compatibility, but it has no impact on any PCI Express device functionality. Reset to 0b.

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7.2.8 PRIMARY LATENCY TIMER REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Primary Latency timer	RO	Does not apply to PCI Express. Must be hardwired to 00h.

7.2.9 HEADER TYPE REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
23:16	Header Type	RO	Read as 01h to indicate that the register layout conforms to the standard PCI-to-PCI Bridge layout.

7.2.10 PRIMARY BUS NUMBER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Primary Bus Number	RW	Indicates the number of the PCI bus to which the primary interface is connected. The value is set in software during configuration. Reset to 00h.

7.2.11 SECONDARY BUS NUMBER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Secondary Bus Number	RW	Indicates the number of the PCI bus to which the secondary interface is connected. The value is set in software during configuration. Reset to 00h.

7.2.12 SUBORDINATE BUS NUMBER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION
23:16	Subordinate Bus Number	RW	Indicates the number of the PCI bus with the highest number that is subordinate to the Bridge. The value is set in software during configuration. Reset to 00h.

7.2.13 SECONDARY LATENCY TIMER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION
31:24	Secondary Latency Timer	RO	Does not apply to PCI Express. Must be hardwired to 00h.

7.2.14 I/O BASE ADDRESS REGISTER – OFFSET 1Ch

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	32-bit Indicator	RO	Read as 01h to indicate 32-bit I/O addressing.
7:4	I/O Base Address [15:12]	RW	Defines the bottom address of the I/O address range for the Bridge to determine when to forward I/O transactions from one interface to the other. The upper 4 bits correspond to address bits [15:12] and are writable. The lower 12 bits corresponding to address bits [11:0] are assumed to be 0. The upper 16 bits corresponding to address bits [31:16] are defined in the I/O base

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BIT	FUNCTION	TYPE	DESCRIPTION
			address upper 16 bits address register. Reset to 0h.

7.2.15 I/O LIMIT ADDRESS REGISTER – OFFSET 1Ch

BIT	FUNCTION	TYPE	DESCRIPTION
11:8	32-bit Indicator	RO	Read as 01h to indicate 32-bit I/O addressing.
15:12	I/O Limit Address [15:12]	RW	Defines the top address of the I/O address range for the Bridge to determine when to forward I/O transactions from one interface to the other. The upper 4 bits correspond to address bits [15:12] and are writable. The lower 12 bits corresponding to address bits [11:0] are assumed to be FFFh. The upper 16 bits corresponding to address bits [31:16] are defined in the I/O limit address upper 16 bits address register. Reset to 0h.

7.2.16 SECONDARY STATUS REGISTER – OFFSET 1Ch

BIT	FUNCTION	TYPE	DESCRIPTION
20:16	Reserved	RO	Reset to 00000b.
21	66MHz Capable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
22	Reserved	RO	Reset to 0b.
23	Fast Back-to-Back Capable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
24	Master Data Parity Error	RWC	Set to 1 (by a requester) whenever a Parity error is detected or forwarded on the secondary side of the port in a Swidge. If the Parity Error Response Enable bit is cleared, this bit is never set. Reset to 0b.
26:25	DEVSEL_L timing	RO	Does not apply to PCI Express. Must be hardwired to 0b.
27	Signaled Target Abort	RO	Set to 1 (by a completer) whenever completing a request in the secondary side using Completer Abort Completion Status. Reset to 0b.
28	Received Target Abort	RO	Set to 1 (by a requestor) whenever receiving a Completion with Completer Abort Completion Status in the secondary side. Reset to 0b.
29	Received Master Abort	RO	Set to 1 (by a requestor) whenever receiving a Completion with Unsupported Request Completion Status in secondary side. Reset to 0b.
30	Received System Error	RWC	Set to 1 when the Swidge sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Bridge Control register is 1. Reset to 0b.
31	Detected Parity Error	RWC	Set to 1 whenever the secondary side of the port in a Swidge receives a Poisoned TLP. Reset to 0b.

7.2.17 MEMORY BASE ADDRESS REGISTER – OFFSET 20h

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	Reserved	RO	Reset to 0h.
15:4	Memory Base Address [15:4]	RW	Defines the bottom address of an address range for the Bridge to determine when to forward memory transactions from one interface to the other. The

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BIT	FUNCTION	TYPE	DESCRIPTION
			upper 12 bits correspond to address bits [31:20] and are able to be written to. The lower 20 bits corresponding to address bits [19:0] are assumed to be 0. Reset to 000h.

7.2.18 MEMORY LIMIT ADDRESS REGISTER – OFFSET 20h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Reserved	RO	Reset to 0h.
31:20	Memory Limit Address [31:20]	RW	Defines the top address of an address range for the Bridge to determine when to forward memory transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are writable. The lower 20 bits corresponding to address bits [19:0] are assumed to be FFFFFh. Reset to 000h.

7.2.19 PREFETCHABLE MEMORY BASE ADDRESS REGISTER – OFFSET 24h

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	64-bit addressing	RO	Read as 0001b to indicate 64-bit addressing.
15:4	Prefetchable Memory Base Address [31:20]	RW	Defines the bottom address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are writable. The lower 20 bits are assumed to be 0. The memory base register upper 32 bits contain the upper half of the base address. Reset to 000h.

7.2.20 PREFETCHABLE MEMORY LIMIT ADDRESS REGISTER – OFFSET 24h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	64-bit addressing	RO	Read as 0001b to indicate 64-bit addressing.
31:20	Prefetchable Memory Limit Address [31:20]	RW	Defines the top address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. The upper 12 bits correspond to address bits [31:20] and are writable. The lower 20 bits are assumed to be FFFFFh. The memory limit upper 32 bits register contains the upper half of the limit address. Reset to 000h.

7.2.21 PREFETCHABLE MEMORY BASE ADDRESS UPPER 32-BITS REGISTER – OFFSET 28h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Prefetchable Memory Base Address, Upper 32-bits [63:32]	RW	Defines the upper 32-bits of a 64-bit bottom address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. Reset to 00000000h.

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7.2.22 PREFETCHABLE MEMORY LIMIT ADDRESS UPPER 32-BITS REGISTER – OFFSET 2Ch

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Prefetchable Memory Limit Address, Upper 32-bits [63:32]	RW	Defines the upper 32-bits of a 64-bit top address of an address range for the Bridge to determine when to forward memory read and write transactions from one interface to the other. Reset to 00000000h.

7.2.23 I/O BASE ADDRESS UPPER 16-BITS REGISTER – OFFSET 30h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	I/O Base Address, Upper 16-bits [31:16]	RW	Defines the upper 16-bits of a 32-bit bottom address of an address range for the Bridge to determine when to forward I/O transactions from one interface to the other. Reset to 0000h.

7.2.24 I/O LIMIT ADDRESS UPPER 16-BITS REGISTER – OFFSET 30h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	I/O Limit Address, Upper 16-bits [31:16]	RW	Defines the upper 16-bits of a 32-bit top address of an address range for the Bridge to determine when to forward I/O transactions from one interface to the other. Reset to 0000h.

7.2.25 CAPABILITY POINTER REGISTER – OFFSET 34h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Capability Pointer	RO	Pointer points to the PCI power management registers (80h). Reset to 80h.

7.2.26 INTERRUPT LINE REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Interrupt Line	RW	Reset to 00h.

7.2.27 INTERRUPT PIN REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Interrupt Pin	RO	The Swidge implements INTA virtual wire interrupt signals to represent hot-plug events at downstream ports. The default value on the downstream ports may be changed by SMBus or auto-loading from EEPROM. Reset to 00h.

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7.2.28 BRIDGE CONTROL REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
16	Parity Error Response	RW	0b: Ignore Poisoned TLPs on the secondary interface 1b: Enable the Poisoned TLPs reporting and detection on the secondary interface Reset to 0b.
17	S_SERR# enable	RW	0b: Disables the forwarding of EER_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary interface 1b: Enables the forwarding of EER_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary interface Reset to 0b.
18	ISA Enable	RW	0b: Forwards downstream all I/O addresses in the address range defined by the I/O Base, I/O Base, and Limit registers 1b: Forwards upstream all I/O addresses in the address range defined by the I/O Base and Limit registers that are in the first 64KB of PCI I/O address space (top 768 bytes of each 1KB block) Reset to 0b.
19	VGA Enable	RW	0: Ignores access to the VGA memory or IO address range 1: Forwards transactions targeted at the VGA memory or IO address range VGA memory range starts from 000A 0000h to 000B FFFFh VGA IO addresses are in the first 64KB of IO address space. AD [9:0] is in the ranges 3B0 to 3BBh and 3C0h to 3DFh. Reset to 0b. Please note that this bit is reserved in Port 2.
20	VGA 16-bit decode	RW	0b: Executes 10-bit address decoding on VGA I/O accesses 1b: Executes 16-bit address decoding on VGA I/O accesses Reset to 0b. Please note that this bit is reserved in Port 2.
21	Master Abort Mode	RO	Does not apply to PCI Express. Must be hardwired to 0b.
22	Secondary Bus Reset	RW	0b: Does not trigger a hot reset on the corresponding PCI Express Port 1b: Triggers a hot reset on the corresponding PCI Express Port At the downstream port, it asserts PORT_RST# to the attached downstream device. At the upstream port, it asserts the PORT_RST# at all the downstream ports. Reset to 0b.
23	Fast Back-to-Back Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
24	Primary Master Timeout	RO	Does not apply to PCI Express. Must be hardwired to 0b.
25	Secondary Master Timeout	RO	Does not apply to PCI Express. Must be hardwired to 0b.
26	Master Timeout Status	RO	Does not apply to PCI Express. Must be hardwired to 0b.
27	Discard Timer SERR# enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
31:28	Reserved	RO	Reset to 0h.

7.2.29 POWER MANAGEMENT CAPABILITY ID REGISTER – OFFSET 80h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 01h to indicate that these are power management enhanced capability registers.

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7.2.30 NEXT ITEM POINTER REGISTER – OFFSET 80h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Item Pointer	RO	At upstream ports, the pointer points to the Vital Protocol Data (VPD) capability register (9Ch). At downstream ports, the pointer points to the Message capability register (8Ch). Reset to 9Ch (Upstream port). Reset to 8Ch (Downstream port).

7.2.31 POWER MANAGEMENT CAPABILITIES REGISTER – OFFSET 80h

BIT	FUNCTION	TYPE	DESCRIPTION
18:16	Power Management Revision	RO	Read as 011b to indicate the device is compliant to Revision 1.2 of *PCI Power Management Interface Specifications.*
19	PME# Clock	RO	Does not apply to PCI Express. Must be hardwired to 0b.
20	Reserved	RO	Reset to 0b.
21	Device Specific Initialization	RO	Read as 0b to indicate Swidge does not have device specific initialization requirements. The default value may be changed by SMBus or auto-loading from EEPROM.
24:22	AUX Current	RO	Reset as 111b to indicate the Swidge needs 375 mA in D3 state. The default value may be changed by SMBus or auto-loading from EEPROM.
25	D1 Power State Support	RO	Read as 1b to indicate Swidge supports the D1 power management state. The default value may be changed by SMBus or auto-loading from EEPROM.
26	D2 Power State Support	RO	Read as 1b to indicate Swidge supports the D2 power management state. The default value may be changed by SMBus or auto-loading from EEPROM.
31:27	PME# Support	RO	Read as 11111b to indicate Swidge supports the forwarding of PME# message in all power states. The default value may be changed by SMBus or auto-loading from EEPROM.

7.2.32 POWER MANAGEMENT DATA REGISTER – OFFSET 84h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Power State	RW	Indicates the current power state of the Swidge. Writing a value of D0 when the previous state was D3 cause a hot reset without asserting DWNRST_L. 00b: D0 state 01b: D1 state 10b: D2 state 11b: D3 hot state Reset to 00b.
2	Reserved	RO	Reset to 0b.
3	No_Soft_Reset	RO	When set, this bit indicates that device transitioning from D3hot to D0 does not perform an internal reset. When clear, an internal reset is performed when power state transits from D3hot to D0. This bit can be rewritten with EEPROM programming. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 1b.
7:4	Reserved	RO	Reset to 0b.
8	PME# Enable	RWS	When asserted, the Swidge will generate the PME# message. Reset to 0b.
12:9	Data Select	RW	Select data registers. Reset to 0h.
14:13	Data Scale	RO	Reset to 00b.
15	PME status	ROS	Read as 0b as the PME# message is not implemented.

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7.2.33 PPB SUPPORT EXTENSIONS – OFFSET 84h

BIT	FUNCTION	TYPE	DESCRIPTION
21:16	Reserved	RO	Reset to 000000b.
22	B2_B3 Support for $D3_{HOT}$	RO	Does not apply to PCI Express. Must be hardwired to 0b.
23	Bus Power / Clock Control Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.

7.2.34 DATA REGISTER – OFFSET 84h

BIT	FUNCTION	TYPE	DESCRIPTION
31:24	Data Register	RO	Data Register. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.

7.2.35 MSI CAPABILITY ID REGISTER – OFFSET 8Ch (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 05h to indicate that this is message signal interrupt capability register.

7.2.36 NEXT ITEM POINTER REGISTER – OFFSET 8Ch (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Item Pointer	RO	Pointer points to Vendor specific capability register (A4h). Reset to A4h.

7.2.37 MESSAGE CONTROL REGISTER – OFFSET 8Ch (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
16	MSI Enable	RW	0b: The function is prohibited from using MSI to request service 1b: The function is permitted to use MSI to request service and is prohibited from using its INTx # pin Reset to 0b.
19:17	Multiple Message Capable	RO	Read as 000b.
22:20	Multiple Message Enable	RW	Reset to 000b.
23	64-bit address capable	RO	0b: The function is not capable of generating a 64-bit message address 1b: The function is capable of generating a 64-bit message address Reset to 1b.
31:24	Reserved	RO	Reset to 00h.

7.2.38 MESSAGE ADDRESS REGISTER – OFFSET 90h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Reserved	RO	Reset to 00b.

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BIT	FUNCTION	TYPE	DESCRIPTION
31:2	Message Address	RW	If the message enable bit is set, the contents of this register specify the DWORD aligned address for MSI memory write transaction. Reset to 0.

7.2.39 MESSAGE UPPER ADDRESS REGISTER – OFFSET 94h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Message Upper Address	RW	This register is only effective if the device supports a 64-bit message address is set. Reset to 00000000h.

7.2.40 MESSAGE DATA REGISTER – OFFSET 98h (Downstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Message Data	RW	Reset to 0000h.

7.2.41 VPD CAPABILITY ID REGISTER – OFFSET 9Ch (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 03h to indicate that these are VPD enhanced capability registers. Reset to 03h.

7.2.42 NEXT ITEM POINTER REGISTER – OFFSET 9Ch (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Item Pointer	RO	Pointer points to the Vendor specific capability register (A4h). Reset to A4h.

7.2.43 VPD REGISTER – OFFSET 9Ch (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
17:16	Reserved	RO	Reset to 00b.
23:18	VPD Address	RW	Contains DWORD address that is used to generate read or write cycle to the VPD table stored in EEPROM. Reset to 000000b.
30:24	Reserved	RO	Reset to 0000000b.
31	VPD operation	RW	0b: Performs VPD read command to VPD table at the location as specified in VPD address. This bit is kept ‘0’ and then set to ‘1’ automatically after EEPROM cycle is finished 1b: Performs VPD write command to VPD table at the location as specified in VPD address. This bit is kept ‘1’ and then set to ‘0’ automatically after EEPROM cycle is finished. Reset to 0b.

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7.2.44 VPD DATA REGISTER – OFFSET A0h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	VPD Data	RW	When read, it returns the last data read from VPD table at the location as specified in VPD Address. When written, it places the current data into VPD table at the location as specified in VPD Address.

7.2.45 VENDOR SPECIFIC CAPABILITY ID REGISTER – OFFSET A4h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 09h to indicate that these are vendor specific capability registers. Reset to 09h.

7.2.46 NEXT ITEM POINTER REGISTER – OFFSET A4h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Item Pointer	RO	Pointer points to the SSID/SSVID capability register (C0h). Reset to C4h.

7.2.47 LENGTH REGISTER – OFFSET A4h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Length Information	RO	The length field provides the information for number of bytes in the capability structure (including the ID and Next pointer bytes). Reset to 000Ch.

7.2.48 XPIP CSR0 – OFFSET A8h (Test Purpose Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Reserved	RW	Reset to 04001060h.

7.2.49 XPIP CSR1 – OFFSET ACh (Test Purpose Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Reserved	RW	Reset to 04000800h.

7.2.50 REPLAY TIME-OUT COUNTER – OFFSET B0h (Upstream Port)

BIT	FUNCTION	TYPE	DESCRIPTION
11:0	User Replay Timer	RW	A 12-bit register contains a user-defined value. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 000h.

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BIT	FUNCTION	TYPE	DESCRIPTION
12	Enable User Replay Timer	RW	When asserted, the user-defined replay time-out value is be employed. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
13	Power Management Capability Disable	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
14	MSI Capability Disable	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
15	AER Capability Disable	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.

7.2.51 ACKNOWLEDGE LATENCY TIMER – OFFSET B0h

BIT	FUNCTION	TYPE	DESCRIPTION
29:16	User ACK Latency Timer	RW	A 14-bit register contains a user-defined value. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0.
30	Enable User ACK Latency	RW	When asserted, the user-defined ACK latency value is be employed. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
31	VGA Capability Enable	RO	When asserted, the VGA Capability is enabled. The value may be changed by auto-loading from EEPROM. Reset to 1b.

7.2.52 SWITCH OPERATION MODE – OFFSET B4h (Upstream Port)

BIT	FUNCTION	TYPE	DESCRIPTION
0	Store-Forward	RW	When set, a store-forward mode is used. Otherwise, the chip is working under cut-through mode. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
2:1	Cut-through Threshold	RW	Cut-through Threshold. When forwarding a packet from low-speed port to high-speed mode, the chip provides the capability to adjust the forwarding threshold. The default value may be changed by SMBus or auto-loading from EEPROM. 00b: the threshold is set at the middle of forwarding packet 01b: the threshold is set ahead 1-cycle of middle point 10b: the threshold is set ahead 2-cycle of middle point. 11b: the threshold is set ahead 3-cycle of middle point. Reset to 01b.
3	Port Arbitration Mode	RW	When set, the round-robin arbitration will stay in the arbitrated port even if the credit is not enough but request is pending. When clear, the round-robin arbitration will always go to the requesting port, which the outgoing credit is enough for the packet queued in the port. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.

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BIT	FUNCTION	TYPE	DESCRIPTION
4	Credit Update Mode	RW	When set, the frequency of releasing new credit to the link partner will be one credit per update. When clear, the frequency of releasing new credit to the link partner will be two credits per update. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
5	Ordering on Different Egress Port Mode	RW	When set, there has ordering rule on packets for different egress port. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
6	Ordering on Different Tag of Completion Mode	RW	When set, there has ordering rule between completion packet with different tag. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
7	Reserved	RO	Reset to 0.
13:8	Power management Control Parameter	RW	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 000001b.
14	RX Polarity Inversion Disable	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
15	Compliance Pattern Parity Control Disable	RO	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.

7.2.53 PHYSICAL LAYER CONTROL 0 – OFFSET B4h (Upstream Port)

BIT	FUNCTION	TYPE	DESCRIPTION
20:16	Drive Amplitude Level (3P5 Nom)	RO	Low Driver Current (LODRV). The default value may be changed by SMBus. Reset to10111b.
25:21	Reserved	RO	Reset to 01101b.
30:26	Reserved	RO	Reset to 01000b.

7.2.54 SWITCH OPERATION MODE – OFFSET B4h (Downstream Port)

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Reserved	RO	Reset to 0.
13:8	Power Management Control Parameter	RW	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 000001b.
14	RX Polarity Inversion Disable	RW	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
15	Compliance Pattern Parity Control Disable	RW	The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.

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7.2.55 PHYSICAL LAYER CONTROL 0 – OFFSET B4h (Downstream Port)

BIT	FUNCTION	TYPE	DESCRIPTION
20:16	Drive Amplitude Level (3P5 Nom)	RO	It indicates the status of the strapping pin LODRV. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to10111b.
25:21	Reserved	RO	Reset to 01101b.
30:26	Reserved	RO	Reset to 01000b.

7.2.56 XPIP CSR2 / TL CSR – OFFSET B8h (Test Purpose Only)

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	FTS Number	RO	Reset to 30h.
9:8	Scramble control	RO	Reset to 00b.
10	Both L0s	RO	Reset to 0b.
11	Reserved	RO	Reset to 0b.
15:12	TL CSR	RO	Reset to 0100b.

7.2.57 PHYSICAL LAYER CONTROL 1 – OFFSET B8h (Test Purpose Only)

BIT	FUNCTION	TYPE	DESCRIPTION
20:16	Drive De-Emphasis Level	RO	Reset to10010b.
25:21	Reserved	RO	Reset to 01110b.
30:26	Reserved	RO	Reset to 10101b.

7.2.58 PHYSCIAL LAYER CONTROL 2 – OFFSET BCh

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	Transmitter PHY Latency	RO	Reset to 0111b.
6:4	Receiver Detection Threshold	RO	Reset to 010b.
7	Reserved	RO	Reset to 0b.
8	CDR Loop Bandwidth Enable	RO	Reset to 0b.
10:9	CDR Threshold	RO	Reset to 11b.
12:11	CDR Loop Bandwidth Gain	RO	Reset to 11b.
15:13	Reserved	RO	Reset to 0b.
16	Per-Lane Main Drive Offset Enable (Margining)	RO	Reset to 0b.
17	Per-Lane Main Drive Offset Enable (Nominal)	RO	Reset to 0b.
18	Per-Lane De-Emphasis Drive Offset Enable (Margining)	RO	Reset to 0b.
19	Per-Lane De-Emphasis Drive Offset Enable (Nominal)	RO	Reset to 0b.
21:20	Receiver Signal Detection	RO	Reset to 01b.

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BIT	FUNCTION	TYPE	DESCRIPTION
25:22	Receiver Equalization	RO	Reset to 0011b.
29:26	Reserved	RO	Reset to 0110b.
30	Transmitter Swing	RO	Reset to 0b.
31	Reserved	RO	Reset to 0b.

7.2.59 PHYSICAL LAYER CONTROL 3 REGISTER – OFFSET C0h

BIT	FUNCTION	TYPE	DESCRIPTION
6:0	Lane Mode	RW	Reset to 0
31:7	Reserved	RO	Reset to 0

7.2.60 SSID/SSVID CAPABILITY ID REGISTER – OFFSET C4h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	SSID/SSVID Capabilities ID	RO	Read as 0Dh to indicate that these are SSID/SSVID capability registers.

7.2.61 NEXT ITEM POINTER REGISTER – OFFSET C4h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Item Pointer	RO	Pointer points to the PCI Express capability register (E0h). Reset to E0h.

7.2.62 SUBSYSTEM VENDOR ID REGISTER – OFFSET C8h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	SSVID	RO	It indicates the sub-system vendor id. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0000h.

7.2.63 SUBSYSTEM ID REGISTER – OFFSET C8h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	SSID	RO	It indicates the sub-system device id. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0000h.

7.2.64 GPIO CONTROL REGISTER – OFFSET D8h (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
0	GPIO [0] Input	RO	State of GPIO [0] pin
1	GPIO [0] Output Enable	RW	0b: GPIO [0] is an input pin 1b: GPIO [0] is an output pin Reset to 0b.

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BIT	FUNCTION	TYPE	DESCRIPTION
2	GPIO [0] Output Register	RW	Value of this bit will be output to GPIO [0] pin if GPIO [0] is configured as an output pin. Reset to 0b.
3	Reserved	RO	Reset to 0b.
4	GPIO [1] Input	RO	State of GPIO [1] pin.
5	GPIO [1] Output Enable	RW	0b: GPIO [1] is an input pin 1b: GPIO [1] is an output pin Reset to 0b.
6	GPIO [1] Output Register	RW	Value of this bit will be output to GPIO [1] pin if GPIO [1] is configured as an output pin. Reset to 0b.
7	Reserved	RO	Reset to 0b.
8	GPIO [2] Input	RO	State of GPIO [2] pin
9	GPIO [2] Output Enable	RW	0b: GPIO [2] is an input pin 1b: GPIO [2] is an output pin Reset to 0b.
10	GPIO [2] Output Register	RW	Value of this bit will be output to GPIO [2] pin if GPIO [2] is configured as an output pin. Reset to 0b.
11	Reserved	RO	Reset to 0b.
12	GPIO [3] Input	RO	State of GPIO [3] pin.
13	GPIO [3] Output Enable	RW	0b: GPIO [3] is an input pin 1b: GPIO [3] is an output pin Reset to 0b.
14	GPIO [3] Output Register	RW	Value of this bit will be output to GPIO [3] pin if GPIO [3] is configured as an output pin. Reset to 0b.
15	Reserved	RO	Reset to 0b.
16	GPIO [4] Input	RO	State of GPIO [4] pin.
17	GPIO [4] Output Enable	RW	0b: GPIO [4] is an input pin 1b: GPIO [4] is an output pin Reset to 0b.
18	GPIO [4] Output Register	RW	Value of this bit will be output to GPIO [4] pin if GPIO [4] is configured as an output pin. Reset to 0b.
19	Reserved	RO	Reset to 0b.
20	GPIO [5] Input	RO	State of GPIO [5] pin.
21	GPIO [5] Output Enable	RW	0b: GPIO [5] is an input pin 1b: GPIO [5] is an output pin Reset to 0b.
22	GPIO [5] Output Register	RW	Value of this bit will be output to GPIO [5] pin if GPIO [5] is configured as an output pin. Reset to 0b.
23	Reserved	RO	Reset to 0b.
24	GPIO [6] Input	RO	State of GPIO [6] pin.
25	GPIO [6] Output Enable	RW	0b: GPIO [6] is an input pin 1b: GPIO [6] is an output pin Reset to 0b.
26	GPIO [6] Output Register	RW	Value of this bit will be output to GPIO [6] pin if GPIO [6] is configured as an output pin. Reset to 0b.
27	Reserved	RO	Reset to 0b.
28	GPIO [7] Input	RO	State of GPIO [7] pin.

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BIT	FUNCTION	TYPE	DESCRIPTION
29	GPIO [7] Output Enable	RW	0b: GPIO [7] is an input pin 1b: GPIO [7] is an output pin Reset to 0b.
30	GPIO [7] Output Register	RW	Value of this bit will be output to GPIO [7] pin if GPIO [7] is configured as an output pin. Reset to 0b.
31	Reserved	RO	Reset to 0b.

7.2.65 EEPROM CONTROL REGISTER – OFFSET DCh (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
0	EEPROM Start	RW	Starts the EEPROM read or write cycle. Reset to 0b.
1	EEPROM Command	RW	Sends the command to the EEPROM. 0b: EEPROM read 1b: EEPROM write Reset to 0b.
2	EEPROM Error Status	RO	1b: EEPROM acknowledge was not received during the EEPROM cycle. Reset to 0b.
3	EEPROM Autoload Success	RO	0b: EEPROM autoload was unsuccessful or is disabled 1b: EEPROM autolad occurred successfully after RESET. Configuration registers were loaded with values in the EEPROM It will be cleared when read at this bit.
4	EEPROM Autoload Status	RO	0b: EEPROM autoload was unsuccessful or is disabled 1b: EEPROM autoload occurred successfully after PREST. Configuration registers were loaded with values stored in the EEPROM Reset to 0b.
5	EEPROM Autoload Disable	RW	0b: EEPROM autoload enabled 1b: EEPROM autoload disabled Reset to 1b.
7:6	EEPROM Clock Rate	RW	Determines the frequency of the EEPROM clock, which is derived from the primary clock. 00b: Reserved 01b: PEXCLK / 1024 (PEXCLK is 125MHz) 10b: Reserved 11b: Test Mode Reset to 01b.

7.2.66 EEPROM ADDRESS REGISTER – OFFSET DCh (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
8	Reserved	RO	Reset to 0b.
15:9	EEPROM Address	RW	Contains the EEPROM address. Reset to 0b.

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7.2.67 EEPROM DATA REGISTER – OFFSET DCh (Upstream Port Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	EEPROM Data	RW	Contains the data to be written to the EEPROM. After completion of a read cycle, this register will contain the data from the EEPROM. Reset to 0000h.

7.2.68 PCI EXPRESS CAPABILITY ID REGISTER – OFFSET E0h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 10h to indicate that these are PCI express enhanced capability registers.

7.2.69 NEXT ITEM POINTER REGISTER – OFFSET E0h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Item Pointer	RO	Read as 00h. No other ECP registers.

7.2.70 PCI EXPRESS CAPABILITIES REGISTER – OFFSET E0h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Capability Version	RO	Read as 0001b to indicate the device is compliant to the *PCI Express Base Specifications.*
23:20	Device/Port Type	RO	Indicates the type of PCI Express logical device. Reset to 0101b (Upstream port). Reset to 0110b (Downstream port).
24	Slot Implemented	HwInt	When set, indicates that the PCIe Link associated with this Port is connected to a slot. This field is valid for downstream port of the Swidge. The default value may be changed by the status of strapped pin, SMBUs, or auto-loading from EEPROM.
29:25	Interrupt Message Number	RO	Read as 0b. No MSI messages are generated in the transparent mode.
31:30	Reserved	RO	Reset to 00b.

7.2.71 DEVICE CAPABILITIES REGISTER – OFFSET E4h

BIT	FUNCTION	TYPE	DESCRIPTION
2:0	Max_Payload_Size Supported	RO	Indicates the maximum payload size that the device can support for TLPs. Each port of the Swidge supports 256 bytes max payload size. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 001b.
4:3	Phantom Functions Supported	RO	Indicates the support for use of unclaimed function numbers as Phantom functions. Read as 00b, since the Swidge does not act as a requester. Reset to 00b.
5	Extended Tag Field Supported	RO	Indicates the maximum supported size of Tag field as a Requester. Read as 0, since the Swidge does not act as a requester. Reset to 0b.

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BIT	FUNCTION	TYPE	DESCRIPTION
8:6	Endpoint L0s Acceptable Latency	RO	Acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state. For Swidge, the ASPM software would not check this value. Reset to 000b.
11:9	Endpoint L1 Acceptable Latency	RO	Acceptable total latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. For Swidge, the ASPM software would not check this value. Reset to 000b.
14:12	Reserved	RO	Reset to 000b.
15	Role_Based Error Reporting	RO	When set, indicates that the device implements the functionality originally defined in the Error Reporting ECN. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 1b.
17:16	Reserved	RO	Reset to 00b.
25:18	Captured Slot Power Limit Value	RO	It applies to Upstream Port only. In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. This value is set by the Set_Slot_Power_Limit message or hardwired to 00h. Reset to 00h.
27:26	Captured Slot Power Limit Scale	RO	It applies to Upstream Port only. Specifies the scale used for the Slot Power Limit Value. This value is set by the Set_Slot_Power_Limit message or hardwired to 00b. Reset to 00b.
31:28	Reserved	RO	Reset to 0h.

7.2.72 DEVICE CONTROL REGISTER – OFFSET E8h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Correctable Error Reporting Enable	RW	0b: Disable Correctable Error Reporting 1b: Enable Correctable Error Reporting Reset to 0b.
1	Non-Fatal Error Reporting Enable	RW	0b: Disable Non-Fatal Error Reporting 1b: Enable Non-Fatal Error Reporting Reset to 0b.
2	Fatal Error Reporting Enable	RW	0b: Disable Fatal Error Reporting 1b: Enable Fatal Error Reporting Reset to 0b.
3	Unsupported Request Reporting Enable	RW	0b: Disable Unsupported Request Reporting 1b: Enable Unsupported Request Reporting Reset to 0b.
4	Enable Relaxed Ordering	RO	When set, it permits the device to set the Relaxed Ordering bit in the attribute field of transaction. Since the Swidge can not either act as a requester or alter the content of packet it forwards, this bit always returns ‘0’ when read. Reset to 0b.
7:5	Max_Payload_Size	RW	This field sets maximum TLP payload size for the device. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported in the Device Capabilities register. Any value exceeding the Max_Payload_Size Supported written to this register results into clamping to the Max_Payload_Size Supported value. Reset to 000b.

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BIT	FUNCTION	TYPE	DESCRIPTION
8	Extended Tag Field Enable	RW	Does not apply to PCI Express Swidge. Returns '0' when read. Reset to 0b.
9	Phantom Function Enable	RW	Does not apply to PCI Express Swidge. Returns '0' when read. Reset to 0b.
10	Auxiliary (AUX) Power PM Enable	RWS	When set, indicates that a device is enabled to draw AUX power independent of PME AUX power. Reset to 0b.
11	Enable No Snoop	RO	When set, it permits to set the No Snoop bit in the attribute field of transaction. Since the Swidge can not either act as a requester or alter the content of packet it forwards, this bit always returns '0' when read. Reset to 0b.
14:12	Max_Read_ Request_Size	RO	This field sets the maximum Read Request size for the device as a Requester. Since the Swidge does not generate read request by itself, these bits are hardwired to 000b. Reset to 000b.
15	Reserved	RO	Reset to 0b.

7.2.73 DEVICE STATUS REGISTER – OFFSET E8h

BIT	FUNCTION	TYPE	DESCRIPTION
16	Correctable Error Detected	RW1C	Asserted when correctable error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.
17	Non-Fatal Error Detected	RW1C	Asserted when non-fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.
18	Fatal Error Detected	RW1C	Asserted when fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.
19	Unsupported Request Detected	RW1C	Asserted when unsupported request is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.
20	AUX Power Detected	RO	Asserted when the AUX power is detected by the Swidge Reset to 1b.
21	Transactions Pending	RO	Each port of Swidge does not issue Non-posted Requests on its own behalf, so this bit is hardwired to 0b. Reset to 0b.
31:22	Reserved	RO	Reset to 0.

7.2.74 LINK CAPABILITIES REGISTER – OFFSET ECh

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	Maximum Link Speed	RO	Read as 0001b to indicate the maximum speed of the Express link is 2.5 Gb/s.

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BIT	FUNCTION	TYPE	DESCRIPTION
9:4	Maximum Link Width	RO	Indicates the maximum width of the given PCIe Link. The width of each port is determined by strapped pin or EEPROM pre-loaded value. Reset to 000001b (x1) for Port 0. Reset to 000001b (x1) for Port 1. Reset to 000001b (x1) for Port 2.
11:10	Active State Power Management (ASPM) Support	RO	Indicates the level of ASPM supported on the given PCIe Link. Each port of Swidge supports L0s and L1 entry. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 01b.
14:12	L0s Exit Latency	RO	Indicates the L0s exit latency for the given PCIe Link. The length of time this port requires to complete transition from L0s to L0 is in the range of 256ns to less than 512ns. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 011b.
17:15	L1 Exit Latency	RO	Indicates the L1 exit latency for the given PCIe Link. The length of time this port requires to complete transition from L1 to L0 is in the range of 16us to less than 32us. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 000b.
18	Reserved	RO	Reset to 0b.
19	Surprise Down Error Reporting Capable	RO	For a Downstream port, this bit must be set to 1b if the component supports the optional capability of detecting and reporting a Surprise Down error condition. For Upstream Ports, which does not support this optional capability, this bit must be hardwired to 0b. Rest to 0b.
20	Data Link Layer Active Reporting Capable	RO	For a Downstream Port, this bit must be set to 1b if the component supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. For a hot-plug capable Downstream Port, this bit must be set to 1b. For Upstream Port, this bit must be hardwired to 0b. Reset to 0b for upstream port. Reset to 1b for downstream ports with hot-plug capable
23:21	Reserved	R0	Reset to 000b
31:24	Port Number	RO	Indicates the PCIe Port Number for the given PCIe Link. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 00h for Port 0. Reset to 01h for Port 1. Reset to 02h for Port 2.

7.2.75 LINK CONTROL REGISTER – OFFSET F0h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Active State Power Management (ASPM) Control	RW	00b: ASPM is Disabled 01b: L0s Entry Enabled 10b: L1 Entry Enabled 11b: L0s and L1 Entry Enabled Note that the receiver must be capable of entering L0s even when the field is disabled. Reset to 00b.
2	Reserved	RO	Reset to 0b.

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BIT	FUNCTION	TYPE	DESCRIPTION
3	Read Completion Boundary (RCB)	RO	Does not apply to PCI Express Swidge. Returns '0' when read. Reset to 0b.
4	Link Disable	RW	At upstream port, it is not allowed to disable the link, so this bit is hardwired to '0'. For downstream ports, it disables the link when this bit is set. Reset to 0b.
5	Retrain Link	RW	At upstream port, it is not allowed to retrain the link, so this bit is hardwired to 0b. For downstream ports, it initiates Link Retraining when this bit is set. This bit always returns 0b when read.
6	Common Clock Configuration	RW	0b: The components at both ends of a link are operating with asynchronous reference clock 1b: The components at both ends of a link are operating with a distributed common reference clock Reset to 0b.
7	Extended Synch	RW	When set, it transmits 4096 FTS ordered sets in the L0s state for entering L0 state and transmits 1024 TS1 ordered sets in the L1 state for entering L0 state. Reset to 0b.
15:8	Reserved	RO	Reset to 00h.

7.2.76 LINK STATUS REGISTER – OFFSET F0h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Link Speed	RO	Read as 0001b to indicate the negotiated speed of the Express link is 2.5 Gb/s.
25:20	Negotiated Link Width	RO	Indicates the negotiated width of the given PCIe link. Reset to 000001b (x1).
26	Training Error	RO	When set, indicates a Link training error occurred. This bit is cleared by hardware upon successful training of the link to the L0 link state. Reset to 0b.
27	Link Training	RO	When set, indicates the link training is in progress. Hardware clears this bit once link training is complete. Reset to 0b.
28	Slot Clock Configuration	HwInt	0b: the Swidge uses an independent clock irrespective of the presence of a reference on the connector 1b: the Swidge uses the same reference clock that the platform provides on the connector The default value may be changed by the status of strapped pin, SMBus, or auto-loading from EEPROM. Reset to 0b.
29	Data Link Layer Link Active	RO	Indicates the status of the Data Link Control and Management State Machine. It returns a 1b to indicate the DL_Active state, 0b otherwise. Reset to 0b.
31:30	Reserved	RO	Reset to 00b.

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7.2.77 SLOT CAPABILITIES REGISTER (Downstream Port Only) – OFFSET F4h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Attention Button Present	RO	When set, it indicates that an Attention Button is implemented on the chassis for this slot. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
1	Power Controller Present	RO	When set, it indicates that a Power Controller is implemented for this slot. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
2	Reserved	RO	Reset to 0b.
3	Attention Indicator Present	RO	When set, it indicates that an Attention Indicator is implemented on the chassis for this slot. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
4	Power Indicator Present	RO	When set, it indicates that a Power Indicator is implemented on the chassis for this slot. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
5	Hot-Plug Surprise	RO	When set, it indicates that a device present in this slot might be removed from the system without any prior notification. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0b.
6	Hot-Capable	HwInt	When set, it indicates that this slot is capable of supporting Hot-Plug operation. The default value may be changed by the status of strapped pin or auto-loading from EEPROM.
14:7	Slot Power Limit Value	RW	It applies to Downstream Port only. In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Writes to this register also cause the Port to send the Set_Slot_Power_Limit message. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 00h.
16:15	Slot Power Limit Scale	RW	It applies to Downstream Port only. Specifies the scale used for the Slot Power Limit Value. Writes to this register also cause the Port to send the Set_Slot_Power_Limit message. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 00b.
18:17	Reserved	RO	Reset to 00b.
31:19	Physical Slot Number	RO	It indicates the physical slot number attached to this Port. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 0.

7.2.78 SLOT CONTROL REGISTER (Downstream Port Only) – OFFSET F8h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Attention Button Pressed Enable	RW	When set, it enables the generation of Hot-Plug interrupt or wakeup event on an attention button pressed event. Reset to 0b.
1	Power Fault Detected Enable	RW	When set, it enables the generation of Hot-Plug interrupt or wakeup event on a power fault event. Reset to 0b.
2	Reserved	RO	Reset to 0b.

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BIT	FUNCTION	TYPE	DESCRIPTION
3	Presence Detect Changed Enable	RW	When set, it enables the generation of Hot-Plug interrupt or wakeup event on a presence detect changed event. Reset to 0b.
4	Command Completed Interrupt Enable	RW	When set, it enables the generation of Hot-Plug interrupt when the Hot-Plug Controller completes a command. Reset to 0b.
5	Hot-Plug Interrupt Enable	RW	When set, it enables generation of Hot-Plug interrupt on enabled Hot-Plug events. Reset to 0b.
7:6	Attention Indicator Control	RW	Controls the display of Attention Indicator. 00b: Reserved 01b: On 10b: Blink 11b: Off Writes to this register also cause the Port to send the ATTENTION_INDICATOR_* Messages. Reset to 11b.
9:8	Power Indicator Control	RW	Controls the display of Power Indicator. 00b: Reserved 01b: On 10b: Blink 11b: Off Writes to this register also cause the Port to send the POWER_INDICATOR_* Messages. Reset to 11b.
10	Power Controller Control	RW	0b: reset the power state of the slot (Power On) 1b: set the power state of the slot (Power Off) Reset to 0b.
11	Reserved	RO	Reset to 0b.
12	Data Link Layer State Changed Enable	RW	If the Data Link Layer Link Active capability is implemented, when set to 1b, this field enables software notification when Data Link Layer Link Active field is changed. Reset to 0b.
15:13	Reserved	RO	Reset to 000b

7.2.79 SLOT STATUS REGISTER (Downstream Port Only) – OFFSET F8h

BIT	FUNCTION	TYPE	DESCRIPTION
16	Attention Button Pressed	RW1C	When set, it indicates the Attention Button is pressed. Reset to 0b.
17	Power Fault Detected	RW1C	When set, it indicates a Power Fault is detected. Reset to 0b.
18	MRL Sensor Changed	RO	When set, it indicates a MRL Sensor Changed is detected. Reset to 0b.
19	Presence Detect Changed	RW1C	When set, it indicates a Presence Detect Changed is detected. Reset to 0b.
20	Command Completed	RW1C	When set, it indicates the Hot-Plug Controller completes an issued command. Reset to 0b.

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BIT	FUNCTION	TYPE	DESCRIPTION
21	MRL Sensor State	RO	Reflects the status of MRL Sensor. 0b: MRL Closed 1b: MRL Opened Reset to 0b.
22	Presence Detect State	RO	Indicates the presence of a card in the slot. 0b: Slot Empty 1b: Card Present in slot This register is implemented on all Downstream Ports that implement slots. For Downstream Ports not connected to slots (where the Slot Implemented bit of the PCI Express Capabilities register is 0b), this bit returns 1b. Reset to 1b.
23	Reserved	RO	Reset to 0.
24	Data Link Layer State Changed	RW1C	This bit is set when the value reported in the Data Link Layer Link Active field of the Link Status register is changed.
31:25	Reserved	RO	Reset to 0

7.2.80 PCI EXPRESS ADVANCED ERROR REPORTING CAPABILITY ID REGISTER – OFFSET 100h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Extended Capabilities ID	RO	Read as 0001h to indicate that these are PCI express extended capability registers for advance error reporting.

7.2.81 CAPABILITY VERSION – OFFSET 100h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Capability Version	RO	Read as 1h. Indicates PCI-SIG defined PCI Express capability structure version number. Reset to 1h.

7.2.82 NEXT ITEM POINTER REGISTER – OFFSET 100h

BIT	FUNCTION	TYPE	DESCRIPTION
31:20	Next Capability Offset	RO	Pointer points to the PCI Express Extended VC capability register (140h). Reset to 140h (upstream port). Reset to 20Ch (downstream port).

7.2.83 UNCORRECTABLE ERROR STATUS REGISTER – OFFSET 104h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Training Error Status	RW1CS	When set, indicates that the Training Error event has occurred. Reset to 0b.
3:1	Reserved	RO	Reset to 000b.
4	Data Link Protocol Error Status	RW1CS	When set, indicates that the Data Link Protocol Error event has occurred. Reset to 0b.
11:5	Reserved	RO	Reset to 0.

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BIT	FUNCTION	TYPE	DESCRIPTION
12	Poisoned TLP Status	RW1CS	When set, indicates that a Poisoned TLP has been received or generated. Reset to 0b.
13	Flow Control Protocol Error Status	RW1CS	When set, indicates that the Flow Control Protocol Error event has occurred. Reset to 0b.
14	Completion Timeout Status	RW1CS	When set, indicates that the Completion Timeout event has occurred. Reset to 0b.
15	Completer Abort Status	RW1CS	When set, indicates that the Completer Abort event has occurred. Reset to 0b.
16	Unexpected Completion Status	RW1CS	When set, indicates that the Unexpected Completion event has occurred. Reset to 0b.
17	Receiver Overflow Status	RW1CS	When set, indicates that the Receiver Overflow event has occurred. Reset to 0b.
18	Malformed TLP Status	RW1CS	When set, indicates that a Malformed TLP has been received. Reset to 0b.
19	ECRC Error Status	RW1CS	When set, indicates that an ECRC Error has been detected. Reset to 0b.
20	Unsupported Request Error Status	RW1CS	When set, indicates that an Unsupported Request event has occurred. Reset to 0b.
31:21	Reserved	RO	Reset to 0.

7.2.84 UNCORRECTABLE ERROR MASK REGISTER – OFFSET 108h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Training Error Mask	RWS	When set, the Training Error event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
3:1	Reserved	RO	Reset to 000b.
4	Data Link Protocol Error Mask	RWS	When set, the Data Link Protocol Error event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
11:5	Reserved	RO	Reset to 0.
12	Poisoned TLP Mask	RWS	When set, an event of Poisoned TLP has been received or generated is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
13	Flow Control Protocol Error Mask	RWS	When set, the Flow Control Protocol Error event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
14	Completion Timeout Mask	RWS	When set, the Completion Timeout event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
15	Completer Abort Mask	RWS	When set, the Completer Abort event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
16	Unexpected Completion Mask	RWS	When set, the Unexpected Completion event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.

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BIT	FUNCTION	TYPE	DESCRIPTION
17	Receiver Overflow Mask	RWS	When set, the Receiver Overflow event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
18	Malformed TLP Mask	RWS	When set, an event of Malformed TLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
19	ECRC Error Mask	RWS	When set, an event of ECRC Error has been detected is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
20	Unsupported Request Error Mask	RWS	When set, the Unsupported Request event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
31:21	Reserved	RO	Reset to 0.

7.2.85 UNCORRECTABLE ERROR SEVERITY REGISTER – OFFSET 10Ch

BIT	FUNCTION	TYPE	DESCRIPTION
0	Training Error Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 1b.
3:1	Reserved	RO	Reset to 000b.
4	Data Link Protocol Error Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 1b.
11:5	Reserved	RO	Reset to 0.
12	Poisoned TLP Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 0b.
13	Flow Control Protocol Error Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 1b.
14	Completion Timeout Error Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 0b.
15	Completer Abort Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 0b.
16	Unexpected Completion Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 0b.
17	Receiver Overflow Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 1b.
18	Malformed TLP Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 1b.
19	ECRC Error Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 0.

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BIT	FUNCTION	TYPE	DESCRIPTION
20	Unsupported Request Error Severity	RWS	0b: Non-Fatal 1b: Fatal Reset to 0b.
31:21	Reserved	RO	Reset to 0.

7.2.86 CORRECTABLE ERROR STATUS REGISTER – OFFSET 110 h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Receiver Error Status	RW1CS	When set, the Receiver Error event is detected. Reset to 0b.
5:1	Reserved	RO	Reset to 00000b.
6	Bad TLP Status	RW1CS	When set, the event of Bad TLP has been received is detected. Reset to 0b.
7	Bad DLLP Status	RW1CS	When set, the event of Bad DLLP has been received is detected. Reset to 0b.
8	REPLAY_NUM Rollover status	RW1CS	When set, the REPLAY_NUM Rollover event is detected. Reset to 0b.
11:9	Reserved	RO	Reset to 000b.
12	Replay Timer Timeout status	RW1CS	When set, the Replay Timer Timeout event is detected. Reset to 0b.
13	Advisory Non-Fatal Error status	RW1CS	When set, the Advisory Non-Fatal Error event is detected. Reset to 0b.
31:14	Reserved	RO	Reset to 0b.

7.2.87 CORRECTABLE ERROR MASK REGISTER – OFFSET 114 h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Receiver Error Mask	RWS	When set, the Receiver Error event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
5:1	Reserved	RO	Reset to 00000b.
6	Bad TLP Mask	RWS	When set, the event of Bad TLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
7	Bad DLLP Mask	RWS	When set, the event of Bad DLLP has been received is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
8	REPLAY_NUM Rollover Mask	RWS	When set, the REPLAY_NUM Rollover event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
11:9	Reserved	RO	Reset to 000b.
12	Replay Timer Timeout Mask	RWS	When set, the Replay Timer Timeout event is not logged in the Header Log register and not issued as an Error Message to RC either. Reset to 0b.
13	Advisory Non-Fatal Error Mask	RWS	When set, the Advisory Non-Fatal Error event is not logged in the Header Long register and not issued as an Error Message to RC either. Reset to 1b.
31:14	Reserved	RO	Reset to 0.

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7.2.88 ADVANCE ERROR CAPABILITIES AND CONTROL REGISTER – OFFSET 118h

BIT	FUNCTION	TYPE	DESCRIPTION
4:0	First Error Pointer	ROS	It indicates the bit position of the first error reported in the Uncorrectable Error Status register. Reset to 00000b.
5	ECRC Generation Capable	RO	When set, it indicates the Swidge has the capability to generate ECRC. Reset to 1b.
6	ECRC Generation Enable	RWS	When set, it enables the generation of ECRC when needed. Reset to 0b.
7	ECRC Check Capable	RO	When set, it indicates the Swidge has the capability to check ECRC. Reset to 1b.
8	ECRC Check Enable	RWS	When set, the function of checking ECRC is enabled. Reset to 0b.
31:9	Reserved	RO	Reset to 0.

7.2.89 HEADER LOG REGISTER – OFFSET From 11Ch to 128h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	1st DWORD	ROS	Hold the 1st DWORD of TLP Header. The Head byte is in big endian.
63:32	2nd DWORD	ROS	Hold the 2nd DWORD of TLP Header. The Head byte is in big endian.
95:64	3rd DWORD	ROS	Hold the 3rd DWORD of TLP Header. The Head byte is in big endian.
127:96	4th DWORD	ROS	Hold the 4th DWORD of TLP Header. The Head byte is in big endian.

7.2.90 PCI EXPRESS VIRTUAL CHANNEL CAPABILITY ID REGISTER – OFFSET 140h (Upstream Only)

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Extended Capabilities ID	RO	Read as 0002h to indicate that these are PCI express extended capability registers for virtual channel.

7.2.91 CAPABILITY VERSION – OFFSET 140h (Upstream Only)

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Capability Version	RO	Read as 1h. Indicates PCIe Base Specification compliance. Reset to 1h.

7.2.92 NEXT ITEM POINTER REGISTER – OFFSET 140h (Upstream Only)

BIT	FUNCTION	TYPE	DESCRIPTION
31:20	Next Capability Offset	RO	Pointer points to the PCI Express Power Budgeting Capability register (20Ch). Reset to 20Ch.

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7.2.93 PORT VC CAPABILITY REGISTER 1 – OFFSET 144h (Upstream Only)

BIT	FUNCTION	TYPE	DESCRIPTION
2:0	Extended VC Count	RO	It indicates the number of extended Virtual Channels in addition to the default VC supported by the Swidge. Reset to 000b.
3	Reserved	RO	Reset to 0b.
6:4	Low Priority Extended VC Count	RO	It indicates the number of extended Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 000b.
7	Reserved	RO	Reset to 0b.
9:8	Reference Clock	RO	It indicates the reference clock for Virtual Channels that support time-based WRR Port Arbitration. Defined encoding is 00b for 100 ns reference clock. Reset to 00b.
11:10	Port Arbitration Table Entry Size	RO	Read as 10b to indicate the size of Port Arbitration table entry in the device is 4 bits. Reset to 10b.
31:12	Reserved	RO	Reset to 0.

7.2.94 PORT VC CAPABILITY REGISTER 2 – OFFSET 148h (Upstream Only)

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	VC Arbitration Capability	RO	It indicates the types of VC Arbitration supported by the device for the LPVC group. This field is valid when LPVC is greater than 0. The Swidge supports Hardware fixed arbitration scheme, e.g., Round Robin and Weight Round Robin arbitration with 32 phases in LPVC. Reset to 00000000b.
23:8	Reserved	RO	Reset to 0.
31:24	VC Arbitration Table Offset	RO	It indicates the location of the VC Arbitration Table as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes). Reset to 00h.

7.2.95 PORT VC CONTROL REGISTER – OFFSET 14Ch (Upstream Only)

BIT	FUNCTION	TYPE	DESCRIPTION
0	Load VC Arbitration Table	RW	When set, the programmed VC Arbitration Table is applied to the hardware. This bit always returns 0b when read. Reset to 0b.
3:1	VC Arbitration Select	RW	This field is used to configure the VC Arbitration by selecting one of the supported VC Arbitration schemes. The valid values for the schemes supported by Swidge are 0b and 1b. Other value than these written into this register will be treated as default. Reset to 0b.
15:4	Reserved	RO	Reset to 0.

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7.2.96 PORT VC STATUS REGISTER – OFFSET 14Ch (Upstream Only)

BIT	FUNCTION	TYPE	DESCRIPTION
16	VC Arbitration Table Status	RO	When set, it indicates that any entry of the VC Arbitration Table is written by software. This bit is cleared when hardware finishes loading values stored in the VC Arbitration Table after the bit of "Load VC Arbitration Table" is set. Reset to 0b.
31:17	Reserved	RO	Reset to 0.

7.2.97 VC RESOURCE CAPABILITY REGISTER (0) – OFFSET 150h (Upstream Only)

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Port Arbitration Capability	RO	It indicates the types of Port Arbitration supported by the VC resource. The Swidge supports Hardware fixed arbitration scheme, e.g., Round Robin, Weight Round Robin (WRR) arbitration with 128 phases (3~4 enabled ports) and Time-based WRR with 128 phases (3~4 enabled ports). Reset to 00001001b.
13:8	Reserved	RO	Reset to 000000b.
14	Advanced Packet Switching	RO	When set, it indicates the VC resource only supports transaction optimized for Advanced Packet Switching (AS). Reset to 0b.
15	Reject Snoop Transactions	RO	This bit is not applied to PCIe Switch. Reset to 0b.
22:16	Maximum Time Slots	RO	It indicates the maximum numbers of time slots (minus one) are allocated for Isochronous traffic. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to 7Fh.
23	Reserved	RO	Reset to 0b.
31:24	Port Arbitration Table Offset	RO	It indicates the location of the Port Arbitration Table (n) as an offset from the base address of the Virtual Channel Capability register in the unit of DQWD (16 bytes). Reset to 04h for Port Arbitration Table (0).

7.2.98 VC RESOURCE CONTROL REGISTER (0) – OFFSET 154h (Upstream Only)

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	TC/VC Map	RW	This field indicates the TCs that are mapped to the VC resource. Bit locations within this field correspond to TC values. When the bits in this field are set, it means that the corresponding TCs are mapped to the VC resource. The default value may be changed by SMBus or auto-loading from EEPROM. Reset to FFh.
15:8	Reserved	RO	Reset to 00h.
16	Load Port Arbitration Table	RW	When set, the programmed Port Arbitration Table is applied to the hardware. This bit always returns 0b when read. Reset to 0b.
19:17	Port Arbitration Select	RW	This field is used to configure the Port Arbitration by selecting one of the supported Port Arbitration schemes. The permissible values for the schemes supported by Swidge are 000b and 011b at VC0, other value than these written into this register will be treated as default. Reset to 000b.

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BIT	FUNCTION	TYPE	DESCRIPTION
23:20	Reserved	RO	Reset to 0h.
26:24	VC ID	RO	This field assigns a VC ID to the VC resource. Reset to 000b.
30:27	Reserved	RO	Reset to 0h.
31	VC Enable	RW	0b: it disables this Virtual Channel 1b: it enables this Virtual Channel Reset to 1b.

7.2.99 VC RESOURCE STATUS REGISTER (0) – OFFSET 158h (Upstream Only)

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Reserved	RO	Reset to 0000h.
16	Port Arbitration Table Status	RO	When set, it indicates that any entry of the Port Arbitration Table is written by software. This bit is cleared when hardware finishes loading values stored in the Port Arbitration Table after the bit of "Load Port Arbitration Table" is set. Reset to 0b.
17	VC Negotiation Pending	RO	When set, it indicates that the VC resource is still in the process of negotiation. This bit is cleared after the VC negotiation is complete. Reset to 0b.
31:18	Reserved	RO	Reset to 0.

7.2.100 PORT ARBITRATION TABLE REGISTER (0) – OFFSET 180h-1BCh (Upstream Only)

The Port arbitration table is a read-write register array that contains a table for Port arbitration. Each table entry allocates two bits to represent Port Number. The table entry size is dependent on the number of enabled ports (refer to bit 10 and 11 of Port VC capability register 1). The arbitration table contains 128 entries if three or four ports are to be enabled. The following table shows the register array layout for the size of entry equal to two.

Table 7-1 Table Entry Size in 4 Bits

63 - 56	55 - 48	47 - 40	39 - 32	31 - 24	23 - 16	15 - 8	7 - 0	Byte Location
Phase [15:14]	Phase [13:12]	Phase [11:10]	Phase [9:8]	Phase [7:6]	Phase [5:4]	Phase [3:2]	Phase [1:0]	00h
Phase [31:30]	Phase [29:28]	Phase [27:26]	Phase [25:24]	Phase [23:22]	Phase [21:20]	Phase [19:18]	Phase [17:16]	08h
Phase [47:46]	Phase [45:44]	Phase [43:42]	Phase [41:40]	Phase [39:38]	Phase [37:36]	Phase [35:34]	Phase [33:32]	10h
Phase [63:62]	Phase [61:60]	Phase [59:58]	Phase [57:56]	Phase [55:54]	Phase [53:52]	Phase [51:50]	Phase [49:48]	18h
Phase [79:78]	Phase [77:76]	Phase [75:74]	Phase [73:72]	Phase [71:70]	Phase [69:68]	Phase [67:66]	Phase [65:64]	20h
Phase [95:94]	Phase [93:92]	Phase [91:90]	Phase [89:88]	Phase [87:86]	Phase [85:84]	Phase [83:82]	Phase [81:80]	28h
Phase [111:110]	Phase [109:108]	Phase [107:106]	Phase [105:104]	Phase [103:102]	Phase [101:100]	Phase [99:98]	Phase [97:96]	30h
Phase [127:126]	Phase [125:124]	Phase [123:122]	Phase [121:120]	Phase [119:118]	Phase [117:116]	Phase [115:114]	Phase [113:112]	38h

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7.2.101 PCI EXPRESS POWER BUDGETING CAPABILITY ID REGISTER – OFFSET 20Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Extended Capabilities ID	RO	Read as 0004h to indicate that these are PCI express extended capability registers for power budgeting.

7.2.102 CAPABILITY VERSION – OFFSET 20Ch

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Capability Version	RO	Read as 1h. Indicates PCIe Base Specification compliance. Reset to 1h.

7.2.103 NEXT ITEM POINTER REGISTER – OFFSET 20Ch

BIT	FUNCTION	TYPE	DESCRIPTION
31:20	Next Capability Offset	RO	Read as 000h. No other ECP registers. Reset to 000h.

7.2.104 DATA SELECT REGISTER – OFFSET 210h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Data Selection	RW	It indexes the power budgeting data reported through the data register. When 00h, it selects D0 Max power budget When 01h, it selects D0 Sustained power budget Other values would return zero power budgets, which means not supported Reset to 00h.
31:8	Reserved	RO	Reset to 000000h.

7.2.105 POWER BUDGETING DATA REGISTER – OFFSET 214h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Base Power	RO	It specifies the base power value in watts. This value represents the required power budget in the given operation condition. The default value may be changed by auto-loading from EEPROM. Reset to 04h.
9:8	Data Scale	RO	It specifies the scale to apply to the base power value. The default value may be changed by auto-loading from EEPROM. Reset to 00b.
12:10	PM Sub State	RO	It specifies the power management sub state of the given operation condition. It is initialized to the default sub state. Reset to 000b.
14:13	PM State	RO	It specifies the power management state of the given operation condition. It defaults to the D0 power state. The default value may be changed by auto-loading from EEPROM. Reset to 00b.

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BIT	FUNCTION	TYPE	DESCRIPTION
17:15	Type	RO	It specifies the type of the given operation condition. It defaults to the Maximum power state. The default value may be changed by auto-loading from EEPROM. Reset to 111b.
20:18	Power Rail	RO	It specifies the power rail of the given operation condition. Reset to 010b.
31:21	Reserved	RO	Reset to 0.

7.2.106 POWER BUDGET CAPABILITY REGISTER – OFFSET 218h

BIT	FUNCTION	TYPE	DESCRIPTION
0	System Allocated	RO	When set, it indicates that the power budget for the device is included within the system power budget. The default value may be changed by auto-loading from EEPROM. Reset to 0b.
31:1	Reserved	RO	Reset to 0.

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7.3 USB DEVICE CONFIGURATION REGISTERS (FUNC0/FUNC1/FUNC2)

The swidge contains two Open HCI (OHCI) host controllers (function number 0 and 1) and one Enhanced HCI (EHCI) controller (function number 2). OHCI host controllers handle full-speed and low-speed device while EHCI host controller handles high speed device. The OHCI and EHCI host controllers are connected to an internal PCI express port (device number 3).

The following table details the allocation of the register fields of the PCI 2.3 compatible type 0 configuration space header.

31 – 24	23 – 16	15 – 8	7 – 0	BYTE OFFSET
Device ID		Vendor ID		00h
Status		Command		04h
Class Code			Revision ID	08h
Reserved	Header Type	Master Latency Timer	Cache Line Size	0Ch
Base Address Register 0				10h
Reserved				14h – 28h
Subsystem ID		Subsystem Vendor ID		2Ch
Reserved				30h
Capability Pointer				34h
Reserved				38h
Reserved		Interrupt Pin	Interrupt Line	3Ch
Reserved				40h – 5Fh
Port Wake Capability Register		FLADJ	SBRN	60h
Reserved				64h
Miscellaneous Register				68h
Reserved				6Ch – 7Fh
Power Management Capabilities		Next ID = 8C	Capability ID = 01	80h
PM Data	PPB Support	Power Management Data		84h
Message Control Register		Next ID =E0	Capability ID = 05	8Ch
Low 32-bit Message Address				90h
Message Data Register				94h
Reserved				98h - 9Ch
USB Physical Layer Control Register (USB Port 1)				A0h
USB Physical Layer Control Register (USB Port 2)				A4h
USB Physical Layer Control Register (USB Port 3)				A8h
USB Physical Layer Control Register (USB Port 4)				ACh
Reserved				B0h – DCh
PCI Express Capability Register		Next ID = 00h	Capability ID = 10	E0h
Device Capability				E4h
Device Status		Device Control		E8h
Link Capability				ECh
Link Status		Link Control		F0h
Reserved				F4h - FCh

7.3.1 VENDOR ID REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Vendor ID	RO	Identifies Pericom as the vendor of this device. The default value may be changed by auto-loading from EEPROM. Reset to 12D8h.

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7.3.2 DEVICE ID REGISTER – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Device ID	RO	Identifies this device as the PCIe to OHCI/EHCI I/O bridge. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 400Eh for OHCI (Func 0 /Func 1). Reset to 400Fh for EHCI (Func 2)

7.3.3 COMMAND REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
0	I/O Space Enable	RW	Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. Reset to 0b.
1	Memory Space Enable	RW	Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to response to memory Space accesses. Reset to 0b.
2	Bus Master Enable	RO	Controls a device's ability to act as a master on the PCI bus. A value of 0 disables the device from generating PCI accesses. A value of 1 allows the device to behave as a bus master. Reset to 0b.
3	Special Cycle Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
4	Memory Write And Invalidate Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
5	VGA Palette Snoop Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
6	Parity Error Response Enable	RW	Controls the device's response to parity errors. When the bit is set, the device must take its normal action when a parity error is detected. When the bit is 0, the device sets its Detected Parity Error Status bit when an error is detected. Reset to 0b.
7	Wait Cycle Control	RO	Does not apply to PCI Express. Must be hardwired to 0b.
8	SERR# enable	RW	This bit, when set, enables reporting of Non-fatal and Fatal errors detected by the device to the Root Complex. Reset to 0b.
9	Fast Back-to-Back Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
10	Interrupt Disable	RW	Controls the ability of the I/O bridge to generate INTx interrupt Messages. Reset to 0b.
15:11	Reserved	RO	Reset to 00000b.

7.3.4 STATUS REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
18:16	Reserved	RO	Reset to 000b.
19	Interrupt Status	RO	Indicates that an INTx interrupt Message is pending internally to the device. Reset to 0b.
20	Capabilities List	RO	Set to 1 to enable support for the capability list (offset 34h is the pointer to the data structure) Reset to 1b.
21	66MHz Capable	RO	Does not apply to PCI Express. Must be hardwired to 0b.

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BIT	FUNCTION	TYPE	DESCRIPTION
22	Reserved	RO	Reset to 0b.
23	Fast Back-to-Back Capable	RO	Does not apply to PCI Express. Must be hardwired to 0b.
24	Master Data Parity Error	RWC	It is not implemented. Hardwired to 0b.
26:25	DEVSEL# Timing	RO	Does not apply to PCI Express. Must be hardwired to 0b.
27	Signaled Target Abort	RWC	Set to 1 (by a completer) whenever completing a request in the I/O bridge side using Completer Abort Completion Status. Reset to 0b.
28	Received Target Abort	RWC	It is not implemented. Hardwired to 0b.
29	Received Master Abort	RWC	It is not implemented. Hardwired to 0b.
30	Signaled System Error	RWC	Set to 1 when the I/O bridge sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR Enable bit in the Command register is 1. Reset to 0b.
31	Detected Parity Error	RWC	Set to 1 whenever the I/O bridge receives a Poisoned TLP. Reset to 0b.

7.3.5 REVISION ID REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Revision	RO	Indicates revision number of the I/O bridge. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 00h.

7.3.6 CLASS CODE REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Programming Interface	RO	Read as 10h to indicate no programming interfaces have been defined for OHCI controllers. Read as 20h to indicate no programming interfaces have been defined for EHCI controllers. The default value may be changed by SMBUS or auto-loading from EEPROM.
23:16	Sub-Class Code	RO	Read as 03h to indicate device is USB bus controller. The default value may be changed by SMBUS or auto-loading from EEPROM.
31:24	Base Class Code	RO	Read as 0Ch to indicate device is a serial bus controller. The default value may be changed by SMBUS or auto-loading from EEPROM.

7.3.7 CACHE LINE REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Cache Line Size	RW	The cache line size register is set by the system firmware and the operating system to system cache line size. This field is implemented by PCI Express devices as a RW field for legacy compatibility purposes but has no impact on any PCI Express device functionality. Reset to 00h.

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7.3.8 MASTER LATENCY TIMER REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Latency timer	RO	Does not apply to PCI Express. Must be hardwired to 00h.

7.3.9 HEADER TYPE REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
23:16	Header Type	RO	Read as 80h to indicate it is a multi-function device.

7.3.10 BASE ADDRESS REGISTER 0 – OFFSET 10h (Func 0 and Func 1)

BIT	FUNCTION	TYPE	DESCRIPTION
11:0	Base Address 0	RO	Reset to 000h.
31:12	Base Address 0	RW	Use this I/O base address to map the OHCI registers. Reset to 00000h.

7.3.11 BASE ADDRESS REGISTER 0 – OFFSET 10h (Func 2 Only)

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Base Address 0	RO	Reset to 00h.
31:8	Base Address 0	RW	Use this I/O base address to map the EHCI registers. Reset to 000000h.

7.3.12 SUBSYSTEM VENDOR REGISTER – OFFSET 2Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Sub Vendor ID	RO	Indicates the sub-system vendor id. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 12D8h.

7.3.13 SUBSYSTEM ID REGISTER – OFFSET 2Ch

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Sub System ID	RO	Indicates the sub-system device id. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 400Eh for OHCI (Func 0 /Func 1) Reset to 400Fh for EHCI (Func 2)

7.3.14 CAPABILITIES POINTER REGISTER – OFFSET 34h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Capabilities Pointer	RO	This optional register points to a linked list of new capabilities implemented by the device. This default value may be changed by SMBUS or auto-loading from EEPROM. The default value is 80h.

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7.3.15 INTERRUPT LINE REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Interrupt Line	RW	Used to communicate interrupt line routing information. POST software will write the routing information into this register as it initializes and configures the system. Reset to 00h.

7.3.16 INTERRUPT PIN REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Interrupt Pin	RO	Identifies the legacy interrupt Message(s) the device uses. Reset to 01h for Func 0. Reset to 02h for Func 1 Reset to 03h for Func 2

7.3.17 SERIAL BUS RELEASE NUMBER REGISTER – OFFSET 60h (Func 2 Only)

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Serial Bus Release Number	RO	Release Number. All other combinations are reserved. Reset to 20h

7.3.18 FRAME LENGTH ADJUSTMENT REGISTER – OFFSET 60h (Func 2 Only)

BIT	FUNCTION	TYPE	DESCRIPTION
13:8	Frame Length Adjustment	RW	Frame Length Timing Value. Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is 32 (20h), which gives a SOF cycle time of 6000. **Frame Length (# High Speed bit times) (decimal)** / **FLADJ Value (Decimal)** 59488 — 0 (00h) 59504 — 1 (01h) 59520 — 2 (02h) … 59984 — 31 (1Fh) 60000 — 32 (20h) … 60480 — 62 (3Eh) 60496 — 63 (3Fh) Reset to 20h
15:14	Reserved	RO	Reset to 0

7.3.19 PORT WAKE CAPABILITY REGISTER – OFFSET 60h (Func 2 Only)

BIT	FUNCTION	TYPE	DESCRIPTION
20:16	Port Wake Capability Mask	RW	Bit position zero of this register indicates whether the register is implemented. A one in bit position zero indicates that the register is implemented. Bit positions 1 through 4 correspond to a physical port implemented on this host controller. For example, bit position 1 corresponds to port 1, position 2 to port 2, etc.

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BIT	FUNCTION	TYPE	DESCRIPTION
			Reset to Fh
31:21	Reserved	RO	Reset to 0

7.3.20 MISCELLANEOUS REGISTER – OFFSET 68h (Func 2 Only)

BIT	FUNCTION	TYPE	DESCRIPTION
0	Enable Basic Mode	RW	When set, only one USB controller will active at the same time. Otherwise, all USB controllers allow active at the same time. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 0b.
1	Enable Boundary 64-byte	RW	When set, the max_read_request_size is set to 64 byte. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 0b.
2	Enable EHCI Prefetch	RW	When set, EHCI will enable the prefetect function. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 0b.
3	Reserved	RW	Reset to 0b.
4	Enable User Max_Read_Request_Size	RW	When set, the user-defined max_read_request_size value is employed. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 0b.
6:5	User Max_Read_Request_Size	RW	A 2-bit register contains a user-defined value. The default value may be changed by SMBUS or auto-loading from EEPROM. 00b: 128 byte 01b: Reserved 10b: Reserved 11b: Reserved Reset to 00b.
7	Reserved	RO	Reset to 0
14:8	Prefetch DW Size	RW	A 7-bit register contains a user-defined value for the prefetch size and the unit is dword. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 10h.
15	Reserved	RW	Reset to 1b.
31:16	Reserved	RO	Reset to 0000h.

7.3.21 POWER MANAGEMENT CAPABILITY ID REGISTER – OFFSET 80h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 01h to indicate that these are power management enhanced capability registers.

7.3.22 NEXT ITEM POINTER REGISTER – OFFSET 80h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Item Pointer	RO	The pointer points to the Message capability register (8Ch). The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 8Ch.

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7.3.23 POWER MANAGEMENT CAPABILITIES REGISTER – OFFSET 80h

BIT	FUNCTION	TYPE	DESCRIPTION
18:16	Power Management Revision	RO	Read as 011b to indicate the I/O bridge is compliant to Revision 1.1 of *PCI Power Management Interface Specifications.*
19	PME# Clock	RO	Does not apply to PCI Express. Must be hardwired to 0b.
20	Reserved	RO	Reset to 0b.
21	Device Specific Initialization	RO	Read as 0b to indicate the I/O bridge does not have device specific initialization requirements. The default value may be changed by SMBUS or auto-loading from EEPROM.
24:22	AUX Current	RO	Reset as 111b to indicate the I/O bridge need 375 mA in D3 state. The default value may be changed by SMBUS or auto-loading from EEPROM.
25	D1 Power State Support	RO	Read as 1b to indicate the I/O bridge supports the D1 power management state. The default value may be changed by SMBUS or auto-loading from EEPROM.
26	D2 Power State Support	RO	Read as 1b to indicate the I/O bridge supports the D2 power management state. The default value may be changed by SMBUS or auto-loading from EEPROM.
31:27	PME# Support	RO	Read as 11111b to indicate the I/O bridge supports the forwarding of PME# message in all power states. The default value may be changed by SMBUS or auto-loading from EEPROM.

7.3.24 POWER MANAGEMENT DATA REGISTER – OFFSET 84h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Power State	RW	Indicates the current power state of the I/O bridge. Writing a value of D0 causes a hot reset without asserting PEREST_L when the previous state was D3. 00b: D0 state 01b: D1 state 10b: D2 state 11b: D3 hot state Reset to 00b.
2	Reserved	RO	Read as 0b.
3	No_Soft_Reset	RO	When set, this bit indicates that I/O bridge transitioning from D3hot to D0 does not perform an internal reset. When clear, an internal reset is performed when power state transits from D3hot to D0. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 1b.
7:4	Reserved	RO	Read as 0h.
8	PME# Enable	RW	When asserted, the I/O bridge will generate the PME# message. Reset to 0b.
12:9	Data Select	RW	Select data registers. Reset to 0h.
14:13	Data Scale	RO	Read as 00b.
15	PME status	RWC / RO	Indicates that the PME# message is pending internally to the I/O bridge for Func 0 and Func 1. This bit is reserved for Func 2 and always read as 0. Reset to 0b (RWC) for OHCI (Func 0 /Func 1). Read as 0b (RO) for EHCI (Func 2)

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7.3.25 PPB SUPPORT EXTENSIONS – OFFSET 84h

BIT	FUNCTION	TYPE	DESCRIPTION
21:16	Reserved	RO	Reset to 000000b.
22	B2_B3 Support for $D3_{HOT}$	RO	Does not apply to PCI Express. Must be hardwired to 0b.
23	Bus Power / Clock Control Enable	RO	Does not apply to PCI Express. Must be hardwired to 0b.

7.3.26 PM DATA REGISTER – OFFSET 84h

BIT	FUNCTION	TYPE	DESCRIPTION
31:24	PM Data Register	RO	PM Data Register. Reset to 00h

7.3.27 MESSAGE SIGNALED INTERRUPT (MSI) Capability ID Register 8Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capability ID	RO	Read as 05h to indicate that this is Message Signaled Interrupt capability register. The MSI Function is not implemented on this device.

7.3.28 MESSAGE SIGNALED INTERRUPT (MSI) NEXT ITEM POINTER 8Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Item Pointer	RO	The pointer points to the PCI Express capability register (E0h). The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to E0h.

7.3.29 MESSAGE CONTROL REGISTER – OFFSET 8Ch

BIT	FUNCTION	TYPE	DESCRIPTION
16	MSI Enable	RW	The MSI Function is not implemented on this device. Reset to 0b.
19:17	Multiple Message Capable	RO	The MSI Function is not implemented on this device. Read as 000b.
22:20	Multiple Message Enable	RW	The MSI Function is not implemented on this device. Reset to 000b.
23	64-bit address capable	RO	The MSI Function is not implemented on this device. Reset to 0b.
31:24	Reserved	RO	Reset to 00h.

7.3.30 MESSAGE ADDRESS REGISTER – OFFSET 90h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Reserved	RO	Reset to 00b.

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BIT	FUNCTION	TYPE	DESCRIPTION
31:2	Message Address	RW	The MSI Function is not implemented on this device. Reset to 0.

7.3.31 MESSAGE DATA REGISTER – OFFSET 94h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Message Data	RW	The MSI Function is not implemented on this device. Reset to 0000h.

7.3.32 USB PHYSICAL LAYER CONTROL REGISTER (USB PORT 1) – OFFSET A0h

BIT	FUNCTION	TYPE	DESCRIPTION
0	PMOS Strength for HS Driver Timing Control	RO	Reset to 0b. The default value may be changed by SMBUS or auto-loading from EEPROM.
2:1	NMOS Strength for HS Driver Timing Control	RO	Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.
4:3	HS Driver Amplitude	RO	Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.
8:5	HS Driver Slope Control	RO	Reset to 0000b. The default value may be changed by SMBUS or auto-loading from EEPROM.
10:9	Reference Voltage for Disconnect Circuit	RO	Reset to 10b. The default value may be changed by SMBUS or auto-loading from EEPROM.
12:11	Reference Voltage for Squelch Circuit	RO	Reset to 10b. The default value may be changed by SMBUS or auto-loading from EEPROM.
15:13	Reference Voltage for Calibration Circuit	RO	Reset to 100b. The default value may be changed by SMBUS or auto-loading from EEPROM.
17:16	Charge Pump Current for PLL	RO	Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.
19:18	FS Rise/Fall Time Control	RO	Reset to 01b. The default value may be changed by SMBUS or auto-loading from EEPROM.
21:20	LS Rise/Fall Time Control	RO	Reset to 01b. The default value may be changed by SMBUS or auto-loading from EEPROM.
23:22	HS Driver Pre-Emphasis	RO	Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.

7.3.33 USB PHYSICAL LAYER CONTROL REGISTER (USB PORT 2) – OFFSET A4h

BIT	FUNCTION	TYPE	DESCRIPTION
0	PMOS Strength for HS Driver Timing Control	RO	Reset to 0b. The default value may be changed by SMBUS or auto-loading from EEPROM.
2:1	NMOS Strength for HS Driver Timing Control	RO	Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.
4:3	HS Driver Amplitude	RO	Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.
8:5	HS Driver Slope Control	RO	Reset to 0000b. The default value may be changed by SMBUS or auto-loading from EEPROM.
10:9	Reference Voltage for Disconnect	RO	Reset to 10b. The default value may be changed by SMBUS or auto-loading from EEPROM.

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BIT	FUNCTION	TYPE	DESCRIPTION
	Circuit		
12:11	Reference Voltage for Squelch Circuit	RO	Reset to 10b. The default value may be changed by SMBUS or auto-loading from EEPROM.
15:13	Reference Voltage for Calibration Circuit	RO	Reset to 100b. The default value may be changed by SMBUS or auto-loading from EEPROM.
17:16	Charge Pump Current for PLL	RO	Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.
19:18	FS Rise/Fall Time Control	RO	Reset to 01b. The default value may be changed by SMBUS or auto-loading from EEPROM.
21:20	LS Rise/Fall Time Control	RO	Reset to 01b. The default value may be changed by SMBUS or auto-loading from EEPROM.
23:22	HS Driver Pre-Emphasis	RO	Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.

7.3.34 USB PHYSICAL LAYER CONTROL REGISTER (USB PORT 3) – OFFSET A8h

BIT	FUNCTION	TYPE	DESCRIPTION
0	PMOS Strength for HS Driver Timing Control	RO	Reset to 0b. The default value may be changed by SMBUS or auto-loading from EEPROM.
2:1	NMOS Strength for HS Driver Timing Control	RO	Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.
4:3	HS Driver Amplitude	RO	Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.
8:5	HS Driver Slope Control	RO	Reset to 0000b. The default value may be changed by SMBUS or auto-loading from EEPROM.
10:9	Reference Voltage for Disconnect Circuit	RO	Reset to 10b. The default value may be changed by SMBUS or auto-loading from EEPROM.
12:11	Reference Voltage for Squelch Circuit	RO	Reset to 10b. The default value may be changed by SMBUS or auto-loading from EEPROM.
15:13	Reference Voltage for Calibration Circuit	RO	Reset to 100b. The default value may be changed by SMBUS or auto-loading from EEPROM.
17:16	Charge Pump Current for PLL	RO	Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.
19:18	FS Rise/Fall Time Control	RO	Reset to 01b. The default value may be changed by SMBUS or auto-loading from EEPROM.
21:20	LS Rise/Fall Time Control	RO	Reset to 01b. The default value may be changed by SMBUS or auto-loading from EEPROM.
23:22	HS Driver Pre-Emphasis	RO	Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.

7.3.35 USB PHYSICAL LAYER CONTROL REGISTER (USB PORT 4) – OFFSET ACh

BIT	FUNCTION	TYPE	DESCRIPTION
0	PMOS Strength for HS Driver Timing Control	RO	Reset to 0b. The default value may be changed by SMBUS or auto-loading from EEPROM.
2:1	NMOS Strength for HS Driver Timing Control	RO	Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.
4:3	HS Driver Amplitude	RO	Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.
8:5	HS Driver Slope Control	RO	Reset to 0000b. The default value may be changed by SMBUS or auto-loading from EEPROM.

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BIT	FUNCTION	TYPE	DESCRIPTION
10:9	Reference Voltage for Disconnect Circuit	RO	Reset to 10b. The default value may be changed by SMBUS or auto-loading from EEPROM.
12:11	Reference Voltage for Squelch Circuit	RO	Reset to 10b. The default value may be changed by SMBUS or auto-loading from EEPROM.
15:13	Reference Voltage for Calibration Circuit	RO	Reset to 100b. The default value may be changed by SMBUS or auto-loading from EEPROM.
17:16	Charge Pump Current for PLL	RO	Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.
19:18	FS Rise/Fall Time Control	RO	Reset to 01b. The default value may be changed by SMBUS or auto-loading from EEPROM.
21:20	LS Rise/Fall Time Control	RO	Reset to 01b. The default value may be changed by SMBUS or auto-loading from EEPROM.
23:22	HS Driver Pre-Emphasis	RO	Reset to 00b. The default value may be changed by SMBUS or auto-loading from EEPROM.

7.3.36 PCI EXPRESS CAPABILITY ID REGISTER – OFFSET E0h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Enhanced Capabilities ID	RO	Read as 10h to indicate that these are PCI express enhanced capability registers. The default value may be changed by SMBUS or auto-loading from EEPROM.

7.3.37 NEXT ITEM POINTER REGISTER – OFFSET E0h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Item Pointer	RO	Read as 00h. No other ECP registers. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 00h.

7.3.38 PCI EXPRESS CAPABILITIES REGISTER – OFFSET E0h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Capability Version	RO	Read as 0001b to indicate the I/O bridge is compliant to Revision 1.0a of *PCI Express Base Specifications*. The default value may be changed by SMBUS or auto-loading from EEPROM.
23:20	Device/Port Type	RO	Indicates the type of Legacy PCI Express Endpoint device. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 1h.
24	Slot Implemented	RO	It is not implemented. Hardwired to 0b.
29:25	Interrupt Message Number	RO	It is not implemented. Hardwired to 00000b.
31:30	Reserved	RO	Reset to 00b.

7.3.39 DEVICE CAPABILITIES REGISTER – OFFSET E4h

BIT	FUNCTION	TYPE	DESCRIPTION
2:0	Max_Payload_Size Supported	RO	Indicates the maximum payload size that the I/O bridge can support for TLPs. The I/O bridge supports 256 bytes max payload size. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 001b.

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BIT	FUNCTION	TYPE	DESCRIPTION
4:3	Phantom Functions Supported	RO	It is not implemented. Hardwired to 00b.
5	Extended Tag Field Supported	RO	It is not implemented. Hardwired to 0b.
8:6	Endpoint L0s Acceptable Latency	RO	Acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 000b.
11:9	Endpoint L1 Acceptable Latency	RO	Acceptable total latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 000b.
12	Attention Button Present	RO	It is not implemented. Hardwired to 0b.
13	Attention Indicator Present	RO	It is not implemented. Hardwired to 0b.
14	Power Indicator Present	RO	It is not implemented. Hardwired to 0b.
15	Role_Base Error Reporting	RO	When set, indicated that the device implements the functionality originally defined in the Error Reporting ECN. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 1b.
17:16	Reserved	RO	Reset to 00b.
25:18	Captured Slot Power Limit Value	RO	In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. This value is set by the Set_Slot_Power_Limit message or hardwired to “00h”. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 00b.
27:26	Captured Slot Power Limit Scale	RO	Specifies the scale used for the Slot Power Limit Value. This value is set by the Set_Slot_Power_Limit message or hardwired to “00b”. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 00b.
31:28	Reserved	RO	Reset to 0h.

7.3.40 DEVICE CONTROL REGISTER – OFFSET E8h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Correctable Error Reporting Enable	RW	0b: Disable Correctable Error Reporting. 1b: Enable Correctable Error Reporting. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 0b.
1	Non-Fatal Error Reporting Enable	RW	0b: Disable Non-Fatal Error Reporting. 1b: Enable Non-Fatal Error Reporting. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 0b.
2	Fatal Error Reporting Enable	RW	0b: Disable Fatal Error Reporting. 1b: Enable Fatal Error Reporting. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 0b.
3	Unsupported Request Reporting Enable	RW	0b: Disable Unsupported Request Reporting. 1b: Enable Unsupported Request Reporting. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 0b.

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BIT	FUNCTION	TYPE	DESCRIPTION
4	Enable Relaxed Ordering	RW	Reset to 1b.
7:5	Max_Payload_Size	RW	This field sets maximum TLP payload size for the device. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported in the Device Capabilities register. Any value exceeding the Max_Payload_Size Supported written to this register results into clamping to the Max_Payload_Size Supported value. The default value may be SMBUS or changed by auto-loading from EEPROM. Reset to 000b.
8	Extended Tag Field Enable	RO	It is not implemented. Hardwired to 0b.
9	Phantom Function Enable	RO	It is not implemented. Hardwired to 0b.
10	Auxiliary (AUX) Power PM Enable	RO	When set, indicates that the I/O bridge is enabled to draw AUX power independent of PME AUX power. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 0b.
11	Enable No Snoop	RO	It is not implemented. Hardwired to 0b.
14:12	Max_Read_ Request_Size	RO	Reset to 000b.
15	Reserved	RO	Reset to 0b.

7.3.41 DEVICE STATUS REGISTER – OFFSET E8h

BIT	FUNCTION	TYPE	DESCRIPTION
16	Correctable Error Detected	RW1C	Asserted when correctable error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.
17	Non-Fatal Error Detected	RW1C	Asserted when non-fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.
18	Fatal Error Detected	RW1C	Asserted when fatal error is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.
19	Unsupported Request Detected	RW1C	Asserted when unsupported request is detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. Reset to 0b.
20	AUX Power Detected	RO	Asserted when the AUX power is detected by the I/O bridge Reset to 1b.
21	Transactions Pending	RO	It is not implemented. Hardwired to 0b.
31:22	Reserved	RO	Reset to 000h.

7.3.42 LINK CAPABILITIES REGISTER – OFFSET ECh

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	Maximum Link Speed	RO	Indicates the Maximum Link Speed of the given PCIe Link. Defined encodings are: 0001b, which indicates 2.5 Gb/s Link Reset to 1h.

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BIT	FUNCTION	TYPE	DESCRIPTION
9:4	Maximum Link Width	RO	Indicates the maximum width of the given PCIe Link. Reset to 000001b (x1).
11:10	Active State Power Management (ASPM) Support	RO	Indicates the level of ASPM supported on the given PCIe Link. The I/O bridge supports L0s and L1 entry. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 01b.
14:12	L0s Exit Latency	RO	Indicates the L0s exit latency for the given PCIe Link. The length of time this I/O bridge requires to complete transition from L0s to L0 is in the range of 256ns to less than 512ns. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 011b.
17:15	L1 Exit Latency	RO	Indicates the L1 exit latency for the given PCIe Link. The length of time this I/O bridge requires to complete transition from L1 to L0 is in the range of 16us to less than 32us. The default value may be changed by SMBUS or auto-loading from EEPROM. Reset to 000b.
23:18	Reserved	RO	Reset to 00000b.
31:24	Port Number	RO	It is not implemented. Hardwired to 00h.

7.3.43 LINK CONTROL REGISTER – OFFSET F0h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Active State Power Management (ASPM) Control	RW	00b: ASPM is Disabled. 01b: L0s Entry Enabled. 10b: L1 Entry Enabled. 11b: L0s and L1 Entry Enabled. Note that the receiver must be capable of entering L0s even when the field is disabled. Reset to 00b.
2	Reserved	RO	Reset to 0h.
3	Read Completion Boundary (RCB)	RO	It is not implemented. Hardwired to 0b.
4	Link Disable	RW	Reset to 0b.
5	Retrain Link	RW	Reset to 0b.
6	Common Clock Configuration	RW	0b: The components at both ends of a link are operating with asynchronous reference clock. 1b: The components at both ends of a link are operating with a distributed common reference clock. Reset to 0b.
7	Extended Synch	RW	When set, it transmits 4096 FTS ordered sets in the L0s state for entering L0 state and transmits 1024 TS1 ordered sets in the L1 state for entering L0 state Reset to 0b.
15:8	RsvdP	RO	Reset to 00h.

7.3.44 LINK STATUS REGISTER – OFFSET F0h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Link Speed	RO	Indicates the negotiated Link Speed of the given PCIe Link. Defined encodings are: 0001b, which indicates 2.5 Gb/s Link Reset to 1h.

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BIT	FUNCTION	TYPE	DESCRIPTION
25:20	Negotiated Link Width	RO	Indicates the negotiated width of the given PCIe Link, Reset to 000001b.
26	Training Error	RO	When set, indicates a Link training error occurred. This bit is cleared by hardware upon successful training of the link to the L0 link state. Reset to 0b.
27	Link Training	RO	When set, indicates the link training is in progress. Hardware clears this bit once link training is complete. Reset to 0b.
28	Slot Clock Configuration	RO	It is not implemented. Hardwired to 0b.
31:29	Reserved	RO	Reset to 000b.

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8 CLOCK SCHEME

8.1 PCI EXPRESS INTERFACE

The PCI Express interface of PI7C9X440SL requires 100MHz differential clock inputs through REFCLKP and REFCLKN Pins as shown in the following table.

Table 8-1 Input Clock Requirements for PCI Express Interface

Parameter	Symbol	Min	Max.	Unit
Reference Frequency(1)	f_j	83.3	312.5	MHz
Accuracy	A_j	-300	+300	ppm
Duty Cycle	DC_j	45	55	%
> 1.5 MHz to Nyquist RMS jitter after applying PCIe filter function	$T_{REFCLK-HF-RMS}$	-	3.1	ps RMS
10 KHz – 1.5 MHz RMS jitter	$T_{REFCLK-LF-RMS}$	-	3.0	ps RMS
Spread Spectrum Clock frequency	SSC_{freq}	30	33	KHz

(1) Does not include ±300ppm. Only certain clock frequencies will produce valid PCI Express data.
(2) Specified as per PCI Express Card Electromechanical specification, Rev 1.1.

8.2 USB INTERFACE

PI7C9X440SL requires an external 12 MHz crystal or oscillator of ±60ppm tolerance.

Table 8-2 Input Clock Requirements for USB Interface

Parameter	Condition	Min	Typ.	Max.	Unit
Clock deviation		-150		150	ppm
Rise/fall time				200	ps
Jitter (peak-to-peak)	<1.2MHz	0		50	ps
Jitter (peak-to-peak)	>1.2MHz	0		100	ps
Duty-cycle		40		60	%

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9 IEEE 1149.1 COMPATIBLE JTAG CONTROLLER

An IEEE 1149.1 compatible Test Access Port (TAP) controller and associated TAP pins are provided to support boundary scan in PI7C9X440SL for board-level continuity test and diagnostics. The TAP pins assigned are TCK, TDI, TDO, TMS and TRST_L. All digital input, output, input/output pins are tested except TAP pins.

9.1 INSTRUCTION REGISTER

The IEEE 1149.1 Test Logic consists of a TAP controller, an instruction register, and a group of test data registers including Bypass and Boundary Scan registers. The TAP controller is a synchronous 16-state machine driven by the Test Clock (TCK) and the Test Mode Select (TMS) pins. An independent power on reset circuit is provided to ensure the machine is in TEST_LOGIC_RESET state at power-up.
PI7C9X440SL implements a 5-bit Instruction register to control the operation of the JTAG logic. The defined instruction codes are shown in the following table. Those bit combinations that are not listed are equivalent to the BYPASS (11111) instruction:

Table 9-1 Instruction Register Codes

Instruction	Operation Code (binary)	Register Selected	Operation
EXTEST	00000	Boundary Scan	Drives / receives off-chip test data
SAMPLE	00001	Boundary Scan	Samples inputs / pre-loads outputs
HIGHZ	00101	Bypass	Tri-states output and I/O pins except TDO pin
CLAMP	00100	Bypass	Drives pins from boundary-scan register and selects Bypass register for shifts
IDCODE	01100	Device ID	Accesses the Device ID register, to read manufacturer ID, part number, and version number
BYPASS	11111	Bypass	Selected Bypass Register
INT_SCAN	00010	Internal Scan	Scan test
MEM_BIST	01010	Memory BIST	Memory BIST test

9.2 BYPASS REGISTER

The required bypass register (one-bit shift register) provides the shortest path between TDI and TDO when a bypass instruction is in effect. This allows rapid movement of test data to and from other components on the board. This path can be selected when no test operation is being performed on the PI7C9X440SL.

9.3 DEVICE ID REGISTER

This register identifies Pericom as the manufacturer of the device and details the part number and revision number for the device.

Table 9-2 JTAG Device ID Register

Bit	Type	Value	Description
31-28	RO	0001	Version number
27-12	RO	1001001000000100	Last 4 digits (hex) of the die part number
11-1	RO	01000111111	Pericom identifier assigned by JEDEC
0	RO	1	Fixed bit equal to 1'b1

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9.4 BOUNDARY SCAN REGISTER

The boundary scan register has a set of serial shift-register cells. A chain of boundary scan cells is formed by connected the internal signal of the PI7C9X440SL package pins. The VDD, VSS, and JTAG pins are not in the boundary scan chain. The input to the shift register is TDI and the output from the shift register is TDO. There are 4 different types of boundary scan cells, based on the function of each signal pin.

The boundary scan register cells are dedicated logic and do not have any system function. Data may be loaded into the boundary scan register master cells from the device input pins and output pin-drivers in parallel by the mandatory SAMPLE and EXTEST instructions. Parallel loading takes place on the rising edge of TCK.

9.5 JTAG BOUNDARY SCAN REGISTER ORDER

Table 9-3 JTAG Boundary Scan Register Definition

Boundary Scan Register Number	Pin Name	Pin No	Type	Tri-state Control Cell
0	TEST5	114	Input	4
1	IRQ1_I	16	Bidir	4
2	IRQ12_I	17	Bidir	4
3	IRQ1_O	18	Bidir	4
4			Control	
5	IRQ12_O	19	Bidir	4
6	LEG_EMU_EN	20	Bidir	4
7	SMBCLK	21	Bidir	4
8	SMBDATA	64	Bidir	4
9	TEST3	65	Bidir	4
10	TEST6	66	Bidir	4
11	GPIO[0]	69	Bidir	12
12			Control	
13	GPIO[1]	70	Bidir	14
14			Control	
15	GPIO[2]	71	Bidir	16
16			Control	
17	GPIO[3]	72	Bidir	18
18			Control	
19	GPIO[4]	73	Bidir	20
20			Control	
21	GPIO[5]	74	Bidir	22
22			Control	
23	GPIO[6]	75	Bidir	24
24			Control	
25	GPIO[7]	76	Bidir	26
26			Control	
27	TEST4	77	Bidir	4
28			Internal	
29			Internal	
30			Internal	
31	EECLK	99	Output2	
32	EEPD	98	Bidir	33
33			Control	
34	PERST_L	104	Input	
35			Internal	
36			Internal	
37			Internal	
38	MAIN_DETECT	24	Input	
39			Internal	
40			Internal	
41	TEST1	1	Bidir	4

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Boundary Scan Register Number	Pin Name	Pin No	Type	Tri-state Control Cell
42			Internal	
43	IO_HIT_I	3	Bidir	4
44	OCI[1]	4	Input	
45	OCI[2]	5	Input	
46	OCI[3]	6	Input	
47	OCI[4]	7	Input	
48	POE[1]	10	Bidir	4
49	POE[2]	11	Bidir	4
50	POE[3]	12	Bidir	4
51	POE[4]	13	Bidir	4
52	SMI_O	14	Bidir	4
53			Internal	

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10 POWER MANAGEMENT

10.1 PCI EXPRESS POWER STATES

The PI7C9X440SL implements a full set of PCI Express power management capabilities including full support for D0, D1, D2, D3-hot, and D3-cold Power States. The PCI Express Physical Link Layer of the PI7C9X440SL device supports the PCI Express Link Power Management with L0, L0s, L1, L2/L3 ready and L3 Power States.

During the transition from D3-hot to D3-cold state, the main power supplies of VDDC and VDDR are turned off to save power. PI7C9X440SL has been designed to have sticky registers that are powered by auxiliary power supplies. PI7C9X440SL forwards power management messages to the upstream Switches or root complex.

PI7C9X440SL also supports ASPM (Active State Power Management) to facilitate the link power saving and PME messaging.

10.2 USB POWER STATES

The EHCI Host Controller implements power management states compliant to PCI Bus Power Management Interface Specification, Revision 1.1 including D0, D1, D2, and D3-hot.

The OHCI Host Controller implements the following power states via the operational registers: USB_Reset, USB_Operational, USB_Suspend and USB_Resume. These states define the Host Controller's responsibilities relating to USB signaling and bus states. The OHCI Host Controller asserts the Power Management Event signal (PME_L) whenever the power state is resumed to Operational State from Suspend State.

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11 ELECTRICAL AND TIMING SPECIFICATIONS

11.1 ABSOLUTE MAXIMUM RATINGS

Table 11-1 Absolute Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Item	Absolute Max. Rating
Storage Temperature	-65°C to 150°C
Junction Temperature, Tj	125 °C
Digital core and analog supply voltage to ground potential (VDDC and AVDD)	-0.3v to 1.2v
Digital I/O and analog high supply voltage to ground potential (VDDR, VDDA and AVDDH)	-0.3v to 3.8v
DC input voltage for Digital I/O signals	-0.3v to 3.8v

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

11.2 Operating Ambient Temperature

Table 11-2 Operating Ambient Temperature

(Above witch the useful life may be impaired.)

Item	Low	High	Unit
Ambient Temperature with power applied	-40	85	°C

Note: Exposure to high temperature conditions for extended periods of time may affect reliability.

11.3 POWER CONSUMPTION

Table 11-3 PI7C9X440SL Power Dissipation

Mode	Typical Power Dissipation (mW)
L0 Normal Mode	432

11.4 DC SPECIFICATIONS

Table 11-4 DC Electrical Characteristics

Power Pins	Min.	Typ.	Max.
VDDC	0.9v	1.0v	1.1v
VDDR	3.0v	3.3v	3.6v
VDDA	3.0v	3.3v	3.6v
AVDD	0.95v	1.0v	1.1v
AVDDH	3.0v	3.3v	3.6v

VDDC: digital power supply for the core
VDDR: digital power supply for 3.3v I/O Interface
VDDA: analog power supply for 3.3v USB Interface
AVDD: analog power supply for 1.0v PCI Express Interface
AVDDH: analog power supply for 3.3v PCI Express Interface

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Table 11-5 DC Electrical Characteristics for Digital I/O

Symbol	Parameter		Min.	Typ.	Max.
V_{IH}	Input High Voltage		2.0V		
V_{IL}	Input Low Voltage				0.8V
V_T	Threshold Point		1.29V	1.39V	1.49V
V_{T+}	Schmitt trig. Low to High Threshold Point		1.47V	1.61V	1.75V
V_{T-}	Schmitt trig. High to Low Threshold Point		0.99V	1.08V	1.18V
I_L	Input Leakage Current				±1uA
I_{oz}	Tri-State Output Leakage Current				±1uA
P_{PU}	Pull-up Resistor		61kohm	75kohm	105kohm
P_{PD}	Pull-down Resistor		101kohm	199kohm	332kohm
V_{OL}	Output Low Voltage @ I_{OL}=2, 4mA				0.4V
V_{OH}	Output High Voltage @ I_{OH}=2, 4mA		2.4V		
I_{OL}	Low Level Output Current @V_{OL} =0.4V	2mA	2.1mA	3.3mA	4.1mA
		4mA	4.2mA	6.6mA	8.2mA
I_{OH}	High Level Output Current @V_{OH} =2.4V	2mA	2.8mA	6.1mA	9.9mA
		4mA	5.5mA	12.2mA	19.8mA

11.5 AC SPECIFICATIONS

Table 11-6 PCI Express Interface - Differential Transmitter (TX) Output Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	399.88	400.0	400.12	ps
Differential p-p TX voltage swing	$V_{TX-DIFF-P-P}$	800	-	-	mV ppd
Lower power differential p-p TX voltage swing	$V_{TX-DIFF-P-P-LOW}$	400	-	-	mV ppd
TX de-emphasis level ratio	$V_{TX-DE-RATIO}$	-3.0	-	-4.0	dB
Minimum TX eye width	T_{TX-EYE}	0.75	-	-	UI
Maximum time between the jitter median and max deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.125	UI
Transmitter rise and fall time	$T_{TX-RISE-FALL}$	0.125	-	-	UI
Maximum TX PLL Bandwidth	BW_{TX-PLL}	-	-	22	MHz
Maximum TX PLL BW for 3dB peaking	$BW_{TX-PLL-LO-3DB}$	1.5	-	-	MHz
Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	0	-	100	mV
Absolute Delta of DC Common Mode Voltage between D+ and D–	$V_{TX-CM-DC-LINE-DELTA}$	0	-	25	mV
Electrical Idle Differential Peak Output Voltage	$V_{TX-IDLE-DIFF-AC-p}$	0	-	20	mV
The Amount of Voltage Change Allowed During Receiver Detection	$V_{TX-RCV-DETECT}$	-	-	600	mV
Transmitter DC Common Mode Voltage	$V_{TX-DC-CM}$	0	-	3.6	V
Transmitter Short-Circuit Current Limit	$I_{TX-SHORT}$	-	-	90	mA
DC Differential TX Impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω
Lane-to-Lane Output Skew	$L_{TX-SKEW}$	-	-	500 ps + 2 UI	ps

Table 11-7 PCI Express Interface - Differential Receiver (RX) Input Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	399.88	400.0	400.12	ps
Differential RX Peak-to-Peak Voltage	$V_{RX-DIFF-PP-CC}$	175	-	1200	mV
Receiver eye time opening	T_{RX-EYE}	0.4	-	-	UI
Maximum time delta between median and deviation from median	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.3	UI
Receiver DC common mode impedance	Z_{RX-DC}	40	-	60	Ω
DC differential impedance	$Z_{RX-DIFF-DC}$	80	-	120	Ω
RX AC Common Mode Voltage	$V_{RX-CM-AC-P}$	-	-	150	mV
DC input CM input impedance during reset or power down	$Z_{RX-HIGH-IMP-DC}$	200	-	-	kΩ

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Parameter	Symbol	Min	Typ	Max	Unit
Electrical Idle Detect Threshold	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$	65	-	175	mV
Lane to Lane skew	$L_{RX\text{-}SKEW}$	-	-	20	ns

Table 11-8 USB Interface Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Timing Characteristics					
t_{rise}	1.5 Mbps 12 Mbps 480 Mbps	75 4 0.5	-	300 20	ns
t_{fall}	1.5 Mbps 12 Mbps 480 Mbps	75 4 0.5	-	300 20	ns
Jitter	1.5 Mbps 12 Mbps 480 Mbps	-	-	10 1 0.2	ns
Electrical Characteristics					
Vcm DC (DC level measured at receiver connector)	HS Mode LS/FS Mode	-0.05 0.8	-	0.5 2.5	V
Crossover Voltages	LS Mode FS Mode	1.3 1.3	-	2 2	V
Power supply ripple noise (Analog 3.3V)	< 1.2MHz	-10	0	10	mV
	> 1.2MHz	-50	0	50	
Power supply ripple noise CORE (Digital Supply)	All conditions	-50	0	50	mV
VBUS Comparators Voltage Thresholds					
A-Device Session Valid	-	0.8	-	2.0	V
B-Device Session Valid	-	0.8	-	4.0	V
B-Device Session End	-	0.2	-	0.8	V
VBUS Valid	-	4.4	-	4.75	V
DC Levels					
LS Idle Voltage		2.7	3.0	3.6	V
FS Idle Voltage		2.7	3.0	3.6	V
HS Test K	D+	-10.0	0.0	10.0	mV
	D-	360	400	440	mV
HS Test J	D+	360	400	440	mV
	D-	-10.0	0.0	10.0	mV
HS Test SE0	D+	-10.0	0.0	10.0	mV
	D-	-10.0	0.0	10.0	mV
CHIRP Levels					
CHIRP 'J'	D+ - D-	700	-	1100	mV
CHIRP 'K'	D+ - D-	-900	-	-500	mV

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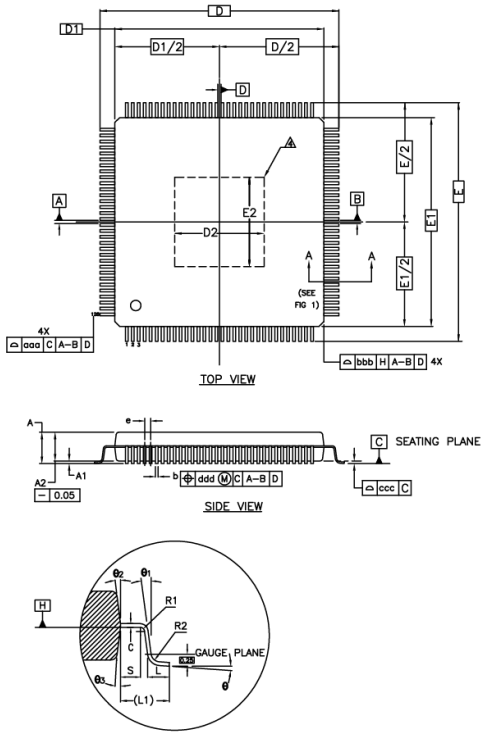
12 PACKAGE INFORMATION

The package of PI7C9X440SL is a 14mm x 14mm LQFP (128 Pin) package. The following are the package information and mechanical dimension:



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	—	0.16	—	—	0.006	—
e	0.40 BSC.			0.016 BSC.		
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		
D2	5.10	—	5.99	0.20	—	0.236
E2	5.10	—	5.99	0.20	—	0.236

NOTE :

1. ALL DIMENSION IN MM
2. REFER JEDEC MS–026
3. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR
4. THE OPTIONAL EXPOSED PAD IS COINCIDENT WITH THE BOTTOM SIDE OF THE PACKAGE AND NOT ALLOWED TO PROTRUDE BEYOND THAT SURFACE.

PERICOM Semiconductor Corporation — DATE: 12/11/14

DESCRIPTION: 128-pin Low Profile Quad Flat Package (LQFP)

PACKAGE CODE: FDE128

DOCUMENT CONTROL #: PD-2193 — REVISION: --

15-0001

Figure 12-1 Package Outline Drawing

1st *: Part Rev
2nd *: Die Rev
YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

Figure 12-2 Part Marking

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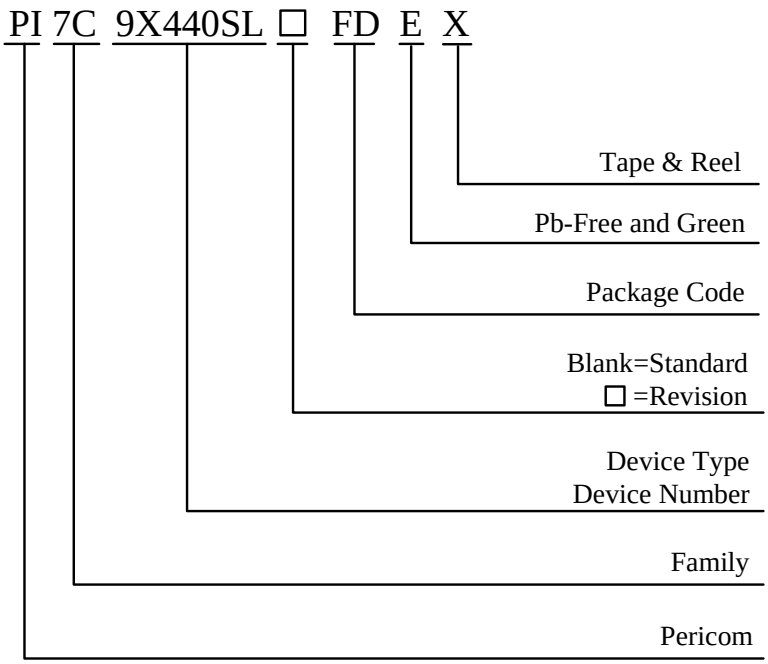
13 ORDERING INFORMATION

Part Number	Temperature Range	Package	Pb-Free & Green
PI7C9X440SL□FDEX	-40° to 85°C (Industrial Temperature Range)	128-pin LQFP 14mm x 14mm	Yes

Notes:

1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See http://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
4. E = Pb-free and Green
5. X suffix = Tape/Reel



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Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург, Промышленная ул, дом № 19, литера Н, помещение 100-Н Офис 331