UM11214 KITPF8121FRDMEVM evaluation board Rev. 1.0 – 22 April 2019

User guide



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1 Introduction

This document is the user guide for the KITPF8121FRDMEVM evaluation board. This document is intended for the engineers involved in the evaluation, design, implementation, and validation of multi-channel power management integrated circuit PF8121.

The scope of this document is to provide the user with information to evaluate the multichannel power management integrated circuit PF8121. This document covers connecting the hardware, installing the software and tools, configuring the environment and using the kit.

The KITPF8121FRDMEVM customer evaluation board provides full access to all the features in the PF8121 device.

Table 1.	Device	support
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Evaluation board	PMIC device	Link
KITPF8121FRDMEVM	PF8121	http://www.nxp.com/KITPF8121FRDMEVM

2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on <u>http://www.nxp.com</u>.

The information page for KITPF8121FRDMEVM evaluation board is at <u>http://</u> <u>www.nxp.com/KITPF8121FRDMEVM</u>. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to using the KITPF8121FRDMEVM evaluation board, including the downloadable assets referenced in this document.

2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community is at http://community.nxp.com.

3 Getting ready

Working with the KITPF8121FRDMEVM requires the kit contents, additional hardware and a Windows PC workstation with installed software.

3.1 Kit contents

- Assembled and tested evaluation board and preprogrammed FRDM-KL25Z microcontroller board in an anti-static bag
- 3.0ft. USB-STD A to USB-B-mini cable
- Quick Start Guide

3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this kit.

• Power supply with a range of 3.0 V to 5.0 V and a current limit set initially to 1.0 A (maximum current consumption can be up to 7.0 A)

3.3 Windows PC workstation

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

• USB-enabled computer with Windows 7, Windows 8, or Windows 10

3.4 Software

Installing software is necessary to work with this evaluation board. All listed software is available on the evaluation board's information page at <u>http://www.nxp.com/</u> <u>KITPF8121FRDMEVM</u> or from the provided link.

Software package NXP_FlexGUI_PF8x_Rev_0.7.x or higher contains:

- KL25Z firmware files
- NXP PF8x FlexGUI

4 Getting to know the hardware

The NXP analog product development boards provide an easy-to-use platform for evaluating NXP products. The boards support a range of analog, mixed-signal and power solutions. They incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost and improved performance in powering state-of-the-art systems.

4.1 Kit overview

The KITPF8121FRDMEVM is a customer evaluation board featuring the PF8121 power management IC. The kit integrates all hardware needed to fully evaluate the PMIC.

It integrates a communication bridge based on the FRDM-KL25Z freedom board to interface with the FlexGUI software interface to fully configure and control the PF8121 PMIC.

4.1.1 KITPF8121FRDMEVM features

Buck regulators

- SW1, SW2, SW3, SW4, SW5, SW6: 0.4 V to 1.8 V; 2500 mA; 2 % accuracy and dynamic voltage scaling and single, dual, triple or quad-phase configuration
- SW7; 1.0 V to 4.1 V; 2500 mA; 2 % accuracy
- Configurable VTT termination mode on SW6
- Programmable current limit
- Spread-spectrum and manual tuning of switching frequency

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LDO regulators

- 4x LDO regulator 1.5 V to 5.0 V, 400 mA: 3 % accuracy with optional load switch mode
- Selectable hardware/software control on LDO2

RTC supply VSNVS 1.8 V/3.0 V/3.3 V, 10 mA

• Battery backed memory including coin cell charger with programmable charge current and voltage

System features

- 2.5 to 5.5 V operating input voltage range
- USB to I²C communication via the FRDM-KL25Z interface
- Selectable hardwire default PMIC configuration or OTP/TBB operation
- Fast mode I²C communication at 400 kHz (high speed operation supported by PMIC)
- · Advance system monitoring/diagnostic via PMIC and/or system AMUX
- Master/slave interface connector
- Onboard I/O regulator with 1.8 V/3.3 V selectable output voltage

4.2 Kit featured components

Figure 2 identifies important components on the board.

KITPF8121FRDMEVM evaluation board



- 1. FRDM-KL25Z Freedom board connector
- 2. PF8121 PMIC
- 3. SW1 to SW4 power connector
- 4. SW5 to SW7 power connector
- 5. LDO output test points
- 6. Input power banana jack
- 7. External analog multiplexer
- 8. PMIC I/O test points
- 9. Analog supplies test points
- 10. 1.8 V/3.3 V external LDO regulator
- 11. Master/slave interface connector

Figure 2. Evaluation board featured component locations

4.2.1 PF8121: 12-channel power management integrated circuit for high performance applications

4.2.1.1 General description

The PF8121 is a power management integrated circuit (PMIC) designed for high performance consumer applications. It features seven high efficiency buck converters and four linear regulators for powering the processor, memory and miscellaneous peripherals.

KITPF8121FRDMEVM evaluation board

Built-in one time programmable memory stores key startup configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I²C after start up offering flexibility for different system states.

PF8121 is the consumer version of the higher end device, it features seven switching regulators and four LDOs, providing same power management and digital control with standard consumer qualification rating to address a cost effective platform for consumer applications.

4.2.1.2 Features

- · Up to seven high efficiency buck converters
- Four linear regulators with load switch options
- RTC supply and coin cell charger
- Watchdog timer/monitor
- Voltage and system monitoring circuits
- One time programmable device configuration
- 3.4 MHz I²C communication interface
- 56-pin 8 x 8 QFN package

4.3 Schematic, board layout and bill of materials

The board layout and bill of materials for the KITPF8121FRDMEVM evaluation board are available at <u>http://www.nxp.com/KITPF8121FRDMEVM</u>.

KITPF8121FRDMEVM evaluation board



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4.4 Default jumper configurations

Table 2. Evaluation board jumper descriptions

Name	Default	Description
J1, J2, J5, J6		Freedom board interface
J3	_	 Master/slave connector Odd row is connected directly to pins in the Master board Even row is used to connect a Slave board signals Interface connection is made via shunt resistors R1 to R11
J7	Shorted	Connects PMIC VIN to main board VIN node
J8	Shorted	Connects LDO4IN to main board VIN node
7 9	Shorted	Connects LDO3IN to main board VIN node
J11	Shorted	Connects LDO12IN to main board VIN node
J12	Shorted	Selects the external LDO voltage
J16	Open	 J12 → 1.8 V J16 → 3.3 V
J14	Open	LDO2EN pin control • 1-2 → LDO2EN pin pulled low • 2-3 → LDO2EN pin pulled high • Open → full MCU control with no pull up
J15	Shorted	Enables the PGOOD green LED
J17	Open	Supplies PMIC VIN from 5.0 V supply on Freedom Board (used only for demo functional operation, no loading capability in this operation mode)
J18	Open	Connects coin cell to the LICELL node
J20	1-2 shorted	 Selects PF8121 default register configuration 1-2 → OTP mode 2-3 → Hardwire mode
J21	Open	 Enables TBB mode on PF8121 device 1-2 → TBB mode disabled 2-3 → TBB mode enabled Open → MCU has control of this pin
J22	1-2 shorted	 Selects VDDIO supply 1-2 → VDDIO is supplied by external LDO regulator 2-3 → VDDIO is supplied by LDO1
J25	Open	 Selects STANDBY pin voltage level 1-2 → STANDBY pin low 2-3 → STANDBY pin high Open → STANDBY pin controlled by MCU
J26	2-3 shorted	Controls PWRON pull up source • 1-2 → PWRON pulled up to VSNVS • 2-3 → PWRON pulled up to VIN • Open → full MCU control with no pull up
J27	2-3 shorted	 Selects pull up for FSOB pin 1-2 → FSOB pulled up to VIN 2-3 → FSOB pulled up to VDDIO
J28	Shorted	Enables the FSOB red LED
J29	Open	Pulls down PWRON pin to ground

Name	Default	Description
J30	Open	 VSELECT pin control 1-2 → VSELECT pin pulled low 2-3 → VSELECT pin pulled low Open → full MCU control with no pull up
J32	Shorted	PWRON connection from PMIC to MCU
J33	Shorted	STANDBY connection from PMIC to MCU

4.5 Test points

Table 3. Evaluation board test point descriptions

Name (label)	Signal name	Description
Ground test points	<u>l</u>	
TP1, TP11, TP16, TP51 (GND)	GND	Ground plane test points
Digital I/O signal		
TP2 (PGOOD)	PGOOD	Connected to pin 42 (PGOOD) on PMIC
TP3 (FSOB)	FSOB	Connected to pin 29 (FSOB) on PMIC
TP4 (SDA)	SDA1	Connected to pin 56 (SDA) on PMIC. Main system I^2C bus.
TP5 (SCL)	SCL1	Connected to pin 55 (SCL) on PMIC. Main system I^2C bus.
TP6 (STANDBY)	STANDBY	Connected to pin 23 (STANDBY) on PMIC
TP7 (PWRON)	PWRON	Connected to pin 22 (PWRON) on PMIC
TP8 (SYNCOUT)	SYNCOUT	Connected to pin 49 (SYNCOUT) on PMIC
TP9 (SYNCIN)	SYNCIN	Connected to pin 48 (SYNCIN) on PMIC
TP10 (INTB)	INTB	Connected to pin 24 (INTB) on PMIC
TP12 (RESETBMCU)	RESETBMCU	Connected to pin 21 (RESETBMCU) on PMIC
TP24 (LDO2EN)	LDO2EN	Connected to pin 43 (LDO2EN) on PMIC
TP52 (EWARN)	EWARN	Connected to pin 20 (EWATN) on PMIC
TP53 (WDI)	WDI	Connected to pin 19 (WDI) on PMIC
TP62 (TBBEN)	TBBEN	Connected to pin 14 (TBBEN) on PMIC
TP65 (VSELECT)	VSELECT	Connected to pin 16 (VSELECT) on PMIC
TP80 (XFAILB)	XFAILB	Connected to pin 44 (XFAILB) on PMIC
Analog signals		
TP15 (VSNVS)	VSNVS	Connected to pin 47 (VSNVS) on PMIC
TP20 (LICELL)	LICELL	Connected to pin 46 (LICELL) on PMIC
TP22 (V1P5D)	V1P5D	Connected to pin 40 (V1P5D) on PMIC
TP23 (VIN_PIN)	VIN_PIN	Connected to pin 50 (VIN) on PMIC
TP25 (V1P5A)	V1P5A	Connected to pin 41 (V1P5A) on PMIC
TP26 (VDDIO)	VDDIO	Connected to pin 54 (VDDIO) on PMIC
TP54 (VREG)	VREG	1.8 V or 3.3 V external regulator output
TP63 (VDDOTP)	VDDOTP	Connected to pin 53 (VDDOTP) on PMIC
TP64 (AMUX)	AMUX	Connected to pin 52 (AMUX) on PMIC
LDO test points		
TP14 (LDO4OUT)	LDO4OUT	Power path for the LDO4 output

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Name (label)	Signal name	Description
TP18 (LDO3OUT)	LDO3OUT	Power path for the LDO3 output
TP19 (LDO2OUT)	LDO2OUT	Power path for the LDO2 output
TP21 (LDO1OUT)	LDO10UT	Power path for the LDO1 output
TP55	LDO4OUT sense	LDO4 output sense path. Connected directly to pin 28 (LDO4OUT) on PMIC.
TP56	LDO3OUT sense	LDO3 output sense path. Connected directly to pin 25 (LDO3OUT) on PMIC.
TP57	LDO2OUT sense	LDO2 output sense path. Connected directly to pin 18 (LDO2OUT) on PMIC.
TP58	LDO1OUT sense	LDO1 output sense path. Connected directly to pin 15 (LDO1OUT) on PMIC.
TP59	LDO12IN sense	LDO1 and LDO2 input sense path. Connected directly to pin 17 (LDO12IN) on PMIC.
TP60	LDO3IN sense	LDO3 input sense path. Connected directly to pin 26 (LDO3IN) on PMIC.
TP61	LDO4IN sense	LDO4 input sense path. Connected directly to pin 27 (LDO4IN) on PMIC.
Switching regulator test	points	,
TP66	SW1IN sense	SW1 input sense path. Connected directly to pin 4 (SW1IN) on PMIC.
TP67	SW2IN sense	SW2 input sense path. Connected directly to pin 7 (SW2IN) on PMIC.
TP68	SW3IN sense	SW3 input sense path. Connected directly to pin 8 (SW3IN) on PMIC.
TP69	SW4IN sense	SW4 input sense path. Connected directly to pin 11 (SW4IN) on PMIC.
TP70	SW5IN sense	SW5 input sense path. Connected directly to pin 32 (SW5IN) on PMIC.
TP71	SW6IN sense	SW6 input sense path. Connected directly to pin 35 (SW6IN) on PMIC.
TP72	SW7IN sense	SW7 input sense path. Connected directly to pin 37 (SW7IN) on PMIC.
TP73	SW1OUT sense	SW1 output sense path. Connected directly to pin 3 (SW1FB) on PMIC through R46.
TP74	SW2OUT sense	SW2 output sense path. Connected directly to pin 2 (SW2FB) on PMIC through R52.
TP75	SW3OUT sense	SW3 output sense path. Connected directly to pin 13 (SW3FB) on PMIC through R58.
TP76	SW4OUT sense	SW4 output sense path. Connected directly to pin 12 (SW4FB) on PMIC through R65.
TP77	SW5OUT sense	SW5 output sense path. Connected directly to pin 31 (SW5FB) on PMIC through R60.
TP78	SW6OUT sense	SW6 output sense path. Connected directly to pin 30 (SW6FB) on PMIC through R53.
TP79	SW7OUT sense	SW7 output sense path. Connected directly to pin 38 (SW7FB) on PMIC through R48.

4.6 Connectors

4.6.1 V_{IN} input power connector

 $V_{\mbox{\scriptsize IN}}$ is supplied to the board through standard banana jacks.

Table 4. V_{IN} Banana connectors

Schematic label	Signal name	Description
J4	GND	Main system ground
J10	V _{IN}	Main system input power supply System operating range from 2.5 V to 5.5 V

4.6.2 Switching regulators output power connectors

Table 5. SW1 through SW4 output power connector (J34)

Schematic label	Signal name	Description
J34-1	GND	System ground
J34-2	SW4OUT	SW4 regulator output
J34-3	SW3OUT	SW3 regulator output
J34-4	GND	System ground
J34-5	GND	System ground
J34-6	SW2OUT	SW2 regulator output
J34-7	SW1OUT	SW1 regulator output
J34-8	GND	System ground

Table 6. SW5 through SW7 output power connector (J35)

Schematic label	Signal name	Description
J34-1	GND	System ground
J34-2	SW7OUT	SW7 regulator output
J34-3	GND	System ground
J34-4	SW6OUT	SW6 regulator output
J34-5	SW5OUT	SW5 regulator output
J34-6	GND	System ground

4.6.3 Interface connector

Table 7. Master/slave interface connector (J3)

Schematic label	Signal name	Description
J3-1	RESETBMCU	Direct connection to RESETBMCU pin on board
J3-2	RESETBMCU_S	 Connection to external RESETBMU signal from slave PMIC RESETBMCU_S may be connected to local RESETBMCU pin through R12 (default)
J3-3	INTB	Direct connection to INTB pin on board

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Schematic label	Signal name	Description
J3-4	INTB_S	 Connection to external INTB signal from slave PMIC INTB_S may be connected to local INTB pin through R10 (optional) INTB_S may be connected to local XINTB pin through R8 (default)
J3-5	SYNCIN	Direct connection to SYNCIN pin on board.
J3-6	SYNCIN_S	 Connection to external SYNCIN signal from slave PMIC SYNCIN_S may be connected to local SYNCOUT pin through R9 (default)
J3-7	SYNCOUT	Direct connection to SYNCOUT pin on board
J3-8	n.c.	not connected
J3-9	XINTB	Direct connection to XINTB pin on board
J3-10	n.c.	not connected
J3-11	WDI	Direct connection to WDI pin on board
J3-12	WDI_S	 Connection to external WDI signal from slave PMIC WDI_S may be connected to local WDI pin through R7 (default)
J3-13	PWRON	Direct connection to PWRON pin on board
J3-14	PWRON_S	 Connection to external PWRON signal from slave PMIC. PWRON_S may be connected to RESETBMCU pin through R11 (optional) PWRON_S may be connected to PWRON pin through R6 (default)
J3-15	STANDBY	Direct connection to STANDBY pin on board
J3-16	STANDBY_S	 Connection to external STANDBY signal from slave PMIC STANDBY_S may be connected to STANDBY pin through R5 (default)
J3-17	SCL1	Direct connection to SCL1 signal on board
J3-18	SCL_S	 Connection to external SCL signal from slave PMIC SCL_S may be connected to SCL1 pin through R4 (default)
J3-19	SDA1	Direct connection to SDA1 signal on board
J3-20	SDA_S	Connection to external SDA signal from slave PMICSDA_S may be connected to SDA1 pin through R3 (default)
J3-21	TBBEN	Direct connection to TBBEN pin on board
J3-22	TBBEN_S	 Connection to external TBB signal from slave PMIC TBBEN_S may be connected to TBBEN2 signal controlled by MCU through R2 (default)
J3-23	XFAIL	Direct connection to XFAILB pin on board
J3-24	XFAIL_S	 Connection to external XFAILB signal from slave PMIC XFAILB_S may be connected to XFAILB signal on PMIC through R1 (default)

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5 Installing and configuring software and tools

The KITPF8121FRDMEVM uses FlexGUI software for PF8121 device. Prior to the installation of the FlexGUI software and performing device firmware updates (if needed), download and unzip the NXP_FlexGUI_PF8x_REV_0.7.x.zip file to any desired location.

The installation package is available at <u>http://www.nxp.com/KITPF8121FRDMEVM</u>.

5.1 Installing the Java JRE

- 1. Download Java JRE (Java SE Runtime Environment), available at <u>http://www.oracle.com/technetwork/java/javase/downloads/jre8-downloads-2133155.html</u> (8u162 or newer).
- 2. Open the installer and follow the installation instructions.
- 3. Following the successful installation, restart the computer.

5.2 Installing FlexGUI software package

The FlexGUI software installation requires only extracting the zip file in a desired location.

- 1. If necessary, install the Java JRE and Windows 7 FlexGUI driver.
- Download the latest FlexGUI (32-bit or 64-bit) version, NXP_FlexGUI_PF8x_REV_0.7.x.zip, available at <u>http://www.nxp.com/</u> <u>KITPF8121FRDMEVM</u>.
- 3. Extract all the files to a desired location on your PC.

FlexGUI is started by running the batch file, NXP_FlexGUI_PF8x_Rev_0.7.x\NXP FlexGUI\bin\flexgui-app-pf8xxxx.bat.

The FlexGUI Rev 0.7.0 or higher, interfaces with the FRDM-KL25Z freedom board via USB-HID protocol which should be recognized automatically by the Windows OS eliminating the need for any extra hardware drivers. See <u>Section 5.4 "Updating the PF8121 FlexGUI firmware"</u> for details on how to update the FRDM-KL25Z, in case the board is not loaded with the latest firmware with USB-HID support.

5.3 Uninstalling the application

The FlexGUI software does not store any files outside of its installation folder.

To uninstall FlexGUI, delete the flexgui.

5.4 Updating the PF8121 FlexGUI firmware

The FRDM-KL25Z freedom board is used as a communication bridge to interface the FlexGUI with the PMIC and other I^2C devices. The firmware is organized in three levels:

- 1. At first level, the SDA uses the BOOTLOADER to operate as the main path to flash the functional code of the SDA processor. The BOOTLOADER is preprogrammed on the FRDM-KL25Z freedom boards and cannot be reflashed to avoid permanent damage to the Freedom board.
- 2. At second level, the SDA provides a *firmware loader* for drag and drop update of the KL25Z MCU firmware.

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 At the third level, the KL25Z MCU provides the FlexGUI firmware in charge of converting the USB communication into MCU instructions to control digital I/Os as well as I²C communication to the PMIC.

If the FRDM-KL25Z is not loaded with the correct firmware to support a future software upgrade, the firmware can be updated in few simple steps.

Note: The following firmware updates are optional and can be skipped if the firmware is up-to-date.

5.4.1 Flashing the FRDM-KL25Z firmware loader

1. Press the push button on the Freedom board and connect the USB cable into the SDA port on the Freedom board. A new BOOTLOADER device should appear on the left pane of the file explorer.



2. Drag and drop the file *MSD-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA* into the BOOTLOADER drive. File should be located in the *KL25Z firmware* folder.

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3. Disconnect and reconnect the USB cable into the SDA port (this time without pressing the push button). A new device called *FRDM_KL25Z* is installed on the PC.

5.4.2 Flashing the FlexGUI firmware

If a new software or silicon release requires a firmware update on the FRDM-KL25Z freedom board, use the following procedure to upgrade or downgrade the firmware of the freedom board as needed. Note that this procedure is needed only to update the firmware and may be skipped if no change is needed.

- 1. Connect the USB cable in the SDA port (without holding the push button).
- 2. Locate the ".bin" FlexGUI driver to be installed, for example *flexgui-fw-kl25z-usb-hid-pf8x00-v0.1.1.bin*, drag and drop the file into the FRDM_KL25Z driver.

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3. Freedom board firmware is successfully loaded.

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6 Configuring the hardware for startup



- 1. With the USB cable connected to the PC and the USB port in the freedom board, apply VIN to the evaluation board.
 - Provide external VIN between 2.5 to 5.5 V on J10 (VIN) and J4 (GND) or
 - Short jumper J17 to provide 3V3 Vin from Freedom board (use this mode of operation for functional demonstration only, no regulation loading allowed in this mode).

Note: Do not apply power to J10 while J17 is shorted. This could damage the onboard regulator on the FRDM-KL25Z Freedom board.

- 2. Press Reset on the Freedom board, to ensure board is properly recognized.
- 3. Browse to the *NXP_FlexGUI/bin/* folder and double-click on the **flexgui-app-8xxx.jar** executable to start the application.
- 4. The FlexGUI launcher is displayed with a list of possible configurations to load the FlexGUI. Select the appropriate option for device and silicon revision to be used. If the device revision populated on the KITPF8121FRDMEVM is not available in the list, please contact your NXP representative to obtain the latest software update suitable for your device.

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FlexGUI Launcher		×
Select a kit, device(s) and its features		
Kit and device(s)		
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Release		
► KITPF8201FRDMEVM		
► KITPF8100FRDMEVM		
► KITPF8101FRDMEVM		
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A kit for PF8200 evaluation.		
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	OK Cancel	
ure 8 ElevGIII launcher		

Silicon revision ^[1]	Description
В0	Use this configuration if you have received B0 silicon samples for preliminary device evaluation.
Release	Use this configuration if you have received C1 silicon samples or production parts.

[1] During new silicon transition, the file versions should be selected according to the silicon being used.

When the FlexGUI is done loading, the USB-HID connection will automatically search for the KITPF8121FRDMEVM, if a valid board is connected, the corresponding *Vendor ID* and *Product ID* should appear, then click **Start** to create a connection.

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Once the device is connected, the system is ready for Hardwire or TBB operation as desired.

6.1 Operating in Hardwire mode

To operate the board with the default hardwire configuration:

- Open J29 and J26 to allow the MCU to control the PWRON pin
- Short J20 in position 2-3 (VDDOTP = V1P5D)
- Open J21 to allow the MCU to control the TBBEN pin

In Hardwire mode, the device is working with the predefined configuration and supplies will turn on when the PWRON pin is set to high. To generate a power on event, the FlexGUI can be set to *Normal mode* in the mode selection box.

PF8xxx Pins Miscellaneous
Device Information
Device ID: N/V
Revision ID: N/V
OTP Program ID: N/V
Device Mode
Switch Mode: normal-m Apply
Current Mode: user-mode Poll
Communication
I2C Address: 0x08 👻
CRC:
Secure Write
Figure 10. Normal mode operation

Click **Apply** to change the operating mode and start using the PMIC with the default configuration.

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See <u>Section 7 "Controlling the PF8121 using FlexGUI"</u> for detail description on how to control the PMIC with the FlexGUI.

6.2 Operating in TBB mode

To operate the board in TBB mode:

- Open J29
- Short J20 in position 1-2 (OTP/TBB operation)
- Open J21 to allow the MCU to control the TBBEN pin

There are two ways to operate the device in TBB mode:

- 1. Manual configuration of the OTP mirror registers using the TBB mode control.
- 2. Load the OTP mirror registers with a custom TBB script using the *PF8121 Custom OTP Request Form* provided in the *SCRIPT & FORMS* folder.

6.2.1 Manual TBB configuration

During manual TBB configuration, use the TBB mode selection to enable access to the OTP mirror registers in the PF8121 device.

	PF8xxx Pins Miscellaneous
	Device Information
	Device ID: N/V
	Revision ID: N/V
	OTP Program ID: N/V
	Device Mode
	Switch Mode: tbb-mode - Apply
	Current Mode: user-mode Poll
	Communication
	I2C Address: 0x08 -
	CRC:
	Secure Write
Figure 11. TBB mo	de operation

Click **Apply** to set the device in TBB mode and manually select the TBB configuration in the mirror registers.

When the FlexGUI is operating in TBB mode, the graphical interface uses command controls to communicate with the OTP mirror registers directly, enabling the user to manually set the default configuration one feature at a time.

After configuring the features to be used during the device evaluation, change the operating mode to normal mode to generate a power on event and allow command controls to modify the functional I^2C registers again.

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Detailed description on how to control the PMIC using the FlexGUI is described in <u>Section 7 "Controlling the PF8121 using FlexGUI"</u>.

6.2.2 Generating a TBB script

To load the OTP mirror registers from a TBB script, choose the device configuration and generate the TBB script using the *PF8121 Custom OTP Request Form* provided in the *SCRIPT & FORMS* folder.

- 1. Use the *PF8121 Custom OTP Request Form* to select the default configuration to be used during the KITPF8121FRDMEVM evaluation. Note that the OTP request form is prepared to generate a TBB script for PF8121, however, make sure you pick the correct device number matching the device soldered on the customer evaluation board.
- 2. Generate a TBB script using the file generation section on the OTP request form (make sure to fill all required fields marked with a * to enable file generation). When generating a TBB script, it is important to match the device name with the device name in the FlexGUI to ensure proper generation of the script commands.



Silicon revision ^[1]	OTP request form version
В0	OTP Customer Request Form Rev 2.2 +
C0	OTP Customer Request Form Rev 3.0 +

[1] During new silicon transition, the file versions should be selected according to the silicon revision.

- 3. Save the generated TBB file in a known location.
- 4. On the Script Editor, use the command section to load the TBB script created, and then click **Run** to start programming the PMIC.

The device is automatically enabled with the selected TBB configuration after the programming is done.

7 Controlling the PF8121 using FlexGUI

7.1 Application environment

The GUI uses standard application layout divided into several working areas (see Figure 12).

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- 1. Menu and connection toolbar
- 2. Command log area
- 3. Global system controls
- 4. Status bar
- 5. Device control area

Filter messages 🔹 🖌 📕 💾	PTB xxx Script editor									
PF8200 [PWRON] = 0	🛗 Register map 🔞 PMIC Config 🛛	Functional Safety 🕛 LDO	Regulators (SW Regulators SW Regulators E≡	Sequencer 🦻 Intern	ipts 🛛 📸 AMUX Con	trol			
PF8200 [PWRON] = 0	Registers Per Page 50 🐥 E	Bit Buttons Per Line 8	Sort	By Address 🖌 Uniform	m Buttons 🖌 Show Bit	Position				
	▼ functional	Write Read	Copy Rese	t						
	ID Registers				LDO2_UV_BYPASS	LDO2_OV_BYPASS	LDO2_JLIM_BYPASS	LDO2_UV_STATE	LDO2_OV_STATE	LDO2_ILIM_STATE
	Fault Management			W 0x0	LDO2_WDBYPASS	LDO2_PG_EN				
	System Configuration	LD02_CONFIG1	0x8B		LDO2_UV_BYPASS	LDO2_OV_BYPASS	LDO2_ILIM_BYPASS	LDO2_UV_STATE	LDO2_OV_STATE	LDO2_ILIM_STATE
	Watchdog Configuration			R 0x1c	LDO2_WDBYPASS	LDO2_PG_EN				
	AMUX Control				LDO2_FLT_REN	LDO2_PDGRP [1]	LDO2_PDGRP [0]	LDO2HW_EN	VSELECT_EN	RESERVED
	SW1 Control			W 0x0	LDO2_RUN_EN	LDO2_STBY_EN				
	SW2 Control SW3 Control	LD02_CONFIG2	0x8C		LDO2_FLT_REN	LDO2_PDGRP [1]	LDO2_PDGRP [0]	LDO2HW_EN	VSELECT_EN	RESERVED
	SW4 Control			R 0x80	LDO2_RUN_EN	LDO2_STBY_EN				
PF8200 Pins Miscellaneous	SW5 Control (5)				LDO2_SEQ [7]	LDO2_SEQ [6]	LDO2_SEQ [5]	LDO2_SEQ [4]	LDO2_SEQ [3]	LDO2_SEQ [2]
Device Information	SW7 Control			W 0x0	LDO2_SEQ [1]	LDO2_SEQ [0]				
Device ID: N/V	LDO1 Control	LDO2_PWRUP	0x8D		2 LDO2_SEQ [7]	LDO2_SEQ [6]	LDO2_SEQ [5]	LDO2_SEQ [4]	LDO2_SEQ [3]	LDO2_SEQ [2]
Revision ID: N/V	LDO2 Control			R 0x0	LDO2_SEQ [1]	LDO2_SEQ [0]				
Device Mode	LDOS Control				RESERVED	RESERVED	RESERVED	RESERVED	VLDO2_RUN [3]	VLDO2_RUN [2]
Switch Mode: user-mode	VSNVS Control			W 0x0	VLDO2_RUN [1]	VLDO2_RUN [0]				
Current Mode: user-mode Poll	Page Select	LDO2_RUN_VOL1	0x8E		RESERVED	RESERVED	RESERVED	RESERVED	VLDO2_RUN [3]	VLDO2_RUN [2]
Communication	- ongainmon			R 0x0	VLDO2_RUN [1]	VLDO2_RUN [0]				
I2C Address: 0x08 +					RESERVED	RESERVED	RESERVED	RESERVED	VLDO2_STBY [3]	VLDO2_STBY [2]
CRC:				W 0x0	VLDO2_STBY [1]	VLDO2_STBY [0]				
Secure Write		LDO2_STBY_VOL	F 0x8F		2					
	1					1/1				

7.1.1 Menu and connection toolbar

The menu and application toolbar offer access to various system dialogs as well as communication actions, see <u>Figure 13</u>. It is further divided into following subareas.

Applications menu	Enables default configuration supportQuits application
Help menu	Provides information regarding the FlexGUI version and support
Hide panel	Hides or shows the global control panel
Communication	 Provides board USB ID Vendor ID: identify vendor ID when a supported board is connected Product ID: identify product ID when a supported board is connected Start/Stop: establish connection with the board connected
Application Help	0v1542

Vendor ID: 0x15A2 Product ID: 0x00D0
Stop

Figure 13. Menu and application toolbar

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7.1.2 Command log area

The command log area informs the user about application events. Verbosity level is given by application configuration. User can interact with the area using toolbar on the top, which has following functions, see <u>Figure 14</u>. It is further divided into following subareas.

Filter selection	Enables various filtering schemes to display specific commands as desired
Clear log	Clears all messages from the log area
Pause log	Stops recording any new commands until the log is resumed again
Save log	Saves the content of the log area into a text file

Filter messages PF8xxx [WDI] = 1 PF8xxx [WDI] = 0 PF8xxx [PWRON] = 1 PF8xxx [TBBEN] = 1 PF8xxx [TBBEN] = 0
PF8xxx [WDI] = 1 PF8xxx [WDI] = 0 PF8xxx [PWRON] = 1 PF8xxx [PWRON] = 0 PF8xxx [TBBEN] = 1 PF8xxx [TBBEN] = 0

7.1.3 Global system controls

The global system control provide access to system configuration controls not related to the PMIC operation, as well as the I/O control signals from the MCU to the PMIC. It is divided into two tabs as shown in Figure 15.

PF8121 system contro	l tab
Device information	Provides device information of the PMIC connected

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Device mode	 Selects the mode of operation of the evaluation board to interact and fully showcase all features provided by the PMIC. The system may be operated in four predefined modes: User mode: no system I/O are modified by the FlexGUI allowing manual control of the PMIC using the Pin control tab. Normal mode: the FlexGUI sets the TBBEN = low, STANDBY = low, WDI = low and PWRON = high, generating a power-on event. In this mode of operation, the user can control the STANBY pin and the corresponding polarity to set the PMIC in Run or Standby modes. In this mode, the FlexGUI control will configure the functional I²C registers to modify the system configuration on-the-go. TBB mode: the FlexGUI sets the TBBEN = high, STANDBY = low, WDI = low and PWRON = low, causing the PMIC to turn off and move to the QPU_OFF state in order to allow the OTP mirror registers to be accessed and modified. In this mode, the FlexGUI uses the PMIC controls to program the default OTP configuration to be used in the next power up event. During TBB mode, only the controls which have OTP bits become available while all other functional bits are disabled until the system is set into Run or Standby modes.
Communication	 I²C address: selects the default address used to communicate with the PMIC. By default the I²C address is set to 0x08, but communication must be changed if the PMIC uses another I²C address as configured in the OTP mirror registers. I²C CRC enable: enables the MCU to add CRC calculation to each I²C transaction. Secure write enable: enables the MCU to perform automatic proofing to write Secure write registers.
Pin control tab	1
LDO2EN	Allows the MCU to control the level of the LDO2EN pin in the PMIC.
	Use this control in conjunction with the LDO2HW_EN bit to allow the LDO2 output to enable or disable by toggling the pin high or low.
XINTB	Allows the MCU to control the level of the XINTB pin in the PMIC. Use this control to generate an external interrupt on the PMIC.
VSELECT	Allows the MCU to control the level of the VSELECT pin in the PMIC. Use this control in conjunction with the VSELECT_EN bit to allow the LDO2 output to toggle between 1.8 V or 3.3 V by toggling the pin high or low.
STANDBY	Allows the MCU to control the level of the STANDBY pin in the PMIC. Use this control in conjunction with the STANDBYINV bit to force the PMIC in and out of the Standby mode by toggling the pin high or low.
PWRON	Allows the MCU to control the level of the PWRON pin in the PMIC. When the OTP_PWRON_MODE bit is set to level sensitive, use this control to generate a power-on or power-off event by toggling the pin high or low. When the OTP_PWRON_MODE bit is set to Edge sensitive, use this control to generate a rising or falling edge to simulate a push button to generate the corresponding power-on or power-off events.
TBBEN	Allows the MCU to control the level of the TBBEN pin in the PMIC. Use this control to enable debugging conditions as well as grant access to the OTP mirror registers.

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WDI	Allows the MCU to control the level of the WDI pin in the PMIC. Use this control in conjunction with the OTP_WDI_INV, to generate a watchdog reset event on a rising or falling edge of the WDI signal.								
Input pins	Allows the MCU to read the level of the EWARN and INTB pins. MCU can be programmed to poll the read or perform a single read.								
Miscellaneous control	Miscellaneous controls								
Watchdog refresh Enables the MCU to perform a watchdog refresh with the selected perio									
System diagnostics	 System diagnostic buttons Use the ABIST Run to start the ABIST on-demand test during the system-on states. Results of the ABIST test can be read in the Functional Safety tab. Use the INTB Test to request a 100 μs pulse in the INTB pin. Use the SW Shutdown to request a software shutdown event. The PMIC will restart if a power-up event is present after shutting down. 								

Output Pins DO2EN: INTB: SELECT:	No valu	Watchdog Refresh Enable: Period [ms]: 1000
DO2EN: INTB: ISELECT:	No valu	Enable:
INTB:	No valu	Period [ms]: 1000
SELECT:	Ne volu 🖉	renou man
	INO Valu +	
TANDBY:	No valu 👻	System Diagnostics
WRON:	Low -	INTB Test: Run
BBEN:	Low -	SW Shutdown: Run
VDI:	High 👻	ABIST: Run
 Input Pins 		
WARN: N	V/V	
500 ms	VV Poll Read	
	TANDBY:	TANDBY: No valu * WRON: Low * Unu *

7.1.4 Status bar

Status bar provides a standard overview of application conditions.

Status area	MCU status CONNECTED: GUI is connected to the MCU DISCONNECTED: GUI does not have connection to the MCU
Version area	 Informs the user about used module versions GUI: informs the user about version of derivative GUI Firmware: informs the user about version of used MCU firmware Build: informs the user about the building date for the current release

7.1.5 Device control area

This area enables the user to interact with all loaded devices. Each device has its own dedicated tab with several subtabs to access all controls dedicated to the specific device loaded, see Figure 16. In addition to the device tab, the FlexGUI provides a Script editor tab to allow sequential configuration and control of one or various devices with a command based script processor.

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Script editor	Enables user to create sequences of commands to control the device/s, see <u>Section 7.3 "Working with the Script editor"</u> for details on this generic component
Device control tab	Tabs/components enable user to work with device on high level abstraction of its features/functionality

functional	Dic buttons Per Line 8	30	rt by Al	uuress	V Onic	ann butt	Ions V Show Bit P	ostuon						
ID Registers	Write Read	opy Ne	set		0.0						1003 01/ 57475			1000.05.01
Interrupt Registers Fault Management	LDO2_CONFIG1	0x8B	0	R	0x1c	0	LDO2_UV_BYPASS	LDO2_OV_BYPASS	LDO2 ILIM BYPASS	LDO2_UV_STATE	LDO2_OV_STATE	LDO2 IUM STATE	LDO2_WDB1PASS	LDO2_PG_EN
System Configuration					0.0			1002 00680 (1)	1003 00680 (0)	LDOORWY EN	VERIERT EN	PESSENCE	1002 RUN EN	LDO2 STRY EN
Watchdog Configuration	LDO2_CONFIG2	0x8C	0	R	0,80	0	LDO2 FLT REN	1002 20682 (1)		LDO2HW EN	VSELECT EN		LDO2 RUN EN	LDO2 STRY EN
AMUX Control					0.00		coold croton	10000000000000						
SW1 Control	LDO2_PWRUP	0x8D	Ø	W	0.0	0	LDOS_SEQ [7]	LDOS_SEG [6]	LDO2_SEQ [5]	LDO2_SEQ [4]	LDOS_SEQ [3]	LDOS_SEQ [2]	rpos"2Ed [1]	rpos726d [0]
SW2 Control				R	0x0		LDO2_SEQ [7]	LDO2_SEQ [6]	LDO2_SEQ [5]	LDO2_SEQ (4)	LDO2_SEQ [3]	LDO2_SEQ [2]	LDO2_SEQ [1]	LDO2_SEQ [0]
SW3 Control SW4 Control	LDO2_RUN_VOLT	0x8E		W	0x0	0	RESERVED	RESERVED	RESERVED	RESERVED	VLDO2_RUN [3]	VLDO2_RUN [2]	VLDO2_RUN [1]	VLDO2_RUN [0]
SW5 Control			-	R	0x0		RESERVED	RESERVED	RESERVED	RESERVED	VLDO2_RUN [3]	VLDO2_RUN [2]	VLDO2_RUN [1]	VLDO2_RUN [0]
SW6 Control		005		W	0x0		RESERVED	RESERVED	RESERVED	RESERVED	VLDO2_STBY [3]	VLDO2_STBY [2]	VLDO2_STBY [1]	VLDO2_STBY [0]
SW7 Control	U02_3181_V011	UXOF	•	R	0x0] •	RESERVED	RESERVED	RESERVED	RESERVED	VLDO2_STBY [3]	VLDO2_STBY [2]	VLDO2_STBY [1]	VLDO2_STBY [0
LD02 Control LD03 Control LD04 Control VSNVS Control Page Select OTP_MIRROR									4 1 k					
ICIL CONNECTED									1/1			GUI: 0.01 FW- 0	1.0 Wed Apr 10.0	8:47:30 MST 201

7.2 Understanding the PF8121 workspace

The PMIC controls are organized in seven tabs specific to the PF8121 device and one tab providing bit by bit access to the register map of the device. The eight control tabs are listed below and are explained in the following sections.

- Register map
- PMIC configuration
- Fault monitoring
- LDO regulators
- Switching regulators
- Sequencer
- System interrupts
- AMUX control

7.2.1 Register map

The PF8121 registers are organized in register pages or sectors. The FlexGUI organizes the registers in various types and multiple register groups. For detailed view of the PF8121 register map, see PF8121 data sheet.

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Registers Per Page 50	Bit Buttons Per Line 8	Sor	rt By Ad	dress	V Unifo	rm Butt	ons 🗸 Show Bit P	osition Inte	erface Forma	tting				
ctional	Write Read C	opy Re	set	G	obal (Cotro	ls							
D Registers				w	0x0	\cap	LDO2_UV_BYPASS	LDO2_OV_BYPASS	LDO2_ILIM_BYPASS	LDO2_UV_STATE	LDO2_OV_STATE	LD02_ILIM_STATE	LDO2_WDBYPASS	LDO2_PG_EI
ault Management	LDO2_CONFIG1	0x8B	\odot	R	0x1c	0	LDO2_UV_BYPASS	LDO2_OV_BYPASS	LDO2_ILIM_BYPASS	LDO2_UV_STATE	LDO2_OV_STATE	LDO2_JUM_STATE	LDO2_WDBYPASS	LDO2_PG_E
stem Configuration														
atchdog Configuration	LD02_CONFIG2	0x8C		W	0x0	0	LDO2_FLT_REN	LDO2_PDGRP [1]	LDO2_PDGRP [0]	LDO2HW_EN	VSELECT_EN		LDO2_RUN_EN	LDO2_STBY_
ult Counters				R	0x80		LDO2_FLT_REN	LDO2_PDGRP [1]	LDO2_PDGRP [0]	LDO2HW_EN	VSELECT_EN	RESERVED	LDO2_RUN_EN	LDO2_STBY_
MUX Control				W	0x0		LDO2_SEQ [7]	LDO2_SEQ [6]	LDO2_SEQ [5]	LDO2_SEQ [4]	LDO2_SEQ [3]	LDO2_SEQ [2]	LDO2_SEQ [1]	LDO2_SEQ (
W1 Control	LDO2_PWRUP	0x8D	\odot	R	0-0	0	1002 SE0 171	1002 550 (6)	1002 550 (5)	1002 550 (4)	1002 550 (31	1002 550 (2)	1002 550 (1)	1002 5501
W2 Control				-	0.00		month (1)	constructed	10002004(0)			coordina (e)	marial	
N3 Control		OVSE		W	0x0	0	RESERVED	RESERVED	RESERVED	RESERVED	VLDO2_RUN [3]	VLDO2_RUN [2]	VLDO2_RUN [1]	VLDO2_RUN
W5 Control	- coordination	0.05	•	R	0x0		RESERVED	RESERVED	RESERVED	RESERVED	VLDO2_RUN [3]	VLDO2_RUN [2]	VLDO2_RUN [1]	VLDO2_RUN
W6 Control				w	0.0		RESERVED				VLDO2 STRY [3]	VLDO2 STRY (2)	VLDO2 STRY [1]	VLDO2 STRY
W7 Control	LDO2_STBY_VOLT	0x8F	\bigcirc	-		0								
DO1 Control				к	UxU	IJ	RESERVED				VLDO2_S18Y [3]	VLDO2_S184 [2]	VLD02_S187 [1]	VLDU2_STBY
DO2 Control	(1)				,	· <u> </u>								
3O3 Control	ě			ž		de,					Siits			
004 Control	<i>gis</i>			5	õ	ပ္ရွိ					7/6			
SNVS Control	e de la		d	2 2	5	٩					24			
age Select				· C	Ġ	อี					ပိ			
MIRROR														
Perister Groups														
Cogister Oroups									4 1 b					

Each register group contains all registers related to a specific channel or feature. Read/ write registers provide independent lines to read and write the values on the selected registers.

Individual registers can be read by clicking the \mathbf{R} button and can be written by using the \mathbf{W} button on the corresponding register.

Multiple registers can be read, written, copied or reset using the global register controls.

Use the Copy button to copy the latest read value onto the write line.

Use the **Reset** button to undo the changes on the write line and reset to the previous value. When using the global register controls, the selected command will be performed on all registers with the checkbox selected. Only functional and OTP mirror registers are intended for user evaluation.

- Functional registers: provide access to the current configuration of the PMIC. Configuration can be changed and changes will be applied once the command is sent.
- OTP mirror registers: provide access to the default configuration to be used at PWRON event. Note that access to these registers are only meant for debug or development purposes, therefore these registers can only be read or modified when TBBEN is high. The TBBEN can be set high externally via the J21 header or by the MCU via the script editor.
- Use the bit decoder buttons to set the register bit based on its actual functional value.
- The FlexGUI provides useful interface formatting controls as defined below:
 - Hide/show panel: use this button to hide or show the Register group panel, allowing more space to display all register bits in a single line.
 - Register per page: use this selector to chose how many registers are shown at the same time. Register count apply only to registers inside the selected register group. When the GUI is set to display limited number of registers, use the page surfing option at the bottom of the register bit area to find the selected register.
 - Bit buttons per line: use this option to chose how many bits are shown in a single line.
 This option is useful to force a certain register partition on low resolutions screens.
 - Sort by address: use this option to force the register to display the address in ascending order.
 - Uniform buttons: when this option is selected, the register bits are displayed with a uniform size. Longer names may get truncated to the button size. If this option

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is not selected, the buttons will change the size to fit the name of the register bit independently.

 Show bit position: use this option to show the bit position for a specific functional bit group.

7.2.2 PMIC configuration

The PMIC configuration tab provides access to the global configuration of the PMIC.

BWRON	OTD M'se	Chal Management	
Select Value Register	Select Value Regist	Select Value Register	Select Value Register
Select Value Register PWRON M Level S N/V PWRON Fu Shutcl N/V Reset Push 4 s N/V Debounce 32 ms N/V	Select Value Regist XFAILB Enable N/V PGODD Check N/V EWARN Time IO IO N/V Default SW M APS * BGMON Bypas N/V	Select Value Register SW Freq 2.500 MHz N/V SYNCOU Disabled N/V SYNCIN Disabled N/V SYNCIN 2000 kHz-3 N/V Spread Spe Disabled N/V Spread Spe Disabled N/V Spread Spe +/- 5% N/V	Select Value Register Watchdog in RL N/V Watchdog in ST N/V Clear Window 10 N/V Watchdog Timer 1 ms * N/V Watchdog Timer 1 ms * N/V Watchdog Timer 0 * N/V Watchdog Timer 1 ms * N/V WD Max Expire 0 * N/V WD Fail Counter 0 * N/V WD Max Fail 0 * N/V
Write Read	Write Read	Write Read	Write Read
PGOOD Select Value Register PGOOD Mode GPO ▼ N/V PGOOD in R PGO ▼ N/V PGOOD in Star PGO ▼ N/V Write Read Read Read	Fault Control Select Value Register Co Fault Disa * N/V Fault C 0 * N/V Fault T 1 ms * N/V Write Read	Vin Overvoltage Lockout Select Value Register Vin OVLO En N/V Vin OVLO De 10 us + Vin OVLO M No Sh + Write Read	MCU Watchdog Clear Time Select Value Register C Watchdog D 1 ms • N/V Write Read
Low Power Mode Select V Register Con OFF Mode Set N/V Write Read	I2C Communication Select Value Register C I2C CRC E N/V I2C Secure N/V I2C Address 0x08 V Write Read	Thermal Monitor Select Value Register Thermal Monito N/V Monitoring Mode 1 ms N/V Write Read Provided in the second se	WDI Control Select Value Register Co WDI Even N/V STBY M N/V WDI M Soft VDI Po Falling Write Read
STANDBY Select Value Register Cont Pola Active Hi • N/V Write Read	Coincell Control Select Value Register C Coincell C Dis V/V Coincell Cha Dis V/V VCOIN 1.8 V V N/V Write Read		

Figure 18. PMIC configuration

The functions that can be programmed in the PMIC configuration are listed below:

- PWRON: configuration and mode of operation of the PWRON pin
- PGOOD: configuration and control of the PGOOD pin
- STANDBY: configuration of the STANDBY pin
- WDI control: configuration of WDI pin and PMIC reaction when WDI pin toggles
- Coin cell control: configuration of coin cell voltage level and the coin cell charger
- Low power mode: configures the selection of the LP_OFF or QPU_OFF state when device is Off
- Clock management: configuration of the clock frequency, spread spectrum and frequency synchronization pins
- Fault control: configuration of the fault protection mechanisms

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- VIN overvoltage lockout: configuration of the OVLO protection circuit
- Thermal monitor: configuration of the thermal monitor
- · Watchdog: configuration and control of the internal Watchdog counter
- MCU watchdog management: provides parameters to allow the MCU to clear the internal PMIC watchdog
- I²C communication: sets the I²C address and enables the CRC check during I²C communication (available in OTP only)
- OTP miscellaneous: sets default OTP configuration for various PMIC features.

See PF8121 data sheet for detail description on the PMIC configuration.

7.2.3 Fault monitoring

The fault monitoring tab provide access to the fault monitoring circuits available on the PF8121 devices.

	ltage Monitori	ing	FSOB Control Hardfaults
VMON EN	UV TH	OV TH	Select Read / Clear Read / Sense Clear
SW1	95% 👻	105% -	Soft Fault PU Fail
SW2	95% 👻	105% 👻	WDI Event WD Fail
SW3	95% 👻	105% -	WD Counter Event REG Fail
W4	95% 👻	105% 👻	
SW5	95% 👻	105% 💌	
SW6	95% 👻	105% 👻	
SW7	95% 👻	105% 👻	
.DO1	95% 👻	105% 👻	
DO2	95% 👻	105% 👻	
LDO3	95% 👻	105% 👻	
LDO4	95% 👻	105% 👻	
UV Debounce	5 us	•	
OV Debounce	30 us	-	

Voltage monitoring: the user can perform the following actions using this control:

- Enable or disable the voltage monitor
- Select the OV and UV threshold (in OTP only)
- Select the OV and UV detection debounce
- Monitor/clear the ABIST flags in case of failure

FSOB control: use this control to select the FSOB mode and select/monitor the FSOB reaction on any of the following faults:

- · Soft fault
- WDI event

- WD counter event
- Hard fault

Hard faults: use this control to monitor the source for the hard fault causing a power down event.

- Power up fail
- Watchdog fail
- Regulator fail
- Thermal shutdown

7.2.4 LDO regulators

The LDO tab is used to configure and control the LDO regulators.

	LDO 2										
	Run Mode			St	andby Mo	de					
	Select Value	Register Co			Select Va	lue	Register Con				
Vout Run M	1.5 V 🔹	N/V		Vout Standby Mo	1.5 V	-	N/V				
LDO in Run		N/V		LDO in Standby			N/V				
	Common			On F	ault Behav	/iour					
	Select Value	Register Co			Select V	alue	Register Co				
Vselect Enable		N/V		Regulator after Fault	Rem	*	N/V				
LDO2 HW E		N/V		LDO on ILIM Fault	Disa	-	N/V				
LDO2 Mode	Nor 🔻	N/V		LDO on OV Fault	Disa	-	N/V				
PG Enable		IN/V		LDO on UV Fault	Disa		N/V				
				WD Bypass Enable			N/V				
				ILIM Event Bypass Enable			N/V				
				OV Event Bypass E			N/V				
				UV Event Bypass E			N/V				
		Writ	te	Read							

Figure 20. LDO control

Each LDO can change the following features:

- The output voltage in Run and Standby state
- LDO status in Run and Standby state
- LDO operating mode (OTP only)
- Set the reaction of the LDO output on an OV, UV or ILIM event
- Bypass OV, UV or ILIM events
- · Bypass reaction during a soft watchdog event
- · Enable the LDO to assert he PGOOD pin on an OV or UV fault

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• Enable or disable the voltage monitor

In addition, the LDO2 can set the output to be enabled and modified via the LDO2EN and the VSELECT pin.

VSNS can be disabled or changed to a different voltage during the system-on states.

	VSNVS	
	Select Value	Register Content
Vout Run Mode	OFF -	N/V
N	Write Read	
gure 21. VSNVS control		

7.2.5 Switching regulators

The SW regulator tab provides access to all features for each one of the switching regulators.

SW1 to SW6 are valley current mode controlled buck regulators configurable as single, dual, triple and quad phase regulators as described in the PF8121 data sheet.

All regulators capable of multiphase operation share the same feature set as shown in the following figure.

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			s٧	V7					
	Run Mode			Sta	ndby Mode				
	Select Value	Register Co			Select Value	Register Co			
Vout	1.00 V 🔹	N/V		SW in Standby	OFF 🔹	N/V			
SW in Normal	OFF -	N/V							
	<i>c</i>				r				
Common				Un	Fault Event	Pagistar Co			
Phase Current Limit pe	45° ▼ 2.1 A ▼	N/V N/V		Regulator after Fault SW on ILIM Fault SW on OV Fault SW on UV Fault ILIM Event Bypass Enable OV Event Bypass E UV Event Bypass E	Re ▼ Dis ▼ Dis ▼ Dis ▼	N/V N/V N/V N/V N/V N/V			
Figure 22 Type	Write Read								

SW7 is a peak current mode controlled buck regulator operating in single phase only which provides higher output voltage settings typically used for 3.3 V I/O supply.

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			sv	V7				
	Run Mode			Standby Mode				
	Select Value	Register Co			Select Value	Register Co		
Vout	1.00 V 👻	N/V		SW in Standby	OFF 👻	N/V		
SW in Normal	OFF 👻	N/V						
	Common			Or	ı Fault Event			
	Select Value	Register Co			Select Value	Register Co		
Phase	45° 👻	N/V		Regulator after Fault	Re 💌	N/V		
Current Limit pe	2.1 A 🔹	N/V		SW on ILIM Fault	Dis 👻	N/V		
				SW on OV Fault	Dis 💌	N/V		
				SW on UV Fault	Dis 💌	N/V		
				ILIM Event Bypass Enable		N/V		
				OV Event Bypass E		N/V		
				UV Event Bypass E		N/V		
		Write		Read				

Figure 23. Type 2 buck regulator

SW regulators can modify the following properties:

- Mode of operation in Run state
- Mode of operation in Standby state
- Output voltage in Run state
- Output voltage in Standby state
- The phase of its switching frequency
- Current limit
- DVS ramp rate
- SW6 can additionally be set in VTT mode to follow the voltage on SW5

7.2.6 Sequencer tab

The sequencer tab is used to write the power-up sequence configuration of all regulators and I/Os on the PF8121 PMIC. The sequence graph shows a graphical representation of the selected sequence.

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Register i	nap 1	PMIC	Config	Ø Fi	inctional Safety	🕛 LDO Regu	lators	SW Regulators	≣ Sequencer		AMUX Control
		POWER I	JP/DOW	/N SEQ	UENCER				Rower up de	lav: 60 up	
					Select all	Write selecter	d	SW1	Power up de	nay. oo us	
me Base:	30	*	[us]	REG:		Ŧ					
N1 SEQ:	Slot 2			REG:		~		5W2 [OFF]			
2 SEQ:	OFF	-		REG:		Ŧ					
/3 SEQ:	OFF	-		REG:		~					
V4 SEQ:	OFF	-		REG:		~					
N5 SEQ:	OFF	-		REG:		~		3004 [OFF]			
V6 SEQ:	OFF	-		REG:		Ŧ					
7 SEQ:	OFF	-		REG:		$\overline{\mathbf{v}}$		300 [011]			
D1 SEQ:	OFF	-		REG:		~		SW6 [OFF]			
2 SEQ;	OFF	-		REG:		$\overline{\nabla}$					
3 SEQ;	OFF	*		REG:		$\overline{\nabla}$		SW7 [OFF]			
O4 SEQ:	OFF	*		REG:		Ŧ					
DOD SEQ:	OFF	*		REG:		p 👻		LDO1 [OFF]			
SETB SEQ:	OFF	*		REG:		WRUP 👻					
wer down n	node:	sequent	.	REG:		Ŧ		LDO2 [OFF]			
								LDO3 [OFF]			

Figure 24. Power up/down sequencer

In Normal mode, writing to the SEQ bits modifies the functional registers to allow a custom power down sequencing when the device is configured to power down in Sequential mode. In TBB mode, writing to the SEQ bits modifies the OTP mirror register to allows a custom power up sequence when OTP/TBB operation is enabled (VDDOTP = GND).

Selecting the power down mode as *Group*, sets the PMIC to power down by groups, allowing the user to temporarily assign each regulator to one of the four power down groups, as well as configuring the group delays used during the power down event. In TBB mode, the FlexGUI grants access to the OTP mirror registers in order to configure the default value of the Group power down registers, however the user can change the power down mode later during the Normal mode if desired.

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Figure 25. Group power down controls

7.2.7 Interrupt tab

The interrupt tab provides access to all the interrupts, mask and status registers in the PF8121.

One system interrupt register is provided to work as first level detection of a physical interrupt. The system interrupt flags will be asserted only when one or more unmasked interrupts are detected in any of the second level interrupts registers and driving the INTB pin low. Interrupt events that are masked will not be notified in the system interrupt register.

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		SYS INT	
	Status	Clear	
STATUS1			
STATUS2			
MODE			
ILIM			
UV			
ov			
PWRON			
EWARN			
	Write	Read Poll	
ystem interrup	ts		

At a second level, the specific interrupt flags are organized in ten registers allowing the system to identify the source of an interrupt in a maximum of three I^2C transactions.

Each interrupt event provides 3 bits to allow a flexible interrupt management scheme:

- Status bits: a red box indicates that an event on the corresponding function has occurred. Setting the clear box and writing to the registers will write a 1 to the corresponding latch, causing the interrupt latch to be cleared.
- Mask bits: checking the mask bit prevents the INTB pin to be asserted when the respective event is present.
- Sense bits: when the sense bit is green, the corresponding sense signal is low and when it is red, the corresponding sense signal is high.

Four global interrupt registers are provided to notify global system events such as thermal interrupts, I/O events, global fault events, switching regulator mode transitions, etc.

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Status Clear Mask Sense	Status Clear Mask Sense
VIN_OVLO	
	THERM_80 N/V
FSOB N/V	THERM_95 N/V
XINTB N/V	THERM_110 N/V
PWRDN N/V	THERM_125 N/V
PWRUP N/V	THERM_140 N/V
CRC N/V	THERM_155 N/V
FREQ_RDY N/V	FSYNC_FLT N/V
SDWN N/V	WDI N/V
Write Read Poll	Write Read Poll
PWRON	SW mode
Status Clear Mask Sense	Status Clear Mask
PWRON_PUSH N/V	SW1_MODE N/V
PWRON_REL N/V	SW2_MODE N/V
PWRON_1S	SW3_MODE N/V
PWRON_2S	SW4_MODE N/V
PWRON_3S	SW5_MODE N/V
PWRON_4S	SW6_MODE N/V
PWRON_8S	SW7_MODE N/V
BG_MON N/V	Write Read Poll

Figure 27. Global interrupts

Three interrupt registers are provided to notify specific OV, UV, and ILIM faults in the switching regulators.

SW UV					SW OV						SW I limit						
	Status	Clear		Mask	Sense		Status	Clear		Mask	Sense		Status	Clear		Mask	Sense
SW1_UV				N/V		SW1_OV				N/V		SW1_ILIM				N/V	
SW2_UV				N/V		SW2_OV				N/V		SW2_ILIM				N/V	
SW3_UV				N/V		SW3_OV				N/V		SW3_ILIM				N/V	
SW4_UV				N/V		SW4_OV				N/V		SW4_ILIM				N/V	
SW5_UV				N/V		SW5_OV				N/V		SW5_ILIM				N/V	
SW6_UV				N/V		SW6_OV				N/V		SW6_ILIM				N/V	
SW7_UV				N/V		SW7_OV				N/V		SW7_ILIM				N/V	
Write Read Poll				Write Read Poll				Write Read Poll									



Three interrupt registers are provided to notify specific OV, UV, and ILIM faults in the LDO regulators.

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	LDO UV				LDO OV					LDO I limit							
	Status	Clear		Mask	Sense		Status	Clear		Mask	Sense		Status	Clear		Mask	Sense
LDO1_UV				N/V		LDO1_OV				N/V		LDO1_ILIM				N/V	
LDO2_UV				N/V		LDO2_OV				N/V		LDO2_ILIM				N/V	
LDO3_UV				N/V		LDO3_OV				N/V		LDO3_ILIM				N/V	
LDO4_UV				N/V		LDO4_OV				N/V		LDO4_ILIM				N/V	
	Write Read Poll					Wri	te R	ead	Poll			Wri	teR	lead	Poll		



See PF8121 data sheet for more details on the specific conditions that may cause any of the interrupt events.

7.2.8 AMUX control

The AMUX control tab provides the ability to automate the AMUX channel selection to display the reading of the selected channels through a polling cycle.

There are two measurement areas, one for voltage measurement and another for temperature measurement. The FlexGUI automatically displays the calculated value to show the real value after applying conversion and scaling factors to eliminate the need for manual calculation using the raw voltage at the AMUX pin.



1. AMUX channel selection:

- Use this drop-down list to select the channel to be added to the AMUX polling cycle.
- Use the + and buttons to add or remove signal from the polling list.
- Use the Clear All button to remove all signals from the polling list.
- 2. Start polling:
 - Use the Poll button to start the polling cycle to read the AMUX channels selected in the polling list.

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3. Display scaling:

- Use the scaling controls to change the display scale for the AMUX measurements.
- 4. Polling list:
 - The selected channels added to this list will be added to the polling cycle in order to provide real time data for all the channels in the list.

7.3 Working with the Script editor

The script editor is a tool that enables sequential execution of commands, which can access registers, digital and analog pins of a device. The graphical interface facilitates creation and working with commands.

7.3.1 Script editor environment

The graphical interface resides in the Script editor tab, see <u>Figure 31</u>. It consists of three main parts: command generation, script area and script log.

The command generation pane assists the user in the creation of script commands. The script area contains a list of commands to be executed, one command per line. The user can write commands manually or use the command generation pane. Format of commands is described in <u>Section 7.3.2 "Definition of commands"</u>. Lastly, the script log shows the results of the script processing. A line in this pane corresponds to the same line in the script control panel.

PFBxxx Scri	ipt editor			
Device:	PFBxx -	Commands:		Results:
Alias:	No values 💌			
 Digital pins 			Ш	
Analog pins			Ш	
 Registers 			Ш	
Mode			Ш	
▶ Generator			Ш	
Co ge	ommand eneration	Script Area		Script Log
	¢		SÒ	
Figure 3	31. Script edito	or environment		

Following steps describe how to create and execute a simple script:

- 1. The FlexGUI must be connected to the device.
- 2. In the command help pane, choose the device for which the script is to be generated. The FlexGUI loads the appropriate values to generate the script commands (i.e. register names, pin names).
- 3. Create commands to be executed. The user can write the command manually or utilize the command generation pane which offers valid options.

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- To automatically generate a command, select the command attributes and the tool inserts a new line into the script control pane. The write register command requires the register value in hexadecimal value (0x prefix, e.g. 0x12).
- I/O control commands can be used to set pin high or low to generate specific events.
- 4. Execute commands using the Run button. To process the script in a loop, set Run in loop option in the script control pane and then run the script. In this case, the script is processed until the user clicks Stop.
- 5. The script log provides a summary of all the command executed in the script. Note that results are cleared when another processing begins.

The user can save or load scripts in .txt format. The execution result can also be saved or loaded from a file.

The Export button can be used to export all the SET commands in a simple hex format:

<register address>, <register value to be written>,

Use the script generation option to create the following commands:

- Read the status of a digital pin
- Set a digital pin high or low
- · Select the analog channel to read at the AMUX
- Write a register
- · Read a register
- · Change the operating mode
- · Generate a TBB or OTP script with the data configured in the device control tabs

When working with a pre-generated script in which the device name may not match the script command ID, use the **Device alias** list to allow the FlexGUI to read commands with a different command ID (see Figure 32).

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	Device:	PF8x0	0	•	
	Device alias:	PF810	00	•	
	Digital pins				
	Pin name:	Sel	ect item	-	
	Pin value:	Sel		*	
	Analog pins				
	Pin name:		Select item	•	
	▼ Registers				
	Operation:		Write reg.	-	
	Reg. set:		functional	-	
	Reg. name/address	S:	INT_MASK1	-	
	Reg. value:		0xFF		
	▼ Mode				
	Mode:	:	Select item 🔹	•	
	 Generator 				
	Script:	Se	elect item 🔹		
Figure 32. Script g	eneration				

7.3.2 Definition of commands

This section describes commands supported by the script editor and their format. All commands are listed in <u>Table 8</u>.

Table 8. Script editor commands

Command name	Description
SET_REG	Sets value of a selected register
READ_REG	Reads value of a selected register
SET_DPIN	Sets value of a selected digital pin
GET_DPIN	Gets value of a selected digital pin
GET_APIN	Gets value of a selected analog pin. Returned value is in mV.

Command name	Description
PAUSE	Shows a dialog with a user defined message. The script execution is paused until the user confirms the dialog.
SET_MODE	Sets the mode of operation

7.3.3 Format of commands

General format of script editor command is as follows:

<command name>:<list of parameters separated by a colon>

Table 9 shows parameters of script editor commands. All parameters are mandatory.

Command name	1. item	2. item	3. item	4. item
SET_REG	Device	Reg. set	Reg. name	Reg. value
GET_REG	Device	Reg. set	Reg. name	
SET_DPIN	Device	Pin name	Pin value	
GET_DPIN	Device	Pin name		
GET_APIN	Device	Pin name		
SET_MODE	Device	Mode of operation		
PAUSE	Message			

Table 9.	Paramete	rs	of script editor of	commands
Common	d nomo	4	itom	2 itom

Device	Device name/ command ID
Reg. set	Register set name. Register set enables association of registers having similar function.
Reg. name	Register name as defined in a data sheet
Reg. address	Register address in the decimal or hexadecimal (with 0x prefix) format
Reg. value	Register value in the decimal or hexadecimal (with 0x prefix) format
Pin name	Name of a digital or analog pin as defined in a device data sheet
Pin value	Value of digital pin. Allowed strings are low and high.
Mode of operation	TBB mode, Normal mode, User mode
Message	A message to be displayed in a dialog. It cannot contain the colon character, which is used as a delimiter of parameters.

8 References

[1] **KITPF8121FRDMEVM** — detailed information on this board, including documentation, downloads, and software and tools

http://www.nxp.com/KITPF8121FRDMEVM

[2] **PF8121** — product information on multi-channel power management integrated circuit <u>http://www.nxp.com/PF8121</u>

9 Revision history

Revision history					
Rev	Date	Description			
v.1	20190422	Initial version			

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Date of release: 22 April 2019 Document identifier: UM11214



Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию.

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России, а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научноисследовательскими институтами России.

С нами вы становитесь еще успешнее!

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