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August 2014

FCMT199N60

N-Channel SuperFET® II MOSFET

600 V, 20.2 A, 199 m Ω

Features

- 650 V @ T_J = 150°C
- $R_{DS(on)} = 170 \text{ m}\Omega \text{ (Typ.)}$
- Ultra Low Gate Charge (Typ. Q_q = 57 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 160 pF)
- · 100% Avalanche Tested
- · RoHS Compliant

Applications

- · Server and Telecom Power Supplies
- · Solar Inverters
- Adaptors

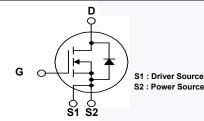
Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as server/telecom power, adaptor and solar inverter applications.

The Power88 package is an ultra-slim surface-mount package (1 mm high) with a low profile and small footprint (8x8 mm²). SuperFET II MOSFET in a Power88 package offers excellent switching performance due to lower parasitic source inductance and separated power and drive sources. Power88 offers Moisture Sensitivity Level 1 (MSL 1).







Power88

Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter		FCMT199N60	Unit
V_{DSS}	Drain to Source Voltage		-	600	V
V _{GSS} Gate to Source Voltage		-DC		±20	V
V_{GSS}	GSS Cate to Source voltage	-AC	(f > 1 Hz)	±30	v
	Drain Current	-Continuous (T _C = 25°C)		20.2	А
^I D	I _D Drain Current	-Continuous (T _C = 100°C)		12.7	7 A
I _{DM}	Drain Current	- Pulsed	(Note 1)	60.6	Α
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		400	mJ	
I _{AR}	Avalanche Current		(Note 1)	4.0	Α
E _{AR}	Repetitive Avalanche Energy		(Note 1)	2.1	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	20	V/ns
αν/αι	MOSFET dv/dt			100	V/ns
D	Dower Dissipation	(T _C = 25°C)		208	W
P_{D}	Power Dissipation	- Derate above 25°C		1.67	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C	
TL	Maximum Lead Temperature for	Soldering, 1/8" from Case for 5 S	Seconds	300	°C

Thermal Characteristics

Symbol	Parameter	FCMT199N60	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (* 1 in² pad of 2 oz copper), Max.	45	- 0/00

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCMT199N60	FCMT199N60	Power88	-	-	3000

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charae	cteristics					
D\/	Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_C = 25^{\circ}\text{C}$	600	-	-	V
DV _{DSS}		$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_C = 150^{\circ}\text{C}$	650	-	-	, v
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, Referenced to 25°C	-	0.67	-	V/°C
	Zoro Cata Valtaga Drain Current	V _{DS} = 600 V, V _{GS} = 0 V	-	-	1	
I _{DSS} Zero Gate Voltage Drain Current	$V_{DS} = 480 \text{ V}, V_{GS} = 0 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	2.2	-	μΑ	
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2.5	-	3.5	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	-	0.170	0.199	Ω
9 _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 10 A	-	20	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 000 V V 0 V	-	2043	2715	pF
C _{oss}	Output Capacitance	$V_{DS} = 380 \text{ V}, V_{GS} = 0 \text{ V}$ f = 1 MHz	-	45	60	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 101112	-\	7	-	pF
Coss eff.	Effective Output Capacitance	$V_{DS} = 0 V \text{ to } 480 V, V_{GS} = 0 V$	- \	160	-	pF
Q _{g(tot)}	Total Gate Charge at 10V	V _{DS} = 380 V, I _D = 10 A	- \	57	74	nC
Q_{gs}	Gate to Source Gate Charge	V _{GS} = 10 V	-	9	-	nC
Q _{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	21	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	1	-	Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		-	20	50	ns
t _r	Turn-On Rise Time	$V_{DD} = 380 \text{ V}, I_D = 10 \text{ A}$	- /	10	30	ns
t _{d(off)}	Turn-Off Delay Time	V_{GS} = 10 V, R_g = 4.7 Ω	-/	64	138	ns
t _f	Turn-Off Fall Time	(Note 4)	-	5	20	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Dioc	de Forward Current	-	-	20.2	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Fo	orward Current	-	-	60.6	Α
V_{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 10 A	-	-	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 10 A	-	320	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	5.1	-	μС

Notes:

- 1. Repetitive Rating: Pulse-width limited by maximum junction temperature.
- 2. I_{AS} = 4 A, R_{G} = 25 Ω , starting T_{J} = 25°C
- 3. I_{SD} \leq 10 A, di/dt \leq 200 A/ μ s, V_{DD} \leq BV_{DSS}, starting T_J = 25°C
- ${\bf 4.} \ {\bf Essentially independent \ of \ operating \ temperature \ typical \ characteristics.}$

Typical Characteristics

Figure 1. On-Region Characteristics

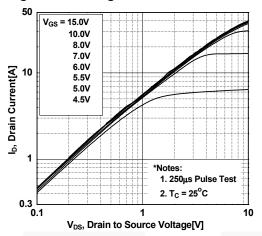


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

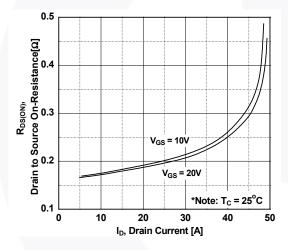


Figure 5. Capacitance Characteristics

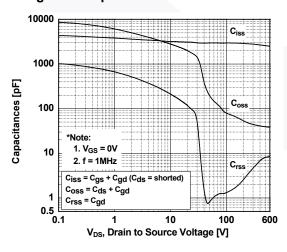


Figure 2. Transfer Characteristics

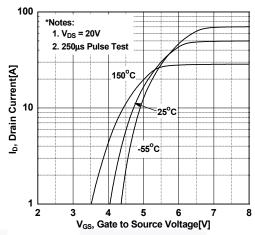


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

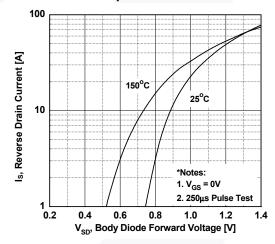
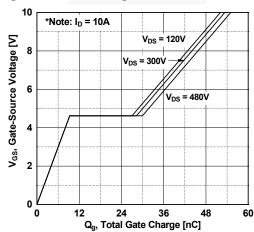


Figure 6. Gate Charge Characteristics



Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

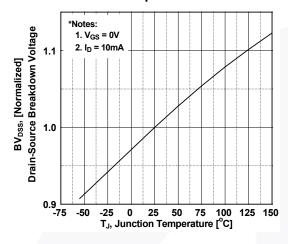


Figure 9. Maximum Safe Operating Area

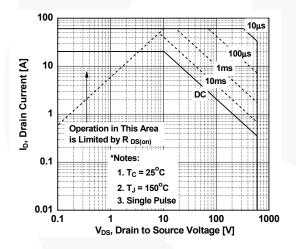


Figure 11. Eoss vs. Drain to Source Voltage Switching Capability

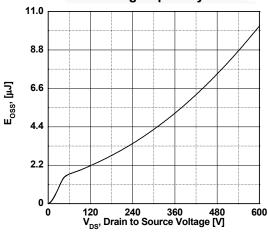


Figure 8. On-Resistance Variation vs. Temperature

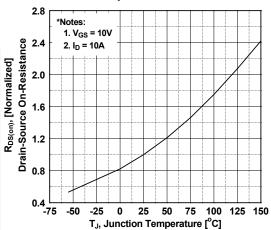
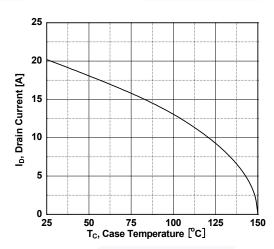
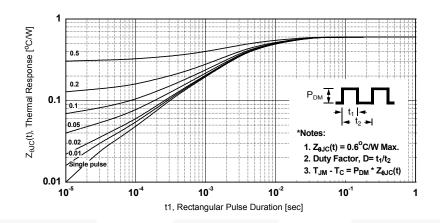


Figure 10. Maximum Drain Current vs. Case Temperature



Typical Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



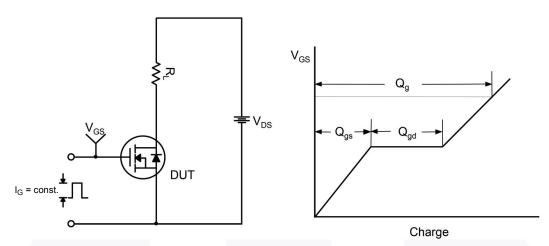


Figure 13. Gate Charge Test Circuit & Waveform

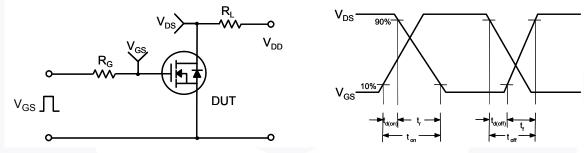


Figure 14. Resistive Switching Test Circuit & Waveforms

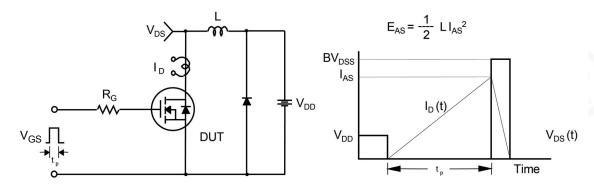
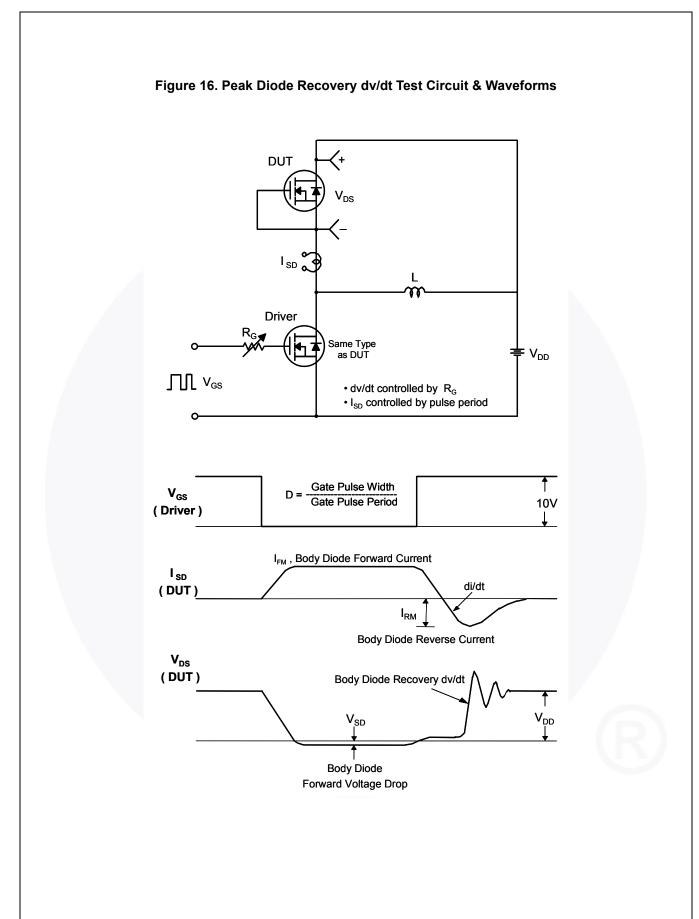


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms



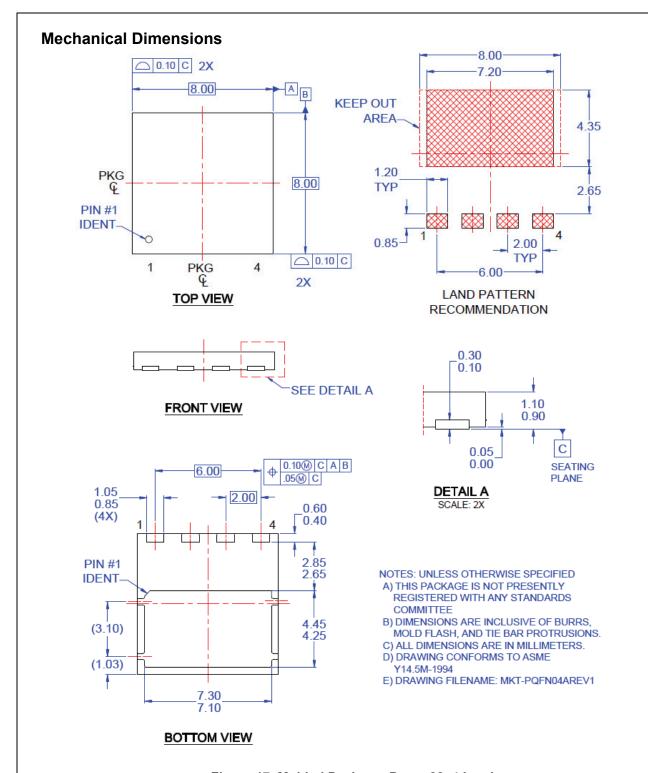


Figure 17. Molded Package, Power88, 4 Lead

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