FAIRCHILD SEMICONDUCTOR®

April 2007

74F191
Up/Down Binary Counter with Preset and Ripple Clock

Features

- High-Speed—125MHz typical count frequency
- Synchronous counting
- Asynchronous parallel load
- Cascadable

General Description

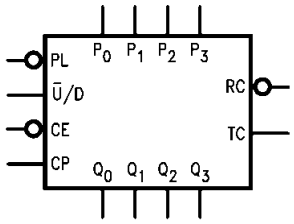
The 74F191 is a reversible modulo-16 binary counter featuring synchronous counting and asynchronous presetting. The preset feature allows the 74F191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

Ordering Information

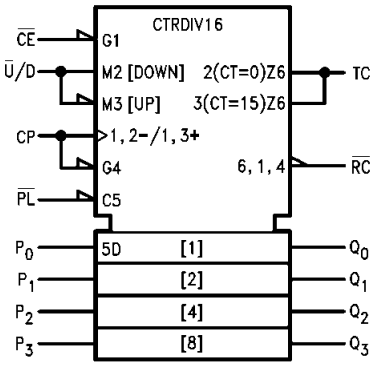
Order Number	Package Number	Package Description
74F191SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74F191SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F191PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

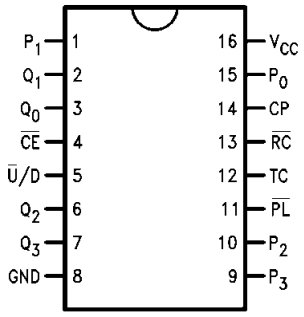
Logic Symbols



IEEE/IEC



Connection Diagram



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Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH / LOW	Input I_{IH} / I_{IL} Output I_{OH} / I_{OL}
$\overline{CE}$	Count Enable Input (Active LOW)	1.0 / 3.0	20µA / -1.8mA
CP	Clock Pulse Input (Active Rising Edge)	1.0 / 1.0	20µA / -0.6 mA
P_0–P_3	Parallel Data Inputs	1.0 / 1.0	20µA / -0.6 mA
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0 / 1.0	20µA / -0.6mA
$\overline{U}$/D	Up/Down Count Control Input	1.0 / 1.0	20µA / -0.6mA
Q_0–Q_3	Flip-Flop Outputs	50 / 33.3	-1mA / 20mA
$\overline{RC}$	Ripple Clock Output (Active LOW)	50 / 33.3	-1mA / 20mA
TC	Terminal Count Output (Active HIGH)	50 / 33.3	-1mA / 20mA

Functional Description

The 74F191 is a synchronous up/down 4-bit binary counter. It contains four edge-triggered flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Data inputs (P_0–P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}$/D input signal, as indicated in the Mode Select Table. $\overline{CE}$ and $\overline{U}$/D can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches 15 in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U}$/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, the $\overline{RC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters, as indicated in Figure 1 and Figure 2. In Figure 1, each $\overline{RC}$ output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse, as indicated in the $\overline{RC}$ Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in Figure 2. All clock inputs are driven in parallel and the $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{RC}$ output of any device goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure 3 avoids ripple delays and their associated restrictions. The $\overline{CE}$ input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figure 1 and Figure 2 doesn't apply, because the TC output of a given stage is not affected by its own $\overline{CE}$.

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Mode Select Table

Inputs				Mode
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	↗	Count Up
H	L	H	↗	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

↗ = LOW-to-HIGH Clock Transition

⊔ = LOW Pulse

$\overline{RC}$ Truth Table

Inputs			Output
$\overline{CE}$	TC(1)	CP	$\overline{RC}$
L	H	⊔	⊔
H	X	X	H
X	L	X	H

Note:

1. TC is generated internally.

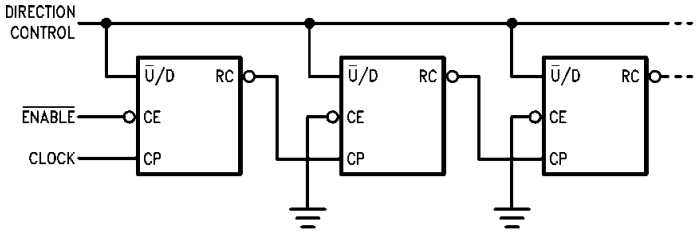


Figure 1. n-Stage Counter Using Ripple Clock

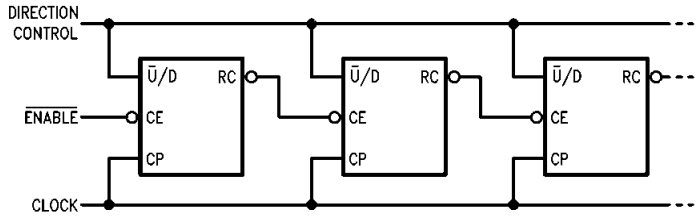


Figure 2. Synchronous n-Stage Counter Using Ripple Carry/Borrow

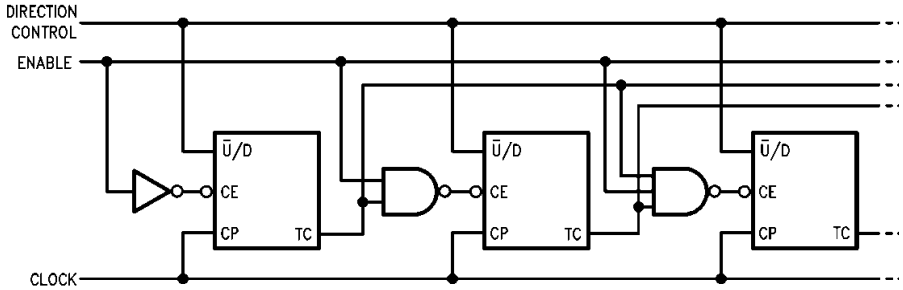
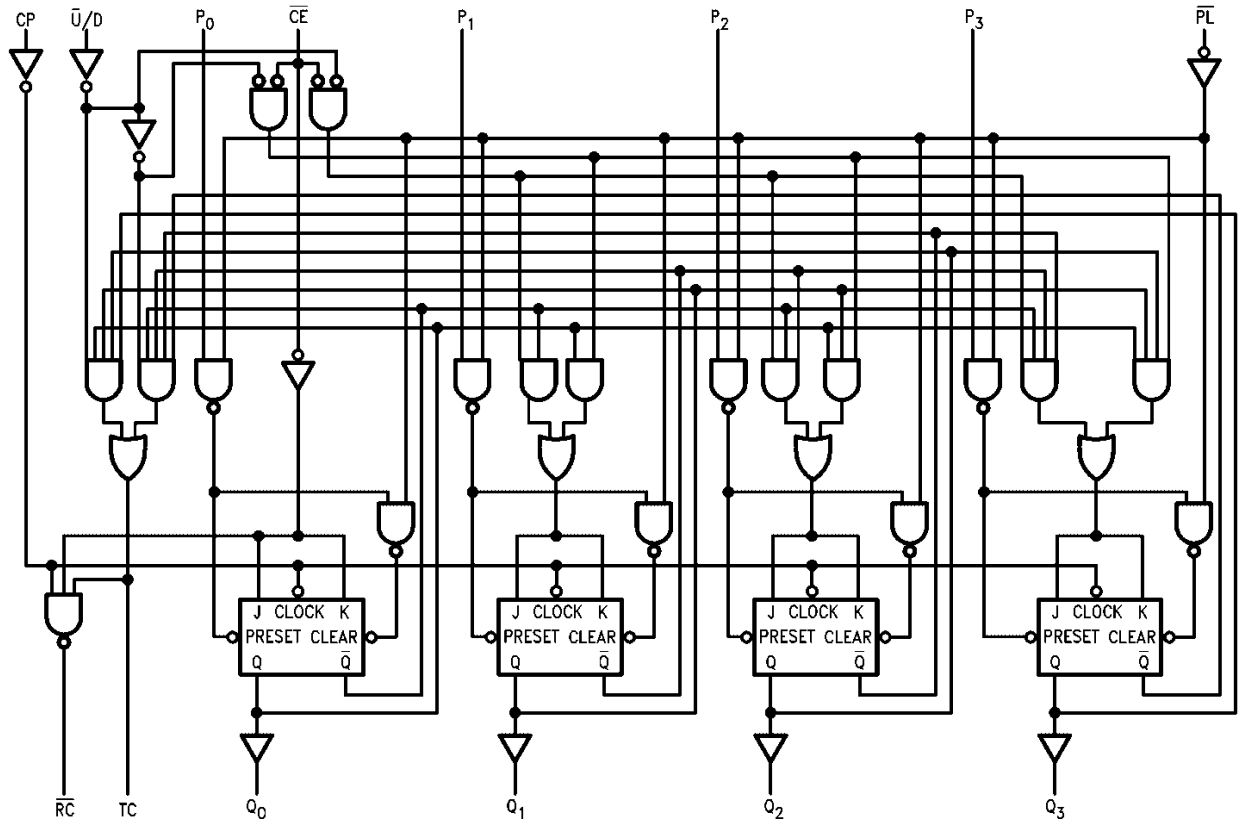


Figure 3. Synchronous n-Stage Counter with Gated Carry/Borrow

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 4.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
T_{STG}	Storage Temperature	–65°C to +150°C
T_A	Ambient Temperature Under Bias	–55°C to +125°C
T_J	Junction Temperature Under Bias	–55°C to +150°C
V_{CC}	V_{CC} Pin Potential to Ground Pin	–0.5V to +7.0V
V_{IN}	Input Voltage(2)	–0.5V to +7.0V
I_{IN}	Input Current(2)	–30mA to +5.0mA
V_O	Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
	Standard Output	–0.5V to V_{CC}
	3-STATE Output	–0.5V to +5.5V
	Current Applied to Output in LOW State (Max.)	twice the rated I_{OL} (mA)

Note:

2. Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
T_A	Free Air Ambient Temperature	0°C to +70°C
V_{CC}	Supply Voltage	+4.5V to +5.5V

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DC Electrical Characteristics

Symbol	Parameter	V_{CC}	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input HIGH Voltage		Recognized as a HIGH Signal	2.0			V
V_{IL}	Input LOW Voltage		Recognized as a LOW Signal			0.8	V
V_{CD}	Input Clamp Diode Voltage	Min.	I_{IN} = –18mA			–1.2	V
V_{OH}	Output HIGH Voltage 10% V_{CC}	Min.	I_{OH} = –1mA	2.5			V
	Output HIGH Voltage 5% V_{CC}			2.7			
V_{OL}	Output LOW Voltage 10% V_{CC}	Min.	I_{OL} = 20mA			0.5	V
I_{IH}	Input HIGH Current	Max.	V_{IN} = 2.7V			5.0	µA
I_{BVI}	Input HIGH Current Breakdown Test	Max.	V_{IN} = 7.0V			7.0	µA
I_{CEX}	Output HIGH Leakage Current	Max.	V_{OUT} = V_{CC}			50	µA
V_{ID}	Input Leakage Test	0.0	I_{ID} = 1.9µA, All Other Pins Grounded	4.75			V
I_{OD}	Output Leakage Circuit Current	0.0	V_{IOD} = 150mV, All Other Pins Grounded			3.75	µA
I_{IL}	Input LOW Current	Max.	V_{IN} = 0.5V (except $\overline{CE}$)			–0.6	mA
			V_{IN} = 0.5V ($\overline{CE}$)			–1.8	
I_{OS}	Output Short-Circuit Current	Max.	V_{OUT} = 0.0V	–60		–150	mA
I_{CC}	Power Supply Voltage	Max.			38	55	mA

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AC Electrical Characteristics

Symbol	Parameter	T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF			T_A = –55°C to +125°C, V_{CC} = +5.0V, C_L = 50pF		T_A = 0°C to 70°C, V_{CC} = +5.0V, C_L = 50pF		Units
		Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}	Maximum Count Frequency		100						MHz
t_{PLH}	Propagation Delay, CP to Q_n	3.0	5.5	7.5	3.0	9.5	3.0	8.5	ns
t_{PHL}		5.0	8.5	11.0	5.0	13.5	5.0	12.0	
t_{PLH}	Propagation Delay, CP to TC	6.0	10.0	13.0	6.0	16.5	6.0	14.0	ns
t_{PHL}		5.0	8.5	11.0	5.0	13.5	5.0	12.0	
t_{PLH}	Propagation Delay, CP to $\overline{RC}$	3.0	5.5	7.5	3.0	9.5	3.0	8.5	ns
t_{PHL}		3.0	5.0	7.0	3.0	9.0	3.0	8.0	
t_{PLH}	Propagation Delay, $\overline{CE}$ to $\overline{RC}$	3.0	5.0	7.0	3.0	9.0	3.0	8.0	ns
t_{PHL}		3.0	5.5	7.0	3.0	9.0	3.0	8.0	
t_{PLH}	Propagation Delay, $\overline{U}$/D to $\overline{RC}$	7.0	11.0	18.0	7.0	22.0	7.0	20.0	ns
t_{PHL}		5.5	9.0	12.0	5.5	14.0	5.5	13.0	
t_{PLH}	Propagation Delay, $\overline{U}$/D to TC	4.0	7.0	10.0	4.0	13.5	4.0	11.0	ns
t_{PHL}		4.0	6.5	10.0	4.0	12.5	4.0	11.0	
t_{PLH}	Propagation Delay, P_n to Q_n	3.0	4.5	7.0	3.0	9.0	3.0	8.0	ns
t_{PHL}		6.0	10.0	13.0	6.0	16.0	6.0	14.0	
t_{PLH}	Propagation Delay, $\overline{PL}$ to Q_n	5.0	8.5	11.0	5.0	13.0	5.0	12.0	ns
t_{PHL}		5.5	9.0	12.0	5.5	14.5	5.5	13.0	
t_{PLH}	Propagation Delay, P_n to TC	5.0		14.0			5.0	15.0	ns
t_{PHL}		6.5		13.0			6.0	14.0	
t_{PLH}	Propagation Delay, P_n to $\overline{RC}$	6.5		19.0			6.5	20.0	ns
t_{PHL}		6.0		14.0			6.0	15.0	
t_{PLH}	Propagation Delay, $\overline{PL}$ to TC	8.0		16.5			8.0	17.5	ns
t_{PHL}		6.0		13.5			6.0	14.5	
t_{PLH}	Propagation Delay, $\overline{PL}$ to $\overline{RC}$	10.0		20.0			10.0	21.0	ns
t_{PHL}		9.0		15.5			9.0	16.0	

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AC Operating Requirements

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$		$T_A = -55°C$ to $+125°C$, $V_{CC} = +5.0V$		$T_A = 0°C$ to $70°C$, $V_{CC} = +5.0V$		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_S(H)$	Setup Time, HIGH or LOW, P_n to $\overline{PL}$	4.5		6.0		5.0		ns
$t_S(L)$		4.5		6.0		5.0		
$t_H(H)$	Hold Time, HIGH or LOW, P_n to $\overline{PL}$	2.0		2.0		2.0		ns
$t_H(L)$		2.0		2.0		2.0		
$t_S(L)$	Setup Time LOW, $\overline{CE}$ to CP	10.0		10.5		10.0		ns
$t_H(L)$	Hold Time LOW, $\overline{CE}$ to CP	0		0		0		ns
$t_S(H)$	Setup Time, HIGH or LOW, $\overline{U}$/D to CP	12.0		12.0		12.0		ns
$t_S(L)$		12.0		12.0		12.0		
$t_H(H)$	Hold Time, HIGH or LOW, $\overline{U}$/D to CP	0		0		0		ns
$t_H(L)$		0		0		0		
$t_W(L)$	$\overline{PL}$ Pulse Width LOW	6.0		8.5		6.0		ns
$t_W(L)$	CP Pulse Width LOW	5.0		7.0		5.0		ns
t_{REC}	Recovery Time, $\overline{PL}$ to CP	6.0		7.5		6.0		ns

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Physical Dimensions

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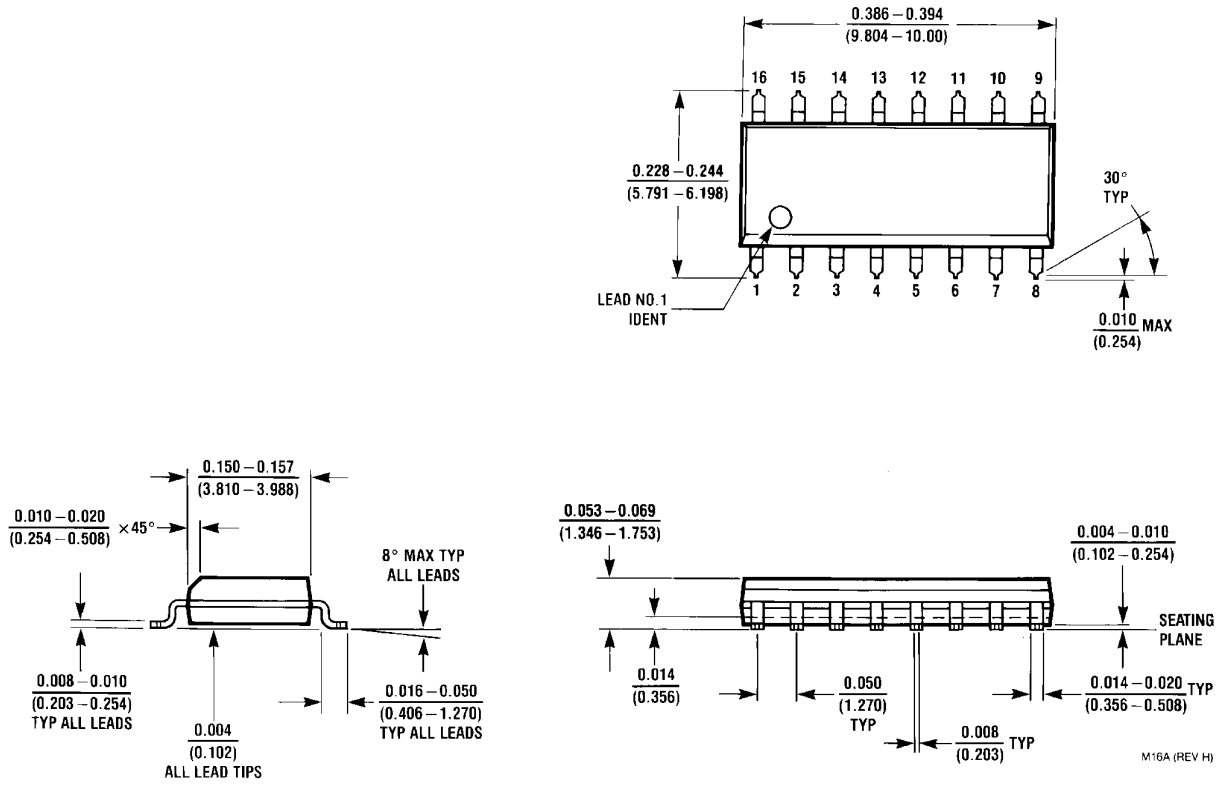
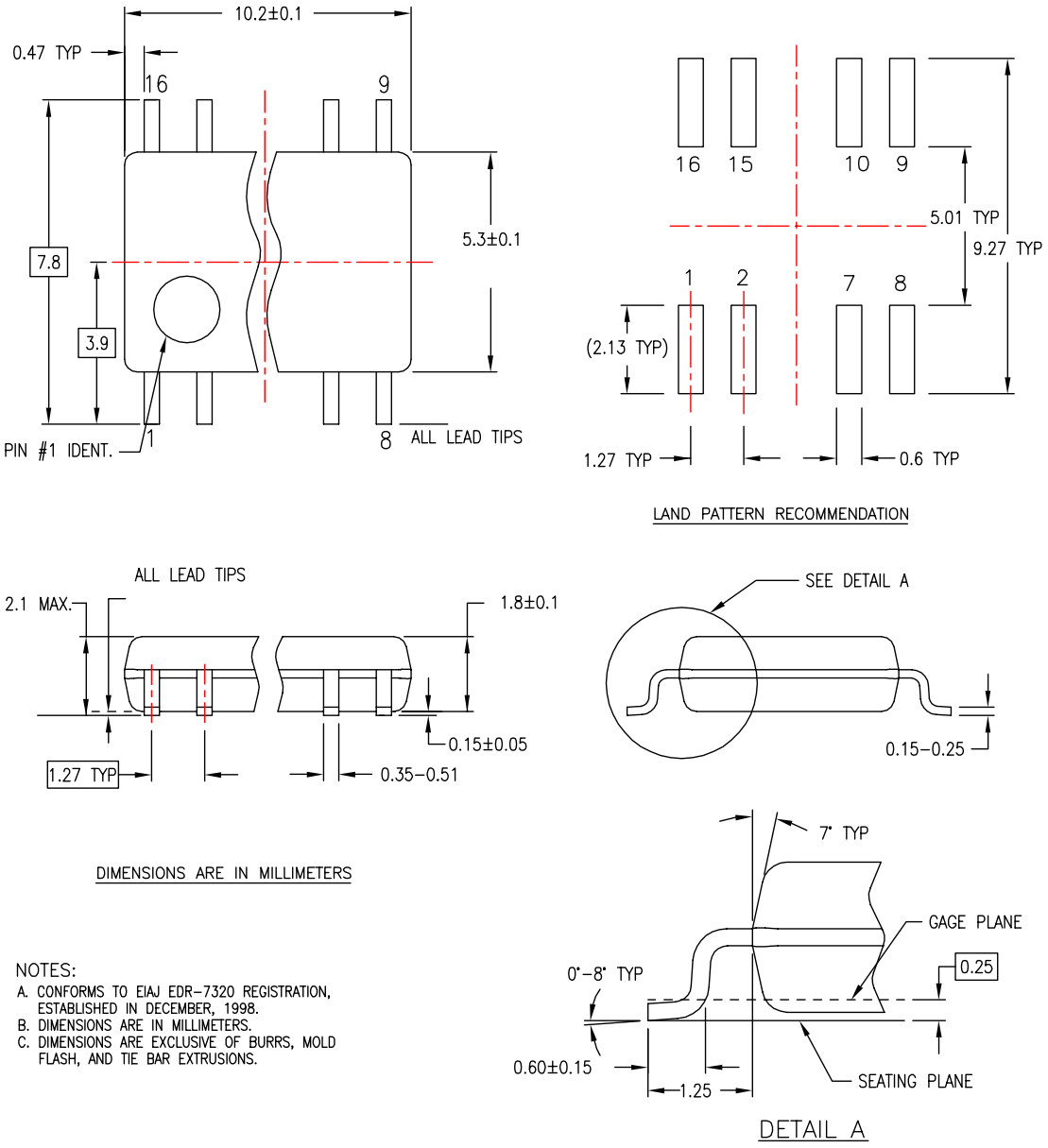


Figure 5. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO EIAJ EDR–7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DREVC

Figure 6. 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions (Continued)

Dimensions are in inches (millimeters) unless otherwise noted.

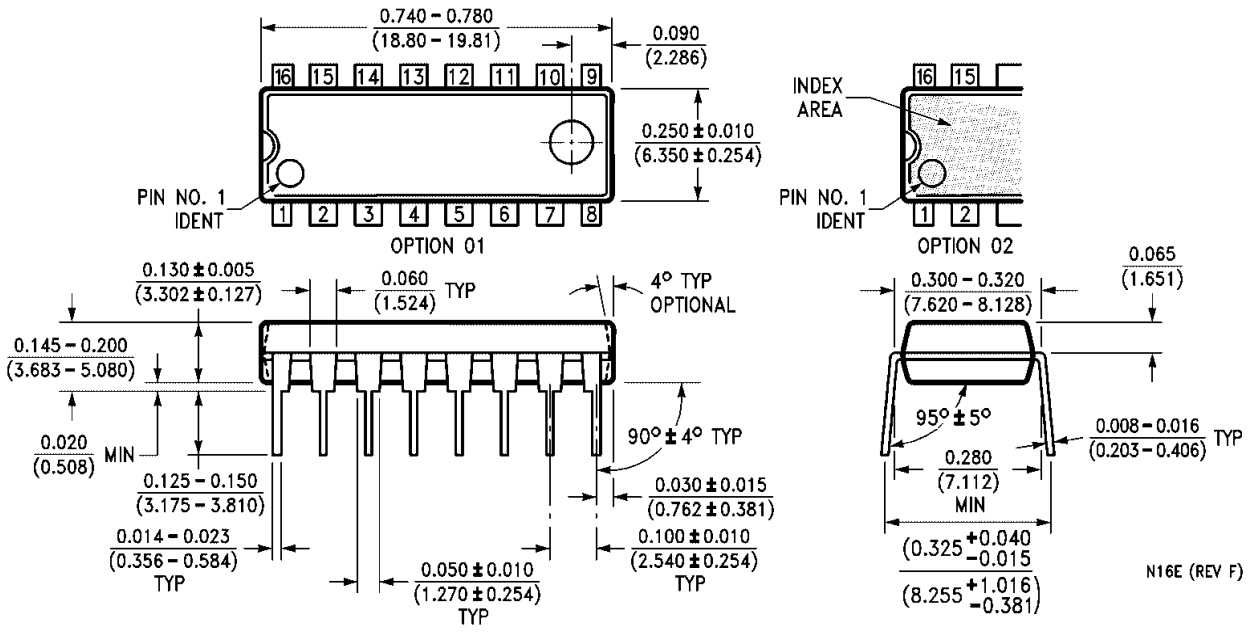


Figure 7. 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

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SuperSOT™-8
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Rev. I24

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