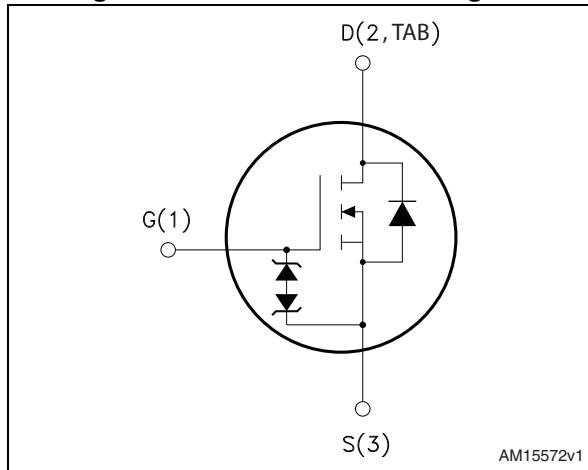


Figure 1. Internal schematic diagram



Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STP16N65M2	710 V	0.36 Ω	11 A
STU16N65M2	710 V	0.36 Ω	11 A

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using MDmesh™ M2 technology. Thanks to their strip layout and improved vertical structure, the devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STP16N65M2	16N65M2	TO-220	Tube
STU16N65M2	16N65M2	IPAK	Tube

Contents

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	11	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	6.9	A
$I_{DM}^{(1)}$	Drain current (pulsed)	44	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	110	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
T_{sig}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 11$ A, $dI/dt \leq 400$ A/ μs ; $V_{DS\ peak} < V_{(BR)DSS}$, $V_{DD}=400$ V.
3. $V_{DS} \leq 520$ V

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	IPAK	
$R_{thj-case}$	Thermal resistance junction-case max	1.14		$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-amb max ⁽¹⁾	62.50	100	$^\circ\text{C/W}$

1. When mounted on 1 inch² FR-4, 2 Oz copper board

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	1.9	A
E_{AS}	Single pulse avalanche energy (starting $T_j=25^\circ\text{C}$, $I_D=I_{AR}$; $V_{DD}=50$)	360	mJ

2 Electrical characteristics

($T_C = 25^\circ\text{C}$ unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{GS} = 0$, $I_D = 1 \text{ mA}$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0$, $V_{DS} = 650 \text{ V}$			1	μA
		$V_{GS} = 0$, $V_{DS} = 650 \text{ V}$, $T_C = 125^\circ\text{C}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0$, $V_{GS} = \pm 25 \text{ V}$			± 10	μA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	2	3	4	V
$R_{DS(\text{on})}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}$, $I_D = 5.5 \text{ A}$		0.32	0.36	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{GS} = 0$, $V_{DS} = 100 \text{ V}$, $f = 1 \text{ MHz}$	-	718	-	pF
C_{oss}	Output capacitance		-	32	-	pF
C_{rss}	Reverse transfer capacitance		-	1.1	-	pF
$C_{oss \text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0$, $V_{DS} = 0$ to 520 V	-	189	-	pF
R_G	Intrinsic gate resistance	$f = 1 \text{ MHz}$ open drain	-	5.2	-	Ω
Q_g	Total gate charge	$V_{DD} = 520 \text{ V}$, $I_D = 11 \text{ A}$, $V_{GS} = 10 \text{ V}$ (see Figure 17)	-	19.5	-	nC
Q_{gs}	Gate-source charge		-	4	-	nC
Q_{gd}	Gate-drain charge		-	8.3	-	nC

1. $C_{oss \text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325 \text{ V}$, $I_D = 5.5 \text{ A}$, $R_G = 4.7 \Omega$, $V_{GS} = 10 \text{ V}$ (see <i>Figure 16</i> and <i>21</i>)	-	11.3	-	ns
t_r	Rise time		-	8.2	-	ns
$t_{d(off)}$	Turn-off delay time		-	36	-	ns
t_f	Fall time		-	11.3	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		44	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0$, $I_{SD} = 11 \text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 11 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see <i>Figure 18</i>)	-	342		ns
Q_{rr}	Reverse recovery charge		-	3.5		μC
I_{RRM}	Reverse recovery current		-	20.4		A
t_{rr}	Reverse recovery time		-	458		ns
Q_{rr}	Reverse recovery charge	$I_{SD} = 11 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$, $T_j=150^\circ\text{C}$ (see <i>Figure 18</i>)	-	4.6		μC
I_{RRM}	Reverse recovery current		-	20.5		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

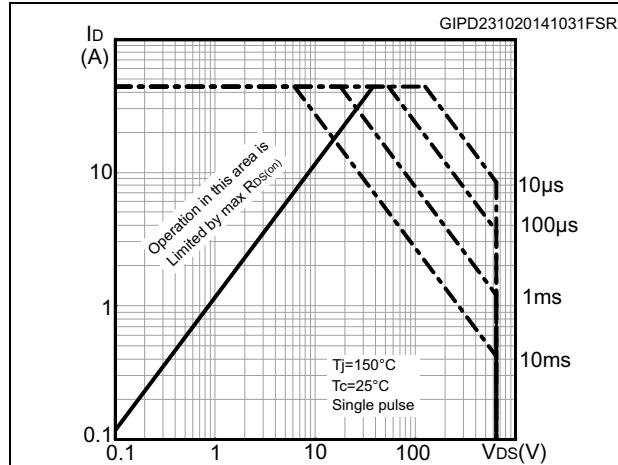


Figure 3. Thermal impedance for TO-220

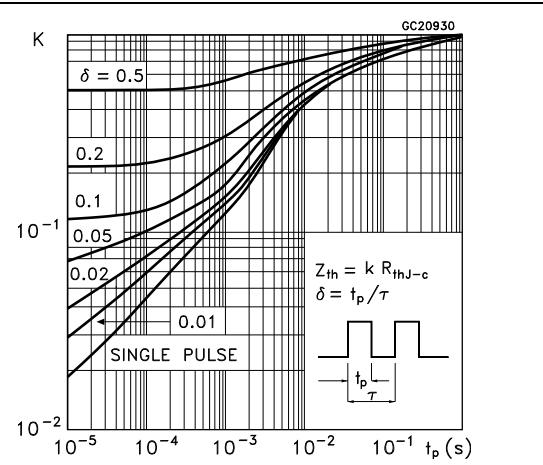


Figure 4. Safe operating area for IPA

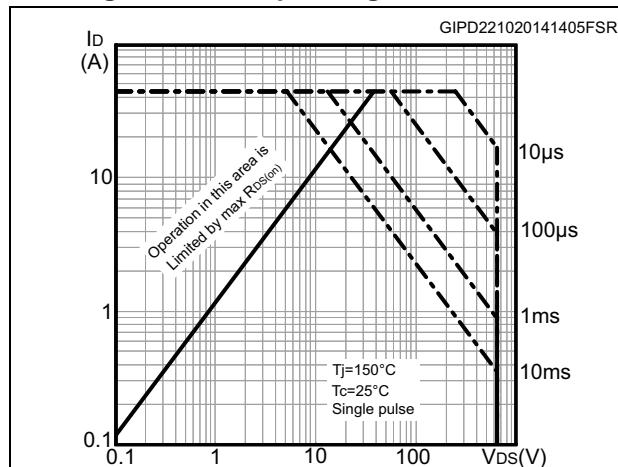


Figure 5. Thermal impedance for IPA

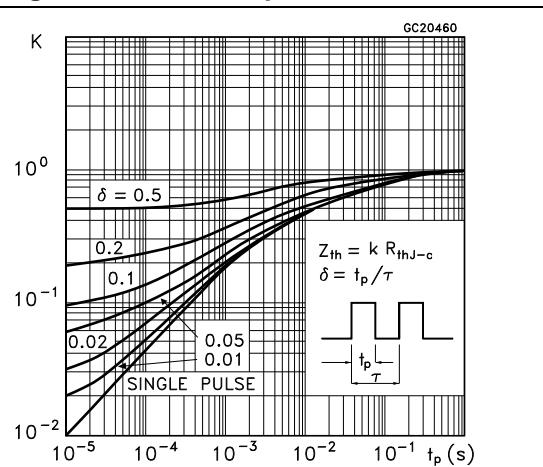


Figure 6. Output characteristics

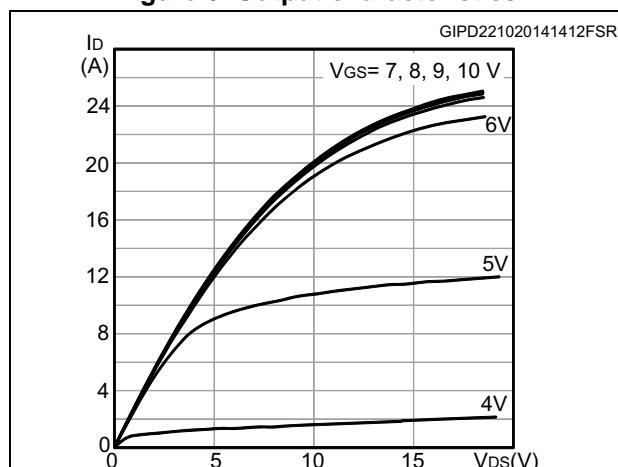


Figure 7. Transfer characteristics

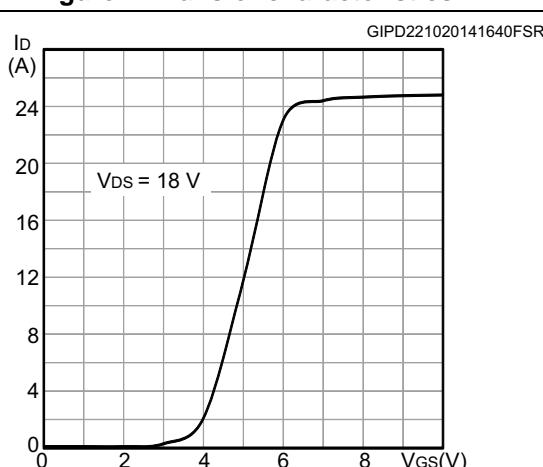


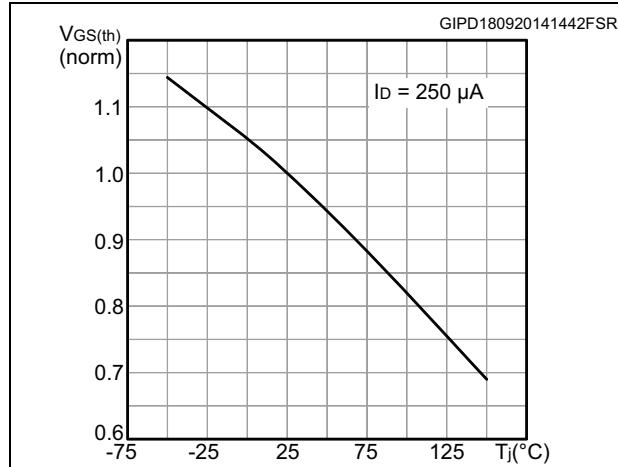
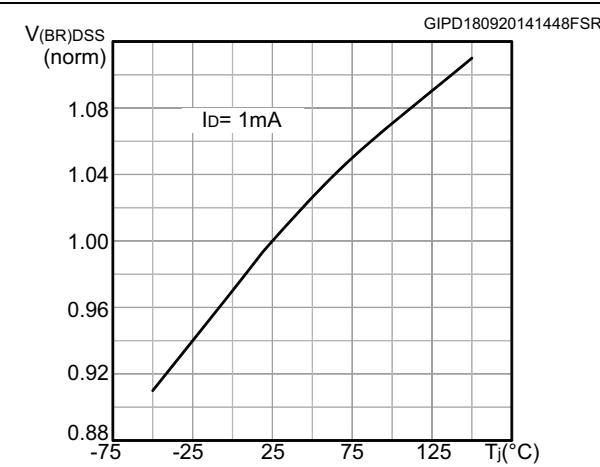
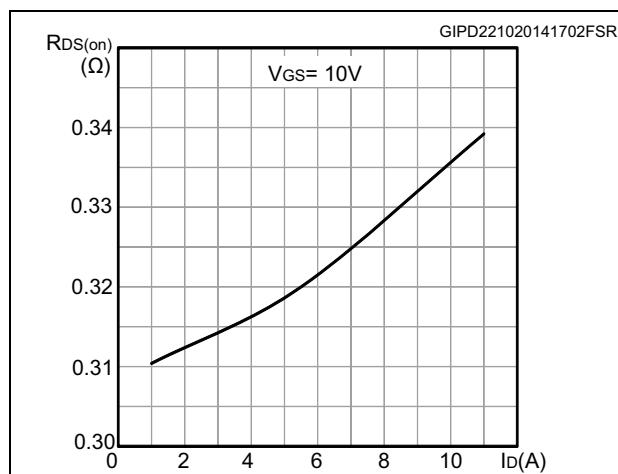
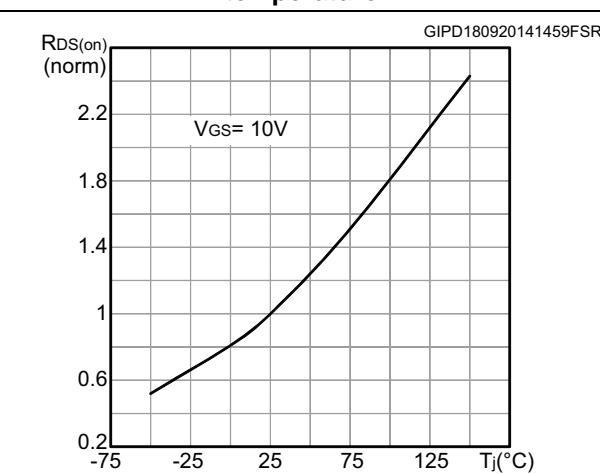
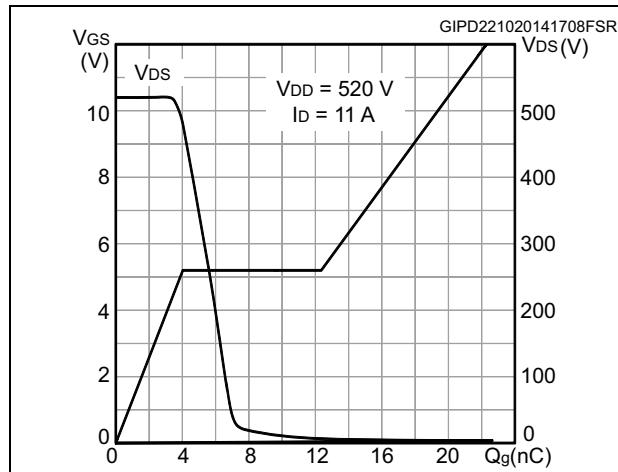
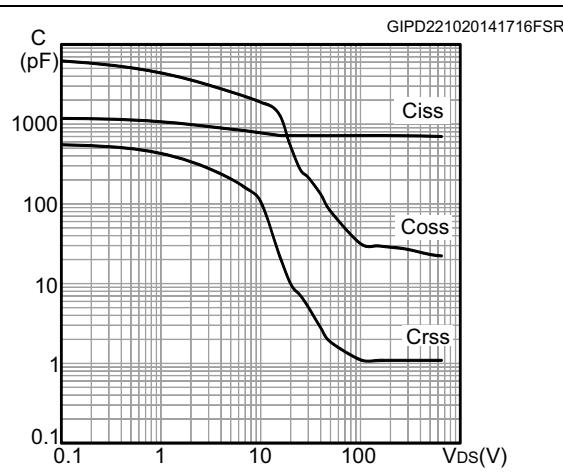
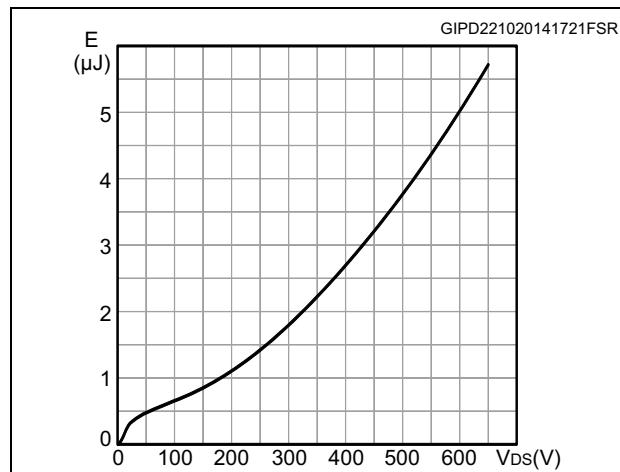
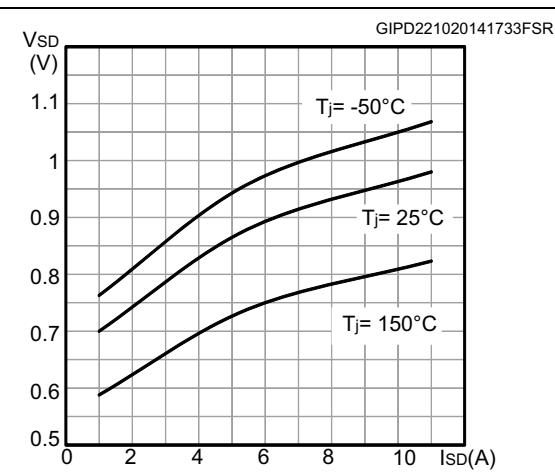
Figure 8. Normalized gate threshold voltage vs. temperature**Figure 9. Normalized $V_{(BR)DSS}$ vs. temperature****Figure 10. Static drain-source on-resistance****Figure 11. Normalized on-resistance vs. temperature****Figure 12. Gate charge vs. gate-source voltage****Figure 13. Capacitance variations**

Figure 14. Output capacitance stored energy**Figure 15. Source-drain diode forward characteristics**

3 Test circuits

Figure 16. Switching times test circuit for resistive load

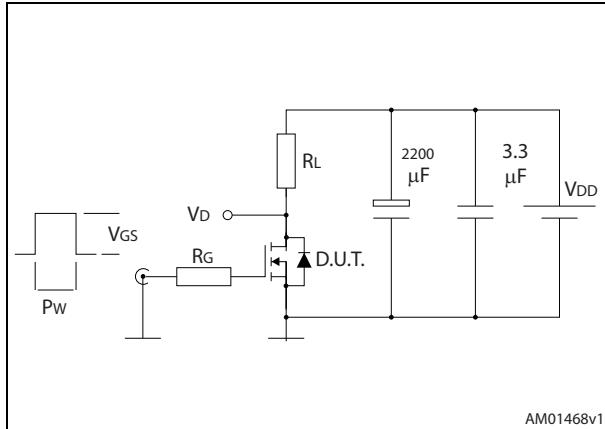


Figure 17. Gate charge test circuit

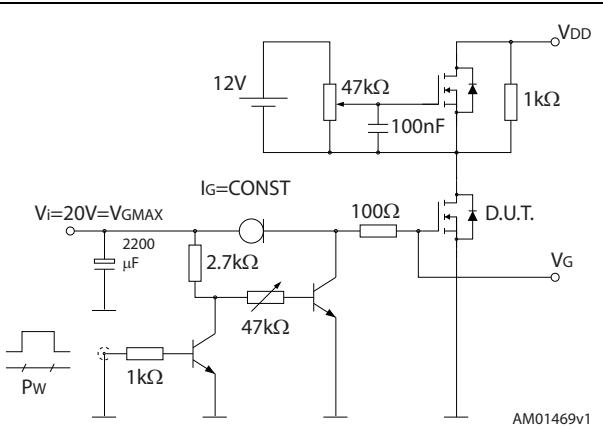


Figure 18. Test circuit for inductive load switching and diode recovery times

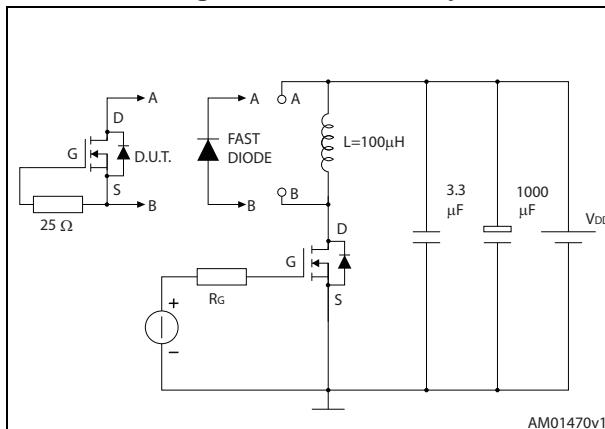


Figure 19. Unclamped inductive load test circuit

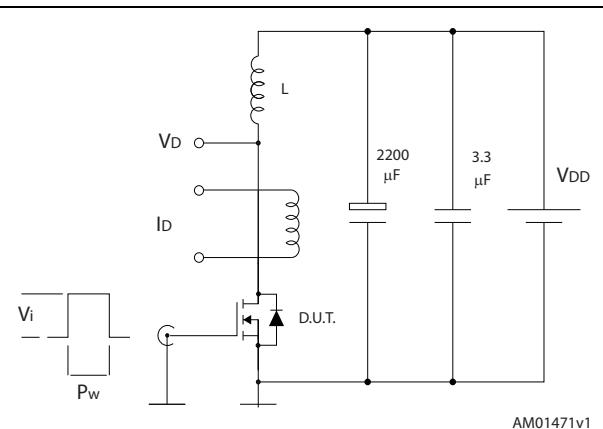


Figure 20. Unclamped inductive waveform

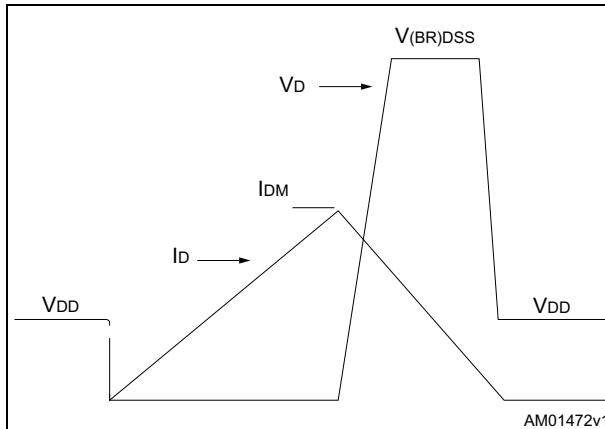
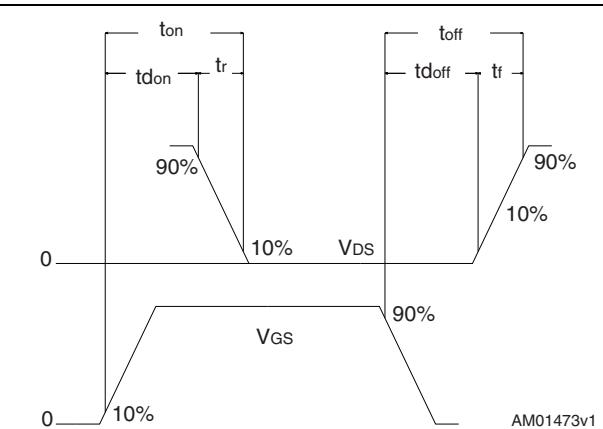


Figure 21. Switching time waveform

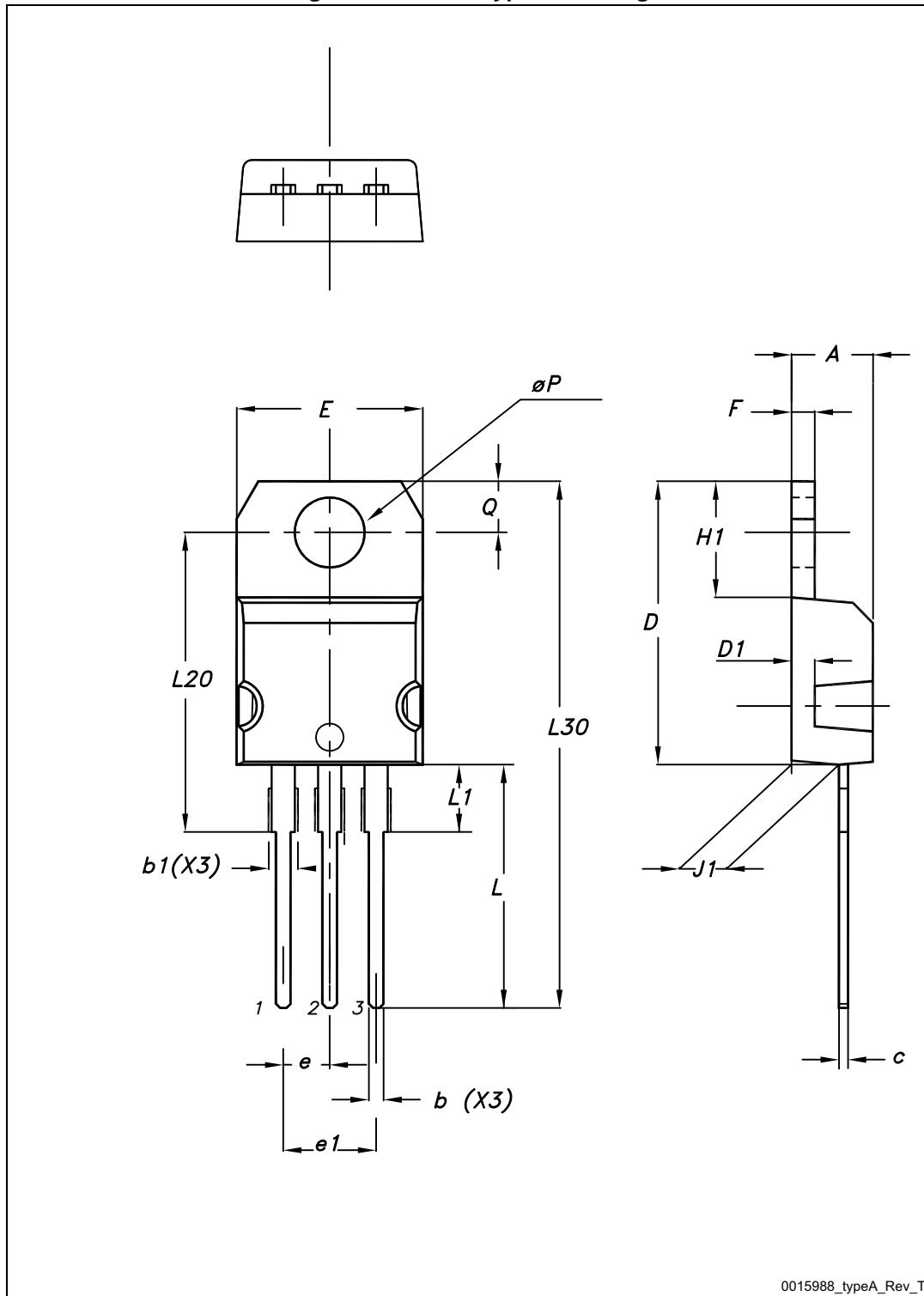


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.
ECOPACK® is an ST trademark.

4.1 TO-220, STP16N65M2

Figure 22. TO-220 type A drawing



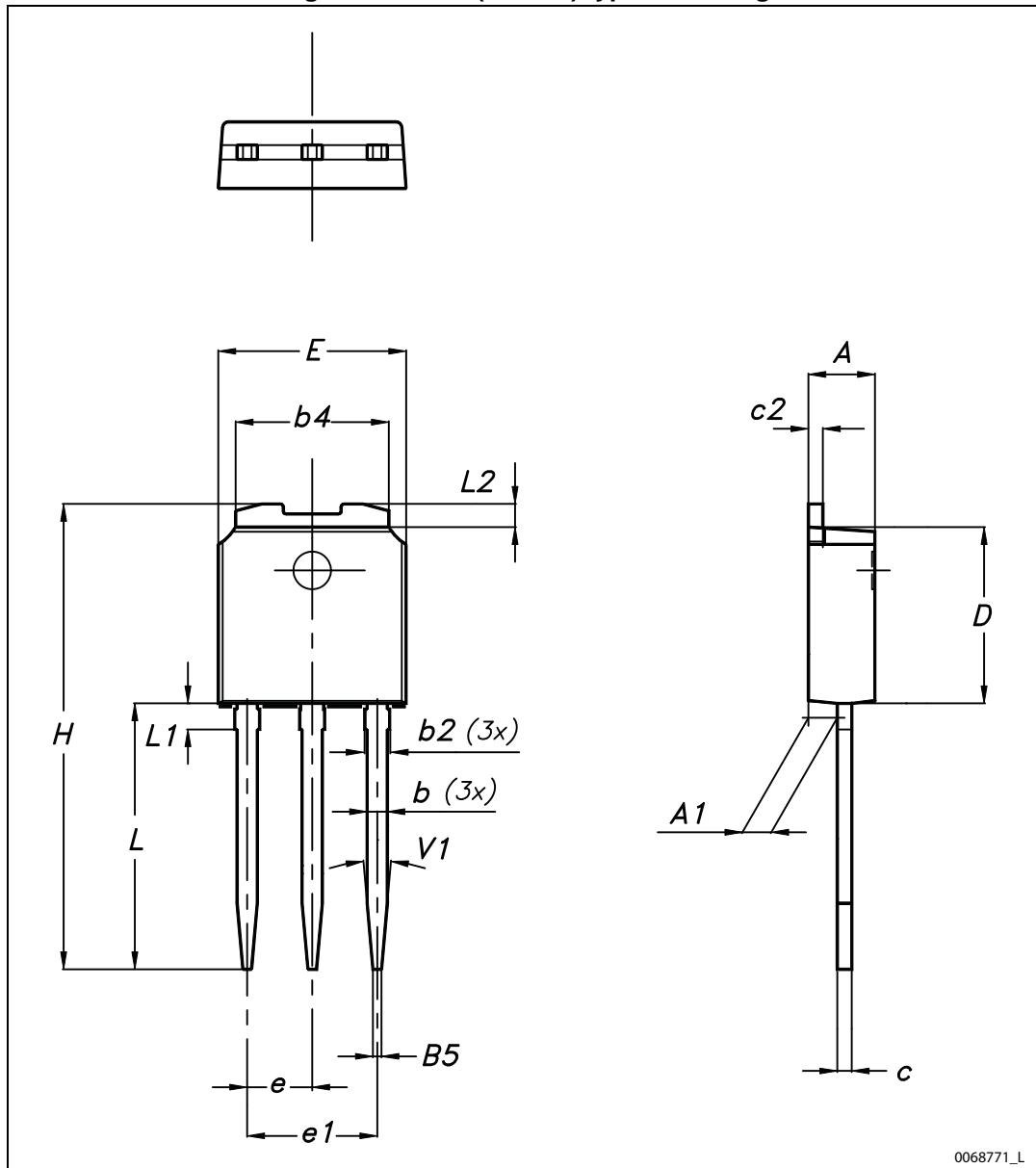
0015988_typeA_Rev_T

Table 9. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.2 IPAK, STU16N65M2

Figure 23. IPAK (TO-251) type A drawing



0068771_L

Table 10. IPAK (TO-251) type A mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

5 Revision history

Table 11. Document revision history

Date	Revision	Changes
24-Oct-2014	1	First release.

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