User Defined Fault Protection and Detection, 0.8 pC Q_{INJ}, Triple SPDT

Data Sheet **ADG5243F**

FEATURES

- **User defined supplies set overvoltage level**
  - **Overvoltage protection up to −55 V and +55 V**
  - **Power-off protection up to −55 V and +55 V**
  - **Overvoltage detection on source pins**
  - **Minimum secondary supply level: 4.5 V single-supply**
  - **Interrupt flags indicate fault status**
- **Low charge injection (Q_{INJ}): 0.8 pC**
- **Low drain/source on capacitance: 10 pF**
- **Latch-up immune under any circumstance**
- **Known state without digital inputs present**
- **V_{SS} to V_{DD} analog signal range**
  - **±5 V to ±22 V dual supply operation**
  - **8 V to 44 V single-supply operation**
  - **Fully specified at ±15 V, ±20 V, +12 V, and +36 V**

APPLICATIONS

- **Analog input/output modules**
- **Process control/distributed control systems**
- **Data acquisition**
- **Instrumentation**
- **Avionics**
- **Automatic test equipment**
- **Communication systems**
- **Relay replacement**

FUNCTIONAL BLOCK DIAGRAM

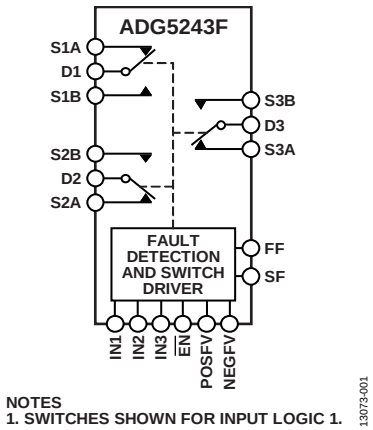

Figure 1.

GENERAL DESCRIPTION

The ADG5243F comprises three independently selectable, single-pole/double-throw (SPDT) switches. All channels exhibit break-before-make switching action that prevents momentary shorting when switching channels. An $\overline{EN}$ input enables or disables the device. When disabled, all channels are switched off. Each switch conducts equally well in both directions when on, and each switch has an input signal range that extends to the supplies. The primary supply voltages define the on-resistance profile, whereas the secondary supply voltages define the voltage level at which the overvoltage protection engages.

When no power supplies are present, the channel remains in the off condition, and the switch inputs are high impedance. Under normal operating conditions, if the analog input signal levels on any Sx pin exceed the positive fault voltage (POSFV) or the negative fault voltage (NEGFV) by a threshold voltage (V_T), the channel turns off and that Sx pin becomes high impedance. If the switch is selected to be on, then the drain pin is pulled to the secondary supply voltage that was exceeded. Input signal levels up to −55 V or +55 V relative to ground are blocked, in both the powered and unpowered conditions.

The low capacitance and charge injection of these switches make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch switching and fast settling times are required.

Note that, throughout this data sheet, multifunction pins, such as IN1/F1, are referred to either by the entire pin name or by a single function of the pin, for example, IN1, when only that function is relevant.

PRODUCT HIGHLIGHTS

1. The source pins are protected against voltages greater than the secondary supply rails, up to −55 V and +55 V.
2. The source pins are protected against voltages between −55 V and +55 V in an unpowered state.
3. Overvoltage detection with the digital output indicates the operating state of the switches.
4. Trench isolation guards against latch-up.
5. Optimized for low charge injection and on-capacitance.
6. The ADG5243F can be operated from a dual supply of ±5 V to ±22 V or a single power supply of 8 V to 44 V.

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REVISION HISTORY

8/2016—Rev. 0 to Rev. A

Added LFCSP Package ... Universal
Updated Outline Dimensions ... 30
Changes to Ordering Guide ... 30

10/2015—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

V_{DD} = 15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, $C_{DECOUPLING}$ = 0.1 µF, unless otherwise noted.

Table 1.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +13.5 V, V_{SS} = −13.5 V, see Figure 35
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	250			Ω typ	V_S = ±10 V, I_S = −1 mA
	270	335	395	Ω max	
	250			Ω typ	V_S = ±9 V, I_S = −1 mA
	270	335	395	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	1			Ω typ	V_S = ±10 V, I_S = −1 mA
	4	5	5	Ω max	
	1			Ω typ	V_S = ±9 V, I_S = −1 mA
	4	5	5	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	7			Ω typ	V_{DD} = +15 V, V_{SS} = −15 V, V_S = ±10 V, I_S = −1 mA
	8.5	9.5	9.5	Ω max	
	1.5			Ω typ	V_{DD} = +15 V, V_{SS} = −15 V, V_S = ±9 V, I_S = −1 mA
	3.5	4.5	4.5	Ω max	
Threshold Voltage, V_T	0.7			V typ	See Figure 27
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = ±10 V, V_D = ∓10 V, see Figure 33
	±1	±2	±5	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = ±10 V, V_D = ∓10 V, see Figure 33
	±1	±2	±5	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.3			nA typ	V_S = V_D = ±10 V, see Figure 34
	±1.5	±5	±10	nA max	
FAULT					
Source Leakage Current, I_S					
With Overvoltage	±66		±78	µA typ	V_{DD} = +16.5 V, V_{SS} = −16.5 V, GND = 0 V, V_S = ±55 V, see Figure 32
Power Supplies Grounded or Floating	±25		±40	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, INx = 0 V or floating, V_S = ±55 V, see Figure 31
Drain Leakage Current, I_D					
With Overvoltage	±2			nA typ	V_{DD} = +16.5 V, V_{SS} = −16.5 V, GND = 0 V, V_S = ±55 V, see Figure 32
	±8	±15	±50	nA max	
Power Supplies Grounded	±5			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±55 V, INx = 0 V, see Figure 31
	±100	±100	±100	nA max	
Power Supplies Floating	±50	±50	±50	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±55 V, INx = 0 V, see Figure 31
DIGITAL INPUTS/OUTPUTS					
Input Voltage					
High, V_{INH}			2.0	V min	
Low, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.7			µA typ	V_{IN} = GND or V_{DD}
	±1.1		±1.2	µA max	
Digital Input Capacitance, C_{IN}	5.0			pF typ	
Output Voltage					
High, V_{OH}	2.0			V min	
Low, V_{OL}	0.4			V max	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	160			ns typ	R_L = 1 kΩ, C_L = 35 pF
	195	210	215	ns max	V_S = 10 V, see Figure 47
t_{ON} ($\overline{EN}$)	165			ns typ	R_L = 1 kΩ, C_L = 35 pF
	205	220	230	ns max	V_S = 10 V, see Figure 46
t_{OFF} ($\overline{EN}$)	70			ns typ	R_L = 1 kΩ, C_L = 35 pF
	90	110	110	ns max	V_S = 10 V, see Figure 46
Break-Before-Make Time Delay, t_D	115			ns typ	R_L = 1 kΩ, C_L = 35 pF
			85	ns min	V_S = 10 V, see Figure 45
Overvoltage Response Time, $t_{RESPONSE}$	90			ns typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 40
	115	130	130	ns max	
Overvoltage Recovery Time, $t_{RECOVERY}$	745			ns typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 41
	945	965	970	ns max	
Interrupt Flag Response Time, $t_{DIGRESP}$	90			ns typ	C_L = 12 pF, see Figure 42
Interrupt Flag Recovery Time, t_{DIGREC}	65			µs typ	C_L = 12 pF, see Figure 43
	900			ns typ	C_L = 12 pF, R_{PULLUP} = 1 kΩ, see Figure 44
Charge Injection, Q_{INJ}	−0.8			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 48
Off Isolation	−74			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 37
Channel-to-Channel Crosstalk	−83			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 39
Total Harmonic Distortion Plus Noise, THD + N	0.005			% typ	R_L = 10 kΩ, V_S = 15 V p-p, f = 20 Hz to 20 kHz, see Figure 36
−3 dB Bandwidth	350			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 38
Insertion Loss	10.5			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 38
C_S (Off)	4			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	4			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	10			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = POSFV = +16.5 V, V_{SS} = NEGFV = −16.5 V, GND = 0 V, digital inputs = 0 V, 5 V, or V_{DD}
Normal Mode					
I_{DD}	1.3			mA typ	
I_{POSFV}	0.15			mA typ	
I_{DD} + I_{POSFV}	2		2.1	mA max	
I_{GND}	0.75			mA typ	
	1.25		1.4	mA max	
I_{SS}	0.65			mA typ	
I_{NEGFV}	0.2			mA typ	
I_{SS} + I_{NEGFV}	0.95		1.0	mA max	
Fault Mode					V_S = ±55 V, all channels in fault
I_{DD}	1.4			mA typ	
I_{POSFV}	0.2			mA typ	
I_{DD} + I_{POSFV}	2.5		2.8	mA max	
I_{GND}	0.9			mA typ	
	1.8		1.9	mA max	
I_{SS}	0.55			mA typ	
I_{NEGFV}	0.2			mA typ	
I_{SS} + I_{NEGFV}	1.0		1.1	mA max	
V_{DD}/V_{SS}			±5	V min	GND = 0 V
			±22	V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

±20 V DUAL SUPPLY

V_{DD} = 20 V ± 10%, V_{SS} = −20 V ± 10%, GND = 0 V, $C_{DECOUPLING}$ = 0.1 µF, unless otherwise noted.

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +18 V, V_{SS} = −18 V, see Figure 35
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	270			Ω typ	V_S = ±15 V, I_S = −1 mA
	290	355	410	Ω max	
	250			Ω typ	V_S = ±13.5 V, I_S = −1 mA
	270	335	395	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	1			Ω typ	V_S = ±15 V, I_S = −1 mA
	4	5	5	Ω max	
	1			Ω typ	V_S = ±13.5 V, I_S = −1 mA
	4	5	5	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	27			Ω typ	V_{DD} = +20 V, V_{SS} = −20 V, V_S = ±15 V, I_S = −1 mA
	29.5	29.5	29.5	Ω max	
	5			Ω typ	V_{DD} = +20 V, V_{SS} = −20 V, V_S = ±13.5 V, I_S = −1 mA
	6.5	8.5	8.5	Ω max	
Threshold Voltage, V_T	0.7			V typ	See Figure 27
LEAKAGE CURRENTS					V_{DD} = +22 V, V_{SS} = −22 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = ±15 V, V_D = ∓15 V, see Figure 33
	±1	±2	±5	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = ±15 V, V_D = ∓15 V, see Figure 33
	±1	±2	±5	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.3			nA typ	V_S = V_D = ±15 V, see Figure 34
	±1.5	±5	±10	nA max	
FAULT					
Source Leakage Current, I_S					
With Overvoltage	±66			µA typ	V_{DD} = +22 V, V_{SS} = −22 V, GND = 0 V, V_S = ±55 V, see Figure 32
Power Supplies Grounded or Floating	±25			µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, INx = 0 V or floating, V_S = ±55 V, see Figure 31
Drain Leakage Current, I_D					
With Overvoltage	±2			nA typ	V_{DD} = +22 V, V_{SS} = −22 V, GND = 0 V, V_S = ±55 V, see Figure 32
	±8	±15	±50	nA max	
Power Supplies Grounded	±5			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±55 V, INx = 0 V, see Figure 31
	±100	±100	±100	nA max	
Power Supplies Floating	±50	±50	±50	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±55 V, INx = 0 V, see Figure 31
DIGITAL INPUTS/OUTPUTS					
Input Voltage					
High, V_{INH}			2.0	V min	
Low, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.7			µA typ	V_{IN} = GND or V_{DD}
	±1.1		±1.2	µA max	
Digital Input Capacitance, C_{IN}	5.0			pF typ	
Output Voltage					
High, V_{OH}	2.0			V min	
Low, V_{OL}	0.4			V max	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	165			ns typ	R_L = 1 kΩ, C_L = 35 pF
	210	230	235	ns max	V_S = 10 V, see Figure 47
t_{ON} ($\overline{EN}$)	170			ns typ	R_L = 1 kΩ, C_L = 35 pF
	215	240	250	ns max	V_S = 10 V, see Figure 46
t_{OFF} ($\overline{EN}$)	70			ns typ	R_L = 1 kΩ, C_L = 35 pF
	85	115	115	ns max	V_S = 10 V, see Figure 46
Break-Before-Make Time Delay, t_D	120			ns typ	R_L = 1 kΩ, C_L = 35 pF
			85	ns min	V_S = 10 V, see Figure 45
Overvoltage Response Time, $t_{RESPONSE}$	75			ns typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 40
	105	105	105	ns max	
Overvoltage Recovery Time, $t_{RECOVERY}$	820			ns typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 41
	1100	1250	1400	ns max	
Interrupt Flag Response Time, $t_{DIGRESP}$	75			ns typ	C_L = 12 pF, see Figure 42
Interrupt Flag Recovery Time, t_{DIGREC}	65			µs typ	C_L = 12 pF, see Figure 43
	1000			ns typ	C_L = 12 pF, R_{PULLUP} = 1 kΩ, see Figure 44
Charge Injection, Q_{INJ}	−1.2			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 48
Off Isolation	−74			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 37
Channel-to-Channel Crosstalk	−82			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 39
Total Harmonic Distortion Plus Noise, THD + N	0.005			% typ	R_L = 10 kΩ, V_S = 20 V p-p, f = 20 Hz to 20 kHz, see Figure 36
−3 dB Bandwidth	350			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 38
Insertion Loss	10.5			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 38
C_S (Off)	4			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	4			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	10			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = POSFV = +22 V, V_{SS} = NEGFV = −22 V, GND = 0 V, digital inputs = 0 V, 5 V, or V_{DD}
Normal Mode					
I_{DD}	1.3			mA typ	
I_{POSFV}	0.15			mA typ	
I_{DD} + I_{POSFV}	2		2.1	mA max	
I_{GND}	0.75			mA typ	
	1.25		1.4	mA max	
I_{SS}	0.65			mA typ	
I_{NEGFV}	0.2			mA typ	
I_{SS} + I_{NEGFV}	1.0		1.0	mA max	
Fault Mode					V_S = ±55 V, all channels in fault
I_{DD}	1.4			mA typ	
I_{POSFV}	0.2			mA typ	
I_{DD} + I_{POSFV}	2.5		2.8	mA max	
I_{GND}	0.9			mA typ	
	1.8		1.9	mA max	
I_{SS}	0.55			mA typ	
I_{NEGFV}	0.2			mA typ	
I_{SS} + I_{NEGFV}	1.0		1.1	mA max	
V_{DD}/V_{SS}			±5	V min	GND = 0 V
			±22	V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, $C_{DECOUPLING}$ = 0.1 µF, unless otherwise noted.

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 10.8 V, V_{SS} = 0 V, see Figure 35
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	630			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA
	690	710	730	Ω max	
	270			Ω typ	V_S = 3.5 V to 8.5 V, I_S = −1 mA
	290	355	410	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	6			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA
	19	19	19	Ω max	
	1			Ω typ	V_S = 3.5 V to 8.5 V, I_S = −1 mA
	5	5	5	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	380			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA
	440	460	460	Ω max	
	25			Ω typ	V_S = 3.5 V to 8.5 V, I_S = −1 mA
	27	28	28	Ω max	
Threshold Voltage, V_T	0.7			V typ	See Figure 27
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 33
	±1	±2	±5	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 33
	±1	±2	±5	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.3			nA typ	V_S = V_D = 1 V/10 V, see Figure 34
	±1.5	±5	±10	nA max	
FAULT					
Source Leakage Current, I_S					
With Overvoltage	±63			µA typ	V_{DD} = 13.2 V, V_{SS} = 0 V, GND = 0 V, V_S = ±55 V, see Figure 32
Power Supplies Grounded or Floating	±25			µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, INx = 0 V or floating, V_S = ±55 V, see Figure 31
Drain Leakage Current, I_D					
With Overvoltage	±2			nA typ	V_{DD} = 13.2 V, V_{SS} = 0 V, GND = 0 V, V_S = ±55 V, see Figure 32
	±8	±15	±50	nA max	
Power Supplies Grounded	±5			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±55 V, INx = 0 V, see Figure 31
	±100	±100	±100	nA max	
Power Supplies Floating	±50	±50	±50	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±55 V, INx = 0 V, see Figure 31
DIGITAL INPUTS/OUTPUTS					
Input Voltage					
High, V_{INH}			2.0	V min	
Low, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.7			µA typ	V_{IN} = GND or V_{DD}
	±1.1		±1.2	µA max	
Digital Input Capacitance, C_{IN}	5.0			pF typ	
Output Voltage					
High, V_{OH}	2.0			V min	
Low, V_{OL}	0.4			V max	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	140			ns typ	R_L = 1 kΩ, C_L = 35 pF
	170	185	195	ns max	V_S = 8 V, see Figure 47
t_{ON} ($\overline{EN}$)	145			ns typ	R_L = 1 kΩ, C_L = 35 pF
	170	185	200	ns max	V_S = 8 V, see Figure 46
t_{OFF} ($\overline{EN}$)	95			ns typ	R_L = 1 kΩ, C_L = 35 pF
	115	125	125	ns max	V_S = 8 V, see Figure 46
Break-Before-Make Time Delay, t_D	80			ns typ	R_L = 1 kΩ, C_L = 35 pF
			60	ns min	V_S = 8 V, see Figure 45
Overvoltage Response Time, $t_{RESPONSE}$	110			ns typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 40
	145	145	145	ns max	
Overvoltage Recovery Time, $t_{RECOVERY}$	500			ns typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 41
	655	720	765	ns max	
Interrupt Flag Response Time, $t_{DIGRESP}$	95			ns typ	C_L = 12 pF, see Figure 42
Interrupt Flag Recovery Time, t_{DIGREC}	65			µs typ	C_L = 12 pF, see Figure 43
	900			ns typ	C_L = 12 pF, R_{PULLUP} = 1 kΩ, see Figure 44
Charge Injection, Q_{INJ}	0.8			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF, see Figure 48
Off Isolation	−74			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 37
Channel-to-Channel Crosstalk	−82			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 39
Total Harmonic Distortion Plus Noise, THD + N	0.044			% typ	R_L = 10 kΩ, V_S = 6 V p-p, f = 20 Hz to 20 kHz, see Figure 36
−3 dB Bandwidth	320			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 38
Insertion Loss	10.5			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 38
C_S (Off)	4			pF typ	V_S = 6 V, f = 1 MHz
C_D (Off)	5			pF typ	V_S = 6 V, f = 1 MHz
C_D (On), C_S (On)	10			pF typ	V_S = 6 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = POSFV = 13.2 V, V_{SS} = NEGFV = 0 V, GND = 0 V, digital inputs = 0 V, 5 V, or V_{DD}
Normal Mode					
I_{DD}	1.3			mA typ	
I_{POSFV}	0.15			mA typ	
I_{DD} + I_{POSFV}	2		2.1	mA max	
I_{GND}	0.75			mA typ	
	1.4		1.5	mA max	
I_{SS}	0.55			mA typ	
I_{NEGFV}	0.2			mA typ	
I_{SS} + I_{NEGFV}	0.95		1.0	mA max	
Fault Mode					V_S = ±55 V, all channels in fault
I_{DD}	1.4			mA typ	
I_{POSFV}	0.2			mA typ	
I_{DD} + I_{POSFV}	2.5		2.8	mA max	
I_{GND}	0.9			mA typ	
	1.8		1.9	mA max	
I_{SS}	0.55			mA typ	Digital inputs = 5 V
I_{NEGFV}	0.2			mA typ	
I_{SS} + I_{NEGFV}	1.0		1.1	mA max	V_S = ±55 V, V_D = 0 V
V_{DD}/V_{SS}			8	V min	GND = 0 V
			44	V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

V_{DD} = 36 V ± 10%, V_{SS} = 0 V, GND = 0 V, $C_{DECOUPLING}$ = 0.1 µF, unless otherwise noted.

Table 4.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 32.4 V, V_{SS} = 0 V, see Figure 35
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	310			Ω typ	V_S = 0 V to 30 V, I_S = −1 mA
	335	415	480	Ω max	
	250			Ω typ	V_S = 4.5 V to 28 V, I_S = −1 mA
	270	335	395	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	3			Ω typ	V_S = 0 V to 30 V, I_S = −1 mA
	7	16	18	Ω max	
	3			Ω typ	V_S = 4.5 V to 28 V, I_S = −1 mA
	6.5	11	12	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	62			Ω typ	V_S = 0 V to 30 V, I_S = −1 mA
	70	85	100	Ω max	
	1.5			Ω typ	V_S = 4.5 V to 28 V, I_S = −1 mA
	3.5	4	4	Ω max	
Threshold Voltage, V_T	0.7			V typ	See Figure 27
LEAKAGE CURRENTS					V_{DD} =39.6 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = 1 V/30 V, V_D = 30 V/1 V, see Figure 33
	±1	±2	±5	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = 1 V/30 V, V_D = 30 V/1 V, see Figure 33
	±1	±2	±5	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.3			nA typ	V_S = V_D = 1 V/30 V, see Figure 34
	±1.5	±5	±10	nA max	
FAULT					
Source Leakage Current, I_S					
With Overvoltage	±58			µA typ	V_{DD} = 39.6 V, V_{SS} = 0 V, GND = 0 V, V_S = +55 V, −40 V, see Figure 32
Power Supplies Grounded or Floating	±25			µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, INx = 0 V or floating, V_S = +55 V, −40 V, see Figure 31
Drain Leakage Current, I_D					
With Overvoltage	±2			nA typ	V_{DD} = 39.6 V, V_{SS} = 0 V, GND = 0 V, V_S = +55 V, −40 V, see Figure 32
	±8	±15	±50	nA max	
Power Supplies Grounded	±5			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = +55 V, −40 V, INx = 0 V, see Figure 31
	±100	±100	±100	nA max	
Power Supplies Floating	±50	±50	±50	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = +55 V, −40 V, INx = 0 V, see Figure 31
DIGITAL INPUTS/OUTPUTS					
Input Voltage					
High, V_{INH}			2.0	V min	
Low, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.7			µA typ	V_{IN} = V_{GND} or V_{DD}
	±1.1		±1.2	µA max	
Digital Input Capacitance, C_{IN}	5.0			pF typ	
Output Voltage					
High, V_{OH}	2.0			V min	
Low, V_{OL}	0.4			V max	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	155			ns typ	R_L = 1 kΩ, C_L = 35 pF
	190	205	210	ns max	V_S = 18 V, see Figure 47
t_{ON} ($\overline{EN}$)	160			ns typ	R_L = 1 kΩ, C_L = 35 pF
	195	210	220	ns max	V_S = 18 V, see Figure 46
t_{OFF} ($\overline{EN}$)	95			ns typ	R_L = 1 kΩ, C_L = 35 pF
	115	125	130	ns max	V_S = 18 V, see Figure 46
Break-Before-Make Time Delay, t_D	100			ns typ	R_L = 1 kΩ, C_L = 35 pF
			70	ns min	V_S = 18 V, see Figure 45
Overvoltage Response Time, $t_{RESPONSE}$	60			ns typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 40
	80	85	85	ns max	
Overvoltage Recovery Time, $t_{RECOVERY}$	1400			ns typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 41
	1900	2100	2200	ns max	
Interrupt Flag Response Time, $t_{DIGRESP}$	85			ns typ	C_L = 12 pF, see Figure 42
Interrupt Flag Recovery Time, t_{DIGREC}	65			µs typ	C_L = 12 pF, see Figure 43
	1600			ns typ	C_L = 12 pF, R_{PULLUP} = 1 kΩ, see Figure 44
Charge Injection, Q_{INJ}	−1.4			pC typ	V_S = 18 V, R_S = 0 Ω, C_L = 1 nF, see Figure 48
Off Isolation	−74			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 37
Channel-to-Channel Crosstalk	−85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 39
Total Harmonic Distortion Plus Noise, THD + N	0.007			% typ	R_L = 10 kΩ, V_S = 18 V p-p, f = 20 Hz to 20 kHz, see Figure 36
−3 dB Bandwidth	355			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 38
Insertion Loss	10.5			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 38
C_S (Off)	4			pF typ	V_S = 18 V, f = 1 MHz
C_D (Off)	4			pF typ	V_S = 18 V, f = 1 MHz
C_D (On), C_S (On)	9			pF typ	V_S = 18 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = POSFV = 39.6 V, V_{SS} = NEGFV = 0 V, GND = 0 V, digital inputs = 0 V, 5 V, or V_{DD}
Normal Mode					
I_{DD}	1.3			mA typ	
I_{POSFV}	0.15			mA typ	
I_{DD} + I_{POSFV}	2		2.1	mA max	
I_{GND}	0.75			mA typ	
	1.4		1.5	mA max	
I_{SS}	0.55			mA typ	
I_{NEGFV}	0.2			mA typ	
I_{SS} + I_{NEGFV}	0.95		1.0	mA max	
Fault Mode					V_S = +55 V, −40 V, all channels in fault
I_{DD}	1.4			mA typ	
I_{POSFV}	0.2			mA typ	
I_{DD} + I_{POSFV}	2.5		2.8	mA max	
I_{GND}	0.9			mA typ	
	1.8		1.9	mA max	
I_{SS}	0.55			mA typ	
I_{NEGFV}	0.2			mA typ	
I_{SS} + I_{NEGFV}	1.0		1.1	mA max	
V_{DD}/V_{SS}			8	V min	GND = 0 V
			44	V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, Sx[1] OR Dx

Table 5.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
20-LEAD TSSOP					
θ_{JA} = 112.6°C/W	17	11	7	mA max	$V_S = V_{SS}$ to $V_{DD} - 4.5$ V
	10	7	5	mA max	$V_S = V_{SS}$ to V_{DD}
20-LEAD LFCSP					
θ_{JA} = 30.4°C/W	29	18	9	mA max	$V_S = V_{SS}$ to $V_{DD} - 4.5$ V
	17	11	7	mA max	$V_S = V_{SS}$ to V_{DD}

[1] Sx is the S1A to S3A and S1B to S3B pins.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	−0.3 V to +48 V
V_{SS} to GND	−48 V to +0.3 V
POSFV to GND	−0.3 V to V_{DD} +0.3 V
NEGFV to GND	V_{SS} − 0.3 V to +0.3 V
Sx Pins	−55 V to +55 V
Sx to V_{DD} or V_{SS}	80 V
V_S to V_D	80 V
Dx Pins[1]	NEGFV − 0.7 V to POSFV + 0.7 V or 30 mA, whichever occurs first
Digital Inputs	GND − 0.7 V to 48 V or 30 mA, whichever occurs first
Peak Current, Sx or Dx Pins	44.5 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx Pins	Data[2] + 15%
Digital Outputs	GND − 0.7 V to 6 V or 30 mA, whichever occurs first
Dx Pins, Overvoltage State, Load Current	1 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	
20-Lead TSSOP, Thermal Impedance (4-Layer Board)	112.6°C/W
20-Lead LFCSP, Thermal Impedance (4-Layer Board)	30.4°C/W
Reflow Soldering Peak Temperature, Pb-Free	As per JEDEC J-STD-020

[1] Overvoltages at the Dx pins are clamped by internal diodes. Limit the current to the maximum ratings given.
[2] See Table 5.

Stresses at or above those listed under Absolute Maximum Ratings cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

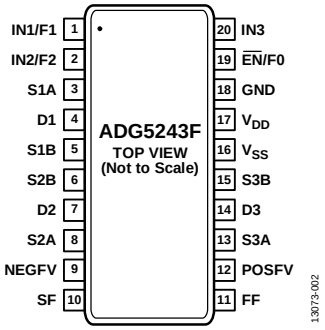
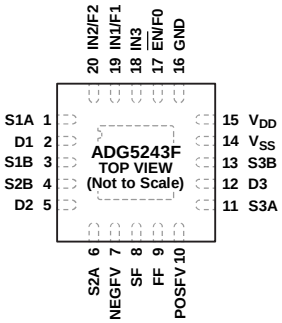


Figure 2. ADG5243F Pin Configuration (TSSOP)



NOTES
1. THE EXPOSED PAD IS CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE SUBSTRATE, V_{SS}.

Figure 3. ADG5243F Pin Configuration (LFCSP)

Table 7. Pin Function Descriptions

Pin No.			
TSSOP	LFCSP	Mnemonic	Description
1	19	IN1/F1	Logic Control Input (IN1) (See Table 8.)
			Decoder Pin (F1). This pin is used together with the specific fault pin (SF) to indicate which input is in a fault condition (see Table 9).
2	20	IN2/F2	Logic Control Input (IN2) (See Table 8).
			Decoder Pin (F2). This pin is used together with the specific fault pin (SF) to indicate which input is in a fault condition (see Table 9).
3	1	S1A	Overvoltage Protected Source Terminal 1A. This pin can be an input or an output.
4	2	D1	Drain Terminal 1. This pin can be an input or an output.
5	3	S1B	Overvoltage Protected Source Terminal 1B. This pin can be an input or an output.
6	4	S2B	Overvoltage Protected Source Terminal 2B. This pin can be an input or an output.
7	5	D2	Drain Terminal 2. This pin can be an input or an output.
8	6	S2A	Overvoltage Protected Source Terminal 2A. This pin can be an input or an output.
9	7	NEGFV	Negative Fault Voltage. This pin is the negative supply voltage that determines the overvoltage protection level. If a secondary supply is not used, connect this pin to V_{SS}.
10	8	SF	Specific Fault Digital Output. This pin has a high output when the device is in normal operation or a low output when a fault condition is detected on a specific pin, depending on the state of F0, F1, and F2 as shown in Table 9. The SF pin has a weak internal pull-up resistor, nominally 3 V output.
11	9	FF	Fault Flag Digital Output. This pin has a high output when the device is in normal operation, or a low output when a fault condition occurs on any of the Sx inputs. The FF pin has a weak internal pull-up resistor that allows multiple signals to be combined into a single interrupt for larger modules that contain multiple devices.
12	10	POSFV	Positive Fault Voltage. This pin is the positive supply voltage that determines the overvoltage protection level. If a secondary supply is not used, connect this pin to V_{DD}.
13	11	S3A	Overvoltage Protected Source Terminal 3A. This pin can be an input or an output.
14	12	D3	Drain Terminal 3. This pin can be an input or an output.
15	13	S3B	Overvoltage Protected Source Terminal 3B. This pin can be an input or an output.
16	14	V_{SS}	Most Negative Power Supply Potential.
17	15	V_{DD}	Most Positive Power Supply Potential.
18	16	GND	Ground (0 V) Reference.
19	17	$\overline{EN}$/F0	Active Low Digital Input. When this pin is high, the device is disabled and all switches are off. When this pin is low, the INx logic inputs determine the on switches.
			Decoder Pin (F0). This pin is used together with the specific fault pin (SF) to indicate which input is in a fault condition (see Table 9).
20	18	IN3	Logic Control Input (See Table 8).
	Exposed Pad	EP	The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS}.

Table 8. Switch Selection Truth Table

$\overline{EN}$	INx	SxA	SxB
1	X[1]	Off	Off
0	0	Off	On
0	1	On	Off

[1] X means don't care.

Table 9. Fault Diagnostic Output Truth Table

	State of Specific Flag (SF) with Control Inputs (F2, F1, F0)						
Switch in Fault[1]	**0, 0, 0**	**0, 1, 0**	**1, 0, 0**	**1, 0, 1**	**1, 1, 0**	**1, 1, 1**	**State of Fault Flag (FF)**
None	1	1	1	1	1	1	1
S1A	0	1	1	1	1	1	0
S1B	1	0	1	1	1	1	0
S2B	1	1	0	1	1	1	0
S2A	1	1	1	1	0	1	0
S3B	1	1	1	0	1	1	0
S3A	1	1	1	1	1	0	0

[1] More than one switch can be in fault. See the Applications Information section for more information.

TYPICAL PERFORMANCE CHARACTERISTICS

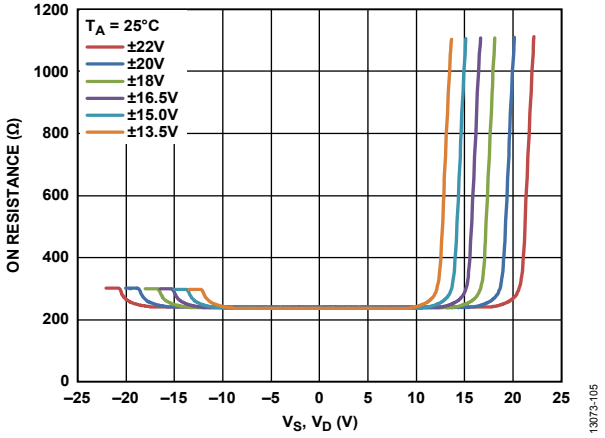


Figure 4. R_{ON} as a Function of V_S, V_D, Dual Supply

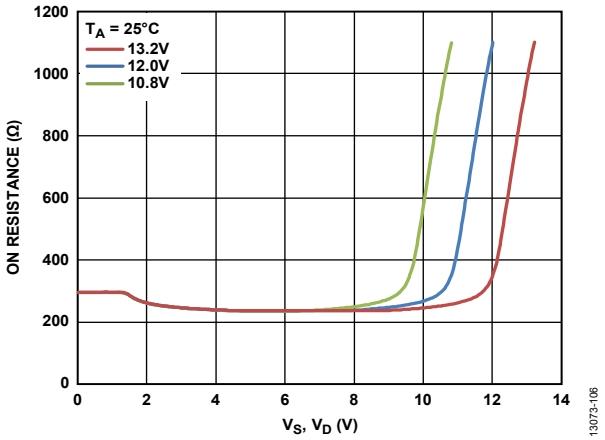


Figure 5. R_{ON} as a Function of V_S, V_D, 12 V Single Supply

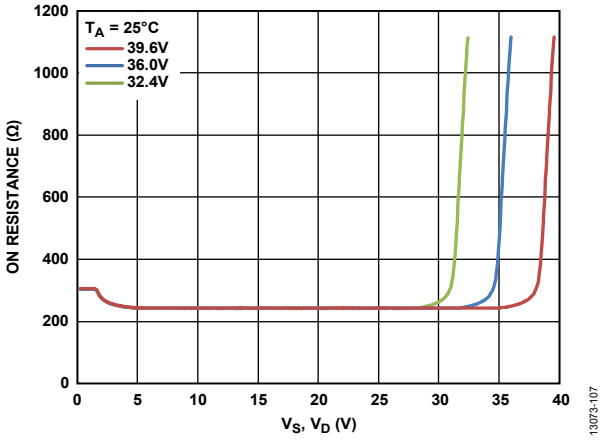


Figure 6. R_{ON} as a Function of V_S, V_D, 36 V Single Supply

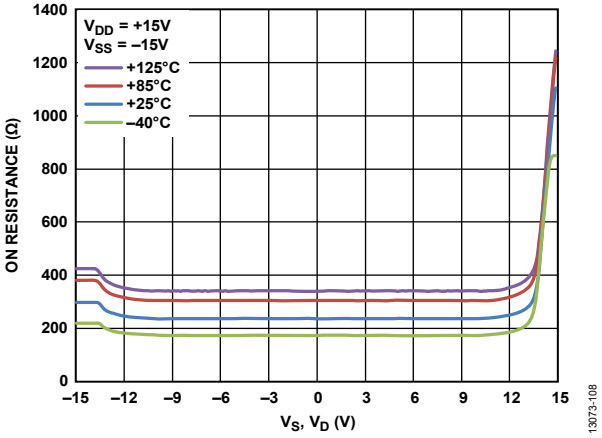


Figure 7. R_{ON} as a Function of V_S, V_D for Different Temperatures, ±15 V Dual Supply

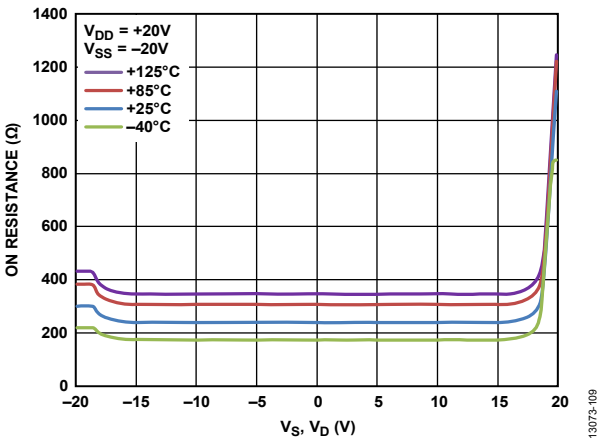


Figure 8. R_{ON} as a Function of V_S, V_D for Different Temperatures, ±20 V Dual Supply

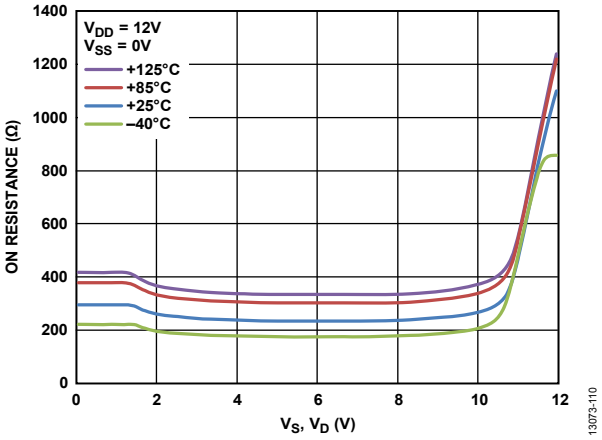


Figure 9. R_{ON} as a Function of V_S, V_D for Different Temperatures, 12 V Single Supply

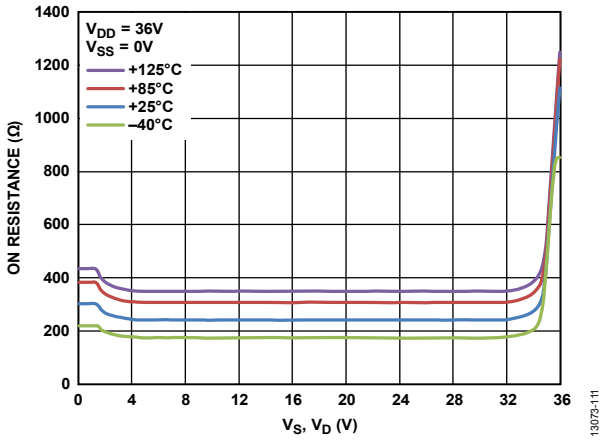


Figure 10. R_{ON} as a Function of V_S, V_D for Different Temperatures, 36 V Single Supply

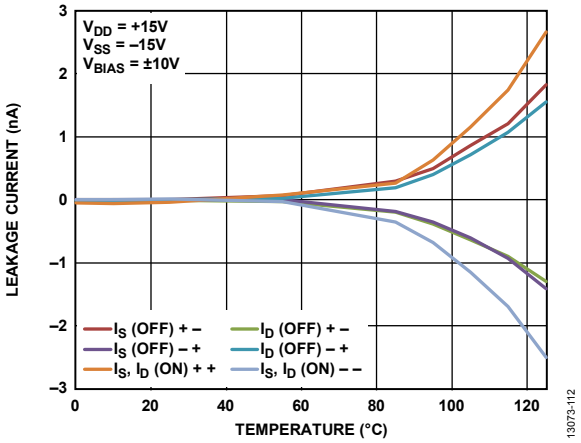


Figure 11. Leakage Current vs. Temperature, ±15 V Dual Supply

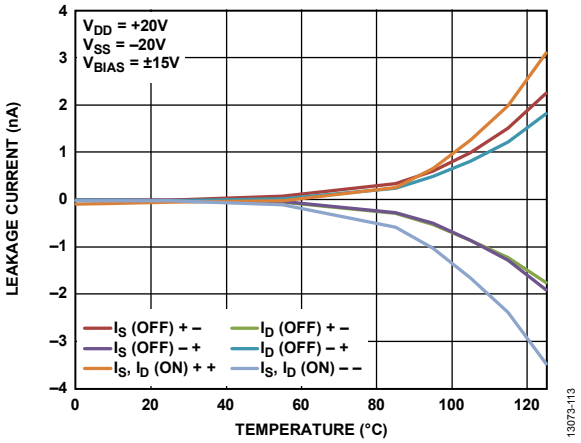


Figure 12. Leakage Current vs. Temperature, ±20 V Dual Supply

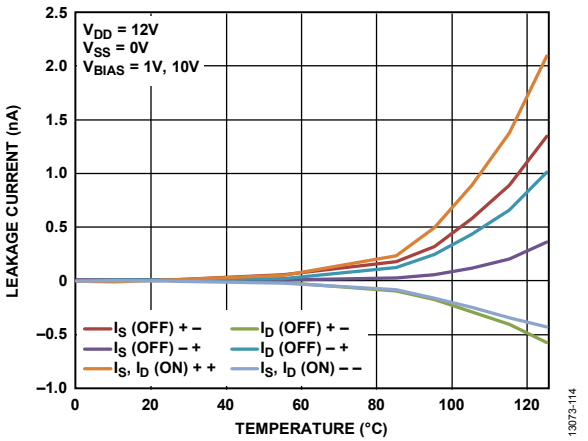


Figure 13. Leakage Current vs. Temperature, 12 V Single Supply

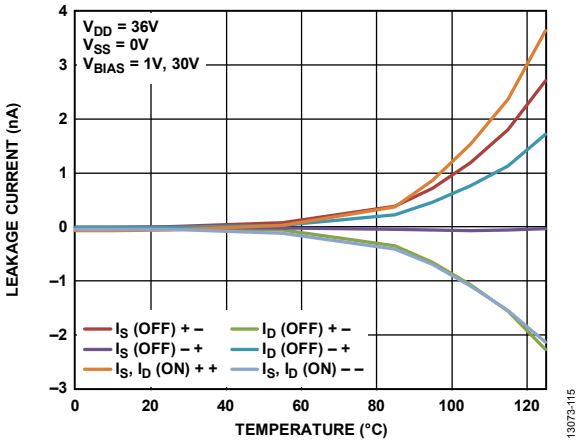


Figure 14. Leakage Current vs. Temperature, 36 V Single Supply

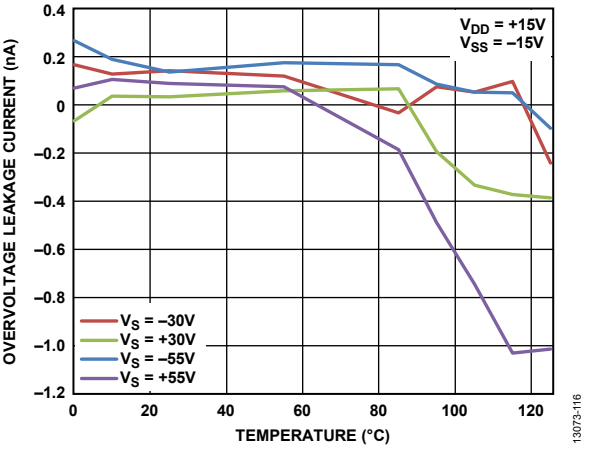


Figure 15. Overvoltage Leakage Current vs. Temperature, ±15 V Dual Supply

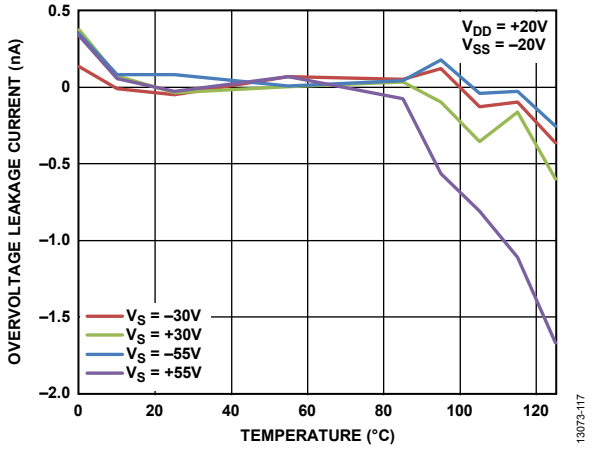


Figure 16. Overvoltage Leakage Current vs. Temperature, ±20 V Dual Supply

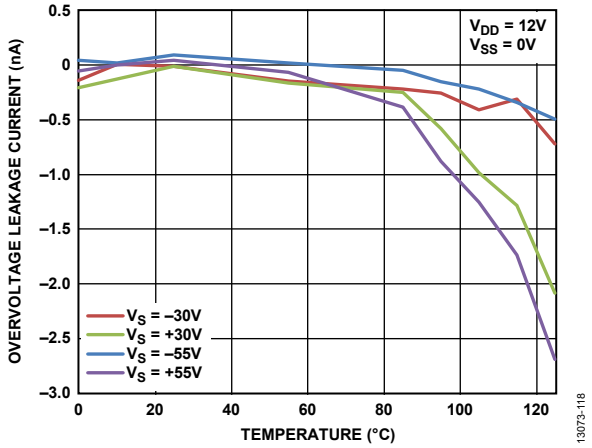


Figure 17. Overvoltage Leakage Current vs. Temperature, 12 V Single Supply

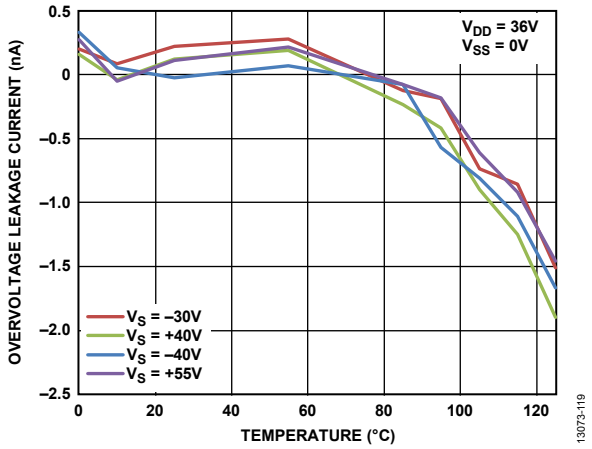


Figure 18. Overvoltage Leakage Current vs. Temperature, 36 V Single Supply

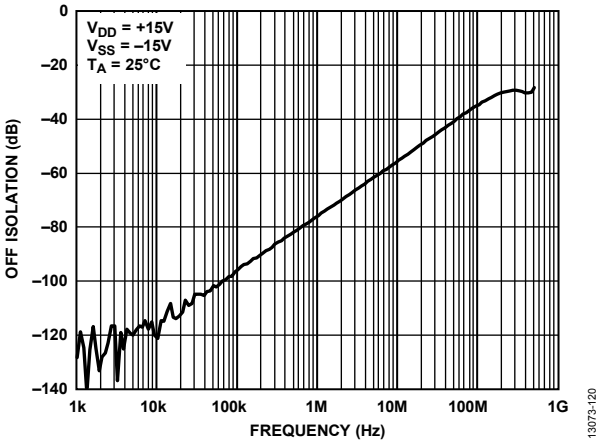


Figure 19. Off Isolation vs. Frequency, ±15 V Dual Supply

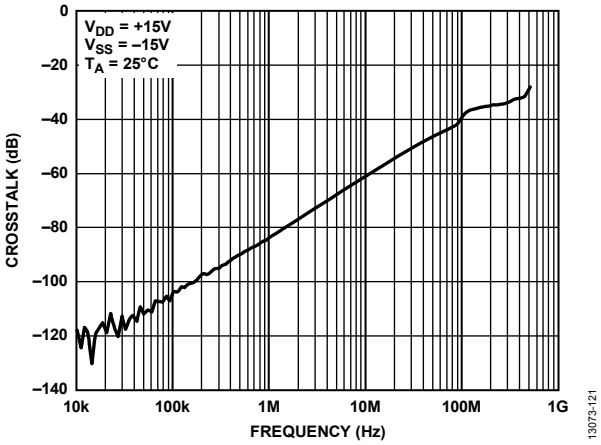


Figure 20. Crosstalk vs. Frequency, ±15 V Dual Supply

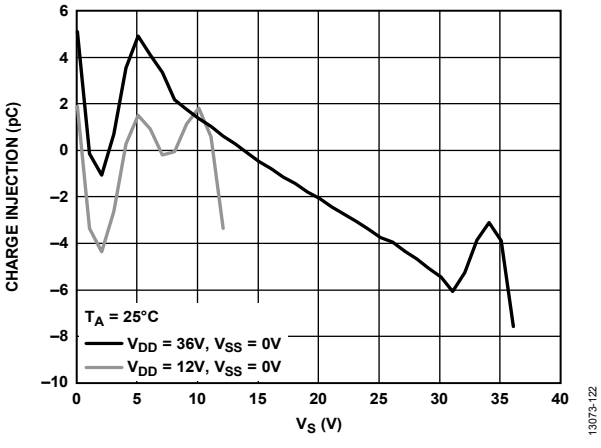


Figure 21. Charge Injection vs. Source Voltage (V_S), Single Supply

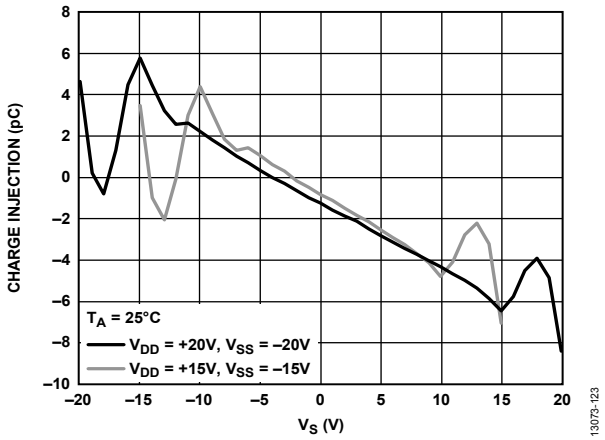


Figure 22. Charge Injection vs. Source Voltage (V_S), Dual Supply

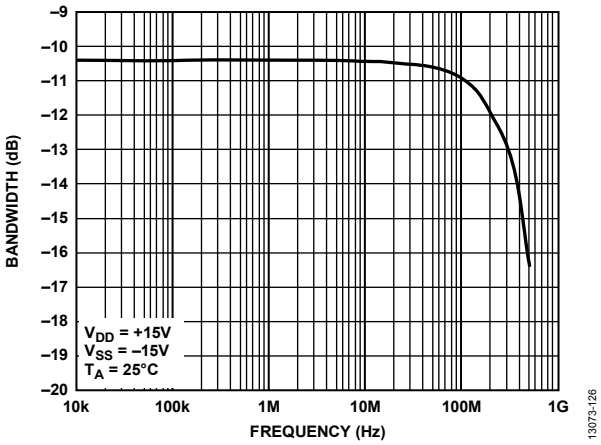


Figure 25. Bandwidth vs. Frequency

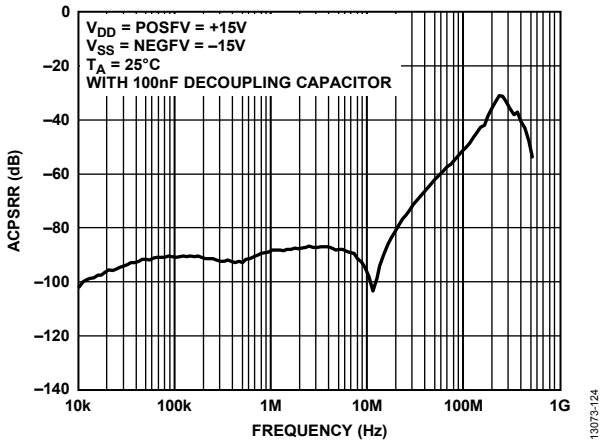


Figure 23. ACPSRR vs. Frequency, ±15 V Dual Supply

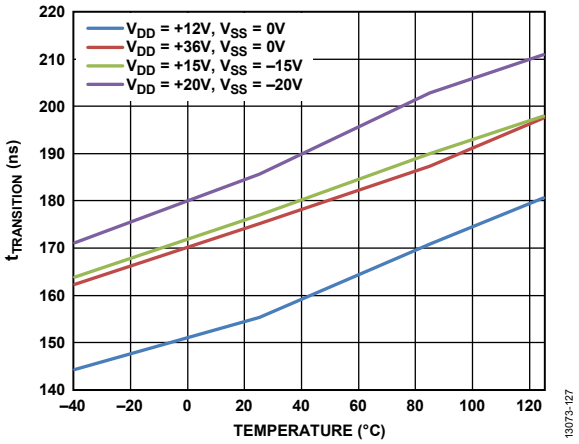


Figure 26. $t_{TRANSITION}$ vs. Temperature

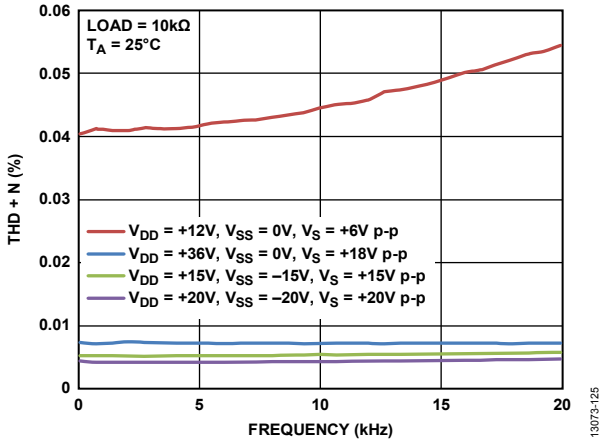


Figure 24. THD + N vs. Frequency

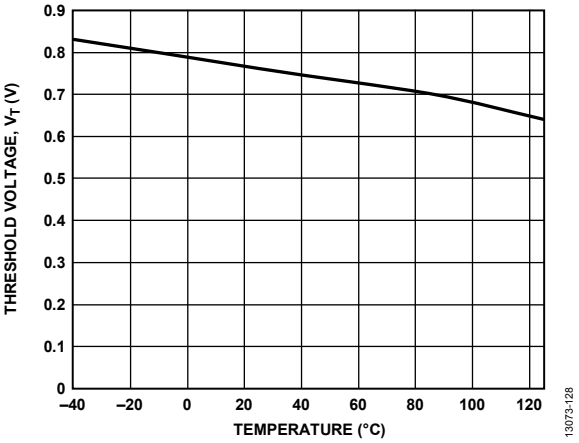


Figure 27. Threshold Voltage (V_T) vs. Temperature

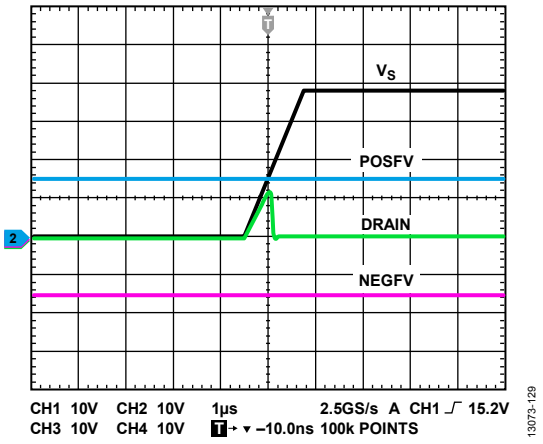


Figure 28. Drain Output Response to Positive Overvoltage (R_L = 1 kΩ)

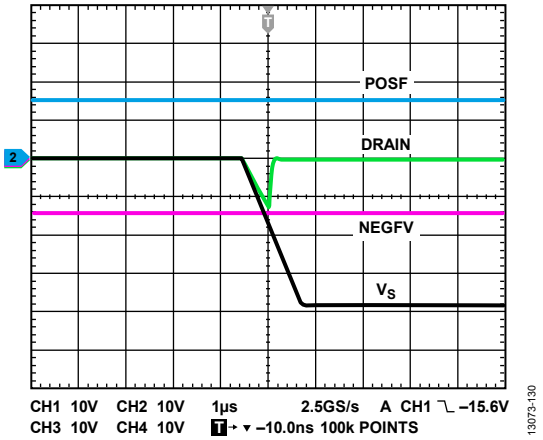


Figure 29. Drain Output Response to Negative Overvoltage (R_L = 1 kΩ)

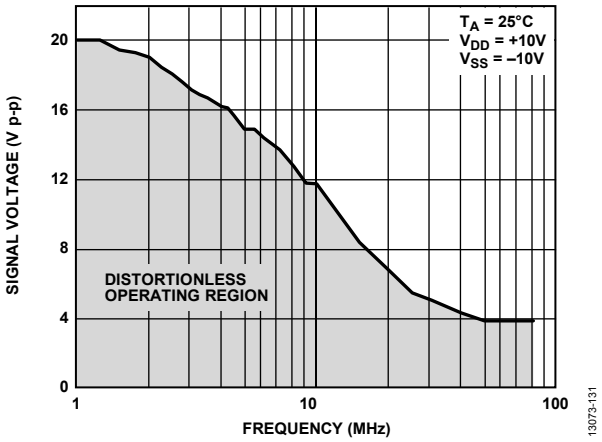


Figure 30. Large Signal Voltage Tracking vs. Frequency

TEST CIRCUITS

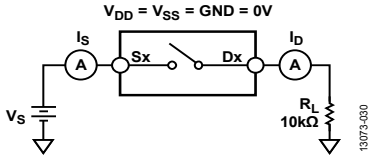


Figure 31. Switch Unpowered Leakage

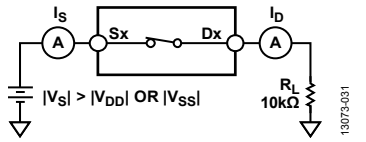


Figure 32. Switch Overvoltage Leakage

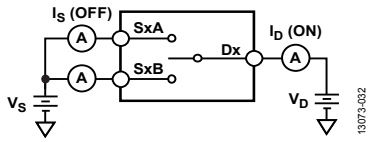


Figure 33. Off Leakage

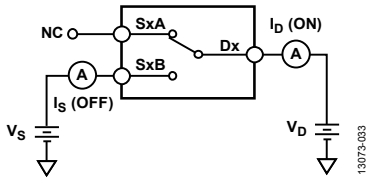


Figure 34. On Leakage

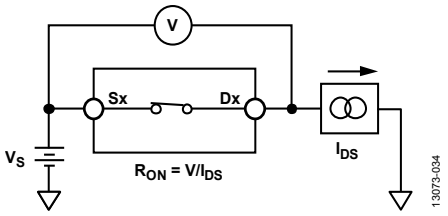


Figure 35. On Resistance

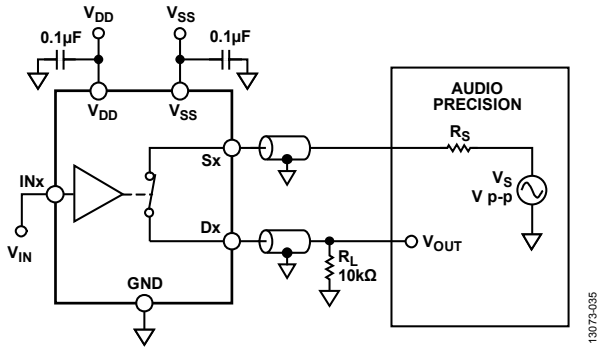


Figure 36. THD + N

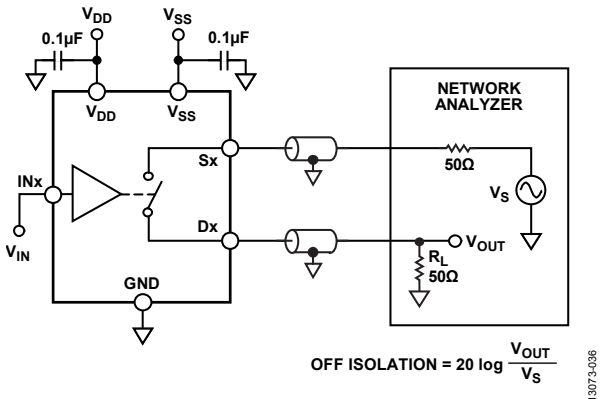


Figure 37. Off Isolation

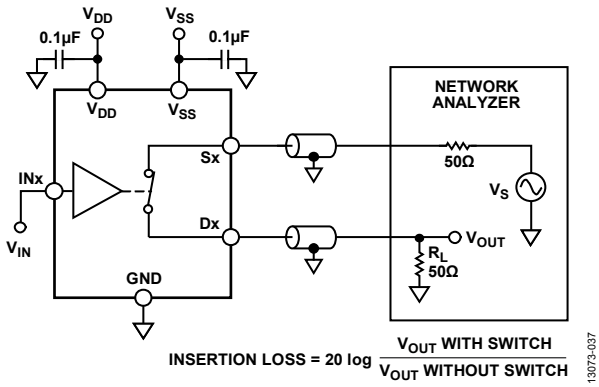


Figure 38. Bandwidth

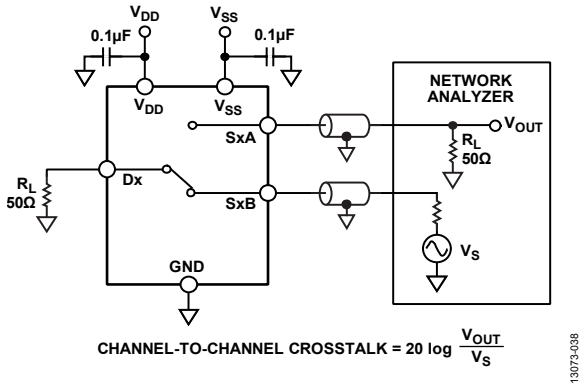


Figure 39. Channel-to-Channel Crosstalk

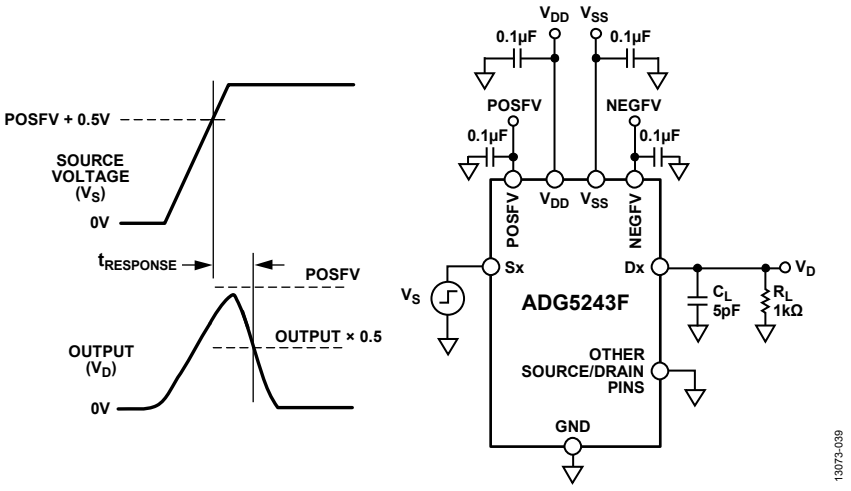
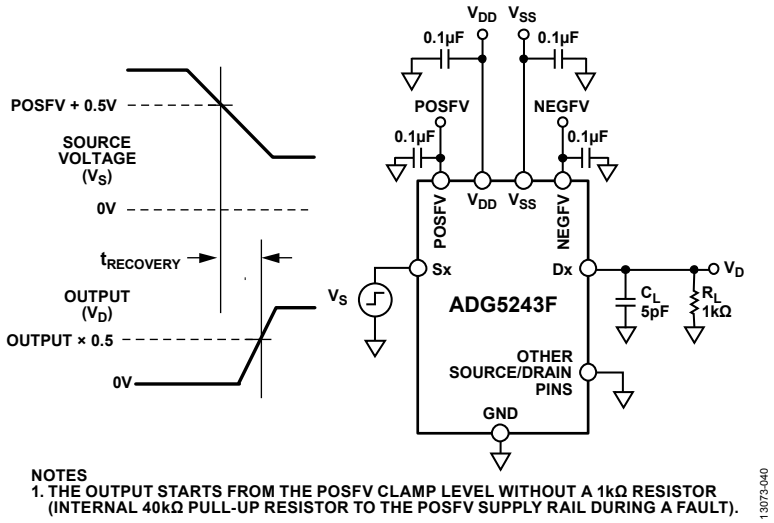
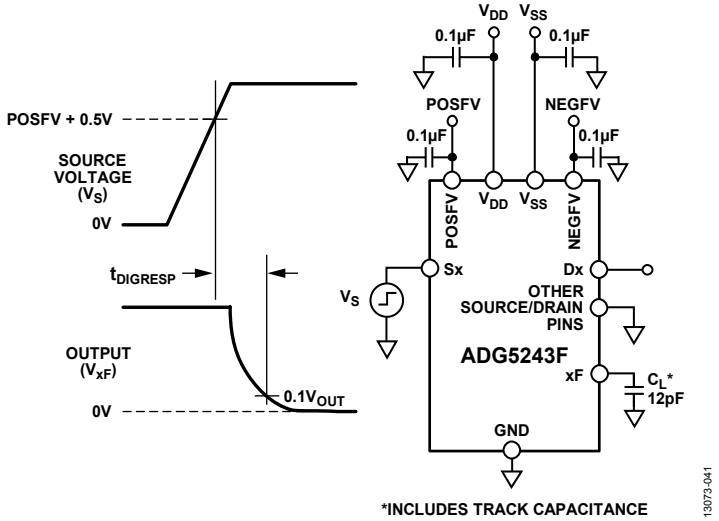


Figure 40. Overvoltage Response Time, $t_{RESPONSE}$



NOTES
1. THE OUTPUT STARTS FROM THE POSFV CLAMP LEVEL WITHOUT A 1kΩ RESISTOR (INTERNAL 40kΩ PULL-UP RESISTOR TO THE POSFV SUPPLY RAIL DURING A FAULT).

Figure 41. Overvoltage Recovery Time, $t_{RECOVERY}$



*INCLUDES TRACK CAPACITANCE

Figure 42. Interrupt Flag Response Time, $t_{DIGRESP}$

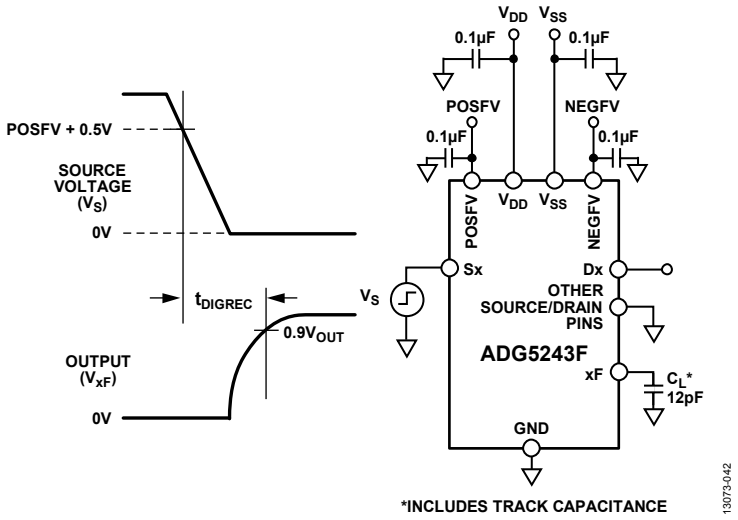


Figure 43. Interrupt Flag Recovery Time, t_{DIGREC}

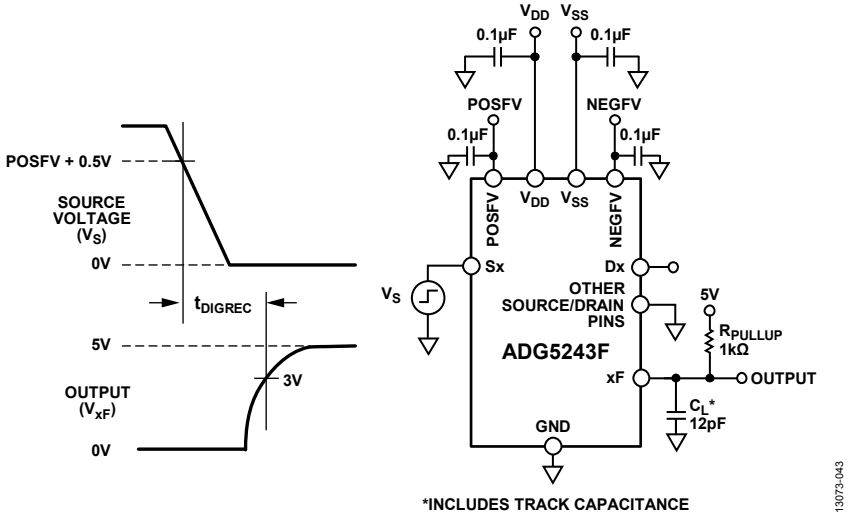


Figure 44. Interrupt Flag Recovery Time, t_{DIGREC}, with a 1 kΩ Pull-Up Resistor

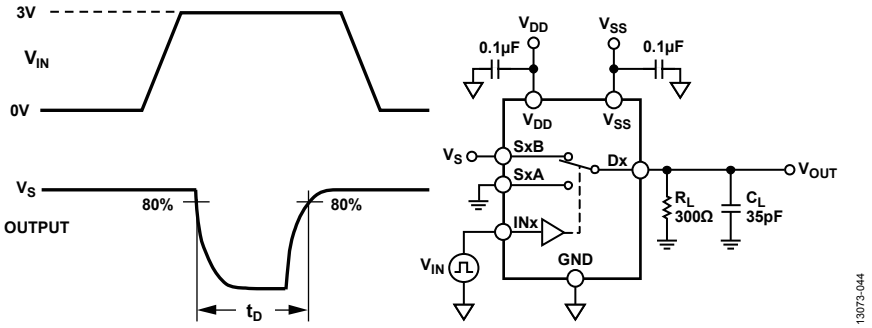


Figure 45. Break-Before-Make Time Delay, t_D

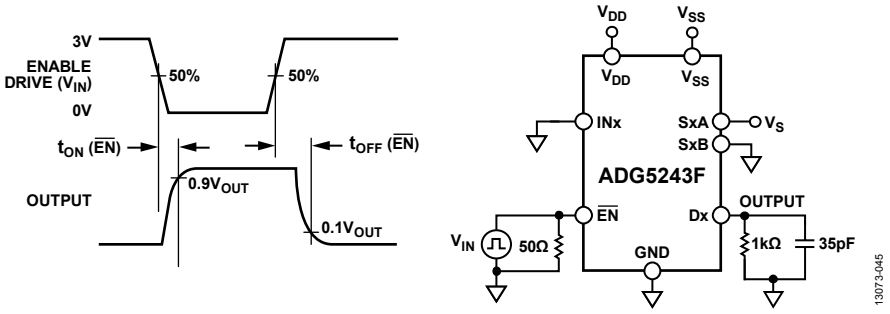


Figure 46. Enable Delay, t_{ON} ($\overline{EN}$), t_{OFF} ($\overline{EN}$)

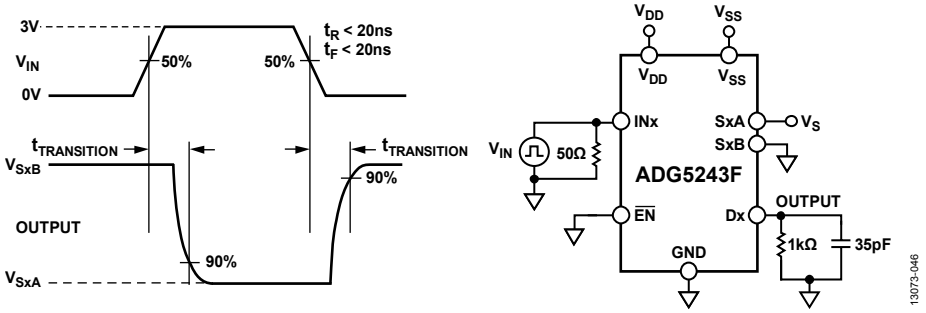


Figure 47.Digital Control Input to Output Switching Time, $t_{TRANSITION}$

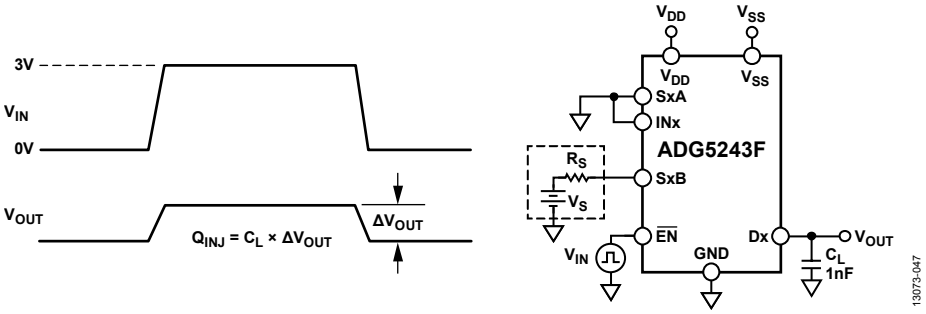


Figure 48. Charge Injection, Q_{INJ}

TERMINOLOGY

I_{DD}
I_{DD} represents the positive supply current.

I_{SS}
I_{SS} represents the negative supply current.

I_{POSFV}
I_{POSFV} represents the positive secondary supply current.

I_{NEGFV}
I_{NEGFV} represents the negative secondary supply current.

V_D
V_D represents the analog voltage on the Dx pins.

V_S
V_S represents the analog voltage on the Sx pins.

R_{ON}
R_{ON} represents the ohmic resistance between the Dx pins and the Sx pins.

ΔR_{ON}
ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$
$R_{FLAT(ON)}$ is the flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

I_S (Off)
I_S (off) is the source leakage current with the switch off.

I_D (Off)
I_D (off) is the drain leakage current with the switch off.

I_D (On), I_S (On)
I_D (on) and I_S (on) represent the channel leakage currents with the switch on.

V_{INL}
V_{INL} is the maximum input voltage for Logic 0.

V_{INH}
V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}
I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)
C_D (off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)
C_S (off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)
C_D (on) and C_S (on) represent the on switch capacitances, which are measured with reference to ground.

C_{IN}
C_{IN} is the digital input capacitance.

t_{ON} ($\overline{EN}$)
t_{ON} ($\overline{EN}$ represents the delay between applying the digital control input and the output switching on (see Figure 46).

t_{OFF} ($\overline{EN}$)
t_{OFF} ($\overline{EN}$) represents the delay between applying the digital control input and the output switching off (see Figure 46).

$t_{TRANSITION}$
$t_{TRANSITION}$ represents the delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one switch state to another.

t_D
t_D represents the off time measured between the 80% points of both switches when switching from one state to another.

$t_{DIGRESP}$
$t_{DIGRESP}$ is the time required for the FF pin to go low (0.3 V), measured with respect to the voltage on the source pin exceeding the supply voltage by 0.5 V.

t_{DIGREC}
t_{DIGREC} is the time required for the FF pin to return high, measured with respect to the voltage on the Sx pin falling below the supply voltage plus 0.5 V.

$t_{RESPONSE}$
$t_{RESPONSE}$ represents the delay between the source voltage exceeding the supply voltage by 0.5 V and the drain voltage falling to 90% of the supply voltage.

$t_{RESPONSE}$($\overline{EN}$)
$t_{RESPONSE}$ ($\overline{EN}$) represents the delay between the enable pin being asserted and the drain reaching 90% of POSFV or NEGFV for a switch that is in fault.

$t_{RECOVERY}$
$t_{RECOVERY}$ represents the delay between an overvoltage on a Sx pin falling below the supply voltage plus 0.5 V and the drain voltage rising from 0 V to 10% of the supply voltage.

Off Isolation
Off isolation is a measure of unwanted signal coupling through an off switch.

Charge Injection
Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Channel to Channel Crosstalk
Channel to channel crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Insertion Loss
Insertion loss is the loss due to the on resistance of the switch.

−3 dB Bandwidth
−3 dB bandwidth is the frequency at which the output is attenuated by 3 dB.

AC Power Supply Rejection Ratio (ACPSRR)
ACPSRR is the ratio of the amplitude of signal on the output to the amplitude of the modulation. ACPSRR is a measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

On Response
On response is the frequency response of the on switch.

V_T
V_T is the voltage threshold at which the overvoltage protection circuitry engages (see Figure 27).

Total Harmonic Distortion Plus Noise (THD + N)
THD + N is the ratio of the harmonic amplitude plus noise of the signal to the fundamental.

THEORY OF OPERATION

SWITCH ARCHITECTURE

Each channel of the ADG5243F consists of a parallel pair of N-channel diffused metal-oxide semiconductor (NDMOS) and P-channel DMOS (PDMOS) transistors. This construction provides excellent performance across the signal range. The ADG5243F channels operate as standard switches when input signals with a voltage between POSFV and NEGFV are applied. For example, the on resistance is 250 Ω typically and opening or closing the switch is controlled using the appropriate control pins.

Additional internal circuitry enables the switch to detect overvoltage inputs by comparing the voltage on a source pin with POSFV and NEGFV. A signal is considered overvoltage if it exceeds these secondary supply voltages by the voltage threshold, V_T. The threshold voltage is typically 0.7 V, but can range from 0.8 V at −40°C down to 0.6 V at +125°C. See Figure 27 to see the change in V_T with operating temperature.

The maximum voltage that can be applied to any source input is +55 V or −55 V. When the device is powered using a single supply of 25 V or greater, the maximum negative signal level is reduced. It reduces from −55 V at V_{DD} = +25 V to −40 V at V_{DD} = +40 V to remain within the 80 V maximum rating. Construction of the process allows the channel to withstand 80 V across the switch when it is opened. These overvoltage limits apply whether the power supplies are present or not.

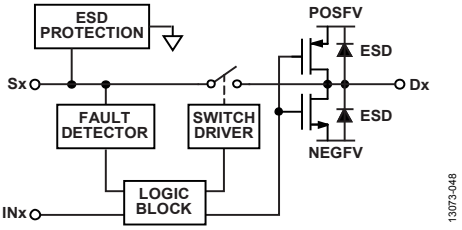


Figure 49. Switch Channel and Control Function

When an overvoltage condition is detected on a source pin (Sx), the switch automatically opens regardless of the digital logic state and the source pin becomes high impedance. If a source pin is selected that is in fault, the drain pin is pulled to the supply that was exceeded. For example, if the source voltage exceeds POSFV, the drain output pulls to POSFV. If the source voltage exceeds NEGFV, the drain output pulls to NEGFV. In Figure 28, the voltage on the drain pin can be seen to follow the voltage on the source pin until the switch turns off completely. The drain pin then pulls to GND due to the 1 kΩ load resistor; otherwise, it pulls to the POSFV supply. The maximum voltage on the drain is limited by the internal ESD diodes and the rate at which the output voltage discharges is dependent on the load at the pin.

During overvoltage conditions, the leakage current into and out of the source pins is limited to tens of microamperes. If the source pin is unselected, only nanoamperes of leakage appear on the drain pin. However, if the source is selected, the pin is pulled to the supply rail. The device that pulls the drain pin to the rail has an impedance of approximately 40 kΩ; thus, the Dx pin current is limited to approximately 1 mA during a shorted load condition. This internal impedance also determines the minimum external load resistance required to ensure that the drain pin is pulled to the desired voltage level during a fault.

When an overvoltage event occurs, the channels undisturbed by the overvoltage input continue to operate normally without additional crosstalk.

ESD Performance

The drain pins have ESD protection diodes to the secondary supply rails and the voltage at these pins must not exceed the secondary supply voltages, POSFV and NEGFV. The source pins have specialized ESD protection that allows the signal voltage to reach ±55 V regardless of supply voltage level. Exceeding ±55 V on any source input can damage the ESD protection circuitry on the device. See Figure 49 for an overview of the switch channel.

Trench Isolation

In the ADG5243F, an insulating oxide layer (trench) is placed between the NDMOS and the PDMOS transistors of each switch. Parasitic junctions, which occur between the transistors in junction-isolated switches, are eliminated, and the result is a switch that is latch-up immune under all circumstances. The device passes a JESD78D latch-up test of ±500 mA for 1 sec, which is the harshest test in the specification.

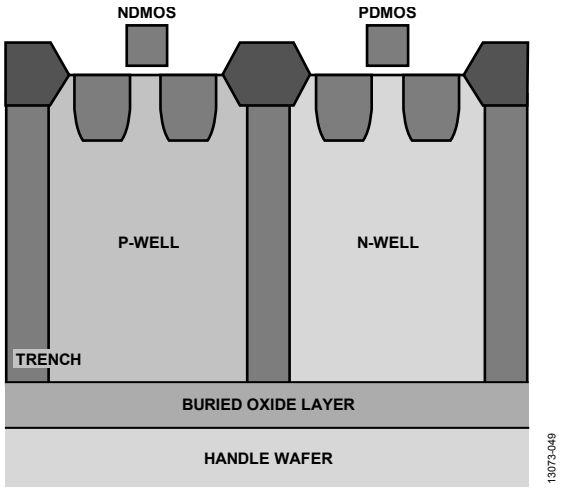


Figure 50. Trench Isolation

USER DEFINED FAULT PROTECTION

POSFV and NEGFV are required secondary power supplies that set the level at which the overvoltage protection is engaged. POSFV can be supplied from 4.5 V to V_{DD}, and NEGFV can be supplied from V_{SS} to 0 V. If a secondary supply is not available, connect these pins to V_{DD} (POSFV) and V_{SS} (NEGFV). The overvoltage protection then engages at the primary supply voltages. When the voltages at the source inputs exceed POSFV or NEGFV by V_T, the switch turns off or, if the device is unpowered, the switch remains off. The switch input remains high impedance regardless of the digital input state and if it is selected, the drain pulls to either POSFV or NEGFV. Signal levels up to +55 V and −55 V are blocked in both the powered and unpowered condition as long as the 80 V limitation between the source and supply pins is met.

Power-On Protection

The following conditions must be satisfied for the switch to be in the on condition:

- The primary supply must be V_{DD} to $V_{SS} \geq 8$ V.
- For POSFV, the secondary supply must be between 4.5 V and V_{DD}, and for NEGFV, the secondary supply must be between V_{SS} and 0 V.
- The input signal must be between NEGFV − V_T and POSFV + V_T.
- The digital logic control input has selected the switch.

When the switch is turned on, signal levels up to the secondary supply rails are passed.

The switch responds to an analog input that exceeds POSFV or NEGFV by a threshold voltage, V_T, by turning off. The absolute input voltage limits are −55 V and +55 V, while maintaining an 80 V limit between the source pin and the supply rails. The switch remains off until the voltage at the source pin returns to between POSFV and NEGFV.

The fault response time ($t_{RESPONSE}$) when powered by ±15 V dual supply is typically 90 ns and the fault recovery time ($t_{RECOVERY}$) is 745 ns. These vary with supply voltages and output load conditions.

The maximum stress across the switch channel is 80 V, therefore, the user must pay close attention to this limit under a fault condition.

For example, consider the case where the device is set up in a multiplexer configuration as shown in Figure 51.

- V_{DD}/V_{SS} and POSFV/NEGFV = ±22 V, S1A = S2B= +22 V, S1B = +55 V, and S2A = −55 V.
- S1A and S2A are selected.
- The voltage between S1B and D1 = +55 V − (22 V) = +33 V.
- The voltage between S2B and D2 = +22 V − (−55 V) = +77 V.

These calculations are all within device specifications: a 55 V maximum fault on the source inputs and a maximum of 80 V across the off switch channel.

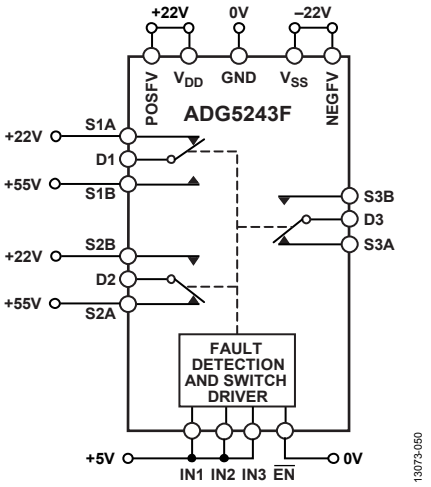


Figure 51. ADG5243F in an Overvoltage Condition

Power-Off Protection

When no power supplies are present, the switch remains in the off condition, and the switch inputs are high impedance. This state ensures that no current flows and prevents damage to the switch or downstream circuitry. The switch output is a virtual open circuit.

The switch remains off regardless of whether the V_{DD} and V_{SS} supplies are 0 V or floating. A GND reference must always be present to ensure proper operation. Signal levels of up to ±55 V are blocked in the unpowered condition.

Digital Input Protection

The ADG5243F can tolerate digital input signals being present on the device without power. When the device is unpowered, the switch is guaranteed to be in the off state, regardless of the state of the digital logic signals.

The digital inputs are protected against positive faults of up to 44 V. The digital inputs do not offer protection against negative overvoltages. ESD protection diodes connected to GND are present on the digital inputs.

Overvoltage Interrupt Flag

The voltages on the source inputs of the ADG5243F are continuously monitored, and the state of the switches is indicated by an active low digital output pin, FF.

The voltage on the FF pin indicates if any of the source input pins are experiencing a fault condition. The output of the FF pin is a nominal 3 V when all source pins are within normal operating range. If any source pin voltage exceeds the secondary supply voltage by V_T, the FF output reduces to below 0.4 V.

Use the specific fault digital output pin, SF, to decode which inputs are experiencing a fault condition. The SF pin reduces to below 0.4 V when a fault condition is detected on a specific pin, depending on the state of F0, F1, and F2 (see Table 9).

APPLICATIONS INFORMATION

The overvoltage protected family of switches and multiplexers provides robust solutions for instrumentation, industrial, automotive, aerospace, and other harsh environments where overvoltage signals can be present and the system must remain operational both during and after the overvoltage has occurred.

POWER SUPPLY RAILS

To guarantee correct operation of the device, 0.1 µF decoupling capacitors are required on the primary and secondary supplies. If they are driven from the same supply, one set of 0.1 µF decoupling capacitors is sufficient.

The secondary supplies (POSFV and NEGFV) provide the current required to operate the fault protection and, thus, must be low impedance supplies. Therefore, they can be derived from the primary supplies by using a resistor divider and buffer.

The secondary supply rails (POSFV and NEGFV) must not exceed the primary supply rails (V_{DD} and V_{SS}) because this can lead to a signal passing through the switch unintentionally.

The ADG5243F can operate with bipolar supplies between ±5 V and ±22 V. The supplies on V_{DD} and V_{SS} need not be symmetrical, but the V_{DD} to V_{SS} range must not exceed 44 V. The ADG5243F can also operate with single supplies between 8 V and 44 V with V_{SS} connected to GND.

The ADG5243F device is fully specified at ±15 V, ±20 V, +12 V, and +36 V supply ranges.

POWER SUPPLY SEQUENCING PROTECTION

The switch channel remains open when the device is unpowered and signals from −55 V to +55 V can be applied without damaging the device. The switch channel closes only when the supplies are connected, a suitable digital control signal is placed on the control pins, and the signal is within normal operating range. Placing the ADG5243F between external connectors and sensitive components offers protection in systems where a signal is presented to the source pins before the supply voltages are available.

SIGNAL RANGE

The primary supplies define the on-resistance profile of the channel, whereas the secondary supplies define the signal range. Using voltages on POSFV and NEGFV that are lower than V_{DD} and V_{SS}, the required signal can benefit from the flat on resistance in the center of the full signal capabilities of the device.

POWER SUPPLY RECOMMENDATIONS

Analog Devices, Inc., has a wide range of power management products to meet the requirements of most high performance signal chains.

An example of a bipolar power solution is shown in Figure 52. The ADP7118 and ADP7182 can be used to generate clean positive and negative rails from the ADP5070 dual switching regulator output. These rails can be used to power the ADG5243F, an amplifier, and/or a precision converter in a typical signal chain.

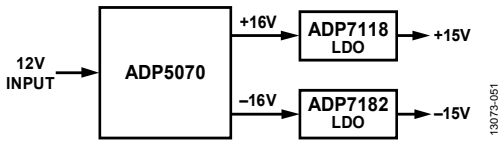


Figure 52. Bipolar Power Solution

Table 10. Recommended Power Management Devices

Product	Description
ADP5070	1 A/0.6 A, dc-to-dc switching regulator with independent positive and negative outputs
ADP7118	20 V, 200 mA, low noise, CMOS LDO
ADP7142	40 V, 200 mA, low noise, CMOS LDO
ADP7182	−28 V, −200 mA, low noise, linear regulator

HIGH VOLTAGE SURGE SUPPRESSION

The ADG5243F is not intended for use in very high voltage applications. The maximum operating voltage of the transistor is 80 V. In applications where the inputs are likely to be subject to overvoltages exceeding the breakdown voltage, use transient voltage suppressors (TVSs) or similar.

INTELLIGENT FAULT DETECTION

The ADG5243F digital output pin, FF, can interface with a microprocessor or control system and can be used as an interrupt flag. This feature provides real-time diagnostic information on the state of the device and the system to which it connects.

The control system can use the digital interrupt, FF, to start a variety of actions, as follows:

- Initiating an investigation into the source of an overvoltage fault.
- Shutting down critical systems in response to the overvoltage condition.
- Using data recorders to mark data during these events as unreliable or out of specification.

For systems that are sensitive during a start-up sequence, the active low operation of the flag allows the system to ensure that the ADG5243F is powered on and that all input voltages are within the normal operating range before initiating operation.

The FF pin has a weak internal pull-up resistor, which allows the signals to combine into a single interrupt for larger modules that contain multiple devices.

The recovery time, t_{DIGREC}, can be decreased from a typical 65 µs to 900 ns by using a 1 kΩ pull-up resistor.

The specific fault digital output, SF decodes which inputs are experiencing a fault condition. The SF pin reduces to below 0.4 V when a fault condition is detected on a specific pin, depending on the state of the F0, F1, and F2 pins (see Table 9).

LARGE VOLTAGE, HIGH FREQUENCY SIGNALS

Figure 30 illustrates the voltage range and frequencies that the ADG5243F can reliably convey. For signals that extend across the full signal range from V_{SS} to V_{DD}, keep the frequency below 1 MHz. If the required frequency is greater than 1 MHz, decrease the signal range appropriately to ensure signal integrity.

OUTLINE DIMENSIONS

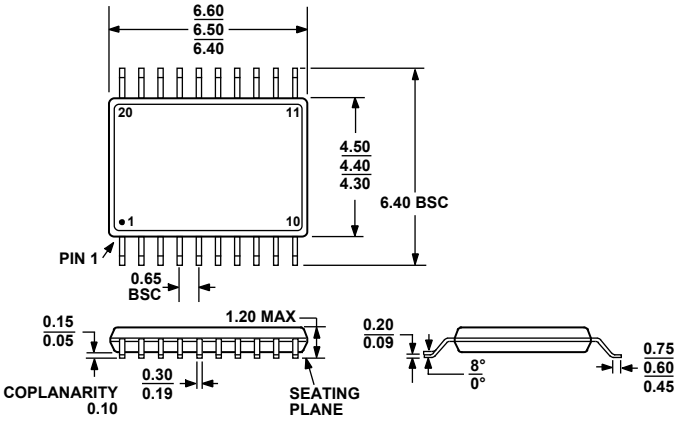


Figure 53. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters

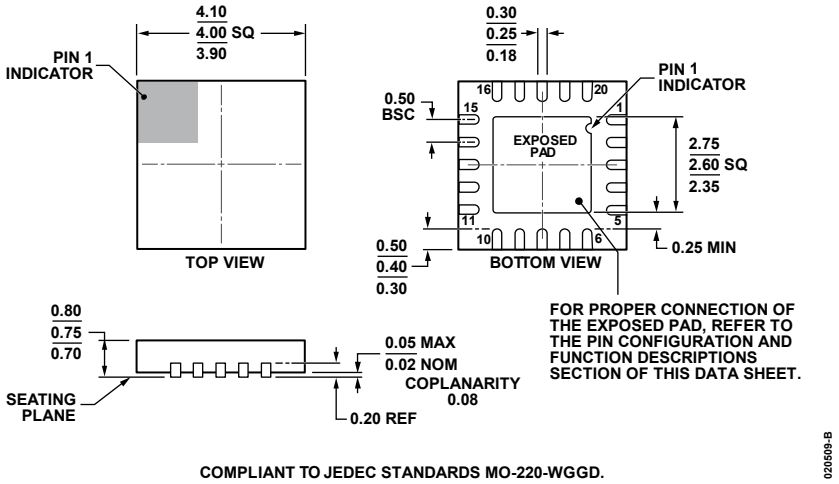


Figure 54. 20–Lead, Lead Frame Chip Scale Package [LFCSP]
4 mm x 4 mm Body and 0.75 mm Package Height
(CP-20-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADG5243FBCPZ-RL7	−40°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-8
ADG5243FBRUZ	−40°C to +125°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
ADG5243FBRUZ-RL7	−40°C to +125°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
EVAL-ADG5243FEBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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D13073-0-8/16(A)

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