



EFR32FG12 Gecko Proprietary Protocol SoC Family Data Sheet

The Gecko proprietary protocol family of SoCs is part of the Wireless Gecko portfolio. Gecko SoCs are ideal for enabling energy-friendly proprietary protocol networking for IoT devices.

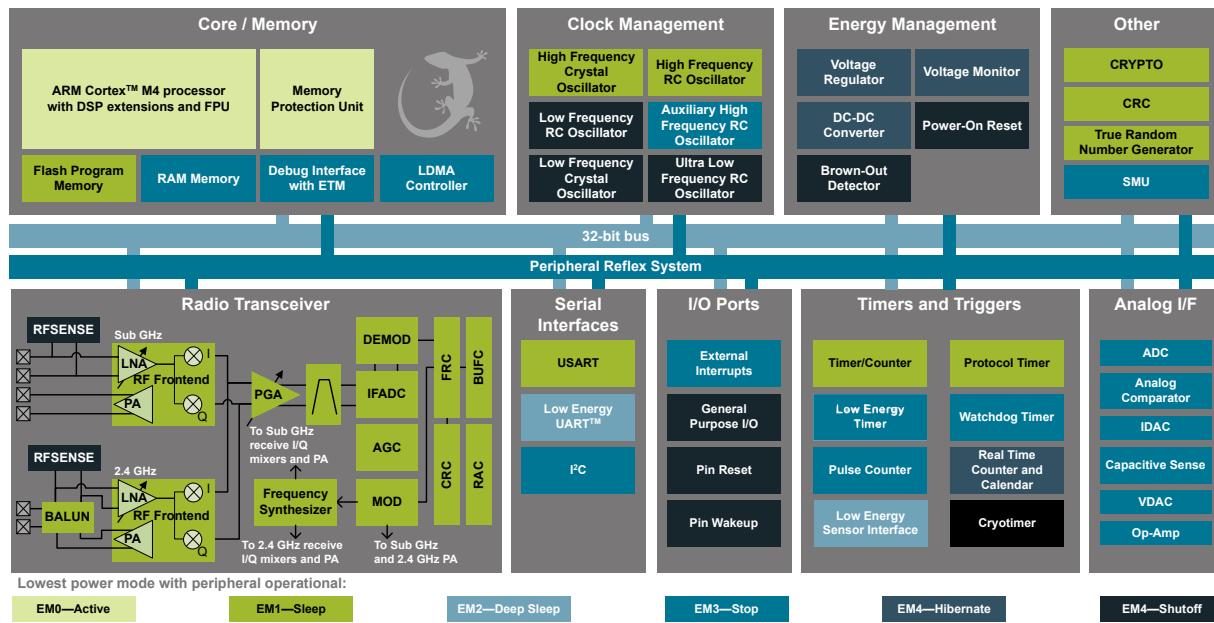
The single-die solution provides industry-leading energy efficiency, ultra-fast wakeup times, a scalable power amplifier, an integrated balun and no-compromise MCU features.

Gecko applications include:

- Home and Building Automation and Security
- Metering
- Electronic Shelf Labels
- Industrial Automation
- Commercial and Retail Lighting and Sensing

KEY FEATURES

- 32-bit ARM® Cortex®-M4 core with 40 MHz maximum operating frequency
- Up to 1 MB of flash and 256 kB of RAM
- Pin-compatible across EFR32FG families (exceptions apply for 5V-tolerant pins)
- 12-channel Peripheral Reflex System, Low-Energy Sensor Interface & Multi-channel Capacitive Sense Interface
- Autonomous Hardware Crypto Accelerator and True Random Number Generator
- Integrated PA with up to 19 dBm (2.4 GHz) or 20 dBm (Sub-GHz) TX power
- Integrated balun for 2.4 GHz
- Robust peripheral set and up to 65 GPIO



1. Feature List

The EFR32FG12 highlighted features are listed below.

• Low Power Wireless System-on-Chip

- High Performance 32-bit 40 MHz ARM Cortex®-M4 with DSP instruction and floating-point unit for efficient signal processing
- Embedded Trace Macrocell (ETM) for advanced debugging
- Up to 1024 kB flash program memory
- Up to 256 kB RAM data memory
- 2.4 GHz and Sub-GHz radio operation
- Transmit power:
 - 2.4 GHz radio: Up to 19 dBm
 - Sub-GHz radio: Up to 20 dBm

• Low Energy Consumption

- 8.4 mA RX current at 38.4 kbps, GFSK, 169 MHz
- 10.0 mA RX current at 1 Mbps, GFSK, 2.4 GHz
- 11 mA RX current at 250 kbps, DSSS-OQPSK, 2.4 GHz
- 8.5 mA TX current at 0 dBm output power at 2.4 GHz
- 35.3 mA TX current at 14 dBm output power at 868 MHz
- 70 μ A/MHz in Active Mode (EM0)
- 1.5 μ A EM2 DeepSleep current (16 kB RAM retention and RTCC running from LFRCO)

• High Receiver Performance

- -94.8 dBm sensitivity at 1 Mbit/s GFSK, 2.4 GHz
- -102.7 dBm sensitivity at 250 kbps DSSS-OQPSK, 2.4 GHz
- -126.2 dBm sensitivity at 600 bps, GFSK, 915 MHz
- -120.6 dBm sensitivity at 2.4 kbps, GFSK, 868 MHz
- -107.4 dBm sensitivity at 4.8 kbps, OOK, 433 MHz
- -112.2 dBm sensitivity at 38.4 kbps, GFSK, 169 MHz

• Supported Modulation Formats

- 2/4 (G)FSK with fully configurable shaping
- BPSK / DBPSK TX
- OOK / ASK
- Shaped OQPSK / (G)MSK
- Configurable DSSS and FEC

• Supported Protocols

- Proprietary Protocols
- Wireless M-Bus
- Selected IEEE 802.15.4g SUN-FSK PHYs
- Low Power Wide Area Networks

• Suitable for Systems Targeting Compliance With:

- FCC Part 90.210 Mask D, FCC part 15.247, 15.231, 15.249
- ETSI Category I Operation, EN 300 220, EN 300 328
- ARIB T-108, T-96
- China regulatory

• Wide selection of MCU peripherals

- 12-bit 1 Msps SAR Analog to Digital Converter (ADC)
- 2 × Analog Comparator (ACMP)
- 2 × Digital to Analog Converter (VDAC)
- 3 × Operational Amplifier (Opamp)
- Digital to Analog Current Converter (IDAC)
- Low-Energy Sensor Interface (LESENSE)
- Multi-channel Capacitive Sense Interface (CSEN)
- Up to 54 pins connected to analog channels (APORT) shared between analog peripherals
- Up to 65 General Purpose I/O pins with output state retention and asynchronous interrupts
- 8 Channel DMA Controller
- 12 Channel Peripheral Reflex System (PRS)
- 2 × 16-bit Timer/Counter
 - 3 or 4 Compare/Capture/PWM channels
- 2 × 32-bit Timer/Counter
 - 3 or 4 Compare/Capture/PWM channels
- 32-bit Real Time Counter and Calendar
- 16-bit Low Energy Timer for waveform generation
- 32-bit Ultra Low Energy Timer/Counter for periodic wake-up from any Energy Mode
- 3 × 16-bit Pulse Counter with asynchronous operation
- 2 × Watchdog Timer with dedicated RC oscillator
- 4 × Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I²S)
- Low Energy UART (LEUART™)
- 2 × I²C interface with SMBus support and address recognition in EM3 Stop

• Wide Operating Range

- 1.8 V to 3.8 V single power supply
- Integrated DC-DC, down to 1.8 V output with up to 200 mA load current for system
- Standard (-40 °C to 85 °C) and Extended (-40 °C to 125 °C) temperature grades available

• Support for Internet Security

- General Purpose CRC
- True Random Number Generator
- 2 × Hardware Cryptographic Acceleration for AES 128/256, SHA-1, SHA-2 (SHA-224 and SHA-256) and ECC
- **QFN48 7x7 mm Package**
- **QFN68 8x8 mm Package**
- **BGA125 7x7 mm Package**

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Protocol Stack	Frequency Band @ Max TX Power	Flash (kB)	RAM (kB)	GPIO	Package	Temp Range
EFR32FG12P433F1024GL125-C	Proprietary	2.4 GHz @ 19 dBm Sub-GHz @ 20 dBm	1024	256	65	BGA125	-40 to +85°C
EFR32FG12P433F1024GM68-C	Proprietary	2.4 GHz @ 19 dBm Sub-GHz @ 20 dBm	1024	256	46	QFN68	-40 to +85°C
EFR32FG12P433F1024GM48-C	Proprietary	2.4 GHz @ 19 dBm Sub-GHz @ 20 dBm	1024	256	28	QFN48	-40 to +85°C
EFR32FG12P432F1024GL125-C	Proprietary	2.4 GHz @ 19 dBm	1024	256	65	BGA125	-40 to +85°C
EFR32FG12P432F1024GM48-C	Proprietary	2.4 GHz @ 19 dBm	1024	256	31	QFN48	-40 to +85°C
EFR32FG12P431F1024GL125-C	Proprietary	Sub-GHz @ 20 dBm	1024	256	65	BGA125	-40 to +85°C
EFR32FG12P431F1024GM68-C	Proprietary	Sub-GHz @ 20 dBm	1024	256	46	QFN68	-40 to +85°C
EFR32FG12P431F512GM68-C	Proprietary	Sub-GHz @ 20 dBm	512	128	46	QFN68	-40 to +85°C
EFR32FG12P431F1024GM48-C	Proprietary	Sub-GHz @ 20 dBm	1024	256	31	QFN48	-40 to +85°C
EFR32FG12P431F1024IM48-C	Proprietary	Sub-GHz @ 20 dBm	1024	256	31	QFN48	-40 to +125°C
EFR32FG12P232F1024GL125-C	Proprietary	2.4 GHz @ 19 dBm	1024	128	65	BGA125	-40 to +85°C
EFR32FG12P232F1024GM48-C	Proprietary	2.4 GHz @ 19 dBm	1024	128	31	QFN48	-40 to +85°C
EFR32FG12P231F1024GL125-C	Proprietary	Sub-GHz @ 20 dBm	1024	128	65	BGA125	-40 to +85°C
EFR32FG12P231F1024GM68-C	Proprietary	Sub-GHz @ 20 dBm	1024	128	46	QFN68	-40 to +85°C
EFR32FG12P231F512GM68-C	Proprietary	Sub-GHz @ 20 dBm	512	64	46	QFN68	-40 to +85°C
EFR32FG12P231F1024GM48-C	Proprietary	Sub-GHz @ 20 dBm	1024	128	31	QFN48	-40 to +85°C

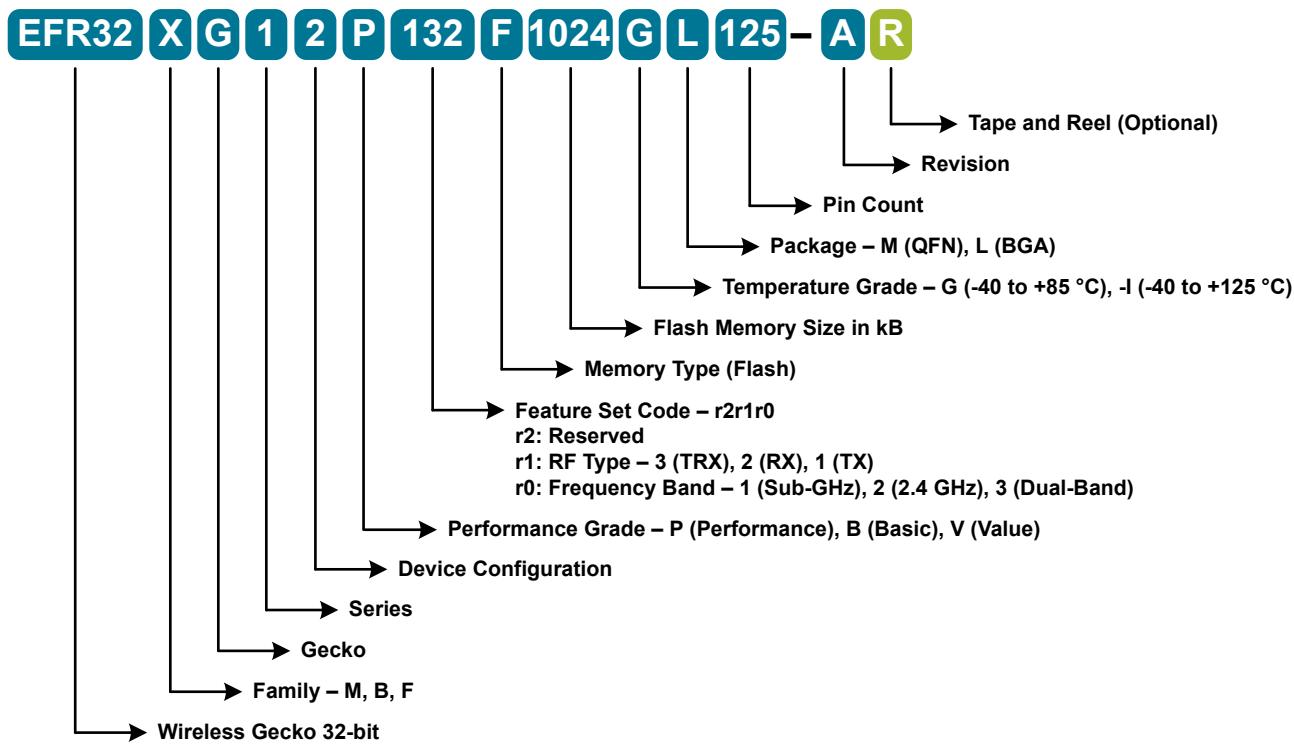


Figure 2.1. Ordering Code Key

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3. System Overview

3.1 Introduction

The EFR32 product family combines an energy-friendly MCU with a highly integrated radio transceiver. The devices are well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the full radio and MCU system. The detailed functional description can be found in the EFR32xG12 Wireless Gecko Reference Manual.

A block diagram of the EFR32FG12 family is shown in [Figure 3.1 Detailed EFR32FG12 Block Diagram on page 8](#). The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult [Ordering Information](#).

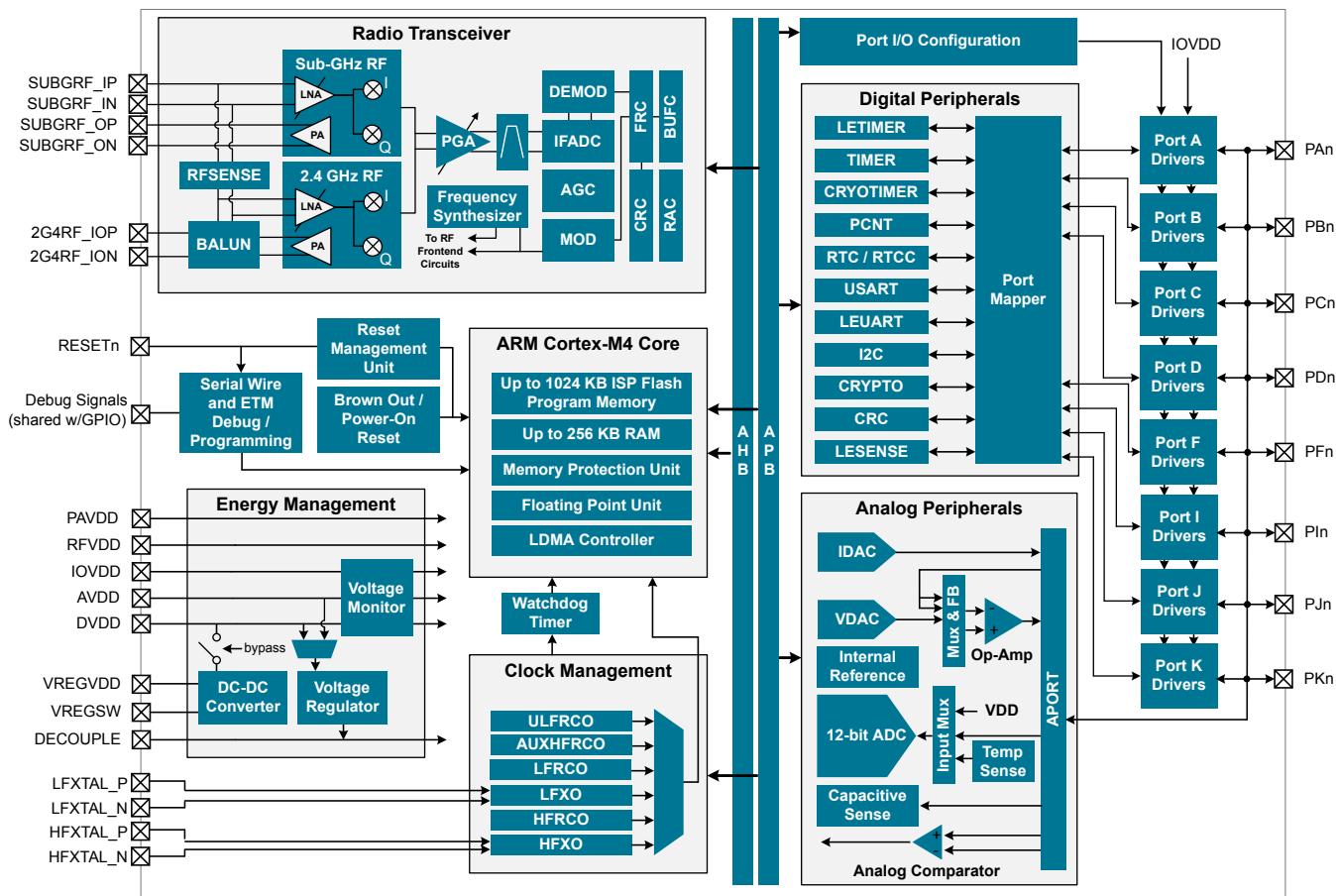


Figure 3.1. Detailed EFR32FG12 Block Diagram

3.2 Radio

The Gecko family features a radio transceiver supporting proprietary wireless protocols.

3.2.1 Antenna Interface

The 2.4 GHz antenna interface consists of two pins (2G4RF_IOP and 2G4RF_ION) that interface directly to the on-chip BALUN. The 2G4RF_ION pin should be grounded externally.

The external components and power supply connections for the antenna interface typical applications are shown in the RF Matching Networks section.

3.2.2 Fractional-N Frequency Synthesizer

The EFR32FG12 contains a high performance, low phase noise, fully integrated fractional-N frequency synthesizer. The synthesizer is used in receive mode to generate the LO frequency used by the down-conversion mixer. It is also used in transmit mode to directly generate the modulated RF carrier.

The fractional-N architecture provides excellent phase noise performance combined with frequency resolution better than 100 Hz, with low energy consumption. The synthesizer has fast frequency settling which allows very short receiver and transmitter wake up times to optimize system energy consumption.

3.2.3 Receiver Architecture

The EFR32FG12 uses a low-IF receiver architecture, consisting of a Low-Noise Amplifier (LNA) followed by an I/Q down-conversion mixer, employing a crystal reference. The I/Q signals are further filtered and amplified before being sampled by the IF analog-to-digital converter (IFADC).

The IF frequency is configurable from 150 kHz to 1371 kHz. The IF can further be configured for high-side or low-side injection, providing flexibility with respect to known interferers at the image frequency.

The Automatic Gain Control (AGC) block adjusts the receiver gain to optimize performance and avoid saturation for excellent selectivity and blocking performance. The 2.4 GHz radio is calibrated at production to improve image rejection performance. The sub-GHz radio can be calibrated on-demand by the user for the desired frequency band.

Demodulation is performed in the digital domain. The demodulator performs configurable decimation and channel filtering to allow receive bandwidths ranging from 0.1 to 2530 kHz. High carrier frequency and baud rate offsets are tolerated by active estimation and compensation. Advanced features supporting high quality communication under adverse conditions include forward error correction by block and convolutional coding as well as Direct Sequence Spread Spectrum (DSSS) for 2.4 GHz and sub-GHz bands.

A Received Signal Strength Indicator (RSSI) is available for signal quality metrics, for level-based proximity detection, and for RF channel access by Collision Avoidance (CA) or Listen Before Talk (LBT) algorithms. An RSSI capture value is associated with each received frame and the dynamic RSSI measurement can be monitored throughout reception.

The EFR32FG12 features integrated support for antenna diversity to mitigate the problem of frequency-selective fading due to multipath propagation and improve link budget. Support for antenna diversity is available for specific PHY configurations in 2.4 GHz and sub-GHz bands. Internal configurable hardware controls an external switch for automatic switching between antennae during RF receive detection operations.

Note: Due to the shorter preamble of 802.15.4 and BLE packets, RX diversity is not supported.

3.2.4 Transmitter Architecture

The EFR32FG12 uses a direct-conversion transmitter architecture. For constant envelope modulation formats, the modulator controls phase and frequency modulation in the frequency synthesizer. Transmit symbols or chips are optionally shaped by a digital shaping filter. The shaping filter is fully configurable, including the BT product, and can be used to implement Gaussian or Raised Cosine shaping.

Carrier Sense Multiple Access - Collision Avoidance (CSMA-CA) or Listen Before Talk (LBT) algorithms can be automatically timed by the EFR32FG12. These algorithms are typically defined by regulatory standards to improve inter-operability in a given bandwidth between devices that otherwise lack synchronized RF channel access.

3.2.5 Wake on Radio

The Wake on Radio feature allows flexible, autonomous RF sensing, qualification, and demodulation without required MCU activity, using a subsystem of the EFR32FG12 including the Radio Controller (RAC), Peripheral Reflex System (PRS), and Low Energy peripherals.

3.2.6 RFSENSE

The RFSENSE peripheral generates a system wakeup interrupt upon detection of wideband RF energy at the antenna interface, providing true RF wakeup capabilities from low energy modes including EM2, EM3 and EM4.

RFSENSE triggers on a relatively strong RF signal and is available in the lowest energy modes, allowing exceptionally low energy consumption. RFSENSE does not demodulate or otherwise qualify the received signal, but software may respond to the wakeup event by enabling normal RF reception.

Various strategies for optimizing power consumption and system response time in presence of false alarms may be employed using available timer peripherals.

3.2.7 Flexible Frame Handling

EFR32FG12 has an extensive and flexible frame handling support for easy implementation of even complex communication protocols. The Frame Controller (FRC) supports all low level and timing critical tasks together with the Radio Controller and Modulator/Demodulator:

- Highly adjustable preamble length
- Up to 2 simultaneous synchronization words, each up to 32 bits and providing separate interrupts
- Frame disassembly and address matching (filtering) to accept or reject frames
- Automatic ACK frame assembly and transmission
- Fully flexible CRC generation and verification:
 - Multiple CRC values can be embedded in a single frame
 - 8, 16, 24 or 32-bit CRC value
 - Configurable CRC bit and byte ordering
- Selectable bit-ordering (least significant or most significant bit first)
- Optional data whitening
- Optional Forward Error Correction (FEC), including convolutional encoding / decoding and block encoding / decoding
- Half rate convolutional encoder and decoder with constraint lengths from 2 to 7 and optional puncturing
- Optional symbol interleaving, typically used in combination with FEC
- Symbol coding, such as Manchester or DSSS, or biphase space encoding using FEC hardware
- UART encoding over air, with start and stop bit insertion / removal
- Test mode support, such as modulated or unmodulated carrier output
- Received frame timestamping

3.2.8 Packet and State Trace

The EFR32FG12 Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data and state information
- Data observability on a single-pin UART data output, or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data and state / meta information in a single serial data stream

3.2.9 Data Buffering

The EFR32FG12 features an advanced Radio Buffer Controller (BUFC) capable of handling up to 4 buffers of adjustable size from 64 bytes to 4096 bytes. Each buffer can be used for RX, TX or both. The buffer data is located in RAM, enabling zero-copy operations.

3.2.10 Radio Controller (RAC)

The Radio Controller controls the top level state of the radio subsystem in the EFR32FG12. It performs the following tasks:

- Precisely-timed control of enabling and disabling of the receiver and transmitter circuitry
- Run-time calibration of receiver, transmitter and frequency synthesizer
- Detailed frame transmission timing, including optional LBT or CSMA-CA

3.2.11 Random Number Generator

The Frame Controller (FRC) implements a random number generator that uses entropy gathered from noise in the RF receive chain. The data is suitable for use in cryptographic applications.

Output from the random number generator can be used either directly or as a seed or entropy source for software-based random number generator algorithms such as Fortuna.

3.3 Power

The EFR32FG12 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFR32FG12 device family includes support for internal supply voltage scaling, as well as two different power domains groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

AVDD and VREGVDD need to be 1.8 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.3.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.3.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Patented RF noise mitigation allows operation of the DC-DC converter without degrading sensitivity of radio components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.3.3 Power Domains

The EFR32FG12 has two peripheral power domains for operation in EM2 and lower. If all of the peripherals in a peripheral power domain are configured as unused, the power domain for that group will be powered off in the low-power mode, reducing the overall current consumption of the device.

Table 3.1. Peripheral Power Subdomains

Peripheral Power Domain 1	Peripheral Power Domain 2
ACMP0	ACMP1
PCNT0	PCNT1
ADC0	PCNT2
LETIMERO0	CSEN
LESENSE	DAC0
APORT	LEUART0
-	I2C0
-	I2C1
-	IDAC

3.4 General Purpose Input/Output (GPIO)

EFR32FG12 has up to 65 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.5 Clocking

3.5.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFR32FG12. Individual enabling and disabling of clocks to all peripherals is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.5.2 Internal and External Oscillators

The EFR32FG12 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 38 to 40 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range.
- An integrated auxiliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire Viewer port with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.6 Counters/Timers and PWM

3.6.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.6.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER_0 only.

3.6.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. When receiving frames, the RTCC value can be used for timestamping. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes down to EM4H.

3.6.4 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.6.5 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.6.6 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The peripheral may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.6.7 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.7 Communications and Other Digital Peripherals

3.7.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O interface. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I²S

3.7.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUARTTM provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.7.3 Inter-Integrated Circuit Interface (I²C)

The I²C interface enables communication between the MCU and a serial I²C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I²C peripheral allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.7.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripherals without software involvement. Peripherals producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals, which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.7.5 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSE™ is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

3.8 Security Features

3.8.1 General Purpose Cyclic Redundancy Check (GPCRC)

The GPCRC block implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.8.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. EFR32 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2^m), SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO1 block is tightly linked to the Radio Buffer Controller (BUFC) enabling fast and efficient autonomous cipher operations on data buffer content. It allows fast processing of GCM (AES), ECC and SHA with little CPU intervention.

CRYPTO also provides trigger signals for DMA read and write operations.

3.8.3 True Random Number Generator (TRNG)

The TRNG is a non-deterministic random number generator based on a full hardware solution. The TRNG is validated with NIST800-22 and AIS-31 test suites as well as being suitable for FIPS 140-2 certification (for the purposes of cryptographic key generation).

Note: TRNG operation is only supported at VSCALE2. TRNG cannot be used at VSCALE0.

3.8.4 Security Management Unit (SMU)

The Security Management Unit (SMU) allows software to set up fine-grained security for peripheral access, which is not possible in the Memory Protection Unit (MPU). Peripherals may be secured by hardware on an individual basis, such that only privileged accesses to the peripheral's register interface will be allowed. When an access fault occurs, the SMU reports the specific peripheral involved and can optionally generate an interrupt.

3.9 Analog

3.9.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog peripherals on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.9.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.9.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.9.4 Capacitive Sense (CSEN)

The CSEN peripheral is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such as switches and sliders. The CSEN peripheral uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The peripheral can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

3.9.5 Digital to Analog Current Converter (IDAC)

The IDAC can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The full-scale current is programmable between 0.05 μ A and 64 μ A with several ranges consisting of various step sizes.

3.9.6 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per single-ended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.9.7 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC peripheral or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

3.10 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFR32FG12. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.11 Core and Memory

3.11.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4 RISC processor achieving 1.25 Dhystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Up to 1024 kB flash program memory
- Up to 256 kB RAM data memory
- Configuration and event handling of all peripherals
- 2-pin Serial-Wire debug interface

3.11.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.11.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.12 Memory Map

The EFR32FG12 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

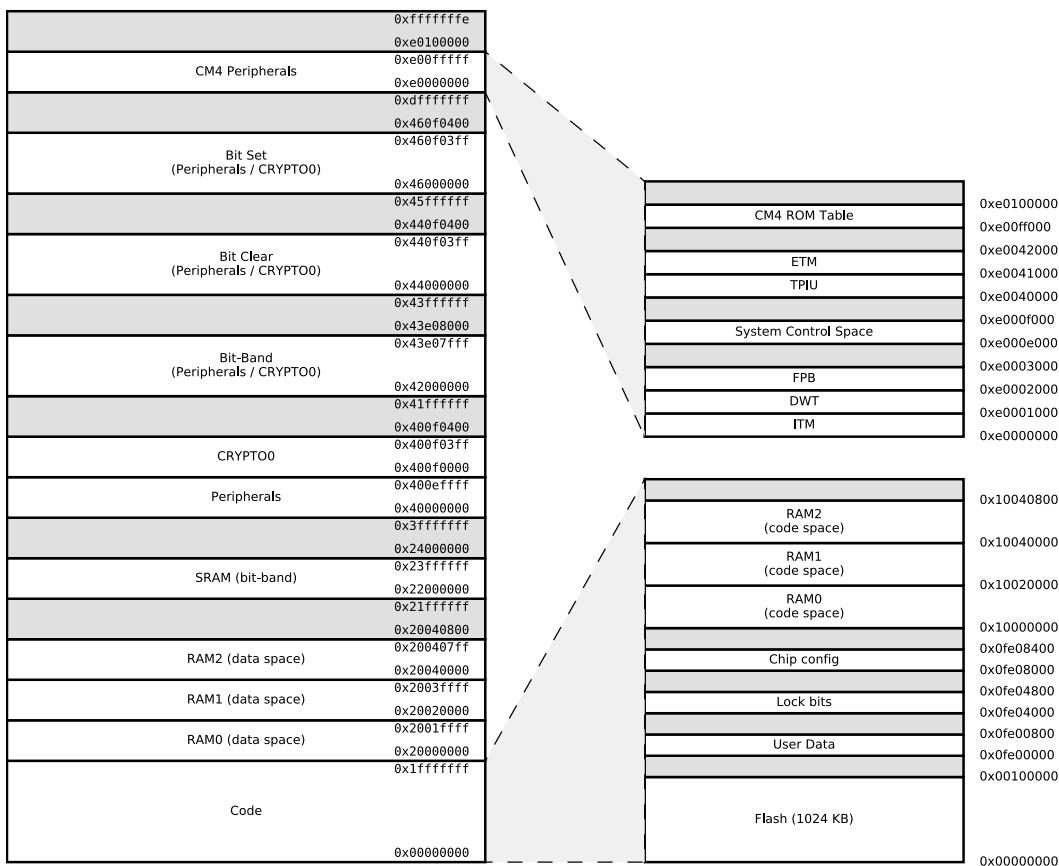


Figure 3.2. EFR32FG12 Memory Map — Core Peripherals and Code Space

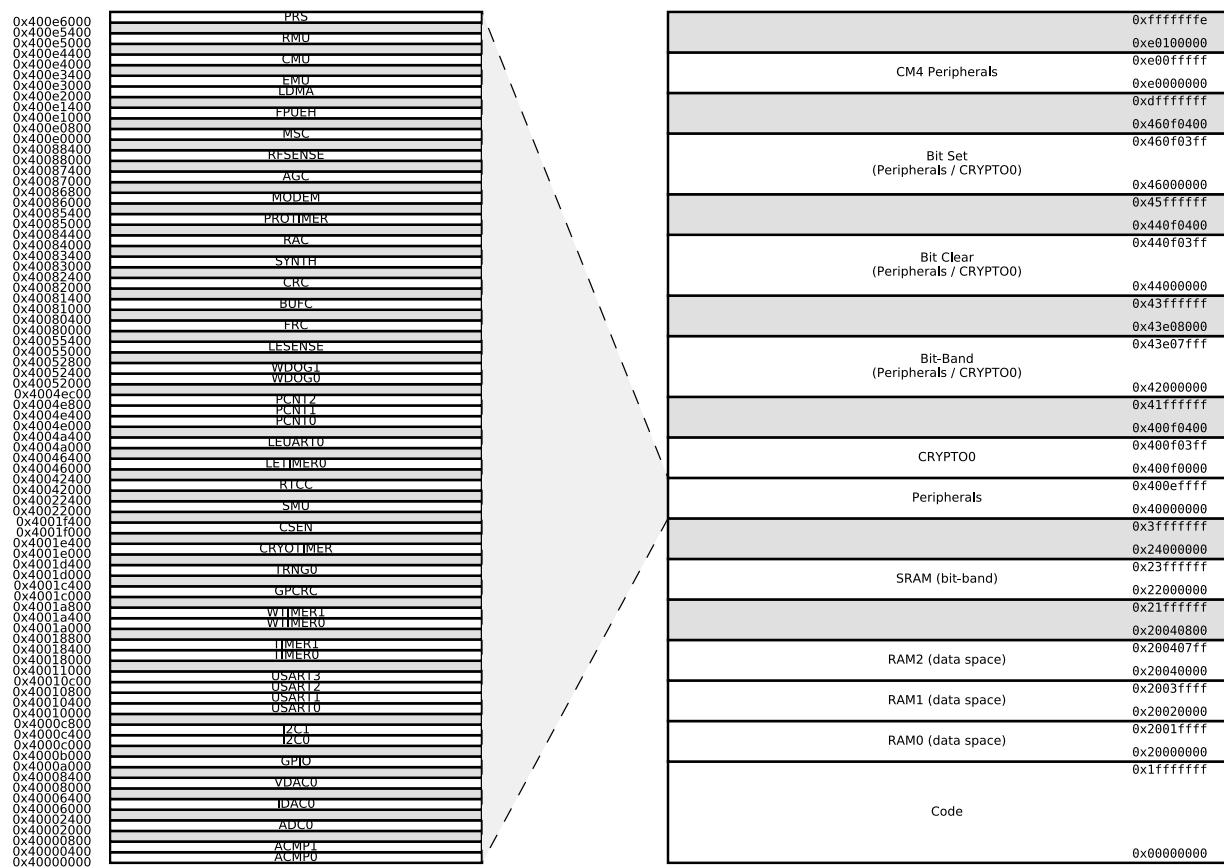


Figure 3.3. EFR32FG12 Memory Map — Peripherals

3.13 Configuration Summary

The features of the EFR32FG12 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.2. Configuration Summary

Module	Configuration	Pin Connections
USART0	IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
	SmartCard	
USART1	I ² S	US1_TX, US1_RX, US1_CLK, US1_CS
	SmartCard	
USART2	IrDA	US2_TX, US2_RX, US2_CLK, US2_CS
	SmartCard	
USART3	I ² S	US3_TX, US3_RX, US3_CLK, US3_CS
	SmartCard	
TIMER0	with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	-	TIM1_CC[3:0]
WTIMER0	with DTI	WTIM0_CC[2:0], WTIM0_CDTI[2:0]
WTIMER1	-	WTIM1_CC[3:0]

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on $T_{AMB}=25\text{ }^{\circ}\text{C}$ and $V_{DD}=3.3\text{ V}$, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a $50\text{ }\Omega$ antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Refer to [4.1.2.1 General Operating Conditions](#) for more details about operational supply and temperature limits.

4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T _{STG}		-50	—	150	°C
Voltage on any supply pin	V _{DDMAX}		-0.3	—	3.8	V
Voltage ramp rate on any supply pin	V _{DDRAMPMAX}		—	—	1	V / μ s
DC voltage on any GPIO pin	V _{DIGPIN}	5V tolerant GPIO pins ^{1 2 3}	-0.3	—	Min of 5.25 and IOVDD +2	V
		Standard GPIO pins	-0.3	—	IOVDD+0.3	V
Voltage on HFXO pins	V _{HFXOPIN}		-0.3	—	1.4	V
Input RF level on pins 2G4RF_IOP and 2G4RF_ION	P _{RFMAX2G4}		—	—	10	dBm
Voltage differential between RF pins (2G4RF_IOP - 2G4RF_ION)	V _{MAXDIFF2G4}		-50	—	50	mV
Absolute voltage on RF pins 2G4RF_IOP and 2G4RF_ION	V _{MAX2G4}		-0.3	—	3.8	V
Absolute voltage on Sub-GHz RF pins	V _{MAXSUBG}	Pins SUBGRF_OP and SUBGRF_ON	-0.3	—	3.8	V
		Pins SUBGRF_IP and SUBGRF_IN,	-0.3	—	0.3	V
Total current into VDD power lines	I _{VDDMAX}	Source	—	—	200	mA
Total current into VSS ground lines	I _{VSSMAX}	Sink	—	—	200	mA
Current per I/O pin	I _{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	I _{IOALLMAX}	Sink	—	—	200	mA
		Source	—	—	200	mA
Junction temperature	T _J	-G grade devices	-40	—	105	°C
		-I grade devices	-40	—	125	°C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note:						
1. When a GPIO pin is routed to the analog block through the APOR						

4.1.2 Operating Conditions

When assigning supply sources, the following requirements must be observed:

- VREGVDD must be greater than or equal to AVDD, DVDD, RFVDD, PAVDD and all IOVDD supplies.
- VREGVDD = AVDD
- DVDD \leq AVDD
- IOVDD \leq AVDD
- RFVDD \leq AVDD
- PAVDD \leq AVDD

4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range ¹	T _A	-G temperature grade	-40	25	85	°C
		-I temperature grade	-40	25	125	°C
AVDD supply voltage ²	V _{AVDD}		1.8	3.3	3.8	V
VREGVDD operating supply voltage ^{2,3}	V _{VREGVDD}	DCDC in regulation	2.4	3.3	3.8	V
		DCDC in bypass, 50mA load	1.8	3.3	3.8	V
		DCDC not in use. DVDD externally shorted to VREGVDD	1.8	3.3	3.8	V
VREGVDD current	I _{VREGVDD}	DCDC in bypass, T ≤ 85 °C	—	—	200	mA
		DCDC in bypass, T > 85 °C	—	—	100	mA
RFVDD operating supply voltage	V _{RFVDD}		1.62	—	V _{VREGVDD}	V
DVDD operating supply voltage	V _{DVDD}		1.62	—	V _{VREGVDD}	V
PAVDD operating supply voltage	V _{PAVDD}		1.62	—	V _{VREGVDD}	V
IOVDD operating supply voltage	V _{IOVDD}	All IOVDD pins ⁴	1.62	—	V _{VREGVDD}	V
DECOPPLE output capacitor ^{5,6}	C _{DECOPPLE}		0.75	1.0	2.75	μF
Difference between AVDD and VREGVDD, ABS(AVDD-VREGVDD) ²	dV _{DD}		—	—	0.1	V
HFCORECLK frequency	f _{CORE}	VSCALE2, MODE = WS1	—	—	40	MHz
		VSCALE2, MODE = WS0	—	—	25	MHz
		VSCALE0, MODE = WS2	—	—	20	MHz
		VSCALE0, MODE = WS1	—	—	14	MHz
		VSCALE0, MODE = WS0	—	—	7	MHz
HFCLK frequency	f _{HFCLK}	VSCALE2	—	—	40	MHz
		VSCALE0	—	—	20	MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note:						
1.		The maximum limit on T_A may be lower due to device self-heating, which depends on the power dissipation of the specific application. T_A (max) = T_J (max) - (θ_{JA} x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_J and θ_{JA} .				
2.		VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate.				
3.		The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as $V_{DVDD_min} + I_{LOAD} * R_{BYP_max}$.				
4.		When the CSEN peripheral is used with chopping enabled (CSEN_CTRL_CHOPEN = ENABLE), IOVDD must be equal to AVDD.				
5.		The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias.				
6.		VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV / usec for approximately 20 usec. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 μ F capacitor) to 70 mA (with a 2.7 μ F capacitor).				

4.1.3 Thermal Characteristics

Table 4.3. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal resistance, QFN48 Package	θ_{JA_QFN48}	2-Layer PCB, Air velocity = 0 m/s	—	75.7	—	°C/W
		2-Layer PCB, Air velocity = 1 m/s	—	61.5	—	°C/W
		2-Layer PCB, Air velocity = 2 m/s	—	55.4	—	°C/W
		4-Layer PCB, Air velocity = 0 m/s	—	30.2	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	26.3	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	24.9	—	°C/W
Thermal resistance, BGA125 Package	θ_{JA_BGA125}	2-Layer PCB, Air velocity = 0 m/s	—	90.7	—	°C/W
		2-Layer PCB, Air velocity = 1 m/s	—	73.7	—	°C/W
		2-Layer PCB, Air velocity = 2 m/s	—	66.4	—	°C/W
		4-Layer PCB, Air velocity = 0 m/s	—	45	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	39.6	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	37.6	—	°C/W
Thermal resistance, QFN68 Package	θ_{JA_QFN68}	4-Layer PCB, Air velocity = 0 m/s	—	21.5	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	18.9	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	17.1	—	°C/W

4.1.4 DC-DC Converter

Test conditions: L_DCDC=4.7 μ H (Murata LQH3NPN4R7MM0L), C_DCDC=4.7 μ F (Samsung CL10B475KQ8NQNC), V_DCDC_I=3.3 V, V_DCDC_O=1.8 V, I_DCDC_LOAD=50 mA, Heavy Drive configuration, F_DCDC_LN=7 MHz, unless otherwise indicated.

Table 4.4. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V _{DCDC_I}	Bypass mode, I _{DCDC_LOAD} = 50 mA	1.8	—	V _{VREGVDD_MAX}	V
		Low noise (LN) mode, 1.8 V output, I _{DCDC_LOAD} = 100 mA, or Low power (LP) mode, 1.8 V output, I _{DCDC_LOAD} = 10 mA	2.4	—	V _{VREGVDD_MAX}	V
		Low noise (LN) mode, 1.8 V output, I _{DCDC_LOAD} = 200 mA	2.6	—	V _{VREGVDD_MAX}	V
Output voltage programmable range ¹	V _{DCDC_O}		1.8	—	V _{VREGVDD}	V
Regulation DC accuracy	ACC _{DC}	Low Noise (LN) mode, 1.8 V target output	1.7	—	1.9	V
Regulation window ²	WIN _{REG}	Low Power (LP) mode, LPCMPBIASEMxx ³ = 0, 1.8 V target output, I _{DCDC_LOAD} \leq 75 μ A	1.63	—	2.2	V
		Low Power (LP) mode, LPCMPBIASEMxx ³ = 3, 1.8 V target output, I _{DCDC_LOAD} \leq 10 mA	1.63	—	2.1	V
Steady-state output ripple	V _R	Radio disabled	—	3	—	mVpp
Output voltage under/overshoot	V _{ov}	CCM Mode (LNFORCECCM ³ = 1), Load changes between 0 mA and 100 mA	—	25	60	mV
		DCM Mode (LNFORCECCM ³ = 0), Load changes between 0 mA and 10 mA	—	45	90	mV
		Overshoot during LP to LN CCM/DCM mode transitions compared to DC level in LN mode	—	200	—	mV
		Undershoot during BYP/LP to LN CCM (LNFORCECCM ³ = 1) mode transitions compared to DC level in LN mode	—	40	—	mV
		Undershoot during BYP/LP to LN DCM (LNFORCECCM ³ = 0) mode transitions compared to DC level in LN mode	—	100	—	mV
DC line regulation	V _{REG}	Input changes between V _{VREGVDD_MAX} and 2.4 V	—	0.1	—	%
DC load regulation	I _{REG}	Load changes between 0 mA and 100 mA in CCM mode	—	0.1	—	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max load current	I _{LOAD_MAX}	Low noise (LN) mode, Heavy Drive ⁴ , T ≤ 85 °C	—	—	200	mA
		Low noise (LN) mode, Heavy Drive ⁴ , T > 85 °C	—	—	100	mA
		Low noise (LN) mode, Medium Drive ⁴	—	—	100	mA
		Low noise (LN) mode, Light Drive ⁴	—	—	50	mA
		Low power (LP) mode, LPCMPBIASEMxx ³ = 0	—	—	75	µA
		Low power (LP) mode, LPCMPBIASEMxx ³ = 3	—	—	10	mA
DCDC nominal output capacitor ⁵	C _{DCDC}	25% tolerance	1	4.7	4.7	µF
DCDC nominal output inductor	L _{DCDC}	20% tolerance	4.7	4.7	4.7	µH
Resistance in Bypass mode	R _{BYP}		—	1.2	2.5	Ω

Note:

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, V_{VREGVDD}.
2. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits.
3. LPCMPBIASEMxx refers to either LPCMPBIASEM234H in the EMU_DCDCMISCCTRL register or LPCMPBIASEM01 in the EMU_DCDCLCLOEM01CFG register, depending on the energy mode.
4. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.
5. Output voltage under/over-shoot and regulation are specified with C_{DCDC} 4.7 µF. Different settings for DCDCLNCOMPCTRL must be used if C_{DCDC} is lower than 4.7 µF. See Application Note AN0948 for details.

4.1.5 Current Consumption

4.1.5.1 Current Consumption 3.3 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = RFVDD = PAVDD = 3.3 V. T = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across process variation at T = 25 °C.

Table 4.5. Current Consumption 3.3 V without DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I _{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash ¹	—	130	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	99	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	99	105	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	124	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	102	108	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	280	435	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled	I _{ACTIVE_VS}	19 MHz HFRCO, CPU running while loop from flash	—	88	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	234	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I _{EM1}	38.4 MHz crystal ¹	—	80	—	µA/MHz
		38 MHz HFRCO	—	50	54	µA/MHz
		26 MHz HFRCO	—	52	58	µA/MHz
		1 MHz HFRCO	—	230	400	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled	I _{EM1_VS}	19 MHz HFRCO	—	47	—	µA/MHz
		1 MHz HFRCO	—	193	—	µA/MHz
Current consumption in EM2 mode, with voltage scaling enabled	I _{EM2_VS}	Full 256 kB RAM retention and RTCC running from LFXO	—	2.9	—	µA
		Full 256 kB RAM retention and RTCC running from LFRCO	—	3.2	—	µA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO ²	—	2.1	3.5	µA
Current consumption in EM3 mode, with voltage scaling enabled	I _{EM3_VS}	Full 256 kB RAM retention and CRYOTIMER running from ULFRCO	—	2.56	4.8	µA
Current consumption in EM4H mode, with voltage scaling enabled	I _{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	1.0	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.45	—	µA
		128 byte RAM retention, no RTCC	—	0.43	0.9	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM4S mode	I_{EM4S}	No RAM retention, no RTCC	—	0.04	0.1	μA

Note:

1. CMU_HFXOCTRL_LOWPOWER=0.
2. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

4.1.5.2 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD = 1.8 V DC-DC output. T = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T = 25 °C.

Table 4.6. Current Consumption 3.3 V using DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise DCM mode ¹	IACTIVE_DCM	38.4 MHz crystal, CPU running while loop from flash ²	—	88	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	70	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	70	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	85	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	77	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	636	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise CCM mode ³	IACTIVE_CCM	38.4 MHz crystal, CPU running while loop from flash ²	—	98	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	81	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	82	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	95	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	95	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1155	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise CCM mode ³	IACTIVE_CCM_VS	19 MHz HFRCO, CPU running while loop from flash	—	101	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1128	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Noise DCM mode ¹	IEM1_DCM	38.4 MHz crystal ²	—	59	—	µA/MHz
		38 MHz HFRCO	—	41	—	µA/MHz
		26 MHz HFRCO	—	48	—	µA/MHz
		1 MHz HFRCO	—	610	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise DCM mode ¹	IEM1_DCM_VS	19 MHz HFRCO	—	52	—	µA/MHz
		1 MHz HFRCO	—	587	—	µA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, with voltage scaling enabled, DCDC in LP mode ⁴	I _{EM2_VS}	Full 256 kB RAM retention and RTCC running from LFXO	—	2.1	—	µA
		Full 256 kB RAM retention and RTCC running from LFRCO	—	2.2	—	µA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO ⁵	—	1.5	—	µA
Current consumption in EM3 mode, with voltage scaling enabled	I _{EM3_VS}	Full 256 kB RAM retention and CRYOTIMER running from ULFR- CO	—	1.81	—	µA
Current consumption in EM4H mode, with voltage scaling enabled	I _{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	0.69	—	µA
		128 byte RAM retention, CRYO- TIMER running from ULFRCO	—	0.39	—	µA
		128 byte RAM retention, no RTCC	—	0.39	—	µA
Current consumption in EM4S mode	I _{EM4S}	No RAM retention, no RTCC	—	0.06	—	µA

Note:

1. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD.
2. CMU_HFXOCTRL_LOWPOWER=0.
3. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD.
4. DCDC Low Power Mode = Medium Drive, LPOSCDIV=1, LPCMPBIASEM234H=0, LPCLIMILIMSEL=1, ANASW=DVDD.
5. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

4.1.5.3 Current Consumption 1.8 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = RFVDD = PAVDD = 1.8 V. T = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across process variation at T = 25 °C.

Table 4.7. Current Consumption 1.8 V without DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I _{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash ¹	—	130	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	99	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	99	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	124	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	102	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	277	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled	I _{ACTIVE_VS}	19 MHz HFRCO, CPU running while loop from flash	—	87	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	231	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I _{EM1}	38.4 MHz crystal ¹	—	80	—	µA/MHz
		38 MHz HFRCO	—	50	—	µA/MHz
		26 MHz HFRCO	—	52	—	µA/MHz
		1 MHz HFRCO	—	227	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled	I _{EM1_VS}	19 MHz HFRCO	—	47	—	µA/MHz
		1 MHz HFRCO	—	190	—	µA/MHz
Current consumption in EM2 mode, with voltage scaling enabled	I _{EM2_VS}	Full 256 kB RAM retention and RTCC running from LFXO	—	2.8	—	µA
		Full 256 kB RAM retention and RTCC running from LFRCO	—	3.0	—	µA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO ²	—	1.9	—	µA
Current consumption in EM3 mode, with voltage scaling enabled	I _{EM3_VS}	Full 256 kB RAM retention and CRYOTIMER running from ULFRCO	—	2.47	—	µA
Current consumption in EM4H mode, with voltage scaling enabled	I _{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	0.91	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.35	—	µA
		128 byte RAM retention, no RTCC	—	0.35	—	µA
Current consumption in EM4S mode	I _{EM4S}	No RAM retention, no RTCC	—	0.04	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note:						
1. CMU_HFXOCTRL_LOWPOWER=0. 2. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1						

4.1.5.4 Current Consumption Using Radio 3.3 V with DC-DC

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD = 1.8 V. T = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T = 25 °C.

Table 4.8. Current Consumption Using Radio 3.3 V with DC-DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), T ≤ 85 °C	I _{RX_ACTIVE}	500 kbit/s, 2GFSK, F = 915 MHz, Radio clock prescaled by 4	—	9.3	10.2	mA
		38.4 kbit/s, 2GFSK, F = 868 MHz, Radio clock prescaled by 4	—	8.6	10.2	mA
		38.4 kbit/s, 2GFSK, F = 490 MHz, Radio clock prescaled by 4	—	8.6	10.2	mA
		50 kbit/s, 2GFSK, F = 433 MHz, Radio clock prescaled by 4	—	8.6	10.2	mA
		38.4 kbit/s, 2GFSK, F = 315 MHz, Radio clock prescaled by 4	—	8.6	10.2	mA
		38.4 kbit/s, 2GFSK, F = 169 MHz, Radio clock prescaled by 4	—	8.4	10.2	mA
		1 Mbit/s, 2GFSK, F = 2.4 GHz, Radio clock prescaled by 4	—	10.0	—	mA
		2 Mbit/s, 2GFSK, F = 2.4 GHz, Radio clock prescaled by 4	—	11.5	—	mA
		802.15.4 receiving frame, F = 2.4 GHz, Radio clock prescaled by 3	—	11	—	mA
Current consumption in receive mode, active packet reception (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), T > 85 °C	I _{RX_ACTIVE_HT}	500 kbit/s, 2GFSK, F = 915 MHz, Radio clock prescaled by 4	—	—	13	mA
		38.4 kbit/s, 2GFSK, F = 868 MHz, Radio clock prescaled by 4	—	—	13	mA
		38.4 kbit/s, 2GFSK, F = 490 MHz, Radio clock prescaled by 4	—	—	13	mA
		50 kbit/s, 2GFSK, F = 433 MHz, Radio clock prescaled by 4	—	—	13	mA
		38.4 kbit/s, 2GFSK, F = 315 MHz, Radio clock prescaled by 4	—	—	13	mA
		38.4 kbit/s, 2GFSK, F = 169 MHz, Radio clock prescaled by 4	—	—	13	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, listening for packet (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), T ≤ 85 °C	I _{RX_LISTEN}	500 kbit/s, 2GFSK, F = 915 MHz, No radio clock prescaling	—	10.2	11	mA
		38.4 kbit/s, 2GFSK, F = 868 MHz, No radio clock prescaling	—	9.5	11	mA
		38.4 kbit/s, 2GFSK, F = 490 MHz, No radio clock prescaling	—	9.5	11	mA
		50 kbit/s, 2GFSK, F = 433 MHz, No radio clock prescaling	—	9.5	11	mA
		38.4 kbit/s, 2GFSK, F = 315 MHz, No radio clock prescaling	—	9.4	11	mA
		38.4 kbit/s, 2GFSK, F = 169 MHz, No radio clock prescaling	—	9.3	11	mA
		1 Mbit/s, 2GFSK, F = 2.4 GHz, No radio clock prescaling	—	10.9	—	mA
		2 Mbit/s, 2GFSK, F = 2.4 GHz, No radio clock prescaling	—	11.9	—	mA
		802.15.4, F = 2.4 GHz, No radio clock prescaling	—	12.5	—	mA
Current consumption in receive mode, listening for packet (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), T > 85 °C	I _{RX_LISTEN_HT}	500 kbit/s, 2GFSK, F = 915 MHz, No radio clock prescaling	—	—	14	mA
		38.4 kbit/s, 2GFSK, F = 868 MHz, No radio clock prescaling	—	—	14	mA
		38.4 kbit/s, 2GFSK, F = 490 MHz, No radio clock prescaling	—	—	14	mA
		50 kbit/s, 2GFSK, F = 433 MHz, No radio clock prescaling	—	—	14	mA
		38.4 kbit/s, 2GFSK, F = 315 MHz, No radio clock prescaling	—	—	14	mA
		38.4 kbit/s, 2GFSK, F = 169 MHz, No radio clock prescaling	—	—	14	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in transmit mode (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), T ≤ 85 °C	I _{TX}	F = 915 MHz, CW, 20 dBm match, External PA supply = 3.3V	—	90.2	134.3	mA
		F = 915 MHz, CW, 14 dBm match, External PA supply connected to DCDC output	—	36	42.5	mA
		F = 868 MHz, CW, 20 dBm match, External PA supply = 3.3V	—	79.7	106.7	mA
		F = 868 MHz, CW, 14 dBm match, External PA supply connected to DCDC output	—	35.3	41	mA
		F = 490 MHz, CW, 20 dBm match, External PA supply = 3.3V	—	93.8	125.4	mA
		F = 433 MHz, CW, 10 dBm match, External PA supply connected to DC-DC output	—	20.3	24	mA
		F = 433 MHz, CW, 14 dBm match, External PA supply connected to DCDC output	—	34	41.5	mA
		F = 315 MHz, CW, 14 dBm match, External PA supply connected to DCDC output	—	33.5	42	mA
		F = 169 MHz, CW, 20 dBm match, External PA supply = 3.3V	—	88.6	116.7	mA
		F = 2.4 GHz, CW, 0 dBm output power, Radio clock prescaled by 3	—	8.5	—	mA
		F = 2.4 GHz, CW, 0 dBm output power, Radio clock prescaled by 1	—	9.5	—	mA
		F = 2.4 GHz, CW, 3 dBm output power	—	16.5	—	mA
		F = 2.4 GHz, CW, 8 dBm output power	—	26	—	mA
		F = 2.4 GHz, CW, 10.5 dBm output power	—	34	—	mA
		F = 2.4 GHz, CW, 16.5 dBm output power, PAVDD connected directly to external 3.3V supply	—	86	—	mA
		F = 2.4 GHz, CW, 19.5 dBm output power, PAVDD connected directly to external 3.3V supply	—	131	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in transmit mode (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled), T > 85 °C	I _{TX_HT}	F = 915 MHz, CW, 20 dBm match, External PA supply = 3.3V	—	—	134.3	mA
		F = 915 MHz, CW, 14 dBm match, External PA supply connected to DCDC output	—	—	42.5	mA
		F = 868 MHz, CW, 20 dBm match, External PA supply = 3.3V	—	—	109.8	mA
		F = 868 MHz, CW, 14 dBm match, External PA supply connected to DCDC output	—	—	41.3	mA
		F = 490 MHz, CW, 20 dBm match, External PA supply = 3.3V	—	—	130.8	mA
		F = 433 MHz, CW, 10 dBm match, External PA supply connected to DC-DC output	—	—	24.4	mA
		F = 433 MHz, CW, 14 dBm match, External PA supply connected to DCDC output	—	—	41.5	mA
		F = 315 MHz, CW, 14 dBm match, External PA supply connected to DCDC output	—	—	42	mA
		F = 169 MHz, CW, 20 dBm match, External PA supply = 3.3V	—	—	122.8	mA

4.1.6 Wake Up Times

Table 4.9. Wake Up Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
Wake up time from EM1	t_{EM1_WU}		—	3	—	AHB Clocks	
Wake up from EM2	t_{EM2_WU}	Code execution from flash	—	10.1	—	μ s	
		Code execution from RAM	—	3.2	—	μ s	
Wake up from EM3	t_{EM3_WU}	Code execution from flash	—	10.1	—	μ s	
		Code execution from RAM	—	3.2	—	μ s	
Wake up from EM4H ¹	t_{EM4H_WU}	Executing from flash	—	80	—	μ s	
Wake up from EM4S ¹	t_{EM4S_WU}	Executing from flash	—	291	—	μ s	
Time from release of reset source to first instruction execution	t_{RESET}	Soft Pin Reset released	—	43	—	μ s	
		Any other reset released	—	350	—	μ s	
Power mode scaling time	t_{SCALE}	VSCALE0 to VSCALE2, HFCLK = 19 MHz ² ³	—	31.8	—	μ s	
		VSCALE2 to VSCALE0, HFCLK = 19 MHz ⁴	—	4.3	—	μ s	
Note:							
1. Time from wake up request until first instruction is executed. Wakeup results in device reset.							
2. Scaling up from VSCALE0 to VSCALE2 requires approximately 30.3 μ s + 28 HFCLKs.							
3. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV/ μ s for approximately 20 μ s. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 μ F capacitor) to 70 mA (with a 2.7 μ F capacitor).							
4. Scaling down from VSCALE2 to VSCALE0 requires approximately 2.8 μ s + 29 HFCLKs.							

4.1.7 Brown Out Detector (BOD)

Table 4.10. Brown Out Detector (BOD)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DVDD BOD threshold	V _{DVDBOD}	DVDD rising	—	—	1.62	V
		DVDD falling (EM0/EM1)	1.35	—	—	V
		DVDD falling (EM2/EM3)	1.3	—	—	V
DVDD BOD hysteresis	V _{DVDBOD_HYST}		—	18	—	mV
DVDD BOD response time	t _{DVDBOD_DELAY}	Supply drops at 0.1V/μs rate	—	2.4	—	μs
AVDD BOD threshold	V _{AVDBOD}	AVDD rising	—	—	1.8	V
		AVDD falling (EM0/EM1)	1.62	—	—	V
		AVDD falling (EM2/EM3)	1.53	—	—	V
AVDD BOD hysteresis	V _{AVDBOD_HYST}		—	20	—	mV
AVDD BOD response time	t _{AVDBOD_DELAY}	Supply drops at 0.1V/μs rate	—	2.4	—	μs
EM4 BOD threshold	V _{EM4DBOD}	AVDD rising	—	—	1.7	V
		AVDD falling	1.45	—	—	V
EM4 BOD hysteresis	V _{EM4BOD_HYST}		—	25	—	mV
EM4 BOD response time	t _{EM4BOD_DELAY}	Supply drops at 0.1V/μs rate	—	300	—	μs

4.1.8 Frequency Synthesizer

Table 4.11. Frequency Synthesizer

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF synthesizer frequency range	f_{RANGE}	2400 - 2483.5 MHz	2400	—	2483.5	MHz
		779 - 956 MHz	779	—	956	MHz
		584 - 717 MHz	584	—	717	MHz
		358 - 574 MHz	358	—	574	MHz
		191 - 358 MHz	191	—	358	MHz
		110 - 191 MHz	110	—	191	MHz
LO tuning frequency resolution with 38.4 MHz crystal	f_{RES}	2400 - 2483.5 MHz	—	—	73	Hz
		779 - 956 MHz	—	—	24	Hz
		584 - 717 MHz	—	—	18.3	Hz
		358 - 574 MHz	—	—	12.2	Hz
		191 - 358 MHz	—	—	7.3	Hz
		110 - 191 MHz	—	—	4.6	Hz
Frequency deviation resolution with 38.4 MHz crystal	df_{RES}	2400 - 2483.5 MHz	—	—	73	Hz
		779 - 956 MHz	—	—	24	Hz
		584 - 717 MHz	—	—	18.3	Hz
		358 - 574 MHz	—	—	12.2	Hz
		191 - 358 MHz	—	—	7.3	Hz
		110 - 191 MHz	—	—	4.6	Hz
Maximum frequency deviation with 38.4 MHz crystal	df_{MAX}	2400 - 2483.5 MHz	—	—	1677	kHz
		779 - 956 MHz	—	—	559	kHz
		584 - 717 MHz	—	—	419	kHz
		358 - 574 MHz	—	—	280	kHz
		191 - 358 MHz	—	—	167	kHz
		110 - 191 MHz	—	—	105	kHz

4.1.9 2.4 GHz RF Transceiver Characteristics

4.1.9.1 RF Transmitter General Characteristics for 2.4 GHz Band

Unless otherwise indicated, typical conditions are: $T = 25^\circ\text{C}$, $\text{VREGVDD} = \text{AVDD} = \text{IOVDD} = 3.3\text{ V}$, $\text{DVDD} = \text{RFVDD} = \text{PAVDD}$. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz.

Table 4.12. RF Transmitter General Characteristics for 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum TX power ¹	POUT_{MAX}	19 dBm-rated part numbers. PAVDD connected directly to external 3.3V supply	—	19.5	—	dBm
Minimum active TX Power	POUT_{MIN}	CW		-30	—	dBm
Output power step size	$\text{POUT}_{\text{STEP}}$	-5 dBm < Output power < 0 dBm	—	1	—	dB
		0 dBm < output power < POUT_{MAX}	—	0.5	—	dB
Output power variation vs supply at POUT_{MAX}	$\text{POUT}_{\text{VAR_V}}$	1.8 V < $\text{V}_{\text{VREGVDD}}$ < 3.3 V, PAVDD connected directly to external supply, for output power > 10 dBm.	—	4.5	—	dB
		1.8 V < $\text{V}_{\text{VREGVDD}}$ < 3.3 V using DC-DC converter	—	2.2	—	dB
Output power variation vs temperature at POUT_{MAX}	$\text{POUT}_{\text{VAR_T}}$	From -40 to +85 °C, PAVDD connected to DC-DC output	—	1.5	—	dB
		From -40 to +125 °C, PAVDD connected to DC-DC output	—	2.2	—	dB
		From -40 to +85 °C, PAVDD connected to external supply	—	1.5	—	dB
		From -40 to +125 °C, PAVDD connected to external supply	—	3.4	—	dB
Output power variation vs RF frequency at POUT_{MAX}	$\text{POUT}_{\text{VAR_F}}$	Over RF tuning frequency range	—	0.4	—	dB
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.

4.1.9.2 RF Receiver General Characteristics for 2.4 GHz Band

Unless otherwise indicated, typical conditions are: $T = 25^\circ\text{C}$, $\text{VREGVDD} = \text{AVDD} = \text{IOVDD} = 3.3\text{ V}$, $\text{DVDD} = \text{RFVDD} = \text{PAVDD}$. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz.

Table 4.13. RF Receiver General Characteristics for 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz
Receive mode maximum spurious emission	SPUR_{RX}	30 MHz to 1 GHz	—	-57	—	dBm
		1 GHz to 12 GHz	—	-47	—	dBm
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	$\text{SPUR}_{\text{RX_FCC}}$	216 MHz to 960 MHz, Conducted Measurement	—	-55.2	—	dBm
		Above 960 MHz, Conducted Measurement	—	-47.2	—	dBm
Level above which RFSENSE will trigger ¹	$\text{RFSENSE}_{\text{TRIG}}$	CW at 2.45 GHz	—	-24	—	dBm
Level below which RFSENSE will not trigger ¹	$\text{RFSENSE}_{\text{THRES}}$	CW at 2.45 GHz	—	-50	—	dBm
1% PER sensitivity	$\text{SENS}_{\text{2GFSK}}$	2 Mbps 2GFSK signal	—	-89.6	—	dBm
		250 kbps 2GFSK signal	—	-100.7	—	dBm

Note:

1. RFSENSE performance is only valid from 0 to 85°C . RFSENSE should be disabled outside this temperature range.

4.1.9.3 RF Transmitter Characteristics for 2GFSK in the 2.4GHz Band, 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency = 38.4MHz. RF center frequency 2.45 GHz. Maximum duty cycle of 85%.

Table 4.14. RF Transmitter Characteristics for 2GFSK in the 2.4GHz Band, 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
Transmit 6dB bandwidth	TXBW	10 dBm	—	781	—	kHz	
Power spectral density limit	PSD _{LIMIT}	Per FCC part 15.247 at 10 dBm	—	-8.4	—	dBm/3kHz	
		Per FCC part 15.247 at 20 dBm	—	-0.4	—	dBm/3kHz	
		Per ETSI 300.328 at 10 dBm/1 MHz	—	10.1	—	dBm	
Occupied channel bandwidth per ETSI EN300.328	OCP _{ETSI328}	99% BW at highest and lowest channels in band, 10 dBm	—	1.1	—	MHz	
Emissions of harmonics out-of-band, per FCC part 15.247	SPUR _{HRM_FCC}	2nd,3rd, 5, 6, 8, 9,10 harmonics; continuous transmission of modulated carrier	—	-47	—	dBm	
Spurious emissions out-of-band, excluding harmonics captured in SPUR _{HARM,FCC} . Emissions taken at POUT _{MAX} , PAVDD connected to external 3.3 V supply	SPUR _{OOB_FCC}	Per FCC part 15.205/15.209, Above 2.483 GHz or below 2.4 GHz; continuous transmission of CW carrier, Restricted Bands ^{1,2}	—	-47	—	dBm	
		Per FCC part 15.247, Above 2.483 GHz or below 2.4 GHz; continuous transmission of CW carrier, Non-Restricted Bands	—	-26	—	dBc	
Spurious emissions out-of-band; per ETSI 300.328	SPUR _{ETSI328}	[2400-BW to 2400] MHz, [2483.5 to 2483.5+BW] MHz	—	-16	—	dBm	
		[2400-2BW to 2400-BW] MHz, [2483.5+BW to 2483.5+2BW] MHz per ETSI 300.328	—	-26	—	dBm	
Spurious emissions per ETSI EN300.440	SPUR _{ETSI440}	47-74 MHz,87.5-108 MHz, 174-230 MHz, 470-862 MHz	—	-60	—	dBm	
		25-1000 MHz	—	-42	—	dBm	
		1-12 GHz	—	-36	—	dBm	
Note:							
1. For 2476 MHz, 1.5 dB of power backoff is used to achieve this value.							
2. For 2478 MHz, 4.2 dB of power backoff is used to achieve this value.							

4.1.9.4 RF Receiver Characteristics for 2GFSK in the 2.4GHz Band, 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: $T = 25^\circ\text{C}$, $\text{VREGVDD} = \text{AVDD} = \text{IOVDD} = 3.3\text{ V}$, $\text{DVDD} = \text{RFVDD} = \text{PAVDD}$. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency = 38.4MHz. RF center frequency 2.45 GHz.

Table 4.15. RF Receiver Characteristics for 2GFSK in the 2.4GHz Band, 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level, 0.1% BER	SAT	Signal is reference signal ¹ . Packet length is 20 bytes.	—	10	—	dBm
Sensitivity, 0.1% BER	SENS	Signal is reference signal ¹ . Using DC-DC converter.	—	-94.8	—	dBm
Signal to co-channel interferer, 0.1% BER	C/I _{CC}	Desired signal 3 dB above reference sensitivity.	—	10.3	—	dB
N+1 adjacent channel selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I ₁₊	Interferer is reference signal at +1 MHz offset. Desired frequency $2402\text{ MHz} \leq F_c \leq 2480\text{ MHz}$	—	-1.8	—	dB
N-1 adjacent channel selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I ₁₋	Interferer is reference signal at -1 MHz offset. Desired frequency $2402\text{ MHz} \leq F_c \leq 2480\text{ MHz}$	—	-0.7	—	dB
Alternate selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I ₂	Interferer is reference signal at ± 2 MHz offset. Desired frequency $2402\text{ MHz} \leq F_c \leq 2480\text{ MHz}$, QFN48 and BGA125 packages.	—	-40.6	—	dB
		Interferer is reference signal at ± 2 MHz offset. Desired frequency $2402\text{ MHz} \leq F_c \leq 2480\text{ MHz}$, QFN68 package.	—	-34.1	—	dB
Alternate selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I ₃	Interferer is reference signal at ± 3 MHz offset. Desired frequency $2404\text{ MHz} \leq F_c \leq 2480\text{ MHz}$	—	-46.2	—	dB
Selectivity to image frequency, 0.1% BER. Desired is reference signal at -67 dBm	C/I _{IM}	Interferer is reference signal at image frequency with 1 MHz precision	—	-38.1	—	dB
Selectivity to image frequency ± 1 MHz, 0.1% BER. Desired is reference signal at -67 dBm	C/I _{IM+1}	Interferer is reference signal at image frequency ± 1 MHz with 1 MHz precision	—	-46.5	—	dB
Blocking, less than 0.1% BER. Desired is -67dBm BLE reference signal at 2426MHz. Interferer is CW in OOB range ²	BLOCK _{OOB}	Interferer frequency $30\text{ MHz} \leq f \leq 2000\text{ MHz}$	-5	—	—	dBm
		Interferer frequency $2003\text{ MHz} \leq f \leq 2399\text{ MHz}$	-24	—	—	dBm
		Interferer frequency $2484\text{ MHz} \leq f \leq 2997\text{ MHz}$	-10	—	—	dBm
		Interferer frequency $3\text{ GHz} \leq f \leq 6\text{ GHz}$	-10	—	—	dBm
		Interferer frequency $6\text{ GHz} \leq f \leq 12.75\text{ GHz}$	-17	—	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note:						
1. Reference signal is defined 2GFSK at -67 dBm, Modulation index = 0.5, BT = 0.5, Bit rate = 1 Mbps, desired data = PRBS9; interferer data = PRBS15; frequency accuracy better than 1 ppm. 2. Interferer max power limited by equipment capabilities and path loss. Minimum specified at 25 °C.						

4.1.9.5 RF Transmitter Characteristics for 2GFSK in the 2.4GHz Band, 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency = 38.4MHz. RF center frequency 2.45 GHz. Maximum duty cycle of 85%.

Table 4.16. RF Transmitter Characteristics for 2GFSK in the 2.4GHz Band, 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6dB bandwidth	TXBW	10 dBm	—	1404	—	kHz
Power spectral density limit	PSD _{LIMIT}	Per FCC part 15.247 at 10 dBm	—	-12.3	—	dBm/3kHz
		Per FCC part 15.247 at 20 dBm	—	-4.0	—	dBm/3kHz
		Per ETSI 300.328 at 10 dBm/1 MHz	—	11.3	—	dBm
Occupied channel bandwidth per ETSI EN300.328	OCP _{ETSI328}	99% BW at highest and lowest channels in band, 10 dBm	—	2.1	—	MHz
Emissions of harmonics out-of-band, per FCC part 15.247	SPUR _{HRM_FCC}	2nd,3rd, 5, 6, 8, 9,10 harmonics; continuous transmission of modulated carrier	—	-47	—	dBm
Spurious emissions out-of-band, excluding harmonics captured in SPUR _{HARM,FCC} . Emissions taken at POUT _{MAX} , PAVDD connected to external 3.3 V supply	SPUR _{OOB_FCC}	Per FCC part 15.205/15.209, Above 2.483 GHz or below 2.4 GHz; continuous transmission of CW carrier, Restricted Bands ^{1 2 3 4}	—	-47	—	dBm
		Per FCC part 15.247, Above 2.483 GHz or below 2.4 GHz; continuous transmission of CW carrier, Non-Restricted Bands	—	-26	—	dBc
Spurious emissions out-of-band; per ETSI 300.328	SPUR _{ETSI328}	[2400-BW to 2400] MHz, [2483.5 to 2483.5+BW] MHz	—	-16	—	dBm
		[2400-2BW to 2400-BW] MHz, [2483.5+BW to 2483.5+2BW] MHz per ETSI 300.328	—	-26	—	dBm
Spurious emissions per ETSI EN300.440	SPUR _{ETSI440}	47-74 MHz,87.5-108 MHz, 174-230 MHz, 470-862 MHz	—	-60	—	dBm
		25-1000 MHz	—	-42	—	dBm
		1-12 GHz	—	-36	—	dBm

Note:

1. For 2472 MHz, 1.3 dB of power backoff is used to achieve this value.
2. For 2474 MHz, 3.8 dB of power backoff is used to achieve this value.
3. For 2476 MHz, 7 dB of power backoff is used to achieve this value.
4. For 2478 MHz, 11.2 dB of power backoff is used to achieve this value.

4.1.9.6 RF Receiver Characteristics for 2GFSK in the 2.4GHz Band, 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T = 25 °C, VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency = 38.4MHz. RF center frequency 2.45 GHz¹.

Table 4.17. RF Receiver Characteristics for 2GFSK in the 2.4GHz Band, 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level, 0.1% BER	SAT	Signal is reference signal ² . Packet length is 20 bytes.	—	10	—	dBm
Sensitivity, 0.1% BER	SENS	Signal is reference signal ² . Using DC-DC converter. QFN48 and BGA125 packages.	—	-91.3	—	dBm
		Signal is reference signal ² . Using DC-DC converter. QFN68 package.	—	-91.3	—	dBm
Signal to co-channel interferer, 0.1% BER	C/I _{CC}	Desired signal 3 dB above reference sensitivity.	—	7.3	—	dB
N+1 adjacent channel selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I ₁₊	Interferer is reference signal at +2 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-10.4	—	dB
N-1 adjacent channel selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I ₁₋	Interferer is reference signal at -2 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-13.9	—	dB
Alternate selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I ₂	Interferer is reference signal at ± 4 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-40.9	—	dB
Alternate selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I ₃	Interferer is reference signal at ± 6 MHz offset. Desired frequency 2404 MHz ≤ Fc ≤ 2480 MHz	—	-43.7	—	dB
Selectivity to image frequency, 0.1% BER. Desired is reference signal at -67 dBm	C/I _{IM}	Interferer is reference signal at image frequency with 1 MHz precision	—	-10.4	—	dB
Selectivity to image frequency ± 2 MHz, 0.1% BER. Desired is reference signal at -67 dBm	C/I _{IM+1}	Interferer is reference signal at image frequency ± 2 MHz with 2 MHz precision	—	-40.9	—	dB
Note:						
1. For the BLE 2Mbps in-band blocking performance, there may be up to 5 spurious response channels where the requirement of 30.8% PER is not met and therefore an exception will need to be taken for each of these frequencies to meet the requirements of the BLE standard.						
2. Reference signal is defined 2GFSK at -67 dBm, Modulation index = 0.5, BT = 0.5, Bit rate = 2 Mbps, desired data = PRBS9; interferer data = PRBS15; frequency accuracy better than 1 ppm.						

4.1.9.7 RF Transmitter Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: $T = 25^\circ\text{C}$, $\text{VREGVDD} = \text{AVDD} = \text{IOVDD} = 3.3\text{ V}$, $\text{DVDD} = \text{RFVDD} = \text{PAVDD}$. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz. Maximum duty cycle of 66%.

Table 4.18. RF Transmitter Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Error vector magnitude (offset EVM), per 802.15.4-2011	EVM	Average across frequency. Signal is DSSS-OQPSK reference packet ¹	—	3.8	—	% rms
Power spectral density limit	PSD _{LIMIT}	Relative, at carrier $\pm 3.5\text{ MHz}$, output power at POUT _{MAX}	—	-26	—	dBc/100kHz
		Absolute, at carrier $\pm 3.5\text{ MHz}$, output power at POUT _{MAX} ²	—	-36	—	dBm/100kHz
		Per FCC part 15.247, output power at POUT _{MAX}	—	-4	—	dBm/3kHz
		ETSI	—	12.1	—	dBm
Occupied channel bandwidth per ETSI EN300.328	OCP _{ETSI328}	99% BW at highest and lowest channels in band	—	2.25	—	MHz
Spurious emissions of harmonics in restricted bands per FCC Part 15.205/15.209, Emissions taken at POUT _{MAX} , PAVDD connected to external 3.3 V supply, Test Frequency is 2450 MHz	SPUR _{HRM_FCC_R}	Continuous transmission of modulated carrier	—	-45.8	—	dBm
Spurious emissions of harmonics in non-restricted bands per FCC Part 15.247/15.35, Emissions taken at POUT _{MAX} , PAVDD connected to external 3.3 V supply, Test Frequency is 2450 MHz	SPUR _{HRM_FCC_NRR}	Continuous transmission of modulated carrier	—	-26	—	dBc
Spurious emissions out-of-band (above 2.483 GHz or below 2.4 GHz) in restricted bands, per FCC part 15.205/15.209, Emissions taken at POUT _{MAX} , PAVDD connected to external 3.3 V supply, Test Frequency = 2450 MHz	SPUR _{OOB_FCC_R}	Restricted bands 30-88 MHz; continuous transmission of modulated carrier	—	-61	—	dBm
		Restricted bands 88-216 MHz; continuous transmission of modulated carrier	—	-58	—	dBm
		Restricted bands 216-960 MHz; continuous transmission of modulated carrier	—	-55	—	dBm
		Restricted bands >960 MHz; continuous transmission of modulated carrier ^{3 4}	—	-47	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band in non-restricted bands per FCC Part 15.247, Emissions taken at POUT _{MAX} , PAVDD connected to external 3.3 V supply, Test Frequency = 2450 MHz	SPUR _{OOB_FCC_NR}	Above 2.483 GHz or below 2.4 GHz; continuous transmission of modulated carrier	—	-26	—	dBc
Spurious emissions out-of-band; per ETSI 300.328 ⁵	SPUR _{ETSI328}	[2400-BW to 2400], [2483.5 to 2483.5+BW];	—	-16	—	dBm
		[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW]; per ETSI 300.328	—	-26	—	dBm
Spurious emissions per ETSI EN300.440 ⁵	SPUR _{ETSI440}	47-74 MHz, 87.5-108 MHz, 174-230 MHz, 470-862 MHz	—	-60	—	dBm
		25-1000 MHz, excluding above frequencies	—	-42	—	dBm
		1G-14G	—	-36	—	dBm

Note:

1. Reference packet is defined as 20 octet PSDU, modulated according to 802.15.4-2011 DSSS-OQPSK in the 2.4GHz band, with pseudo-random packet data content.
2. For 2415 MHz, 2 dB of power backoff is used to achieve this value.
3. For 2475 MHz, 2 dB of power backoff is used to achieve this value.
4. For 2480 MHz, 13 dB of power backoff is used to achieve this value.
5. Specified at maximum power output level of 10 dBm.

4.1.9.8 RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: $T = 25^{\circ}\text{C}$, $\text{VREGVDD} = \text{AVDD} = \text{IOVDD} = 3.3\text{ V}$, $\text{DVDD} = \text{RFVDD} = \text{PAVDD}$. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency = 38.4 MHz. RF center frequency 2.45 GHz.

Table 4.19. RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level, 1% PER	SAT	Signal is reference signal ¹ . Packet length is 20 octets.	—	10	—	dBm
Sensitivity, 1% PER	SENS	Signal is reference signal. Packet length is 20 octets. Using DC-DC converter.	—	-102.7	—	dBm
		Signal is reference signal. Packet length is 20 octets. Without DC-DC converter.	—	-102.7	—	dBm
Co-channel interferer rejection, 1% PER	CCR	Desired signal 3 dB above sensitivity limit	—	-4.6	—	dB
High-side adjacent channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level ²	ACRP1	Interferer is reference signal at +1 channel-spacing.	—	40.7	—	dB
		Interferer is filtered reference signal ³ at +1 channel-spacing.	—	47	—	dB
		Interferer is CW at +1 channel-spacing ⁴ .	—	54.3	—	dB
Low-side adjacent channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level ²	ACRM1	Interferer is reference signal at -1 channel-spacing.	—	40.8	—	dB
		Interferer is filtered reference signal ³ at -1 channel-spacing.	—	47.5	—	dB
		Interferer is CW at -1 channel-spacing.	—	56.5	—	dB
Alternate channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level ²	ACR2	Interferer is reference signal at ± 2 channel-spacing	—	51.5	—	dB
		Interferer is filtered reference signal ³ at ± 2 channel-spacing	—	53.7	—	dB
		Interferer is CW at ± 2 channel-spacing	—	62.4	—	dB
Image rejection , 1% PER, Desired is reference signal at 3dB above reference sensitivity level ²	IR	Interferer is CW in image band ⁴	—	50.4	—	dB
Blocking rejection of all other channels. 1% PER, Desired is reference signal at 3dB above reference sensitivity level ² . Interferer is reference signal	BLOCK	Interferer frequency < Desired frequency - 3 channel-spacing	—	58.5	—	dB
		Interferer frequency > Desired frequency + 3 channel-spacing	—	56.4	—	dB
Blocking rejection of 802.11g signal centered at +12MHz or -13MHz ⁵	BLOCK _{80211G}	Desired is reference signal at 6dB above reference sensitivity level ²	—	53	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Upper limit of input power range over which RSSI resolution is maintained	RSSI _{MAX}		—	—	5	dBm
Lower limit of input power range over which RSSI resolution is maintained	RSSI _{MIN}		-98	—	—	dBm
RSSI resolution	RSSI _{RES}	over RSSI _{MIN} to RSSI _{MAX}	—	0.25	—	dB
RSSI accuracy in the linear region as defined by 802.15.4-2003	RSSI _{LIN}		—	+/-6	—	dB

Note:

1. Reference signal is defined as O-QPSK DSSS per 802.15.4, Frequency range = 2400-2483.5 MHz, Symbol rate = 62.5 ksym-bols/s.
2. Reference sensitivity level is -85 dBm.
3. Filter is characterized as a symmetric bandpass centered on the adjacent channel having a 3dB bandwidth of 4.6 MHz and stop-band rejection better than 26 dB beyond 3.15 MHz from the adjacent carrier.
4. Due to low-IF frequency, there is some overlap of adjacent channel and image channel bands. Adjacent channel CW blocker tests place the Interferer center frequency at the Desired frequency \pm 5 MHz on the channel raster, whereas the image rejection test places the CW interferer near the image frequency of the Desired signal carrier, regardless of the channel raster.
5. This is an IEEE 802.11b/g ERP-PBCC 22 MBit/s signal as defined by the IEEE 802.11 specification and IEEE 802.11g addendum.

4.1.10 Sub-GHz RF Transceiver Characteristics

4.1.10.1 Sub-GHz RF Transmitter characteristics for 915 MHz Band

Unless otherwise indicated, typical conditions are: $T = 25^\circ\text{C}$, $V_{REGVDD} = AVDD = IOVDD = 3.3\text{ V}$, $DVDD = RFVDD = \text{External PA Supply}$. RFVDD and external PA supply paths filtered using ferrites. Crystal frequency = 38.4 MHz. RF center frequency 915 MHz.

Table 4.20. Sub-GHz RF Transmitter characteristics for 915 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		902	—	930	MHz
Maximum TX Power ¹	$POUT_{MAX}$	External PA supply = 3.3V, 20 dBm output power setting	18	19.8	23.3	dBm
		External PA supply connected to DC-DC output, 14 dBm output power setting	12.6	14.2	16.1	dBm
Minimum active TX Power	$POUT_{MIN}$		—	-45.5	—	dBm
Output power step size	$POUT_{STEP}$	output power > 0 dBm	—	0.5	—	dB
Output power variation vs supply at $POUT_{MAX}$	$POUT_{VAR_V}$	1.8 V < $V_{VREGVDD}$ < 3.3 V, External PA supply = 3.3 V, $T = 25^\circ\text{C}$	—	4.8	—	dB
		1.8 V < $V_{VREGVDD}$ < 3.3 V, External PA supply connected to DC-DC output, $T = 25^\circ\text{C}$	—	1.9	—	dB
Output power variation vs temperature, peak to peak	$POUT_{VAR_T}$	-40 to +85 °C with External PA supply = 3.3 V	—	0.6	1.3	dB
		-40 to +85 °C with External PA supply connected to DC-DC output	—	0.7	1.4	dB
Output power variation vs RF frequency	$POUT_{VAR_F}$	External PA supply = 3.3 V, $T = 25^\circ\text{C}$	—	0.2	0.6	dB
		External PA supply connected to DC-DC output, $T = 25^\circ\text{C}$	—	0.3	0.6	dB
Spurious emissions of harmonics at 20 dBm output power, Conducted measurement, 20dBm match, External PA supply = 3.3V, Test Frequency = 915 MHz	$SPUR_{HARM_FCC_20}$	In restricted bands, per FCC Part 15.205 / 15.209	—	-45	-42	dBm
		In non-restricted bands, per FCC Part 15.247	—	-26	-20	dBc
Spurious emissions out-of-band at 20 dBm output power, Conducted measurement, 20dBm match, External PA supply = 3.3V, Test Frequency = 915 MHz	$SPUR_{OOB_FCC_20}$	In non-restricted bands, per FCC Part 15.247	—	-26	-20	dBc
		In restricted bands (30-88 MHz), per FCC Part 15.205 / 15.209	—	-62	-56	dBm
		In restricted bands (88-216 MHz), per FCC Part 15.205 / 15.209	—	-61	-56	dBm
		In restricted bands (216-960 MHz), per FCC Part 15.205 / 15.209	—	-58	-52	dBm
		In restricted bands (>960 MHz), per FCC Part 15.205 / 15.209	—	-47	-42	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
Spurious emissions of harmonics at 14 dBm output power, Conducted measurement, 14dBm match, External PA supply connected to DC-DC output, Test Frequency = 915 MHz	SPUR _{HARM_FCC_14}	In restricted bands, per FCC Part 15.205 / 15.209	—	-47	-42	dBm	
		In non-restricted bands, per FCC Part 15.247	—	-26	-20	dBc	
Spurious emissions out-of-band at 14 dBm output power, Conducted measurement, 14dBm match, External PA supply connected to DC-DC output, Test Frequency = 915 MHz	SPUR _{OOB_FCC_14}	In non-restricted bands, per FCC Part 15.247	—	-26	-20	dBc	
		In restricted bands (30-88 MHz), per FCC Part 15.205 / 15.209	—	-62	-56	dBm	
		In restricted bands (88-216 MHz), per FCC Part 15.205 / 15.209	—	-61	-56	dBm	
		In restricted bands (216-960 MHz), per FCC Part 15.205 / 15.209	—	-58	-52	dBm	
		In restricted bands (>960 MHz), per FCC Part 15.205 / 15.209	—	-45	-42	dBm	
Error vector magnitude (offset EVM), per 802.15.4-2011	EVM	Signal is DSSS-OQPSK reference packet. Modulated according to 802.15.4-2011 DSSS-OQPSK in the 915MHz band, with pseudo-random packet data content. External PA supply = 3.3V.	—	1.0	2.8	%rms	
Power spectral density limit ²	PSD	Relative, at carrier ± 1.2 MHz. Average spectral power shall be measured using a 100kHz resolution bandwidth. The reference level shall be the highest average spectral power measured within ± 600 kHz of the carrier frequency. External PA supply = 3.3V.	—	-37.1	-24.8	dBc/100kHz	
		Absolute, at carrier ± 1.2 MHz. Average spectral power shall be measured using a 100kHz resolution bandwidth. External PA supply = 3.3V.	—	-24.2	-20	dBm/100kHz	
Note:							
<ol style="list-style-type: none"> Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table. Definition of reference signal is O-QPSK DSSS per 802.15.4, Frequency Range = 902-928 MHz, Data rate = 250 kbps, 16-chip PN sequence mapping. 							

4.1.10.2 Sub-GHz RF Receiver Characteristics for 915 MHz Band

Unless otherwise indicated, typical conditions are: $T = 25^\circ\text{C}$, $\text{VREGVDD} = \text{AVDD} = \text{IOVDD} = 3.3\text{ V}$, $\text{DVDD} = \text{RFVDD} = \text{External PA Supply}$. RFVDD and external PA supply paths filtered using ferrites. Crystal frequency = 38.4 MHz. RF center frequency 915 MHz.

Table 4.21. Sub-GHz RF Receiver Characteristics for 915 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Tuning frequency range	F_{RANGE}		902	—	930	MHz
Max usable input level, 0.1% BER	$\text{SAT}_{500\text{K}}$	Desired is reference 500 kbps GFSK signal ¹	—	10	—	dBm
Sensitivity	SENS	Desired is reference 4.8 kbps OOK signal ² , 20% PER, $T \leq 85^\circ\text{C}$	—	-105.2	-100.7	dBm
		Desired is reference 600 bps GFSK signal ³ , 0.1% BER	—	-126.2	—	dBm
		Desired is reference 50 kbps GFSK signal ⁴ , 0.1% BER, $T \leq 85^\circ\text{C}$	—	-108.2	-104.2	dBm
		Desired is reference 100 kbps GFSK signal ⁵ , 0.1% BER, $T \leq 85^\circ\text{C}$	—	-105.1	-101.5	dBm
		Desired is reference 500 kbps GFSK signal ¹ , 0.1% BER, $T \leq 85^\circ\text{C}$	—	-98.2	-93.2	dBm
		Desired is reference 400 kbps 4GFSK signal ⁶ , 1% PER, $T \leq 85^\circ\text{C}$	—	-95.2	-91	dBm
Level above which RFSENSE will trigger ⁸	$\text{RFSENSE}_{\text{TRIG}}$	CW at 915 MHz	—	-28.1	—	dBm
	$\text{RFSENSE}_{\text{THRES}}$	CW at 915 MHz	—	-50	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Adjacent channel selectivity, Interferer is CW at $\pm 1 \times$ channel-spacing	C/I ₁	Desired is 4.8 kbps OOK signal ² at 3dB above sensitivity level, 20% PER	—	48.1	—	dB
		Desired is 600 bps GFSK signal ³ at 3dB above sensitivity level, 0.1% BER	—	71.4	—	dB
		Desired is 50 kbps GFSK signal ⁴ at 3dB above sensitivity level, 0.1% BER	—	49.8	—	dB
		Desired is 100 kbps GFSK signal ⁵ at 3dB above sensitivity level, 0.1% BER	—	51.1	—	dB
		Desired is 500 kbps GFSK signal ¹ at 3dB above sensitivity level, 0.1% BER	—	48.1	—	dB
		Desired is 400 kbps 4GFSK signal ⁶ at 3dB above sensitivity level, 0.1% BER	—	41.4	—	dB
		Desired is reference O-QPSK DSSS signal ⁷ at 3dB above sensitivity level, 1% PER	—	49.1	—	dB
Alternate channel selectivity, Interferer is CW at $\pm 2 \times$ channel-spacing	C/I ₂	Desired is 4.8 kbps OOK signal ² at 3dB above sensitivity level, 20% PER	—	56.3	—	dB
		Desired is 600 bps GFSK signal ³ at 3dB above sensitivity level, 0.1% BER	—	74.7	—	dB
		Desired is 50 kbps GFSK signal ⁴ at 3dB above sensitivity level, 0.1% BER	—	55.8	—	dB
		Desired is 100 kbps GFSK signal ⁵ at 3dB above sensitivity level, 0.1% BER	—	56.4	—	dB
		Desired is 500 kbps GFSK signal ¹ at 3dB above sensitivity level, 0.1% BER	—	51.8	—	dB
		Desired is 400 kbps 4GFSK signal ⁶ at 3dB above sensitivity level, 0.1% BER	—	46.8	—	dB
		Desired is reference O-QPSK DSSS signal ⁷ at 3dB above sensitivity level, 1% PER	—	57.7	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Image rejection, Interferer is CW at image frequency	C/I _{IMAGE}	Desired is 4.8 kbps OOK signal ² at 3dB above sensitivity level, 20% PER	—	48.4	—	dB
		Desired is 50 kbps GFSK signal ⁴ at 3dB above sensitivity level, 0.1% BER	—	54.9	—	dB
		Desired is 100 kbps GFSK signal ⁵ at 3dB above sensitivity level, 0.1% BER	—	49.1	—	dB
		Desired is 500 kbps GFSK signal ¹ at 3dB above sensitivity level, 0.1% BER	—	47.9	—	dB
		Desired is 400 kbps 4GFSK signal ⁶ at 3dB above sensitivity level, 0.1% BER	—	42.8	—	dB
		Desired is reference O-QPSK DSSS signal ⁷ at 3dB above sensitivity level, 1% PER	—	48.9	—	dB
Blocking selectivity, 0.1% BER. Desired is 100 kbps GFSK signal at 3dB above sensitivity level	C/I _{BLOCKER}	Interferer CW at Desired \pm 1 MHz	—	58.7	—	dB
		Interferer CW at Desired \pm 2 MHz	—	62.5	—	dB
		Interferer CW at Desired \pm 10 MHz	—	76.4	—	dB
Intermod selectivity, 0.1% BER. CW interferers at 400 kHz and 800 kHz offsets	C/I _{IM}	Desired is 100 kbps GFSK signal ⁵ at 3dB above sensitivity level	—	45	—	dB
Upper limit of input power range over which RSSI resolution is maintained	RSSI _{MAX}		—	—	5	dBm
Lower limit of input power range over which RSSI resolution is maintained	RSSI _{MIN}		-98	—	—	dBm
RSSI resolution	RSSI _{RES}	Over RSSI _{MIN} to RSSI _{MAX} range	—	0.25	—	dBm
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	SPUR _{RX_FCC}	216-960 MHz	—	-55	-49.2	dBm
		Above 960 MHz	—	-47	-41.2	dBm
Max spurious emissions during active receive mode, per ARIB STD-T108 Section 3.3	SPUR _{RX_ARIB}	Below 710 MHz, RBW=100kHz	—	-60	-54	dBm
		710-900 MHz, RBW=1MHz	—	-61	-55	dBm
		900-915 MHz, RBW=100kHz	—	-61	-55	dBm
		915-930 MHz, RBW=100kHz	—	-61	-55	dBm
		930-1000 MHz, RBW=100kHz	—	-61	-55	dBm
		Above 1000 MHz, RBW=1MHz	—	-53	-47	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note:						
1. Definition of reference signal is 500 kbps 2GFSK, BT=0.5, Δf = 175 kHz, RX channel BW = 835.076 kHz, channel spacing = 1 MHz.						
2. Definition of reference signal is 4.8 kbps OOK, RX channel BW = 306.036 kHz, channel spacing = 500 kHz.						
3. Definition of reference signal is 600 bps 2GFSK, BT=0.5, Δf = 0.3 kHz, RX channel BW = 1.2 kHz, channel spacing = 300 kHz.						
4. Definition of reference signal is 50 kbps 2GFSK, BT=0.5, Δf = 25 kHz, RX channel BW = 99.012 kHz, channel spacing = 200 kHz.						
5. Definition of reference signal is 100 kbps 2GFSK, BT=0.5, Δf = 50 kHz, RX channel BW = 198.024 kHz, channel spacing = 400 kHz.						
6. Definition of reference signal is 400 kbps 4GFSK, BT=0.5, inner deviation = 33.3 kHz, RX channel BW = 368.920 kHz, channel spacing = 600 kHz.						
7. Definition of reference signal is O-QPSK DSSS per 802.15.4, Frequency Range = 902-928 MHz, Data rate = 250 kbps, 16-chip PN sequence mapping.						
8. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.						

4.1.10.3 Sub-GHz RF Transmitter characteristics for 868 MHz Band

Unless otherwise indicated, typical conditions are: $T = 25^\circ\text{C}$, $\text{VREGVDD} = \text{AVDD} = \text{IOVDD} = 3.3\text{ V}$, $\text{DVDD} = \text{RFVDD} = \text{External PA Supply}$. RFVDD and external PA supply paths filtered using ferrites. Crystal frequency = 38.4 MHz. RF center frequency 868 MHz.

Table 4.22. Sub-GHz RF Transmitter characteristics for 868 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		863	—	876	MHz
Maximum TX Power ¹	POUT_{MAX}	External PA supply = 3.3V, 20 dBm output power setting, $T \leq 85^\circ\text{C}$	17.1	19.3	22.9	dBm
		External PA supply connected to DC-DC output, 14 dBm output power setting	11.4	13.7	16.5	dBm
Minimum active TX Power	POUT_{MIN}		—	-43.5	—	dBm
Output power step size	$\text{POUT}_{\text{STEP}}$	output power > 0 dBm	—	0.5	—	dB
Output power variation vs supply at POUT_{MAX}	$\text{POUT}_{\text{VAR_V}}$	1.8 V < $\text{V}_{\text{VREGVDD}}$ < 3.3 V, External PA supply = 3.3 V, $T = 25^\circ\text{C}$	—	5	—	dB
		1.8 V < $\text{V}_{\text{VREGVDD}}$ < 3.3 V, External PA supply connected to DC-DC output, $T = 25^\circ\text{C}$	—	2	—	dB
Output power variation vs temperature, peak to peak	$\text{POUT}_{\text{VAR_T}}$	-40 to +85 °C with External PA supply = 3.3 V	—	0.6	0.9	dB
		-40 to +85 °C with External PA supply connected to DC-DC output	—	0.5	1.2	dB
Output power variation vs RF frequency	$\text{POUT}_{\text{VAR_F}}$	External PA supply = 3.3 V, $T = 25^\circ\text{C}$	—	0.2	0.6	dB
		External PA supply connected to DC-DC output, $T = 25^\circ\text{C}$	—	0.2	0.8	dB
Spurious emissions of harmonics, Conducted measurement, External PA supply connected to DC-DC output, Test Frequency = 868 MHz	$\text{SPUR}_{\text{HARM_ETSI}}$	Per ETSI EN 300-220, Section 7.8.2.1	—	-35	-30	dBm
Spurious emissions out-of-band, Conducted measurement, External PA supply connected to DC-DC output, Test Frequency = 868 MHz	$\text{SPUR}_{\text{OOB_ETSI}}$	Per ETSI EN 300-220, Section 7.8.2.1 (47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz)	—	-59	-54	dBm
		Per ETSI EN 300-220, Section 7.8.2.1 (other frequencies below 1 GHz)	—	-42	-36	dBm
		Per ETSI EN 300-220, Section 7.8.2.1 (frequencies above 1 GHz)	—	-36	-30	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Error vector magnitude (offset EVM), per 802.15.4-2015	EVM	Signal is DSSS-BPSK reference packet. Modulated according to 802.15.4-2015 DSSS-BPSK in the 868MHz band, with pseudo-random packet data content. External PA supply connected to external 3.3V supply	—	5.7	—	%rms

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.

4.1.10.4 Sub-GHz RF Receiver Characteristics for 868 MHz Band

Unless otherwise indicated, typical conditions are: $T = 25^\circ\text{C}$, $\text{VREGVDD} = \text{AVDD} = \text{IOVDD} = 3.3\text{ V}$, $\text{DVDD} = \text{RFVDD} = \text{External PA Supply}$. RFVDD and external PA supply paths filtered using ferrites. Crystal frequency = 38.4 MHz. RF center frequency 868 MHz.

Table 4.23. Sub-GHz RF Receiver Characteristics for 868 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Tuning frequency range	F_{RANGE}		863	—	876	MHz
Max usable input level, 0.1% BER	$\text{SAT}_{2\text{k}4}$	Desired is reference 2.4 kbps GFSK signal ¹	—	10	—	dBm
Max usable input level, 0.1% BER	$\text{SAT}_{38\text{k}4}$	Desired is reference 38.4 kbps GFSK signal ²	—	10	—	dBm
Sensitivity	SENS	Desired is reference 2.4 kbps GFSK signal ¹ , 0.1% BER	—	-120.6	—	dBm
		Desired is reference 38.4 kbps GFSK signal ² , 0.1% BER, $T \leq 85^\circ\text{C}$	—	-109.5	-105.4	dBm
		Desired is reference 500 kbps GFSK signal ³ , 0.1% BER	—	-96.4	—	dBm
		Desired is reference BPSK signal ⁴ , 1% PER	—	-110.6	—	dBm
Level above which RFSENSE will trigger ⁵	$\text{RFSENSE}_{\text{TRIG}}$	CW at 868 MHz	—	-28.1	—	dBm
Level below which RFSENSE will not trigger ⁵	$\text{RFSENSE}_{\text{THRES}}$	CW at 868 MHz	—	-50	—	dBm
Adjacent channel selectivity, Interferer is CW at $\pm 1 \times$ channel-spacing	C/I ₁	Desired is 2.4 kbps GFSK signal ¹ at 3dB above sensitivity level, 0.1% BER	44.5	56.9	—	dB
		Desired is 38.4kbps GFSK signal ² at 3dB above sensitivity level, 0.1% BER	35.4	43	—	dB
Alternate channel selectivity, Interferer is CW at $\pm 2 \times$ channel-spacing	C/I ₂	Desired is 2.4kbps GFSK signal ¹ at 3dB above sensitivity level, 0.1% BER	—	56.8	—	dB
		Desired is 38.4kbps GFSK signal ² at 3dB above sensitivity level, 0.1% BER	—	48.2	—	dB
Image rejection, Interferer is CW at image frequency	C/I _{IMAGE}	Desired is 2.4kbps GFSK signal ¹ at 3dB above sensitivity level, 0.1% BER	—	50.2	—	dB
		Desired is 38.4kbps GFSK signal ² at 3dB above sensitivity level, 0.1% BER	—	48.7	—	dB
Blocking selectivity, 0.1% BER. Desired is 2.4 kbps GFSK signal ¹ at 3 dB above sensitivity level	C/I _{BLOCKER}	Interferer CW at Desired ± 1 MHz	—	72.1	—	dB
		Interferer CW at Desired ± 2 MHz	—	77.5	—	dB
		Interferer CW at Desired ± 10 MHz	—	90.4	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Upper limit of input power range over which RSSI resolution is maintained	RSSI _{MAX}		—	—	5	dBm
Lower limit of input power range over which RSSI resolution is maintained	RSSI _{MIN}		-98	—	—	dBm
RSSI resolution	RSSI _{RES}	Over RSSI _{MIN} to RSSI _{MAX} range	—	0.25	—	dBm
Max spurious emissions during active receive mode	SPUR _{RX}	30 MHz to 1 GHz	—	-63	-57	dBm
		1 GHz to 12 GHz	—	-53	-47	dBm

Note:

1. Definition of reference signal is 2.4 kbps 2GFSK, BT=0.5, Δf = 1.2 kHz, RX channel BW = 4.797 kHz, channel spacing = 12.5 kHz.
2. Definition of reference signal is 38.4 kbps 2GFSK, BT=0.5, Δf = 20 kHz, RX channel BW = 74.809 kHz, channel spacing = 100 kHz.
3. Definition of reference signal is 500 kbps 2GFSK, BT=0.5, Δf = 125 kHz, RX channel BW = 753.320 kHz.
4. Definition of reference signal is 20 kbps BPSK
5. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.

4.1.10.5 Sub-GHz RF Transmitter characteristics for 490 MHz Band

Unless otherwise indicated, typical conditions are: $T = 25^\circ\text{C}$, $\text{VREGVDD} = \text{AVDD} = \text{IOVDD} = 3.3\text{ V}$, $\text{DVDD} = \text{RFVDD} = \text{External PA Supply}$. RFVDD and external PA supply paths filtered using ferrites. Crystal frequency = 38.4 MHz. RF center frequency 490 MHz.

Table 4.24. Sub-GHz RF Transmitter characteristics for 490 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		470	—	510	MHz
Maximum TX Power ¹	POUT_{MAX}	External PA supply = 3.3V	18.1	20.3	23.7	dBm
Minimum active TX Power	POUT_{MIN}			-44.9	—	dBm
Output power step size	$\text{POUT}_{\text{STEP}}$	output power > 0 dBm	—	0.5	—	dB
Output power variation vs supply, peak to peak	$\text{POUT}_{\text{VAR_V}}$	at 20 dBm; $1.8\text{ V} < \text{V}_{\text{VREGVDD}} < 3.3\text{ V}$, External PA supply connected directly to external supply, $T = 25^\circ\text{C}$	—	4.3	—	dB
Output power variation vs temperature, peak to peak	$\text{POUT}_{\text{VAR_T}}$	-40 to +85 °C at 20 dBm	—	0.2	0.9	dB
Output power variation vs RF frequency	$\text{POUT}_{\text{VAR_F}}$	$T = 25^\circ\text{C}$	—	0.2	0.4	dB
Harmonic emissions, 20 dBm output power setting, 490 MHz	$\text{SPUR}_{\text{HARM_CN}}$	Per China SRW Requirement, Section 2.1, frequencies below 1GHz	—	-40	-36	dBm
		Per China SRW Requirement, Section 2.1, frequencies above 1GHz	—	-36	-30	dBm
Spurious emissions, 20 dBm output power setting, 490 MHz	$\text{SPUR}_{\text{OOB_CN}}$	Per China SRW Requirement, Section 3 (48.5-72.5MHz, 76-108MHz, 167-223MHz, 470-556MHz, and 606-798MHz)	—	-54	—	dBm
		Per China SRW Requirement, Section 2.1 (other frequencies below 1GHz)	—	-42	—	dBm
		Per China SRW Requirement, Section 2.1 (frequencies above 1GHz)	—	-36	—	dBm

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.

4.1.10.6 Sub-GHz RF Receiver Characteristics for 490 MHz Band

Unless otherwise indicated, typical conditions are: $T = 25^\circ\text{C}$, $\text{VREGVDD} = \text{AVDD} = \text{IOVDD} = 3.3\text{ V}$, $\text{DVDD} = \text{RFVDD} = \text{External PA Supply}$. RFVDD and external PA supply paths filtered using ferrites. Crystal frequency = 38.4 MHz. RF center frequency 490 MHz.

Table 4.25. Sub-GHz RF Receiver Characteristics for 490 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Tuning frequency range	F_{RANGE}		470	—	510	MHz
Max usable input level, 0.1% BER	$\text{SAT}_{2\text{k}4}$	Desired is reference 2.4 kbps GFSK signal ¹	—	10	—	dBm
Max usable input level, 0.1% BER	$\text{SAT}_{38\text{k}4}$	Desired is reference 38.4 kbps GFSK signal ²	—	10	—	dBm
Sensitivity	SENS	Desired is reference 2.4 kbps GFSK signal ¹ , 0.1% BER	—	-122.2	—	dBm
		Desired is reference 38.4 kbps GFSK signal ² , 0.1% BER, $T \leq 85^\circ\text{C}$	—	-111.4	-108.9	dBm
		Desired is reference 10 kbps GFSK signal ³ , 0.1% BER, $T \leq 85^\circ\text{C}$	—	-116.8	-113.9	dBm
		Desired is reference 100 kbps GFSK signal ⁴ , 0.1% BER, $T \leq 85^\circ\text{C}$	—	-107.3	-104.7	dBm
Level above which RFSENSE will trigger ⁵	$\text{RFSENSE}_{\text{TRIG}}$	Desired is reference 100 kbps GFSK signal ⁴ , 0.1% BER	—	-28.1	—	dBm
Level below which RFSENSE will not trigger ⁵	$\text{RFSENSE}_{\text{THRES}}$	CW at 490 MHz	—	-50	—	dBm
Adjacent channel selectivity, Interferer is CW at $\pm 1 \times$ channel-spacing	C/I ₁	Desired is 2.4 kbps GFSK signal ¹ at 3dB above sensitivity level, 0.1% BER	48	60.3	—	dB
		Desired is 38.4kbps GFSK signal ² at 3dB above sensitivity level, 0.1% BER	38.3	45.6	—	dB
Alternate channel selectivity, Interferer is CW at $\pm 2 \times$ channel-spacing	C/I ₂	Desired is 2.4kbps GFSK signal ¹ at 3dB above sensitivity level, 0.1% BER	—	60.4	—	dB
		Desired is 38.4kbps GFSK signal ² at 3dB above sensitivity level, 0.1% BER	—	52.6	—	dB
Image rejection, Interferer is CW at image frequency	C/I _{IMAGE}	Desired is 2.4kbps GFSK signal ¹ at 3dB above sensitivity level, 0.1% BER	—	56.5	—	dB
		Desired is 38.4kbps GFSK signal ² at 3dB above sensitivity level, 0.1% BER	—	54.1	—	dB
Blocking selectivity, 0.1% BER. Desired is 2.4 kbps GFSK signal ¹ at 3 dB above sensitivity level	C/I _{BLOCKER}	Interferer CW at Desired ± 1 MHz	—	73.9	—	dB
		Interferer CW at Desired ± 2 MHz	—	75.4	—	dB
		Interferer CW at Desired ± 10 MHz	—	90.2	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Upper limit of input power range over which RSSI resolution is maintained	RSSI _{MAX}		—	—	5	dBm
Lower limit of input power range over which RSSI resolution is maintained	RSSI _{MIN}		-98	—	—	dBm
RSSI resolution	RSSI _{RES}	Over RSSI _{MIN} to RSSI _{MAX} range	—	0.25	—	dBm
Max spurious emissions during active receive mode	SPUR _{RX}	30 MHz to 1 GHz	—	-53	-47	dBm
		1 GHz to 12 GHz	—	-53	-47	dBm

Note:

1. Definition of reference signal is 2.4 kbps 2GFSK, BT=0.5, Δf = 1.2 kHz, RX channel BW = 4.798 kHz, channel spacing = 12.5 kHz.
2. Definition of reference signal is 38.4 kbps 2GFSK, BT=0.5, Δf = 20 kHz, RX channel BW = 74.809 kHz, channel spacing = 100 kHz.
3. Definition of reference signal is 10 kbps 2GFSK, BT=0.5, Δf = 5 kHz, RX channel BW = 20.038 kHz.
4. Definition of reference signal is 100 kbps 2GFSK, BT=0.5, Δf = 50 kHz, RX channel BW = 198.024 kHz.
5. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.

4.1.10.7 Sub-GHz RF Transmitter characteristics for 433 MHz Band

Unless otherwise indicated, typical conditions are: $T = 25^\circ\text{C}$, $V_{REGVDD} = AVDD = IOVDD = 3.3\text{ V}$, $DVDD = RFVDD = \text{External PA Supply}$. RFVDD and external PA supply paths filtered using ferrites. Crystal frequency = 38.4 MHz. RF center frequency 433 MHz.

Table 4.26. Sub-GHz RF Transmitter characteristics for 433 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		426	—	445	MHz
Maximum TX Power ¹	$POUT_{MAX}$	External PA supply connected to DC-DC output, 14dBm output power	12.5	15.1	17.4	dBm
		External PA supply connected to DC-DC output, 10dBm output power	8.3	10.6	13.3	dBm
Minimum active TX Power	$POUT_{MIN}$		—	-42	—	dBm
Output power step size	$POUT_{STEP}$	output power > 0 dBm	—	0.5	—	dB
Output power variation vs supply, peak to peak, $Pout = 10\text{dBm}$	$POUT_{VAR_V}$	At 10 dBm; $1.8\text{ V} < V_{REGVDD} < 3.3\text{ V}$, External PA supply = DC-DC output, $T = 25^\circ\text{C}$	—	1.7	—	dB
Output power variation vs temperature, peak to peak, $Pout = 10\text{dBm}$	$POUT_{VAR_T}$	-40 to +85C at 10dBm	—	0.5	1.2	dB
Output power variation vs RF frequency, $Pout = 10\text{dBm}$	$POUT_{VAR_F}$	$T = 25^\circ\text{C}$	—	0.1	0.2	dB
Spurious emissions of harmonics FCC, Conducted measurement, 14dBm match, External PA supply connected to DC-DC output, Test Frequency = 434 MHz	$SPUR_{HARM_FCC}$	In restricted bands, per FCC Part 15.205 / 15.209	—	-47	-42	dBm
		In non-restricted bands, per FCC Part 15.231	—	-26	-20	dBc
Spurious emissions out-of-band FCC, Conducted measurement, 14dBm match, External PA supply connected to DC-DC output, Test Frequency = 434 MHz	$SPUR_{OOB_FCC}$	In non-restricted bands, per FCC Part 15.231	—	-26	-20	dBc
		In restricted bands (30-88 MHz), per FCC Part 15.205 / 15.209	—	-52	-46	dBm
		In restricted bands (88-216 MHz), per FCC Part 15.205 / 15.209	—	-61	-56	dBm
		In restricted bands (216-960 MHz), per FCC Part 15.205 / 15.209	—	-58	-52	dBm
		In restricted bands (>960 MHz), per FCC Part 15.205 / 15.209	—	-47	-42	dBm
Spurious emissions of harmonics ETSI, Conducted measurement, 14dBm match, External PA supply connected to DC-DC output, Test Frequency = 434 MHz	$SPUR_{HARM_ETSI}$	Per ETSI EN 300-220, Section 7.8.2.1 (frequencies below 1Ghz)	—	-42	-36	dBm
		Per ETSI EN 300-220, Section 7.8.2.1 (frequencies above 1Ghz)	—	-36	-30	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band ETSI, Conducted measurement, 14dBm match, External PA supply connected to DC-DC output, Test Frequency = 434 MHz	SPUR _{OOB_ETS} I	Per ETSI EN 300-220, Section 7.8.2.1 (47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz)	—	-60	-54	dBm
		Per ETSI EN 300-220, Section 7.8.2.1 (other frequencies below 1 GHz)	—	-42	-36	dBm
		Per ETSI EN 300-220, Section 7.8.2.1 (frequencies above 1 GHz)	—	-36	-30	dBm

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.

4.1.10.8 Sub-GHz RF Receiver Characteristics for 433 MHz Band

Unless otherwise indicated, typical conditions are: $T = 25^\circ\text{C}$, $\text{VREGVDD} = \text{AVDD} = \text{IOVDD} = 3.3\text{ V}$, $\text{DVDD} = \text{RFVDD} = \text{External PA Supply}$. RFVDD and external PA supply paths filtered using ferrites. Crystal frequency = 38.4 MHz. RF center frequency 433 MHz.

Table 4.27. Sub-GHz RF Receiver Characteristics for 433 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Tuning frequency range	F_{RANGE}		426	—	445	MHz
Max usable input level, 0.1% BER	$\text{SAT}_{2\text{k4}}$	Desired is reference 2.4 kbps GFSK signal ¹	—	10	—	dBm
Max usable input level, 0.1% BER	$\text{SAT}_{50\text{k}}$	Desired is reference 50 kbps GFSK signal ²	—	10	—	dBm
Sensitivity	SENS	Desired is reference 4.8 kbps OOK signal ³ , 20% PER	—	-107.4	—	dBm
		Desired is reference 100 kbps GFSK signal ⁴ , 0.1% BER, $T \leq 85^\circ\text{C}$	—	-107.3	-105	dBm
		Desired is reference 50 kbps GFSK signal ² , 0.1% BER, $T \leq 85^\circ\text{C}$	—	-110.3	-107.2	dBm
		Desired is reference 2.4 kbps GFSK signal ¹ , 0.1% BER	—	-123.1	—	dBm
		Desired is reference 9.6 kbps GFSK signal ⁵ , 1% PER, $T \leq 85^\circ\text{C}$	—	-112.6	-109	dBm
Level above which RFSENSE will trigger ⁶	$\text{RFSENSE}_{\text{TRIG}}$	CW at 433 MHz	—	-28.1	—	dBm
Level below which RFSENSE will not trigger ⁶	$\text{RFSENSE}_{\text{THRES}}$	CW at 433 MHz	—	-50	—	dBm
Adjacent channel selectivity, Interferer is CW at $\pm 1 \times$ channel-spacing	C/I ₁	Desired is 4.8 kbps OOK signal ³ at 3dB above sensitivity level, 20% PER	—	51.6	—	dB
		Desired is 100 kbps GFSK signal ⁴ at 3dB above sensitivity level, 0.1% BER	35	44.1	—	dB
		Desired is 2.4 kbps GFSK signal ¹ at 3dB above sensitivity level, 0.1% BER	47	61.5	—	dB
		Desired is 50 kbps GFSK signal ² at 3dB above sensitivity level, 0.1% BER	45.6	53.1	—	dB
		Desired is 9.6 kbps 4GFSK signal ⁵ at 3dB above sensitivity level, 1% PER	—	35.7	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Alternate channel selectivity, Interferer is CW at $\pm 2 \times$ channel-spacing	C/I ₂	Desired is 4.8 kbps OOK signal ³ at 3dB above sensitivity level, 20% PER	—	57.8	—	dB
		Desired is 100 kbps GFSK signal ⁴ at 3dB above sensitivity level, 0.1% BER	—	54.6	—	dB
		Desired is 2.4 kbps GFSK signal ¹ at 3dB above sensitivity level, 0.1% BER	—	62.4	—	dB
		Desired is 50 kbps GFSK signal ² at 3dB above sensitivity level, 0.1% BER	—	58.1	—	dB
		Desired is 9.6 kbps 4GFSK signal ⁵ at 3dB above sensitivity level, 1% PER	—	50.6	—	dB
Image rejection, Interferer is CW at image frequency	C/I _{IMAGE}	Desired is 4.8 kbps OOK signal ³ at 3dB above sensitivity level, 20% PER	—	46.5	—	dB
		Desired is 100 kbps GFSK signal ⁴ at 3dB above sensitivity level, 0.1% BER	—	51.7	—	dB
		Desired is 2.4 kbps GFSK signal ¹ at 3dB above sensitivity level, 0.1% BER	—	57.5	—	dB
		Desired is 50 kbps GFSK signal ² at 3dB above sensitivity level, 0.1% BER	—	54.4	—	dB
		Desired is 9.6 kbps 4GFSK signal ⁵ at 3dB above sensitivity level, 1% PER	—	48	—	dB
Blocking selectivity, 0.1% BER. Desired is 2.4 kbps GFSK signal ¹ at 3dB above sensitivity level	C/I _{BLOCKER}	Interferer CW at Desired ± 1 MHz	—	75.7	—	dB
		Interferer CW at Desired ± 2 MHz	—	77.2	—	dB
		Interferer CW at Desired ± 10 MHz	—	92	—	dB
Intermod selectivity, 0.1% BER. CW interferers at 12.5 kHz and 25 kHz offsets	C/I _{IM}	Desired is 2.4 kbps GFSK signal ¹ at 3dB above sensitivity level	—	58.8	—	dB
Upper limit of input power range over which RSSI resolution is maintained	RSSI _{MAX}		—	—	5	dBm
Lower limit of input power range over which RSSI resolution is maintained	RSSI _{MIN}		-98	—	—	dBm
RSSI resolution	RSSI _{RES}	Over RSSI _{MIN} to RSSI _{MAX} range	—	0.25	—	dBm
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	SPUR _{RX_FCC}	216-960 MHz	—	-55	-49	dBm
		Above 960 MHz	—	-47	-41	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max spurious emissions during active receive mode, per ETSI 300-220 Section 8.6	SPUR _{RX_ETS}	Below 1000 MHz	—	-63	-57	dBm
		Above 1000 MHz	—	-53	-47	dBm
Max spurious emissions during active receive mode, per ARIB STD T67 Section 3.3(5)	SPUR _{RX_ARIB}	Below 710 MHz, RBW=100kHz	—	-60	-54	dBm

Note:

1. Definition of reference signal is 2.4 kbps 2GFSK, BT=0.5, Δf = 1.2 kHz, RX channel BW = 4.798 kHz, channel spacing = 12.5 kHz.
2. Definition of reference signal is 50 kbps 2GFSK, BT=0.5, Δf = 25 kHz, RX channel BW = 99.012 kHz, channel spacing = 200 kHz.
3. Definition of reference signal is 4.8 kbps OOK, RX channel BW = 306.036 kHz, channel spacing = 500 kHz.
4. Definition of reference signal is 100 kbps 2GFSK, BT=0.5, Δf = 50 kHz, RX channel BW = 198.024 kHz, channel spacing = 200 kHz.
5. Definition of reference signal is 9.6 kbps 4GFSK, BT=0.5, inner deviation = 0.8 kHz, RX channel BW = 8.5 kHz, channel spacing = 12.5 kHz.
6. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.

4.1.10.9 Sub-GHz RF Transmitter characteristics for 315 MHz Band

Unless otherwise indicated, typical conditions are: $T = 25^\circ\text{C}$, $\text{VREGVDD} = \text{AVDD} = \text{IOVDD} = 3.3\text{ V}$, $\text{DVDD} = \text{RFVDD} = \text{External PA Supply}$. RFVDD and external PA supply paths filtered using ferrites. Crystal frequency = 38.4 MHz. RF center frequency 315 MHz.

Table 4.28. Sub-GHz RF Transmitter characteristics for 315 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		195	—	358	MHz
Maximum TX Power ¹	POUT_{MAX}	External PA supply connected to DC-DC output, $T \leq 85^\circ\text{C}$	13.8	17.2	21.1	dBm
Minimum active TX Power	POUT_{MIN}			-43.9	—	dBm
Output power step size	$\text{POUT}_{\text{STEP}}$	output power > 0 dBm	—	0.5	—	dB
Output power variation vs supply	$\text{POUT}_{\text{VAR_V}}$	$1.8\text{ V} < \text{V}_{\text{VREGVDD}} < 3.3\text{ V}$, External PA supply = DC-DC output, $T = 25^\circ\text{C}$	—	1.8	—	dB
Output power variation vs temperature	$\text{POUT}_{\text{VAR_T}}$	-40 to +85C	—	0.5	1.2	dB
Output power variation vs RF frequency	$\text{POUT}_{\text{VAR_F}}$	$T = 25^\circ\text{C}$	—	0.1	0.7	dB
Spurious emissions of harmonics at 14 dBm output power, Conducted measurement, 14dBm match, External PA supply connected to DC-DC output, Test Frequency = 303 MHz	$\text{SPUR}_{\text{HARM_FCC}}$	In restricted bands, per FCC Part 15.205 / 15.209	—	-47	-42	dBm
		In non-restricted bands, per FCC Part 15.231	—	-26	-20	dBc
Spurious emissions out-of-band at 14 dBm output power, Conducted measurement, 14dBm match, External PA supply connected to DC-DC output, Test Frequency = 303 MHz	$\text{SPUR}_{\text{OOB_FCC}}$	In non-restricted bands, per FCC Part 15.231	—	-26	-20	dBc
		In restricted bands (30-88 MHz), per FCC Part 15.205 / 15.209	—	-52	-46	dBm
		In restricted bands (88-216 MHz), per FCC Part 15.205 / 15.209	—	-61	-56	dBm
		In restricted bands (216-960 MHz), per FCC Part 15.205 / 15.209	—	-58	-52	dBm
		In restricted bands (>960 MHz), per FCC Part 15.205 / 15.209	—	-47	-42	dBm

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.

4.1.10.10 Sub-GHz RF Receiver Characteristics for 315 MHz Band

Unless otherwise indicated, typical conditions are: $T = 25^\circ\text{C}$, $\text{VREGVDD} = \text{AVDD} = \text{IOVDD} = 3.3\text{ V}$, $\text{DVDD} = \text{RFVDD} = \text{External PA Supply}$. RFVDD and external PA supply paths filtered using ferrites. Crystal frequency = 38.4 MHz. RF center frequency 315 MHz.

Table 4.29. Sub-GHz RF Receiver Characteristics for 315 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Tuning frequency range	F_{RANGE}		195	—	358	MHz
Max usable input level, 0.1% BER	$\text{SAT}_{2\text{k}4}$	Desired is reference 2.4 kbps GFSK signal ¹	—	10	—	dBm
Max usable input level, 0.1% BER	$\text{SAT}_{38\text{k}4}$	Desired is reference 38.4 kbps GFSK signal ²	—	10	—	dBm
Sensitivity	SENS	Desired is reference 2.4 kbps GFSK signal ¹ , 0.1% BER, $T \leq 85^\circ\text{C}$	—	-123.2	-120.7	dBm
		Desired is reference 38.4 kbps GFSK signal ² , 0.1% BER, $T \leq 85^\circ\text{C}$	—	-111.4	-108.6	dBm
		Desired is reference 500 kbps GFSK signal ³ , 0.1% BER, $T \leq 85^\circ\text{C}$	—	-98.8	-95.5	dBm
Level above which RFSENSE will trigger ⁴	$\text{RFSENSE}_{\text{TRIG}}$	CW at 315 MHz	—	-28.1	—	dBm
Level below which RFSENSE will not trigger ⁴	$\text{RFSENSE}_{\text{THRES}}$	CW at 315 MHz	—	-50	—	dBm
Adjacent channel selectivity, Interferer is CW at $\pm 1 \times$ channel-spacing	C/I ₁	Desired is 2.4 kbps GFSK signal ¹ at 3dB above sensitivity level, 0.1% BER	54.1	63.6	—	dB
		Desired is 38.4kbps GFSK signal ² at 3dB above sensitivity level, 0.1% BER	—	49.9	—	dB
Alternate channel selectivity, Interferer is CW at $\pm 2 \times$ channel-spacing	C/I ₂	Desired is 2.4kbps GFSK signal ¹ at 3dB above sensitivity level, 0.1% BER	—	64.2	—	dB
		Desired is 38.4kbps GFSK signal ² at 3dB above sensitivity level ² , 0.1% BER	—	56.2	—	dB
Image rejection, Interferer is CW at image frequency	C/I _{IMAGE}	Desired is 2.4kbps GFSK signal ¹ at 3dB above sensitivity level, 0.1% BER	—	53	—	dB
		Desired is 38.4kbps GFSK signal ² at 3dB above sensitivity level, 0.1% BER	—	51.4	—	dB
Blocking selectivity, 0.1% BER. Desired is 2.4 kbps GFSK signal ¹ at 3 dB above sensitivity level	C/I _{BLOCKER}	Interferer CW at Desired ± 1 MHz	—	75	—	dB
		Interferer CW at Desired ± 2 MHz	—	76.5	—	dB
		Interferer CW at Desired ± 10 MHz	72.6	91.9	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Upper limit of input power range over which RSSI resolution is maintained	RSSI _{MAX}		—	—	5	dBm
Lower limit of input power range over which RSSI resolution is maintained	RSSI _{MIN}		-98	—	—	dBm
RSSI resolution	RSSI _{RES}	Over RSSI _{MIN} to RSSI _{MAX} range	—	0.25	—	dBm
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	SPUR _{RX_FCC}	216-960 MHz	—	-63	-57	dBm
		Above 960MHz	—	-53	-47	dBm

Note:

1. Definition of reference signal is 2.4 kbps 2GFSK, BT=0.5, Δf = 1.2 kHz, RX channel BW = 4.798 kHz, channel spacing = 12.5 kHz.
2. Definition of reference signal is 38.4 kbps 2GFSK, BT=0.5, Δf = 20 kHz, RX channel BW = 74.809 kHz, channel spacing = 100 kHz.
3. Definition of reference signal is 500 kbps 2GFSK, BT=0.5, Δf = 125 kHz, RX channel BW = 753.320 kHz.
4. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.

4.1.10.11 Sub-GHz RF Transmitter Characteristics for 169 MHz Band

Unless otherwise indicated, typical conditions are: $T = 25^\circ\text{C}$, $\text{VREGVDD} = \text{AVDD} = \text{IOVDD} = 3.3\text{ V}$, $\text{DVDD} = \text{RFVDD} = \text{External PA Supply}$. RFVDD and external PA supply paths filtered using ferrites. Crystal frequency = 38.4 MHz. RF center frequency 169 MHz.

Table 4.30. Sub-GHz RF Transmitter Characteristics for 169 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
RF tuning frequency range	F_{RANGE}		169	—	170	MHz	
Maximum TX Power ¹	POUT_{MAX}	External PA supply = 3.3 V	18.1	19.7	22.4	dBm	
Minimum active TX Power	POUT_{MIN}			-42.6	—	dBm	
Output power step size	$\text{POUT}_{\text{STEP}}$	output power > 0 dBm	—	0.5	—	dB	
Output power variation vs supply, peak to peak	$\text{POUT}_{\text{VAR_V}}$	$1.8\text{ V} < \text{V}_{\text{VREGVDD}} < 3.3\text{ V}$, External PA supply = 3.3 V, $T = 25^\circ\text{C}$	—	4.8	5.0	dB	
Output power variation vs temperature, peak to peak	$\text{POUT}_{\text{VAR_T}}$	-40 to +85 °C at 20 dBm	—	0.6	1.2	dB	
Spurious emissions of harmonics, Conducted measurement, External PA supply = 3.3 V, Test Frequency = 169 MHz	SPUR _{HARM_ETS}	Per ETSI EN 300-220, Section 7.8.2.1 (47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz)	—	-42	—	dBm	
		Per ETSI EN 300-220, Section 7.8.2.1 (other frequencies below 1 GHz) ²	—	-38	—	dBm	
		Per ETSI EN 300-220, Section 7.8.2.1 (frequencies above 1 GHz) ²	—	-36	—	dBm	
Spurious emissions out-of-band, Conducted measurement, External PA supply = 3.3 V, Test Frequency = 169 MHz	SPUR _{OOB_ETS}	Per ETSI EN 300-220, Section 7.8.2.1 (47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz)	—	-42	-36	dBm	
		Per ETSI EN 300-220, Section 7.8.2.1 (other frequencies below 1 GHz)	—	-42	-36	dBm	
		Per ETSI EN 300-220, Section 7.8.2.1 (frequencies above 1 GHz)	—	-36	-30	dBm	
Note:							
1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.							
2. Typical value marginally passes specification. Additional margin can be obtained by increasing the order of the harmonic filter.							

4.1.10.12 Sub-GHz RF Receiver Characteristics for 169 MHz Band

Unless otherwise indicated, typical conditions are: $T = 25^\circ\text{C}$, $\text{VREGVDD} = \text{AVDD} = \text{IOVDD} = 3.3\text{ V}$, $\text{DVDD} = \text{RFVDD} = \text{External PA Supply}$. RFVDD and external PA supply paths filtered using ferrites. Crystal frequency = 38.4 MHz. RF center frequency 169 MHz.

Table 4.31. Sub-GHz RF Receiver Characteristics for 169 MHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Tuning frequency range	F_{RANGE}		169	—	170	MHz
Max usable input level, 0.1% BER	$\text{SAT}_{2\text{k4}}$	Desired is reference 2.4 kbps GFSK signal ¹	—	10	—	dBm
Max usable input level, 0.1% BER	$\text{SAT}_{38\text{k4}}$	Desired is reference 38.4 kbps GFSK signal ²	—	10	—	dBm
Sensitivity	SENS	Desired is reference 2.4 kbps GFSK signal ¹ , 0.1% BER	—	-124	—	dBm
		Desired is reference 38.4 kbps GFSK signal ² , 0.1% BER, $T \leq 85^\circ\text{C}$	—	-112.2	-108	dBm
		Desired is reference 500 kbps GFSK signal ³ , 0.1% BER, $T \leq 85^\circ\text{C}$	—	-99.2	-96	dBm
Level above which RFSENSE will trigger ⁴	$\text{RFSENSE}_{\text{TRIG}}$	CW at 169 MHz	—	-28.1	—	dBm
Level below which RFSENSE will not trigger ⁴	$\text{RFSENSE}_{\text{THRES}}$	CW at 169 MHz	—	-50	—	dBm
Adjacent channel selectivity, Interferer is CW at $\pm 1 \times$ channel-spacing	C/I ₁	Desired is 2.4 kbps GFSK signal ¹ at 3dB above sensitivity level, 0.1% BER	—	64.8	—	dB
		Desired is 38.4kbps GFSK signal ¹ at 3dB above sensitivity level, 0.1% BER	43.3	51.4	—	dB
Alternate channel selectivity, Interferer is CW at $\pm 2 \times$ channel-spacing	C/I ₂	Desired is 2.4kbps GFSK signal ¹ at 3dB above sensitivity level, 0.1% BER	—	67.4	—	dB
		Desired is 38.4kbps GFSK signal ² at 3dB above sensitivity level, 0.1% BER	—	60.6	—	dB
Image rejection, Interferer is CW at image frequency	C/I _{IMAGE}	Desired is 2.4kbps GFSK signal ¹ at 3dB above sensitivity level, 0.1% BER	—	47.1	—	dB
		Desired is 38.4kbps GFSK signal ² at 3dB above sensitivity level, 0.1% BER	—	47.1	—	dB
Blocking selectivity, 0.1% BER. Desired is 2.4 kbps GFSK signal ¹ at 3 dB above sensitivity level	C/I _{BLOCKER}	Interferer CW at Desired ± 1 MHz	—	73.4	—	dB
		Interferer CW at Desired ± 2 MHz	—	75	—	dB
		Interferer CW at Desired ± 10 MHz	80	90.1	—	dB
Upper limit of input power range over which RSSI resolution is maintained	RSS _{MAX}		—	—	5	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
Lower limit of input power range over which RSSI resolution is maintained	RSSI _{MIN}		-98	—	—	dBm	
RSSI resolution	RSSI _{RES}	Over RSSI _{MIN} to RSSI _{MAX} range	—	0.25	—	dBm	
Max spurious emissions during active receive mode	SPUR _{RX}	30 MHz to 1 GHz	—	-63	-57	dBm	
		1 GHz to 12 GHz	—	-53	-47	dBm	
Note:							
1. Definition of reference signal is 2.4 kbps 2GFSK, BT=0.5, Δf = 1.2 kHz, RX channel BW = 4.798 kHz, channel spacing = 12.5 kHz. 2. Definition of reference signal is 38.4 kbps 2GFSK, BT=0.5, Δf = 20 kHz, RX channel BW = 74.809 kHz, channel spacing = 100 kHz. 3. Definition of reference signal is 500 kbps 2GFSK, BT=0.5, Δf = 125 kHz, RX channel BW = 753.320 kHz. 4. RFSENSE performance is only valid from 0 to 85 °C. RFSENSE should be disabled outside this temperature range.							

4.1.11 Modem

Table 4.32. Modem

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Receive bandwidth	BW _{RX}	Configurable range with 38.4 MHz crystal	0.1	—	2530	kHz
IF frequency	f _{IF}	Configurable range with 38.4 MHz crystal. Selected steps available.	150	—	1371	kHz
DSSS symbol length	SL _{DSSS}	Configurable in steps of 1 chip	2	—	32	chips
DSSS bits per symbol	BPS _{DSSS}	Configurable	1	—	4	bits/symbol

4.1.12 Oscillators

4.1.12.1 Low-Frequency Crystal Oscillator (LFXO)

Table 4.33. Low-Frequency Crystal Oscillator (LFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{LFXO}		—	32.768	—	kHz
Supported crystal equivalent series resistance (ESR)	ESR_{LFXO}		—	—	70	$k\Omega$
Supported range of crystal load capacitance ¹	C_{LFXO_CL}		6	—	18	pF
On-chip tuning cap range ²	C_{LFXO_T}	On each of LFXTAL_N and LFXTAL_P pins	8	—	40	pF
On-chip tuning cap step size	SS_{LFXO}		—	0.25	—	pF
Current consumption after startup ³	I_{LFXO}	$ESR = 70 \text{ kOhm}$, $C_L = 7 \text{ pF}$, $\text{GAIN}^4 = 2$, $\text{AGC}^4 = 1$	—	273	—	nA
Start- up time	t_{LFXO}	$ESR = 70 \text{ kOhm}$, $C_L = 7 \text{ pF}$, $\text{GAIN}^4 = 2$	—	308	—	ms

Note:

1. Total load capacitance as seen by the crystal.
2. The effective load capacitance seen by the crystal will be $C_{LFXO_T} / 2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.
3. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
4. In CMU_LFXOCTRL register.

4.1.12.2 High-Frequency Crystal Oscillator (HFXO)

Table 4.34. High-Frequency Crystal Oscillator (HFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{HFXO}	38.4 MHz required for radio transciever operation	38	38.4	40	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO_38M4}	Crystal frequency 38.4 MHz	—	—	60	Ω
Supported range of crystal load capacitance ¹	C_{HFXO_CL}		6	—	12	pF
On-chip tuning cap range ²	C_{HFXO_T}	On each of HFXTAL_N and HFXTAL_P pins	9	20	25	pF
On-chip tuning capacitance step	SS_{HFXO}		—	0.04	—	pF
Startup time	t_{HFXO}	38.4 MHz, ESR = 50 Ohm, C_L = 10 pF	—	300	—	μ s
Frequency tolerance for the crystal	FT_{HFXO}	38.4 MHz, ESR = 50 Ohm, C_L = 10 pF	-40	—	40	ppm
Note:						
1. Total load capacitance as seen by the crystal.						
2. The effective load capacitance seen by the crystal will be $C_{HFXO_T} / 2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.						

4.1.12.3 Low-Frequency RC Oscillator (LFRCO)

Table 4.35. Low-Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
Oscillation frequency	f_{LFRCO}	ENVREF ¹ = 1, $T \leq 85^{\circ}\text{C}$	31.3	32.768	33.6	kHz	
		ENVREF ¹ = 1, $T > 85^{\circ}\text{C}$	31.6	32.768	36.8	kHz	
		ENVREF ¹ = 0, $T \leq 85^{\circ}\text{C}$	31.3	32.768	33.4	kHz	
		ENVREF ¹ = 0, $T > 85^{\circ}\text{C}$	30.0	32.768	33.4	kHz	
Startup time	t_{LFRCO}		—	500	—	μ s	
Current consumption ²	I_{LFRCO}	ENVREF = 1 in CMU_LFRCOCTRL	—	370	—	nA	
		ENVREF = 0 in CMU_LFRCOCTRL	—	520	—	nA	
Note:							
1. In CMU_LFRCOCTRL register.							
2. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.							

4.1.12.4 High-Frequency RC Oscillator (HFRCO)

Table 4.36. High-Frequency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	f_{HFRCO_ACC}	At production calibrated frequencies, across supply voltage and temperature	-2.5	—	2.5	%
Start-up time	t_{HFRCO}	$f_{HFRCO} \geq 19 \text{ MHz}$	—	300	—	ns
		$4 < f_{HFRCO} < 19 \text{ MHz}$	—	1	—	μs
		$f_{HFRCO} \leq 4 \text{ MHz}$	—	2.5	—	μs
Current consumption on all supplies	I_{HFRCO}	$f_{HFRCO} = 38 \text{ MHz}$	—	244	265	μA
		$f_{HFRCO} = 32 \text{ MHz}$	—	204	222	μA
		$f_{HFRCO} = 26 \text{ MHz}$	—	173	188	μA
		$f_{HFRCO} = 19 \text{ MHz}$	—	143	156	μA
		$f_{HFRCO} = 16 \text{ MHz}$	—	123	136	μA
		$f_{HFRCO} = 13 \text{ MHz}$	—	110	124	μA
		$f_{HFRCO} = 7 \text{ MHz}$	—	85	94	μA
		$f_{HFRCO} = 4 \text{ MHz}$	—	32	37	μA
		$f_{HFRCO} = 2 \text{ MHz}$	—	28	34	μA
		$f_{HFRCO} = 1 \text{ MHz}$	—	26	31	μA
Coarse trim step size (% of period)	SS_{HFRCO_COARSE}		—	0.8	—	%
Fine trim step size (% of period)	SS_{HFRCO_FINE}		—	0.1	—	%
Period jitter	PJ_{HFRCO}		—	0.2	—	% RMS

4.1.12.5 Auxiliary High-Frequency RC Oscillator (AUXHFRCO)

Table 4.37. Auxiliary High-Frequency RC Oscillator (AUXHFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	$f_{AUXHFRCO_ACC}$	At production calibrated frequencies, across supply voltage and temperature	-3	—	3	%
Start-up time	$t_{AUXHFRCO}$	$f_{AUXHFRCO} \geq 19 \text{ MHz}$	—	400	—	ns
		$4 < f_{AUXHFRCO} < 19 \text{ MHz}$	—	1.4	—	μs
		$f_{AUXHFRCO} \leq 4 \text{ MHz}$	—	2.5	—	μs
Current consumption on all supplies	$I_{AUXHFRCO}$	$f_{AUXHFRCO} = 38 \text{ MHz}$	—	193	213	μA
		$f_{AUXHFRCO} = 32 \text{ MHz}$	—	157	175	μA
		$f_{AUXHFRCO} = 26 \text{ MHz}$	—	135	151	μA
		$f_{AUXHFRCO} = 19 \text{ MHz}$	—	108	122	μA
		$f_{AUXHFRCO} = 16 \text{ MHz}$	—	100	113	μA
		$f_{AUXHFRCO} = 13 \text{ MHz}$	—	77	88	μA
		$f_{AUXHFRCO} = 7 \text{ MHz}$	—	53	63	μA
		$f_{AUXHFRCO} = 4 \text{ MHz}$	—	29	36	μA
		$f_{AUXHFRCO} = 2 \text{ MHz}$	—	28	34	μA
		$f_{AUXHFRCO} = 1 \text{ MHz}$	—	27	31	μA
Coarse trim step size (% of period)	$SS_{AUXHFRCO_CO_COARSE}$		—	0.8	—	%
Fine trim step size (% of period)	$SS_{AUXHFRCO_CO_FINE}$		—	0.1	—	%
Period jitter	$PJ_{AUXHFRCO}$		—	0.2	—	% RMS

4.1.12.6 Ultra-low Frequency RC Oscillator (ULFRCO)

Table 4.38. Ultra-low Frequency RC Oscillator (ULFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{ULFRCO}		0.95	1	1.07	kHz

4.1.13 Flash Memory Characteristics¹Table 4.39. Flash Memory Characteristics¹

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC _{FLASH}		10000	—	—	cycles
Flash data retention	RET _{FLASH}	T ≤ 85 °C	10	—	—	years
		T ≤ 125 °C	10	—	—	years
Word (32-bit) programming time	t _{W_PROG}	Burst write, 128 words, average time per word	20	24.4	30	μs
		Single word	60	68.4	80	μs
Page erase time ²	t _{PERASE}		20	26.4	35	ms
Mass erase time ³	t _{MERASE}		20	26.5	35	ms
Device erase time ^{4 5}	t _{DERASE}	T ≤ 85 °C	—	82	100	ms
		T ≤ 125 °C	—	82	110	ms
Erase current ⁶	I _{ERASE}	Page Erase	—	—	1.6	mA
Write current ⁶	I _{WRITE}		—	—	3.8	mA
Supply voltage during flash erase and write	V _{FLASH}		1.62	—	3.6	V

Note:

1. Flash data retention information is published in the Quarterly Quality and Reliability Report.
2. From setting the ERASEPAGE bit in MSC_WRITECMD to 1 until the BUSY bit in MSC_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
3. Mass erase is issued by the CPU and erases all flash.
4. Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW).
5. From setting the DEVICEERASE bit in AAP_CMD to 1 until the ERASEBUSY bit in AAP_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
6. Measured at 25 °C.

4.1.14 General-Purpose I/O (GPIO)

Table 4.40. General-Purpose I/O (GPIO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage ¹	V _{IL}	GPIO pins	—	—	IOVDD*0.3	V
Input high voltage ¹	V _{IH}	GPIO pins	IOVDD*0.7	—	—	V
Output high voltage relative to IOVDD	V _{OH}	Sourcing 3 mA, IOVDD \geq 3 V, DRIVESTRENGTH ² = WEAK	IOVDD*0.8	—	—	V
		Sourcing 1.2 mA, IOVDD \geq 1.62 V, DRIVESTRENGTH ² = WEAK	IOVDD*0.6	—	—	V
		Sourcing 20 mA, IOVDD \geq 3 V, DRIVESTRENGTH ² = STRONG	IOVDD*0.8	—	—	V
		Sourcing 8 mA, IOVDD \geq 1.62 V, DRIVESTRENGTH ² = STRONG	IOVDD*0.6	—	—	V
Output low voltage relative to IOVDD	V _{OL}	Sinking 3 mA, IOVDD \geq 3 V, DRIVESTRENGTH ² = WEAK	—	—	IOVDD*0.2	V
		Sinking 1.2 mA, IOVDD \geq 1.62 V, DRIVESTRENGTH ² = WEAK	—	—	IOVDD*0.4	V
		Sinking 20 mA, IOVDD \geq 3 V, DRIVESTRENGTH ² = STRONG	—	—	IOVDD*0.2	V
		Sinking 8 mA, IOVDD \geq 1.62 V, DRIVESTRENGTH ² = STRONG	—	—	IOVDD*0.4	V
Input leakage current	I _{IOLEAK}	All GPIO except LFXO pins, GPIO \leq IOVDD, T \leq 85 °C	—	0.1	30	nA
		LFXO Pins, GPIO \leq IOVDD, T \leq 85 °C	—	0.1	50	nA
		All GPIO except LFXO pins, GPIO \leq IOVDD, T $>$ 85 °C	—	—	110	nA
		LFXO Pins, GPIO \leq IOVDD, T $>$ 85 °C	—	—	250	nA
Input leakage current on 5VTOL pads above IOVDD	I _{5VTOLLEAK}	IOVDD $<$ GPIO \leq IOVDD + 2 V	—	3.3	15	µA
I/O pin pull-up/pull-down resistor ³	R _{PU}		30	40	65	kΩ
Pulse width of pulses removed by the glitch suppression filter	t _{IOGLITCH}		15	25	45	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output fall time, From 70% to 30% of V_{IO}	t_{IOOF}	$C_L = 50 \text{ pF}$, DRIVESTRENGTH ² = STRONG, SLEWRATE ² = 0x6	—	1.8	—	ns
		$C_L = 50 \text{ pF}$, DRIVESTRENGTH ² = WEAK, SLEWRATE ² = 0x6	—	4.5	—	ns
Output rise time, From 30% to 70% of V_{IO}	t_{IOOR}	$C_L = 50 \text{ pF}$, DRIVESTRENGTH ² = STRONG, SLEWRATE = 0x6 ²	—	2.2	—	ns
		$C_L = 50 \text{ pF}$, DRIVESTRENGTH ² = WEAK, SLEWRATE ² = 0x6	—	7.4	—	ns

Note:

1. GPIO input threshold are proportional to the IOVDD supply, except for RESETn which is proportional to AVDD.
2. In GPIO_Pn_CTRL register.
3. GPIO pull-ups are referenced to the IOVDD supply, except for RESETn, which connects to AVDD.

4.1.15 Voltage Monitor (VMON)

Table 4.41. Voltage Monitor (VMON)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current (including I_SENSE)	I _{VMON}	In EM0 or EM1, 1 active channel, T ≤ 85 °C	—	6.3	10	µA
		In EM0 or EM1, 1 active channel, T > 85 °C	—	—	14	µA
		In EM0 or EM1, All channels active, T ≤ 85 °C	—	12.5	17	µA
		In EM0 or EM1, All channels active, T > 85 °C	—	—	21	µA
		In EM2, EM3 or EM4, 1 channel active and above threshold	—	62	—	nA
		In EM2, EM3 or EM4, 1 channel active and below threshold	—	62	—	nA
		In EM2, EM3 or EM4, All channels active and above threshold	—	99	—	nA
		In EM2, EM3 or EM4, All channels active and below threshold	—	99	—	nA
Loading of monitored supply	I _{SENSE}	In EM0 or EM1	—	2	—	µA
		In EM2, EM3 or EM4	—	2	—	nA
Threshold range	V _{VMON_RANGE}		1.62	—	3.4	V
Threshold step size	N _{VMON_STESP}	Coarse	—	200	—	mV
		Fine	—	20	—	mV
Response time	t _{VMON_RES}	Supply drops at 1V/µs rate	—	460	—	ns
Hysteresis	V _{VMON_HYST}		—	26	—	mV

4.1.16 Analog to Digital Converter (ADC)

Specified at 1 Msps, ADCCLK = 16 MHz, BIASPROG = 0, GPBIASACC = 0, unless otherwise indicated.

Table 4.42. Analog to Digital Converter (ADC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	V _{RESOLUTION}		6	—	12	Bits
Input voltage range ¹	V _{ADCIN}	Single ended	—	—	V _{FS}	V
		Differential	-V _{FS} /2	—	V _{FS} /2	V
Input range of external reference voltage, single ended and differential	V _{ADCREFIN_P}		1	—	V _{AVDD}	V
Power supply rejection ²	PSRR _{ADC}	At DC	—	80	—	dB
Analog input common mode rejection ratio	CMRR _{ADC}	At DC	—	80	—	dB
Current from all supplies, using internal reference buffer. Continuous operation. WAR-MUPMODE ³ = KEEPADC-WARM	I _{ADC_CONTINUOUS_LP}	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 ⁴	—	270	315	µA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 1 ⁴	—	125	—	µA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 1 ⁴	—	80	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WAR-MUPMODE ³ = NORMAL	I _{ADC_NORMAL_LP}	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 ⁴	—	45	—	µA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 1 ⁴	—	8	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE ³ = KEEPINSTANDBY or KEEPIN-SLOWACC	I _{ADC_STANDBY_LP}	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 ⁴	—	105	—	µA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 ⁴	—	70	—	µA
Current from all supplies, using internal reference buffer. Continuous operation. WAR-MUPMODE ³ = KEEPADC-WARM	I _{ADC_CONTINUOUS_HP}	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ⁴	—	325	—	µA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 0 ⁴	—	175	—	µA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 0 ⁴	—	125	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WAR-MUPMODE ³ = NORMAL	I _{ADC_NORMAL_HP}	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ⁴	—	85	—	µA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 0 ⁴	—	16	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE ³ = KEEPINSTANDBY or KEEPIN-SLOWACC	I _{ADC_STANDBY_HP}	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ⁴	—	160	—	µA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ⁴	—	125	—	µA
Current from HPERCLK	I _{ADC_CLK}	HPERCLK = 16 MHz	—	160	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC clock frequency	f_{ADCCLK}		—	—	16	MHz
Throughput rate	$f_{ADC RATE}$		—	—	1	Msps
Conversion time ⁵	$t_{ADCCONV}$	6 bit	—	7	—	cycles
		8 bit	—	9	—	cycles
		12 bit	—	13	—	cycles
Startup time of reference generator and ADC core	$t_{ADCSTART}$	WARMUPMODE ³ = NORMAL	—	—	5	μ s
		WARMUPMODE ³ = KEEPIN-STANDBY	—	—	2	μ s
		WARMUPMODE ³ = KEEPINSLOWACC	—	—	1	μ s
SNDR at 1Msps and $f_{IN} = 10\text{kHz}$	SNDR_{ADC}	Internal reference ⁶ , differential measurement	58	67	—	dB
		External reference ⁷ , differential measurement	—	68	—	dB
Spurious-free dynamic range (SFDR)	SFDR_{ADC}	1 MSamples/s, 10 kHz full-scale sine wave	—	75	—	dB
Differential non-linearity (DNL)	DNL_{ADC}	12 bit resolution, No missing codes	-1	—	2	LSB
Integral non-linearity (INL), End point method	INL_{ADC}	12 bit resolution	-6	—	6	LSB
Offset error	$V_{\text{ADC OFFSETERR}}$		-3	0	3	LSB
Gain error in ADC	V_{ADCGAIN}	Using internal reference	—	-0.2	3.5	%
		Using external reference	—	-1	—	%
Temperature sensor slope	$V_{\text{TS_SLOPE}}$		—	-1.84	—	$\text{mV}/^{\circ}\text{C}$

Note:

1. The absolute voltage allowed at any ADC input is dictated by the power rail supplied to on-chip circuitry, and may be lower than the effective full scale voltage. All ADC inputs are limited to the ADC supply (AVDD or DVDD depending on EMU_PWRCTRL_ANASW). Any ADC input routed through the APOR will further be limited by the IOVDD supply to the pin.
2. PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU_PWRCTRL.
3. In ADCn_CTRL register.
4. In ADCn_BIASPROG register.
5. Derived from ADCCLK.
6. Internal reference option used corresponds to selection 2V5 in the SINGLECTRL_REF or SCANCTRL_REF register field. The differential input range with this configuration is $\pm 1.25\text{ V}$. Typical value is characterized using full-scale sine wave input. Minimum value is production-tested using sine wave input at 1.5 dB lower than full scale.
7. External reference is 1.25 V applied externally to ADCnEXTREFP, with the selection CONF in the SINGLECTRL_REF or SCANCTRL_REF register field and VREFP in the SINGLECTRLX_VREFSEL or SCANCTRLX_VREFSEL field. The differential input range with this configuration is $\pm 1.25\text{ V}$.

4.1.17 Analog Comparator (ACMP)

Table 4.43. Analog Comparator (ACMP)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V _{ACMPIN}	ACMPVDD = ACMPn_CTRL_PWRSEL ¹	—	—	V _{ACMPVDD}	V
Supply voltage	V _{ACMPVDD}	BIASPROG ² ≤ 0x10 or FULL-BIAS ² = 0	1.8	—	V _{VREGVDD_MAX}	V
		0x10 < BIASPROG ² ≤ 0x20 and FULLBIAS ² = 1	2.1	—	V _{VREGVDD_MAX}	V
Active current not including voltage reference ³	I _{ACMP}	BIASPROG ² = 1, FULLBIAS ² = 0	—	50	—	nA
		BIASPROG ² = 0x10, FULLBIAS ² = 0	—	306	—	nA
		BIASPROG ² = 0x02, FULLBIAS ² = 1	—	6.5	—	μA
		BIASPROG ² = 0x20, FULLBIAS ² = 1	—	75	92	μA
Current consumption of internal voltage reference ³	I _{ACMPREF}	VLP selected as input using 2.5 V Reference / 4 (0.625 V)	—	50	—	nA
		VLP selected as input using VDD	—	20	—	nA
		VBDIV selected as input using 1.25 V reference / 1	—	4.1	—	μA
		VADIV selected as input using VDD/1	—	2.4	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Hysteresis ($V_{CM} = 1.25$ V, $BIASPROG^2 = 0x10$, $FULLBIAS^2 = 1$)	VACMPHYST	HYSTSEL ⁴ = HYST0	-3	0	3	mV
		HYSTSEL ⁴ = HYST1	5	18	27	mV
		HYSTSEL ⁴ = HYST2	12	33	50	mV
		HYSTSEL ⁴ = HYST3	17	46	65	mV
		HYSTSEL ⁴ = HYST4	23	57	82	mV
		HYSTSEL ⁴ = HYST5	26	68	98	mV
		HYSTSEL ⁴ = HYST6	30	79	130	mV
		HYSTSEL ⁴ = HYST7	34	90	150	mV
		HYSTSEL ⁴ = HYST8	-3	0	3	mV
		HYSTSEL ⁴ = HYST9	-27	-18	-5	mV
		HYSTSEL ⁴ = HYST10	-50	-33	-12	mV
		HYSTSEL ⁴ = HYST11	-65	-45	-17	mV
		HYSTSEL ⁴ = HYST12	-82	-57	-23	mV
		HYSTSEL ⁴ = HYST13	-98	-67	-26	mV
		HYSTSEL ⁴ = HYST14	-130	-78	-30	mV
		HYSTSEL ⁴ = HYST15	-150	-88	-34	mV
Comparator delay ⁵	tACMPDELAY	BIASPROG ² = 1, FULLBIAS ² = 0	—	30	—	μs
		BIASPROG ² = 0x10, FULLBIAS ² = 0	—	3.7	—	μs
		BIASPROG ² = 0x02, FULLBIAS ² = 1	—	360	—	ns
		BIASPROG ² = 0x20, FULLBIAS ² = 1	—	35	—	ns
Offset voltage	VACMPOFFSET	BIASPROG ² = 0x10, FULLBIAS ² = 1	-35	—	35	mV
Reference voltage	VACMPREF	Internal 1.25 V reference	1	1.25	1.47	V
		Internal 2.5 V reference	2	2.5	2.8	V
Capacitive sense internal resistance	RCSRES	CSRESSEL ⁶ = 0	—	infinite	—	kΩ
		CSRESSEL ⁶ = 1	—	15	—	kΩ
		CSRESSEL ⁶ = 2	—	27	—	kΩ
		CSRESSEL ⁶ = 3	—	39	—	kΩ
		CSRESSEL ⁶ = 4	—	51	—	kΩ
		CSRESSEL ⁶ = 5	—	100	—	kΩ
		CSRESSEL ⁶ = 6	—	162	—	kΩ
		CSRESSEL ⁶ = 7	—	235	—	kΩ

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note:						
1.	ACMPVDD	is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD.				
2.	In ACMPn_CTRL register.					
3.	The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference. $I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$.					
4.	In ACMPn_HYSTERESIS registers.					
5.	± 100 mV differential drive.					
6.	In ACMPn_INPUTSEL register.					

4.1.18 Digital to Analog Converter (VDAC)

DRIVESTRENGTH = 2 unless otherwise specified. Primary VDAC output.

Table 4.44. Digital to Analog Converter (VDAC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output voltage	V _{DACOUT}	Single-Ended	0	—	V _{VREF}	V
		Differential ¹	-V _{VREF}	—	V _{VREF}	V
Current consumption including references (2 channels) ²	I _{DAC}	500 ksps, 12-bit, DRIVESTRENGTH = 2, REFSEL = 4	—	396	—	μA
		44.1 ksps, 12-bit, DRIVESTRENGTH = 1, REFSEL = 4	—	72	—	μA
		200 Hz refresh rate, 12-bit Sample-Off mode in EM2, DRIVESTRENGTH = 2, REFSEL = 4, SETTLETIME = 0x02, WARMUPTIME = 0x0A	—	1.2	—	μA
Current from HPERCLK ³	I _{DAC_CLK}		—	5.8	—	μA/MHz
Sample rate	S _R _{DAC}		—	—	500	ksps
DAC clock frequency	f _{DAC}		—	—	1	MHz
Conversion time	t _{DACCONV}	f _{DAC} = 1MHz	2	—	—	μs
Settling time	t _{DACSETTLE}	50% fs step settling to 5 LSB	—	2.5	—	μs
Startup time	t _{DACSTARTUP}	Enable to 90% fs output, settling to 10 LSB	—	—	12	μs
Output impedance	R _{OUT}	DRIVESTRENGTH = 2, 0.4 V ≤ V _{OUT} ≤ V _{OPA} - 0.4 V, -8 mA < I _{OUT} < 8 mA, Full supply range	—	2	—	Ω
		DRIVESTRENGTH = 0 or 1, 0.4 V ≤ V _{OUT} ≤ V _{OPA} - 0.4 V, -400 μA < I _{OUT} < 400 μA, Full supply range	—	2	—	Ω
		DRIVESTRENGTH = 2, 0.1 V ≤ V _{OUT} ≤ V _{OPA} - 0.1 V, -2 mA < I _{OUT} < 2 mA, Full supply range	—	2	—	Ω
		DRIVESTRENGTH = 0 or 1, 0.1 V ≤ V _{OUT} ≤ V _{OPA} - 0.1 V, -100 μA < I _{OUT} < 100 μA, Full supply range	—	2	—	Ω
Power supply rejection ratio ⁴	P _{SRR}	V _{out} = 50% fs. DC	—	65.5	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 250 kHz	SNDR _{DAC}	500 ksps, single-ended, internal 1.25V reference	—	60.4	—	dB
		500 ksps, single-ended, internal 2.5V reference	—	61.6	—	dB
		500 ksps, single-ended, 3.3V VDD reference	—	64.0	—	dB
		500 ksps, differential, internal 1.25V reference	—	63.3	—	dB
		500 ksps, differential, internal 2.5V reference	—	64.4	—	dB
		500 ksps, differential, 3.3V VDD reference	—	65.8	—	dB
Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 22 kHz	SNDR _{DAC_BAND}	500 ksps, single-ended, internal 1.25V reference	—	65.3	—	dB
		500 ksps, single-ended, internal 2.5V reference	—	66.7	—	dB
		500 ksps, single-ended, 3.3V VDD reference	—	70.0	—	dB
		500 ksps, differential, internal 1.25V reference	—	67.8	—	dB
		500 ksps, differential, internal 2.5V reference	—	69.0	—	dB
		500 ksps, differential, 3.3V VDD reference	—	68.5	—	dB
Total harmonic distortion	THD		—	70.2	—	dB
Differential non-linearity ⁵	DNL _{DAC}		-0.99	—	1	LSB
Integral non-linearity	INL _{DAC}		-4	—	4	LSB
Offset error ⁶	V _{OFFSET}	T = 25 °C	-8	—	8	mV
		Across operating temperature range	-25	—	25	mV
Gain error ⁶	V _{GAIN}	T = 25 °C, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN)	-2.5	—	2.5	%
		T = 25 °C, Internal reference (REFSEL = 1V25 or 2V5)	-5	—	5	%
		T = 25 °C, External reference (REFSEL = VDD or EXT)	-1.8	—	1.8	%
		Across operating temperature range, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN)	-3.5	—	3.5	%
		Across operating temperature range, Internal reference (REFSEL = 1V25 or 2V5)	-7.5	—	7.5	%
		Across operating temperature range, External reference (REFSEL = VDD or EXT)	-2.0	—	2.0	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External load capacitance, OUTSCALE=0	C _{LOAD}		—	—	75	pF

Note:

1. In differential mode, the output is defined as the difference between two single-ended outputs. Absolute voltage on each output is limited to the single-ended range.
2. Supply current specifications are for VDAC circuitry operating with static output only and do not include current required to drive the load.
3. Current from HFPERCLK is dependent on HFPERCLK frequency. This current contributes to the total supply current used when the clock to the DAC peripheral is enabled in the CMU.
4. PSRR calculated as $20 * \log_{10}(\Delta VDD / \Delta V_{OUT})$, VDAC output at 90% of full scale
5. Entire range is monotonic and has no missing codes.
6. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.

4.1.19 Current Digital to Analog Converter (IDAC)

Table 4.45. Current Digital to Analog Converter (IDAC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Number of ranges	N _{IDAC_RANGES}		—	4	—	ranges
Output current	I _{IDAC_OUT}	RANGESEL ¹ = RANGE0	0.05	—	1.6	μA
		RANGESEL ¹ = RANGE1	1.6	—	4.7	μA
		RANGESEL ¹ = RANGE2	0.5	—	16	μA
		RANGESEL ¹ = RANGE3	2	—	64	μA
Linear steps within each range	N _{IDAC_STEPS}		—	32	—	steps
Step size	SS _{IDAC}	RANGESEL ¹ = RANGE0	—	50	—	nA
		RANGESEL ¹ = RANGE1	—	100	—	nA
		RANGESEL ¹ = RANGE2	—	500	—	nA
		RANGESEL ¹ = RANGE3	—	2	—	μA
Total accuracy, STEPSEL ¹ = 0x10	ACC _{IDAC}	EM0 or EM1, AVDD=3.3 V, T = 25 °C	-3	—	3	%
		EM0 or EM1, Across operating temperature range	-18	—	22	%
		EM2 or EM3, Source mode, RANGESEL ¹ = RANGE0, AVDD=3.3 V, T = 25 °C	—	-2	—	%
		EM2 or EM3, Source mode, RANGESEL ¹ = RANGE1, AVDD=3.3 V, T = 25 °C	—	-1.7	—	%
		EM2 or EM3, Source mode, RANGESEL ¹ = RANGE2, AVDD=3.3 V, T = 25 °C	—	-0.8	—	%
		EM2 or EM3, Source mode, RANGESEL ¹ = RANGE3, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
		EM2 or EM3, Sink mode, RANGESEL ¹ = RANGE0, AVDD=3.3 V, T = 25 °C	—	-0.7	—	%
		EM2 or EM3, Sink mode, RANGESEL ¹ = RANGE1, AVDD=3.3 V, T = 25 °C	—	-0.6	—	%
		EM2 or EM3, Sink mode, RANGESEL ¹ = RANGE2, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
		EM2 or EM3, Sink mode, RANGESEL ¹ = RANGE3, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
Start up time	t _{IDAC_SU}	Output within 1% of steady state value	—	5	—	μs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Settling time, (output settled within 1% of steady state value),	t _{IDAC_SETTLE}	Range setting is changed	—	5	—	μs
		Step value is changed	—	1	—	μs
Current consumption ²	I _{IDAC}	EM0 or EM1 Source mode, excluding output current, Across operating temperature range	—	11	18	μA
		EM0 or EM1 Sink mode, excluding output current, Across operating temperature range	—	13	21	μA
		EM2 or EM3 Source mode, excluding output current, T = 25 °C	—	0.023	—	μA
		EM2 or EM3 Sink mode, excluding output current, T = 25 °C	—	0.041	—	μA
		EM2 or EM3 Source mode, excluding output current, T ≥ 85 °C	—	11	—	μA
		EM2 or EM3 Sink mode, excluding output current, T ≥ 85 °C	—	13	—	μA
Output voltage compliance in source mode, source current change relative to current sourced at 0 V	I _{COMP_SRC}	RANGESEL ¹ = RANGE0, output voltage = min(V _{IOVDD} , V _{AVDD} ² -100 mV)	—	0.11	—	%
		RANGESEL ¹ = RANGE1, output voltage = min(V _{IOVDD} , V _{AVDD} ² -100 mV)	—	0.06	—	%
		RANGESEL ¹ = RANGE2, output voltage = min(V _{IOVDD} , V _{AVDD} ² -150 mV)	—	0.04	—	%
		RANGESEL ¹ = RANGE3, output voltage = min(V _{IOVDD} , V _{AVDD} ² -250 mV)	—	0.03	—	%
Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD	I _{COMP_SINK}	RANGESEL ¹ = RANGE0, output voltage = 100 mV	—	0.12	—	%
		RANGESEL ¹ = RANGE1, output voltage = 100 mV	—	0.05	—	%
		RANGESEL ¹ = RANGE2, output voltage = 150 mV	—	0.04	—	%
		RANGESEL ¹ = RANGE3, output voltage = 250 mV	—	0.03	—	%

Note:

1. In IDAC_CURPROG register.
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

4.1.20 Capacitive Sense (CSEN)

Table 4.46. Capacitive Sense (CSEN)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single conversion time (1x accumulation)	t _{CNV}	12-bit SAR Conversions	—	20.2	—	μs
		16-bit SAR Conversions	—	26.4	—	μs
		Delta Modulation Conversion (single comparison)	—	1.55	—	μs
Maximum external capacitive load	C _{EXTMAX}	IREFPROG=7 (Gain = 1x), including routing parasitics	—	68	—	pF
		IREFPROG=0 (Gain = 10x), including routing parasitics	—	680	—	pF
Maximum external series impedance	R _{EXTMAX}		—	1	—	kΩ
Supply current, EM2 bonded conversions, WARMUP-MODE=NORMAL, WARMUPCNT=0	I _{CSEN_BOND}	12-bit SAR conversions, 20 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹	—	326	—	nA
		Delta Modulation conversions, 20 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹	—	226	—	nA
		12-bit SAR conversions, 200 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹	—	33	—	nA
		Delta Modulation conversions, 200 ms conversion rate, IREFPROG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹	—	25	—	nA
Supply current, EM2 scan conversions, WARMUP-MODE=NORMAL, WARMUPCNT=0	I _{CSEN_EM2}	12-bit SAR conversions, 20 ms scan rate, IREFPROG=0 (Gain = 10x), 8 samples per scan ¹	—	690	—	nA
		Delta Modulation conversions, 20 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), IREFPROG=0 (Gain = 10x), 8 samples per scan ¹	—	515	—	nA
		12-bit SAR conversions, 200 ms scan rate, IREFPROG=0 (Gain = 10x), 8 samples per scan ¹	—	79	—	nA
		Delta Modulation conversions, 200 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), IREFPROG=0 (Gain = 10x), 8 samples per scan ¹	—	57	—	nA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current, continuous conversions, WARMUP-MODE=KEEPSENWARM	I _{CSEN_ACTIVE}	SAR or Delta Modulation conversions of 33 pF capacitor, IRE-FPROG=0 (Gain = 10x), always on	—	90.5	—	µA
HFPERCLK supply current	I _{CSEN_HFPERCLK}	Current contribution from HFPERCLK when clock to CSEN block is enabled.	—	2.25	—	µA/MHz
Note:						
1. Current is specified with a total external capacitance of 33 pF per channel. Average current is dependent on how long the peripheral is actively sampling channels within the scan period, and scales with the number of samples acquired. Supply current for a specific application can be estimated by multiplying the current per sample by the total number of samples per period (total_current = single_sample_current * (number_of_channels * accumulation)).						

4.1.21 Operational Amplifier (OPAMP)

Unless otherwise indicated, specified conditions are: Non-inverting input configuration, VDD = 3.3 V, DRIVESTRENGTH = 2, MAINOUTEN = 1, C_{LOAD} = 75 pF with OUTSCALE = 0, or C_{LOAD} = 37.5 pF with OUTSCALE = 1. Unit gain buffer and 3X-gain connection as specified in table footnotes^{1 2}.

Table 4.47. Operational Amplifier (OPAMP)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply voltage (from AVDD)	V _{OPA}	HCMDIS = 0, Rail-to-rail input range	2	—	3.8	V
		HCMDIS = 1	1.62	—	3.8	V
Input voltage	V _{IN}	HCMDIS = 0, Rail-to-rail input range	V _{VSS}	—	V _{OPA}	V
		HCMDIS = 1	V _{VSS}	—	V _{OPA} -1.2	V
Input impedance	R _{IN}		100	—	—	MΩ
Output voltage	V _{OUT}		V _{VSS}	—	V _{OPA}	V
Load capacitance ³	C _{LOAD}	OUTSCALE = 0	—	—	75	pF
		OUTSCALE = 1	—	—	37.5	pF
Output impedance	R _{OUT}	DRIVESTRENGTH = 2 or 3, 0.4 V ≤ V _{OUT} ≤ V _{OPA} - 0.4 V, -8 mA < I _{OUT} < 8 mA, Buffer connection, Full supply range	—	0.25	—	Ω
		DRIVESTRENGTH = 0 or 1, 0.4 V ≤ V _{OUT} ≤ V _{OPA} - 0.4 V, -400 μA < I _{OUT} < 400 μA, Buffer connection, Full supply range	—	0.6	—	Ω
		DRIVESTRENGTH = 2 or 3, 0.1 V ≤ V _{OUT} ≤ V _{OPA} - 0.1 V, -2 mA < I _{OUT} < 2 mA, Buffer connection, Full supply range	—	0.4	—	Ω
		DRIVESTRENGTH = 0 or 1, 0.1 V ≤ V _{OUT} ≤ V _{OPA} - 0.1 V, -100 μA < I _{OUT} < 100 μA, Buffer connection, Full supply range	—	1	—	Ω
Internal closed-loop gain	G _{CCL}	Buffer connection	0.99	1	1.01	-
		3x Gain connection	2.93	2.99	3.05	-
		16x Gain connection	15.07	15.7	16.33	-
Active current ⁴	I _{OPA}	DRIVESTRENGTH = 3, OUTSCALE = 0	—	580	—	μA
		DRIVESTRENGTH = 2, OUTSCALE = 0	—	176	—	μA
		DRIVESTRENGTH = 1, OUTSCALE = 0	—	13	—	μA
		DRIVESTRENGTH = 0, OUTSCALE = 0	—	4.7	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Open-loop gain	G _{OL}	DRIVESTRENGTH = 3	—	135	—	dB
		DRIVESTRENGTH = 2	—	137	—	dB
		DRIVESTRENGTH = 1	—	121	—	dB
		DRIVESTRENGTH = 0	—	109	—	dB
Loop unit-gain frequency ⁵	UGF	DRIVESTRENGTH = 3, Buffer connection	—	3.38	—	MHz
		DRIVESTRENGTH = 2, Buffer connection	—	0.9	—	MHz
		DRIVESTRENGTH = 1, Buffer connection	—	132	—	kHz
		DRIVESTRENGTH = 0, Buffer connection	—	34	—	kHz
		DRIVESTRENGTH = 3, 3x Gain connection	—	2.57	—	MHz
		DRIVESTRENGTH = 2, 3x Gain connection	—	0.71	—	MHz
		DRIVESTRENGTH = 1, 3x Gain connection	—	113	—	kHz
		DRIVESTRENGTH = 0, 3x Gain connection	—	28	—	kHz
Phase margin	PM	DRIVESTRENGTH = 3, Buffer connection	—	67	—	°
		DRIVESTRENGTH = 2, Buffer connection	—	69	—	°
		DRIVESTRENGTH = 1, Buffer connection	—	63	—	°
		DRIVESTRENGTH = 0, Buffer connection	—	68	—	°
Output voltage noise	N _{OUT}	DRIVESTRENGTH = 3, Buffer connection, 10 Hz - 10 MHz	—	146	—	µVrms
		DRIVESTRENGTH = 2, Buffer connection, 10 Hz - 10 MHz	—	163	—	µVrms
		DRIVESTRENGTH = 1, Buffer connection, 10 Hz - 1 MHz	—	170	—	µVrms
		DRIVESTRENGTH = 0, Buffer connection, 10 Hz - 1 MHz	—	176	—	µVrms
		DRIVESTRENGTH = 3, 3x Gain connection, 10 Hz - 10 MHz	—	313	—	µVrms
		DRIVESTRENGTH = 2, 3x Gain connection, 10 Hz - 10 MHz	—	271	—	µVrms
		DRIVESTRENGTH = 1, 3x Gain connection, 10 Hz - 1 MHz	—	247	—	µVrms
		DRIVESTRENGTH = 0, 3x Gain connection, 10 Hz - 1 MHz	—	245	—	µVrms

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Slew rate ⁶	SR	DRIVESTRENGTH = 3, INCBW=1 ⁷	—	4.7	—	V/μs
		DRIVESTRENGTH = 3, INCBW=0	—	1.5	—	V/μs
		DRIVESTRENGTH = 2, INCBW=1 ⁷	—	1.27	—	V/μs
		DRIVESTRENGTH = 2, INCBW=0	—	0.42	—	V/μs
		DRIVESTRENGTH = 1, INCBW=1 ⁷	—	0.17	—	V/μs
		DRIVESTRENGTH = 1, INCBW=0	—	0.058	—	V/μs
		DRIVESTRENGTH = 0, INCBW=1 ⁷	—	0.044	—	V/μs
		DRIVESTRENGTH = 0, INCBW=0	—	0.015	—	V/μs
Startup time ⁸	T _{START}	DRIVESTRENGTH = 2	—	—	12	μs
Input offset voltage	V _{OSI}	DRIVESTRENGTH = 2 or 3, T = 25 °C	-2	—	2	mV
		DRIVESTRENGTH = 1 or 0, T = 25 °C	-2	—	2	mV
		DRIVESTRENGTH = 2 or 3, across operating temperature range	-12	—	12	mV
		DRIVESTRENGTH = 1 or 0, across operating temperature range	-30	—	30	mV
DC power supply rejection ratio ⁹	PSRR _{DC}	Input referred	—	70	—	dB
DC common-mode rejection ratio ⁹	CMRR _{DC}	Input referred	—	70	—	dB
Total harmonic distortion	THD _{OPA}	DRIVESTRENGTH = 2, 3x Gain connection, 1 kHz, V _{OUT} = 0.1 V to V _{OPA} - 0.1 V	—	90	—	dB
		DRIVESTRENGTH = 0, 3x Gain connection, 0.1 kHz, V _{OUT} = 0.1 V to V _{OPA} - 0.1 V	—	90	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note:						
1.	Specified configuration for Unit gain buffer configuration is: INCBW = 0, HCMDIS = 0, RESINSEL = DISABLE. $V_{INPUT} = 0.5$ V, $V_{OUTPUT} = 0.5$ V.					
2.	Specified configuration for 3X-Gain configuration is: INCBW = 1, HCMDIS = 1, RESINSEL = VSS, $V_{INPUT} = 0.5$ V, $V_{OUTPUT} = 1.5$ V. Nominal voltage gain is 3.					
3.	If the maximum C_{LOAD} is exceeded, an isolation resistor is required for stability. See AN0038 for more information.					
4.	Current into the load resistor is excluded. When the OPAMP is connected with closed-loop gain > 1 , there will be extra current to drive the resistor feedback network. The internal resistor feedback network has total resistance of 143.5 kOhm, which will cause another ~ 10 μ A current when the OPAMP drives 1.5 V between output and ground.					
5.	In unit gain connection, UGF is the gain-bandwidth product of the OPAMP. In 3x Gain connection, UGF is the gain-bandwidth product of the OPAMP and 1/3 attenuation of the feedback network.					
6.	Step between 0.2V and $V_{OPA}-0.2$ V, 10%-90% rising/falling range.					
7.	When INCBW is set to 1 the OPAMP bandwidth is increased. This is allowed only when the non-inverting close-loop gain is ≥ 3 , or the OPAMP may not be stable.					
8.	From enable to output settled. In sample-and-off mode, RC network after OPAMP will contribute extra delay. Settling error < 1 mV.					
9.	When HCMDIS=1 and input common mode transitions the region from $V_{OPA}-1.4$ V to $V_{OPA}-1$ V, input offset will change. PSRR and CMRR specifications do not apply to this transition region.					

4.1.22 Pulse Counter (PCNT)

Table 4.48. Pulse Counter (PCNT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input frequency	F_{IN}	Asynchronous Single and Quadrature Modes	—	—	20	MHz
		Sampled Modes with Debounce filter set to 0.	—	—	8	kHz

4.1.23 Analog Port (APORT)

Table 4.49. Analog Port (APORT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current ^{1 2}	I_{APORT}	Operation in EM0/EM1	—	7	—	μ A
		Operation in EM2/EM3	—	67	—	nA

Note:

- Supply current increase that occurs when an analog peripheral requests access to APORT. This current is not included in reported peripheral currents. Additional peripherals requesting access to APORT do not incur further current.
- Specified current is for continuous APORT operation. In applications where the APORT is not requested continuously (e.g. periodic ACMP requests from LESENSE in EM2), the average current requirements can be estimated by multiplying the duty cycle of the requests by the specified continuous current number.

4.1.24 I2C

4.1.24.1 I2C Standard-mode (Sm)¹Table 4.50. I2C Standard-mode (Sm)¹

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency ²	f_{SCL}		0	—	100	kHz
SCL clock low time	t_{LOW}		4.7	—	—	μs
SCL clock high time	t_{HIGH}		4	—	—	μs
SDA set-up time	t_{SU_DAT}		250	—	—	ns
SDA hold time ³	t_{HD_DAT}		100	—	3450	ns
Repeated START condition set-up time	t_{SU_STA}		4.7	—	—	μs
(Repeated) START condition hold time	t_{HD_STA}		4	—	—	μs
STOP condition set-up time	t_{SU_STO}		4	—	—	μs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	—	μs

Note:

1. For CLHR set to 0 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time (t_{HD_DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

4.1.24.2 I2C Fast-mode (Fm)¹Table 4.51. I2C Fast-mode (Fm)¹

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency ²	f_{SCL}		0	—	400	kHz
SCL clock low time	t_{LOW}		1.3	—	—	μs
SCL clock high time	t_{HIGH}		0.6	—	—	μs
SDA set-up time	t_{SU_DAT}		100	—	—	ns
SDA hold time ³	t_{HD_DAT}		100	—	900	ns
Repeated START condition set-up time	t_{SU_STA}		0.6	—	—	μs
(Repeated) START condition hold time	t_{HD_STA}		0.6	—	—	μs
STOP condition set-up time	t_{SU_STO}		0.6	—	—	μs
Bus free time between a STOP and START condition	t_{BUF}		1.3	—	—	μs

Note:

1. For CLHR set to 1 in the I2Cn_CTRL register.
2. For the minimum HFFPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

4.1.24.3 I2C Fast-mode Plus (Fm+)¹Table 4.52. I2C Fast-mode Plus (Fm+)¹

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency ²	f_{SCL}		0	—	1000	kHz
SCL clock low time	t_{LOW}		0.5	—	—	μ s
SCL clock high time	t_{HIGH}		0.26	—	—	μ s
SDA set-up time	t_{SU_DAT}		50	—	—	ns
SDA hold time	t_{HD_DAT}		100	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		0.26	—	—	μ s
(Repeated) START condition hold time	t_{HD_STA}		0.26	—	—	μ s
STOP condition set-up time	t_{SU_STO}		0.26	—	—	μ s
Bus free time between a STOP and START condition	t_{BUF}		0.5	—	—	μ s

Note:

1. For CLHR set to 0 or 1 in the I2Cn_CTRL register.
2. For the minimum HFFPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual.

4.1.25 USART SPI

SPI Master Timing

Table 4.53. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 2 3}	t_{SCLK}		$2 * t_{HFPERCLK}$	—	—	ns
CS to MOSI ^{1 2}	t_{CS_MO}		-14.5	—	13.5	ns
SCLK to MOSI ^{1 2}	t_{SCLK_MO}		-8.5	—	8	ns
MISO setup time ^{1 2}	t_{SU_MI}	IOVDD = 1.62 V	92	—	—	ns
		IOVDD = 3.0 V	42	—	—	ns
MISO hold time ^{1 2}	t_{H_MI}		-10	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).
3. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.

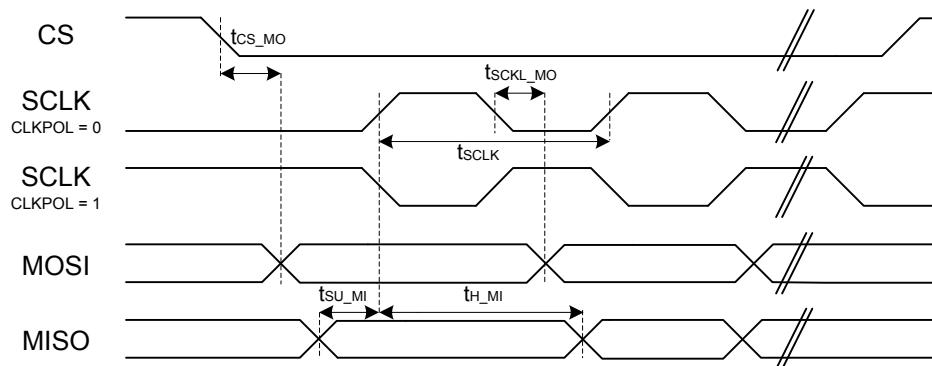


Figure 4.1. SPI Master Timing Diagram

SPI Slave Timing

Table 4.54. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 2 3}	t_{SCLK}		6 * $t_{HFPERCLK}$	—	—	ns
SCLK high time ^{1 2 3}	t_{SCLK_HI}		2.5 * $t_{HFPERCLK}$	—	—	ns
SCLK low time ^{1 2 3}	t_{SCLK_LO}		2.5 * $t_{HFPERCLK}$	—	—	ns
CS active to MISO ^{1 2}	$t_{CS_ACT_MI}$		4	—	70	ns
CS disable to MISO ^{1 2}	$t_{CS_DIS_MI}$		4	—	50	ns
MOSI setup time ^{1 2}	t_{SU_MO}		8	—	—	ns
MOSI hold time ^{1 2 3}	t_{H_MO}		7	—	—	ns
SCLK to MISO ^{1 2 3}	t_{SCLK_MI}		10 + 1.5 * $t_{HFPERCLK}$	—	65 + 2.5 * $t_{HFPERCLK}$	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).
3. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.

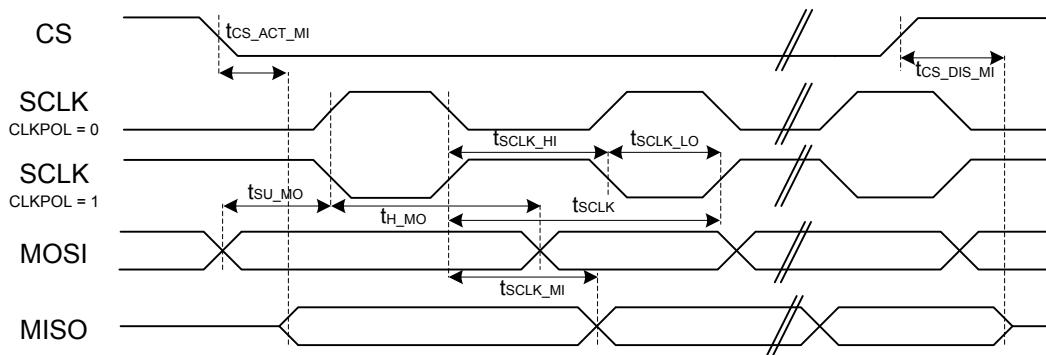


Figure 4.2. SPI Slave Timing Diagram

4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

4.2.1 Supply Current

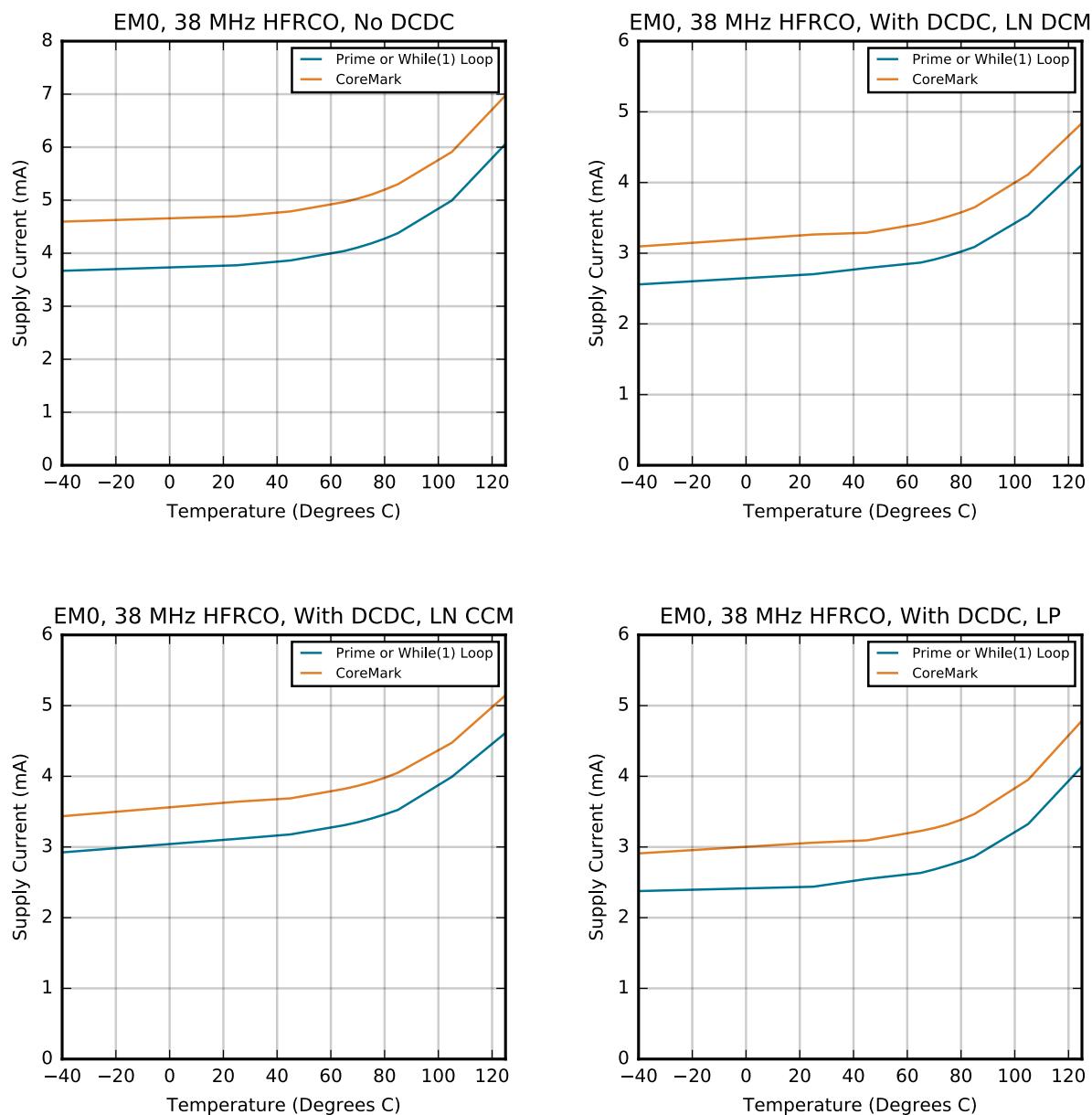


Figure 4.3. EM0 Active Mode Typical Supply Current vs. Temperature

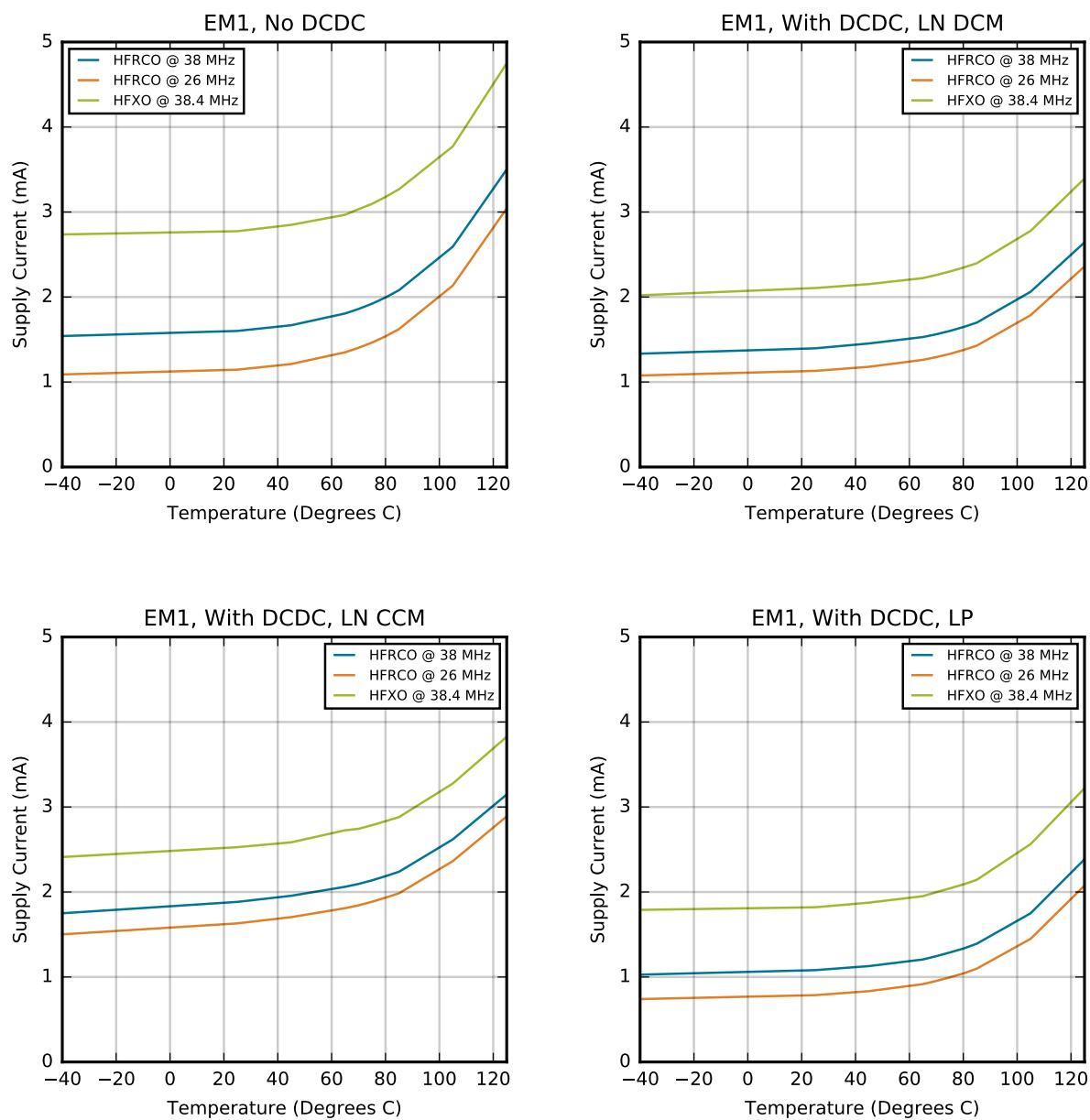


Figure 4.4. EM1 Sleep Mode Typical Supply Current vs. Temperature

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

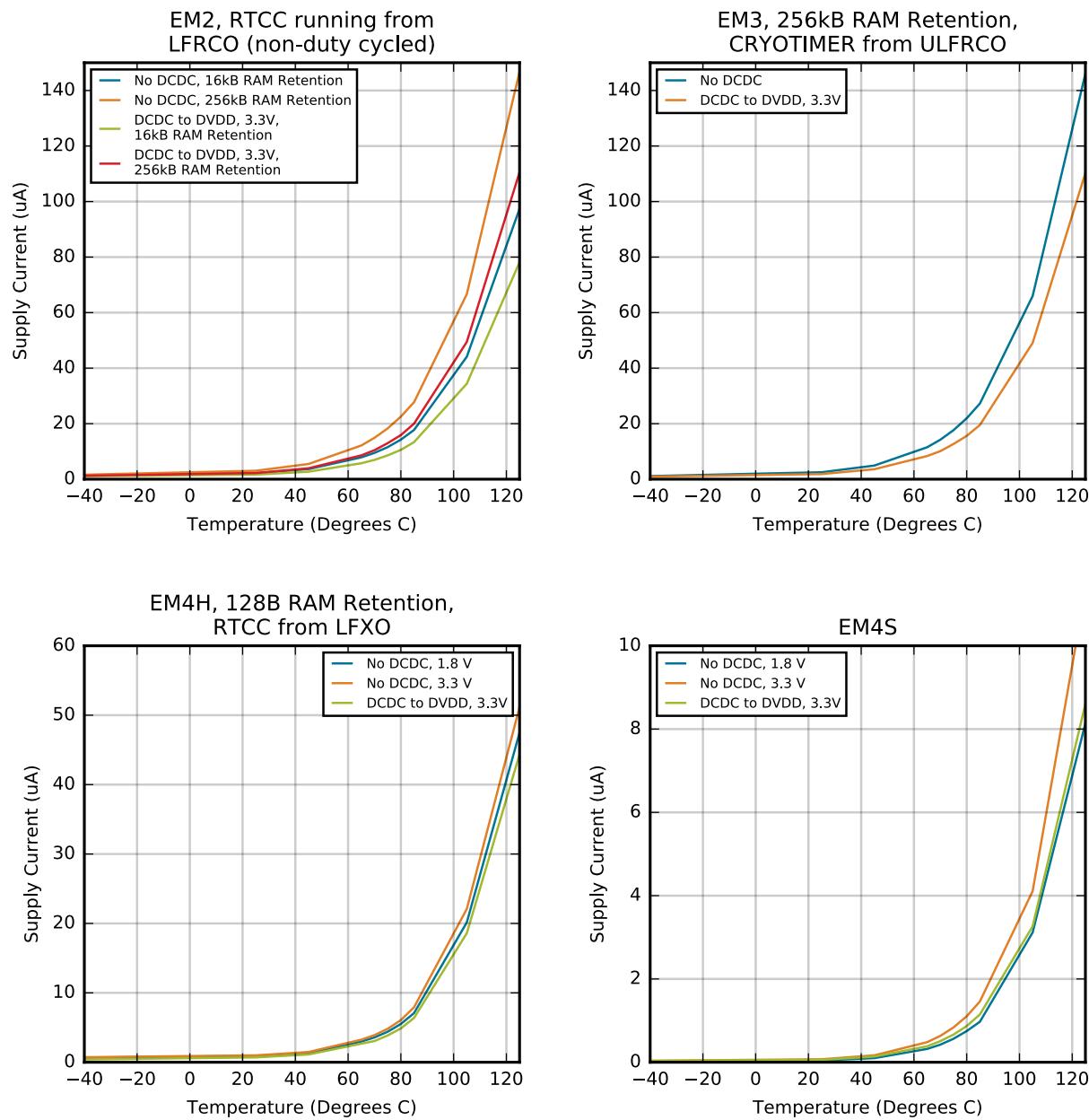


Figure 4.5. EM2, EM3, EM4H and EM4S Typical Supply Current vs. Temperature

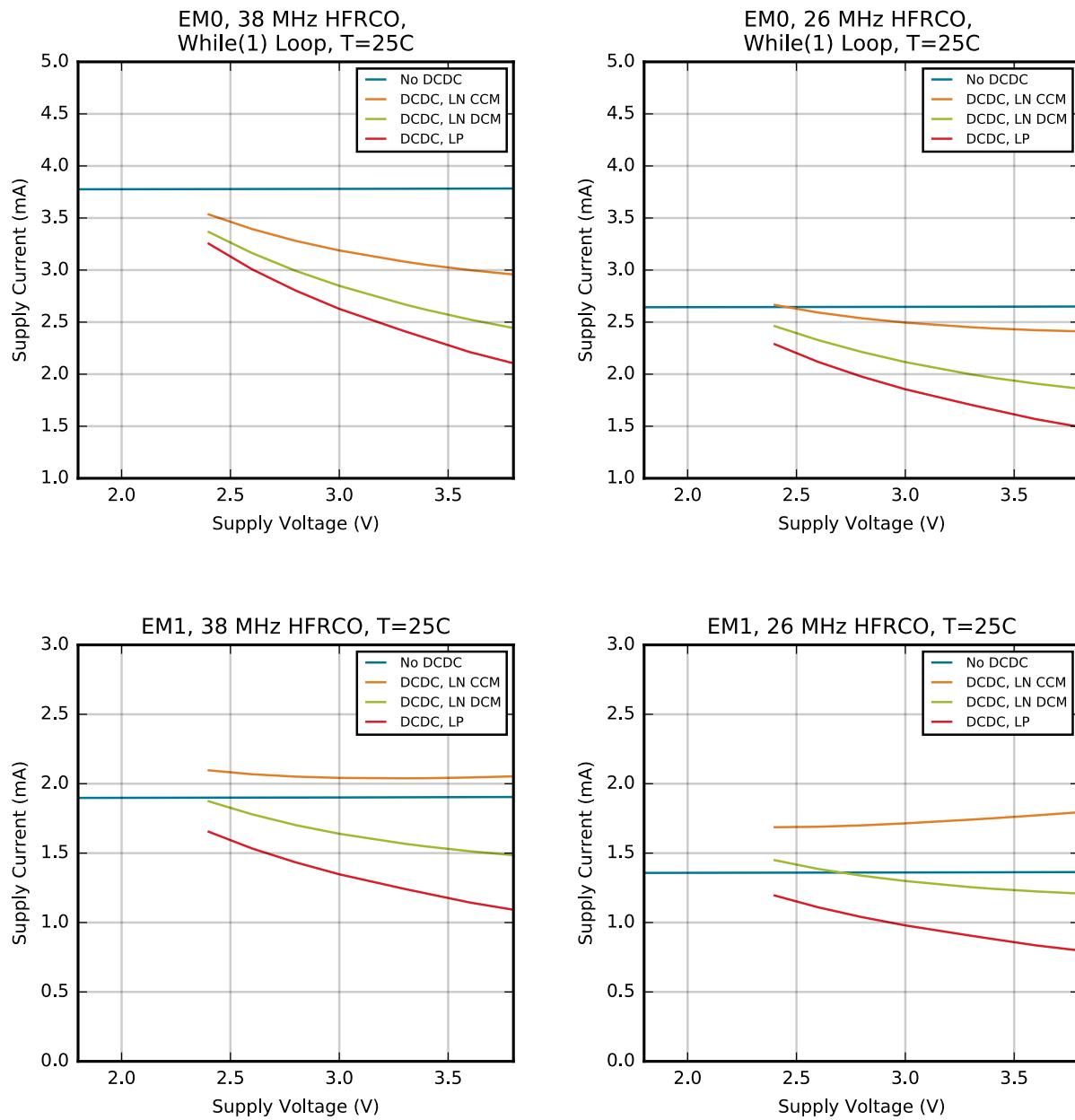


Figure 4.6. EM0 and EM1 Mode Typical Supply Current vs. Supply

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

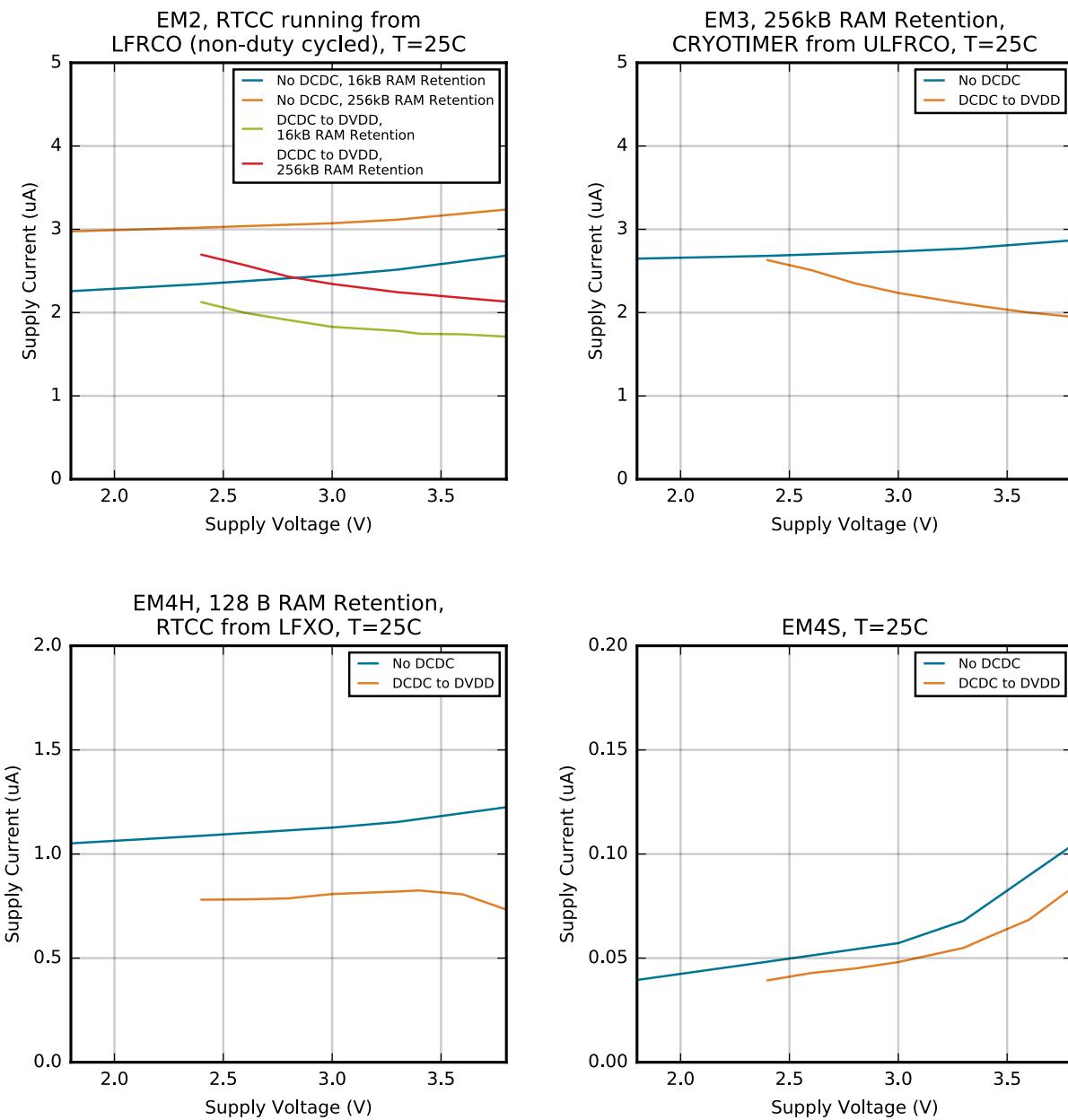


Figure 4.7. EM2, EM3, EM4H and EM4S Typical Supply Current vs. Supply

4.2.2 DC-DC Converter

Default test conditions: CCM mode, LDCDC = 4.7 μ H, CDCDC = 4.7 μ F, VDCDC_I = 3.3 V, VDCDC_O = 1.8 V, FDCDC_LN = 7 MHz

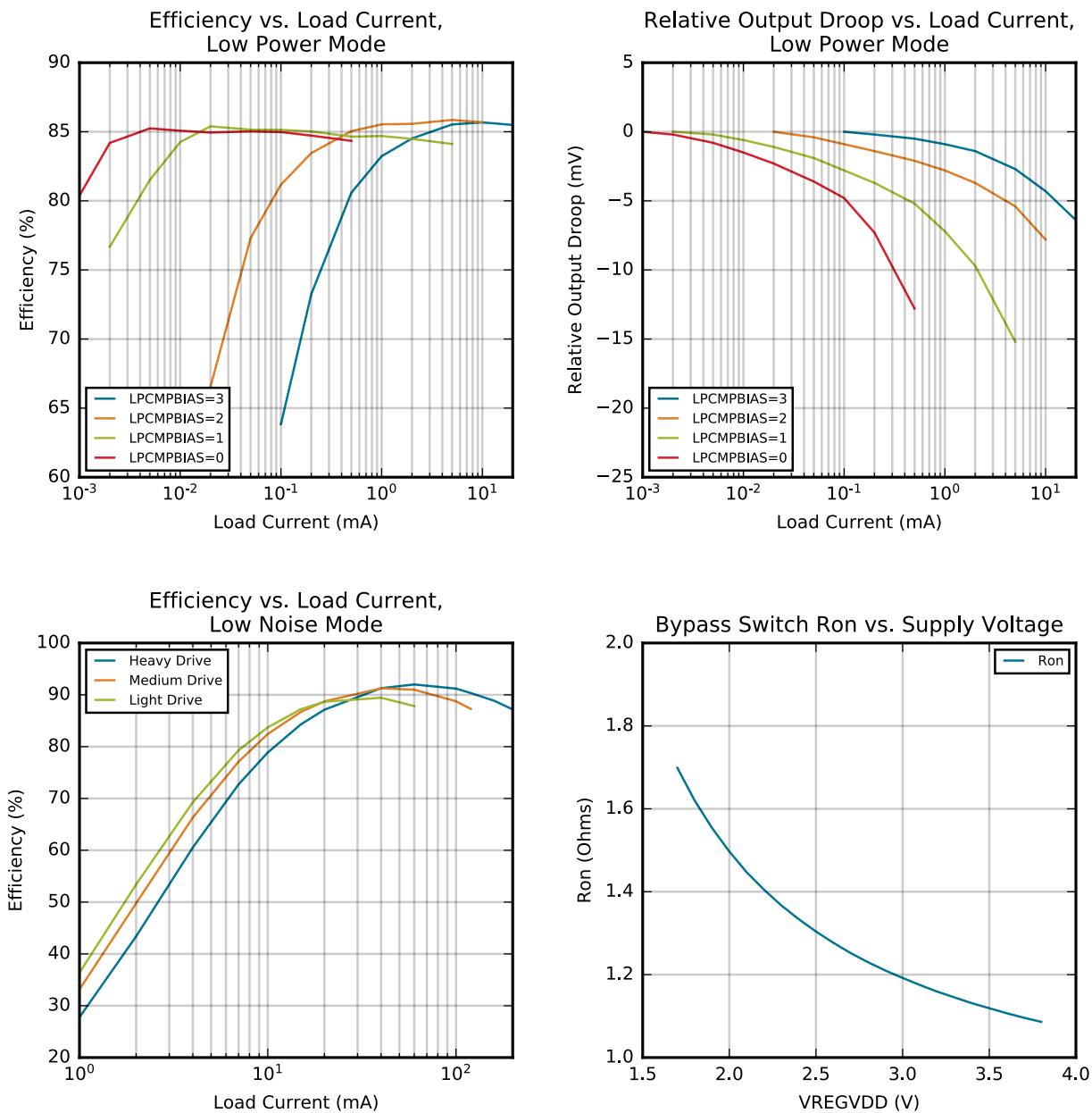


Figure 4.8. DC-DC Converter Typical Performance Characteristics

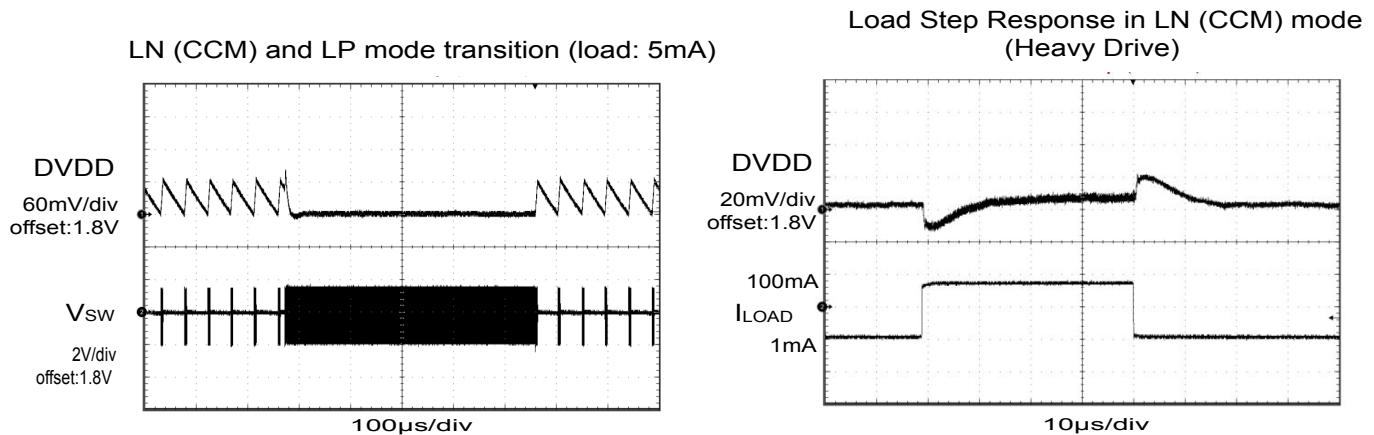


Figure 4.9. DC-DC Converter Transition Waveforms

4.2.3 2.4 GHz Radio

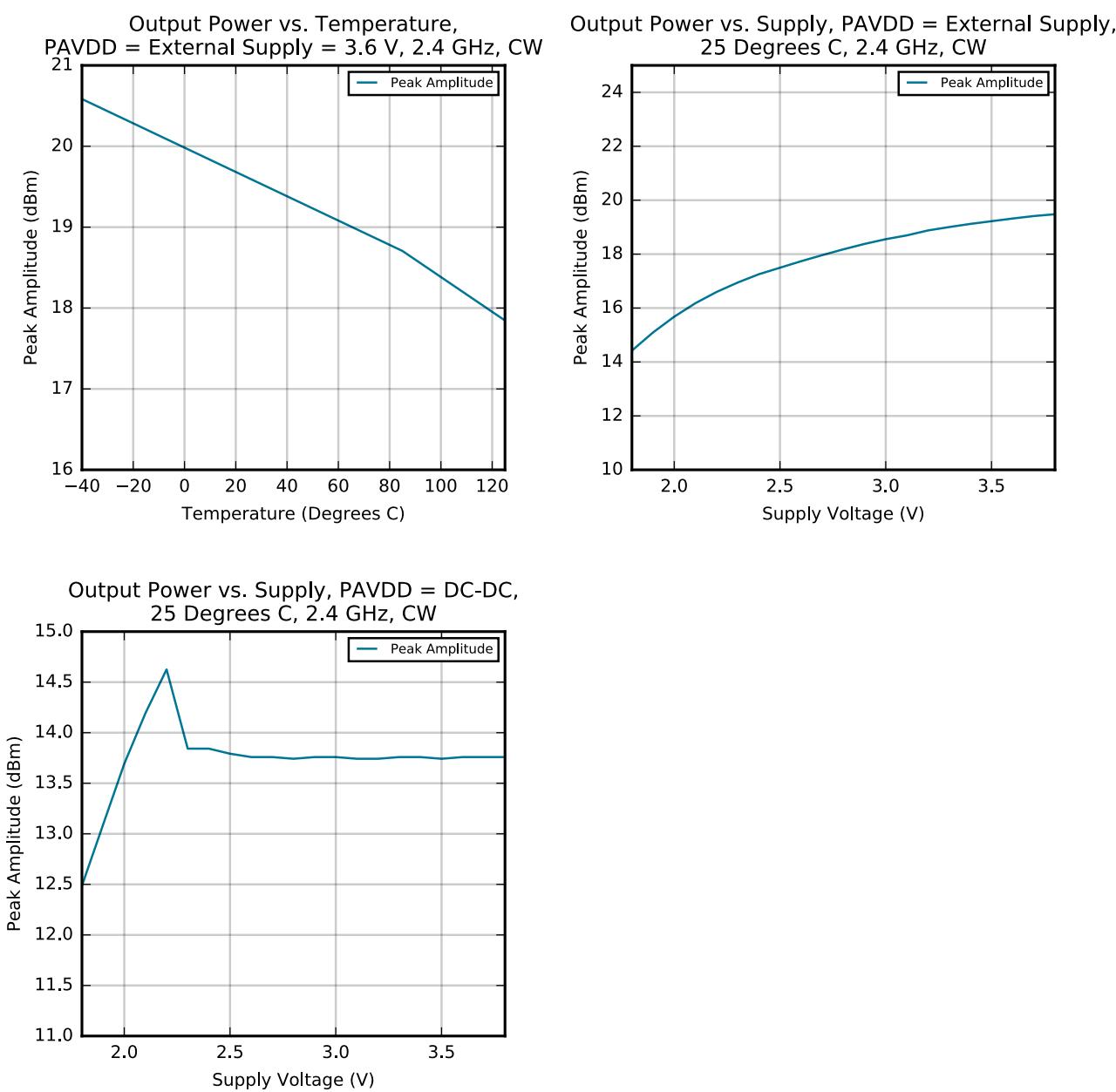


Figure 4.10. 2.4 GHz RF Transmitter Output Power

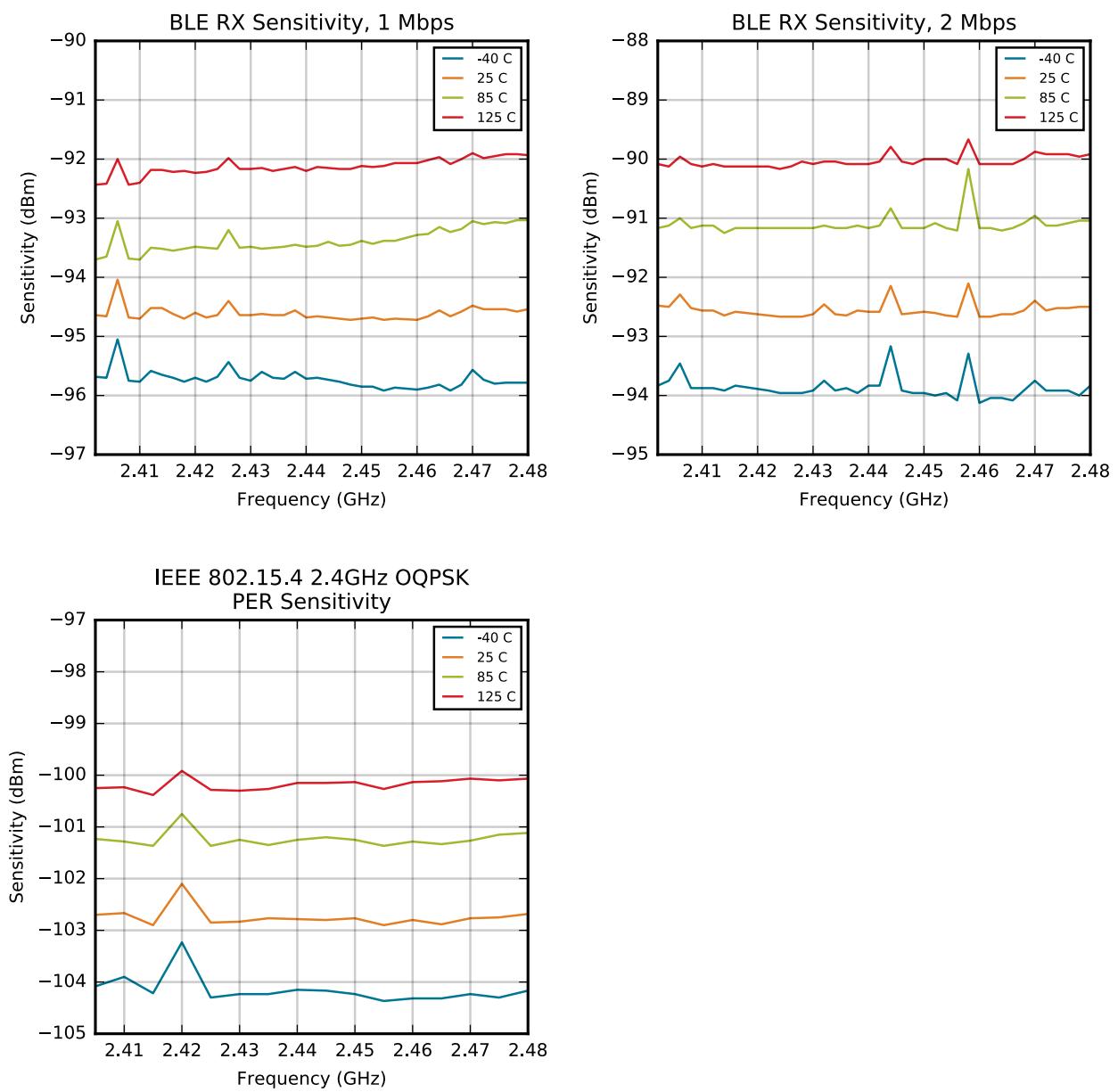


Figure 4.11. 2.4 GHz RF Receiver Sensitivity

5. Typical Connection Diagrams

5.1 Power

Typical power supply connections for direct supply, without using the internal DC-DC converter, are shown in the following figure.

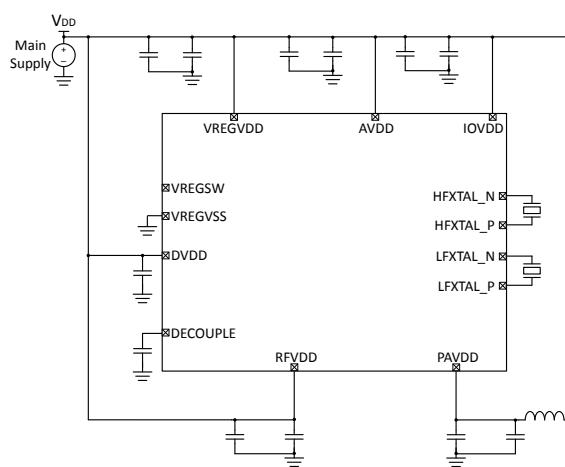


Figure 5.1. EFR32FG12 Typical Application Circuit: Direct Supply Configuration without DC-DC converter

Typical power supply circuits using the internal DC-DC converter are shown below. The MCU operates from the DC-DC converter supply. For low RF transmit power applications less than 13dBm, the RF PA may be supplied by the DC-DC converter. For OPNs supporting high power RF transmission, the RF PA must be directly supplied by VDD for RF transmit power greater than 13 dBm.

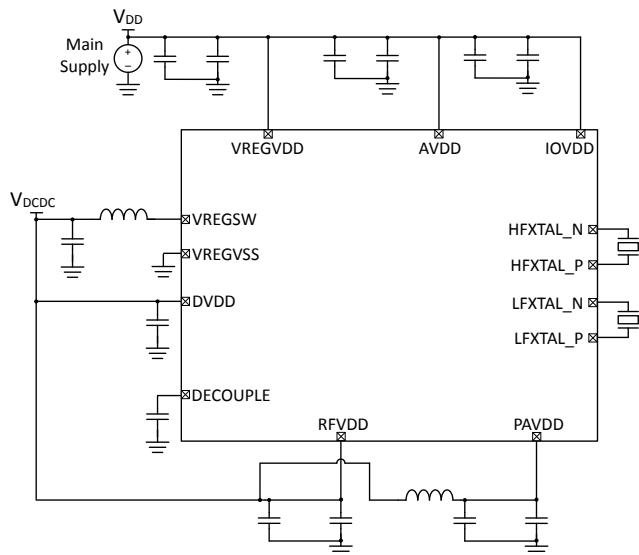


Figure 5.2. EFR32FG12 Typical Application Circuit: Configuration with DC-DC converter (PAVDD from VDCDC)

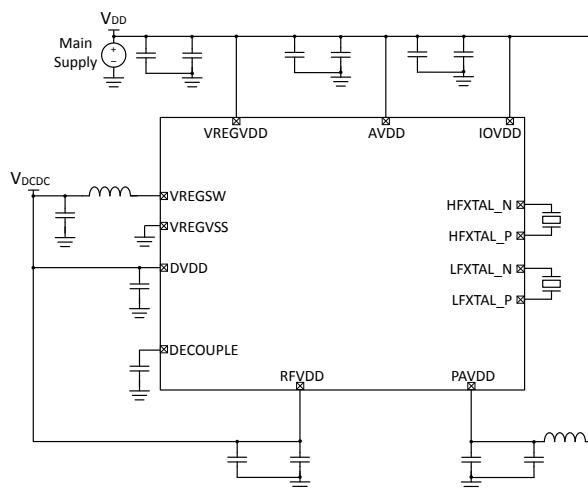


Figure 5.3. EFR32FG12 Typical Application Circuit: Configuration with DC-DC converter (PAVDD from VDD)

5.2 RF Matching Networks

Typical RF matching network circuit diagrams are shown in [Figure 5.4 Typical 2.4 GHz RF impedance-matching network circuits on page 118](#) for applications in the 2.4GHz band, and in [Figure 5.5 Typical Sub-GHz RF impedance-matching network circuits on page 118](#) for applications in the sub-GHz band. Application-specific component values can be found in application notes *AN923: EFR32 sub-GHz Matching Guide* and *AN930: EFR32 2.4 GHz Matching Guide*. For low RF transmit power applications less than 13dBm, the two-element match is recommended. For OPNs supporting high power RF transmission, the four-element match is recommended for high RF transmit power (> 13dBm).

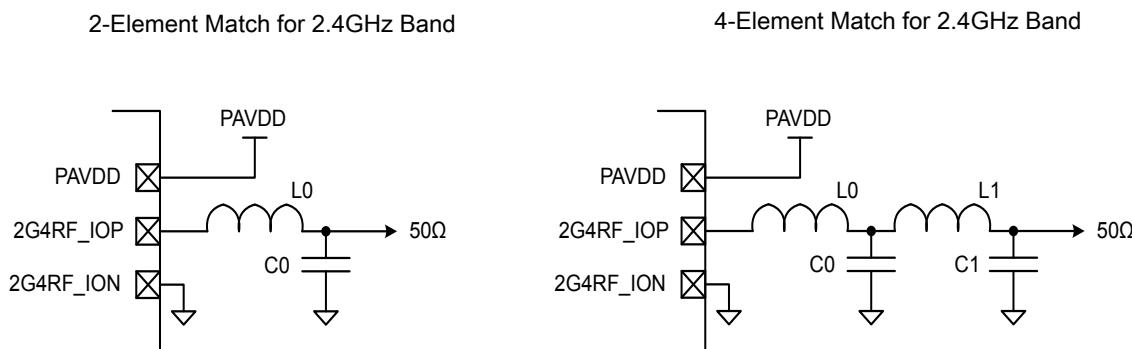


Figure 5.4. Typical 2.4 GHz RF impedance-matching network circuits

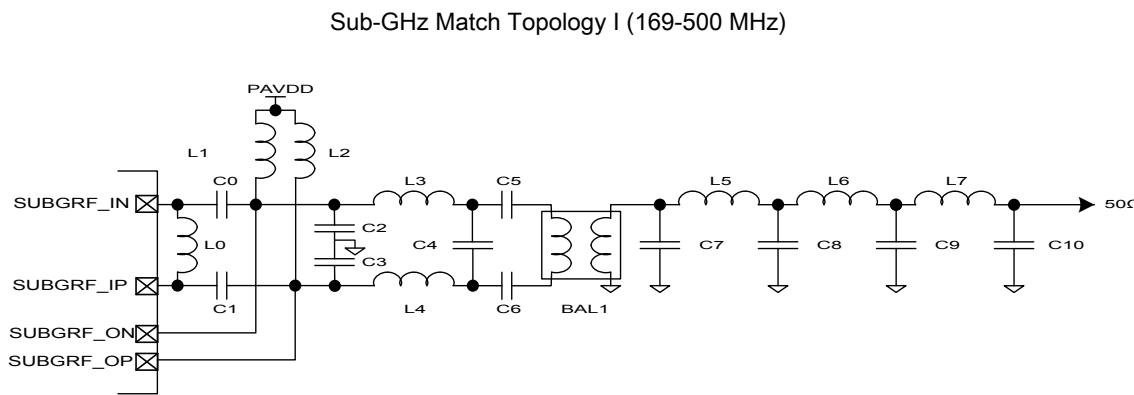


Figure 5.5. Typical Sub-GHz RF impedance-matching network circuits

5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN0002: "Hardware Design Considerations" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/32bit-appnotes).

6. Pin Definitions

6.1 BGA125 2.4 GHz and Sub-GHz Device Pinout

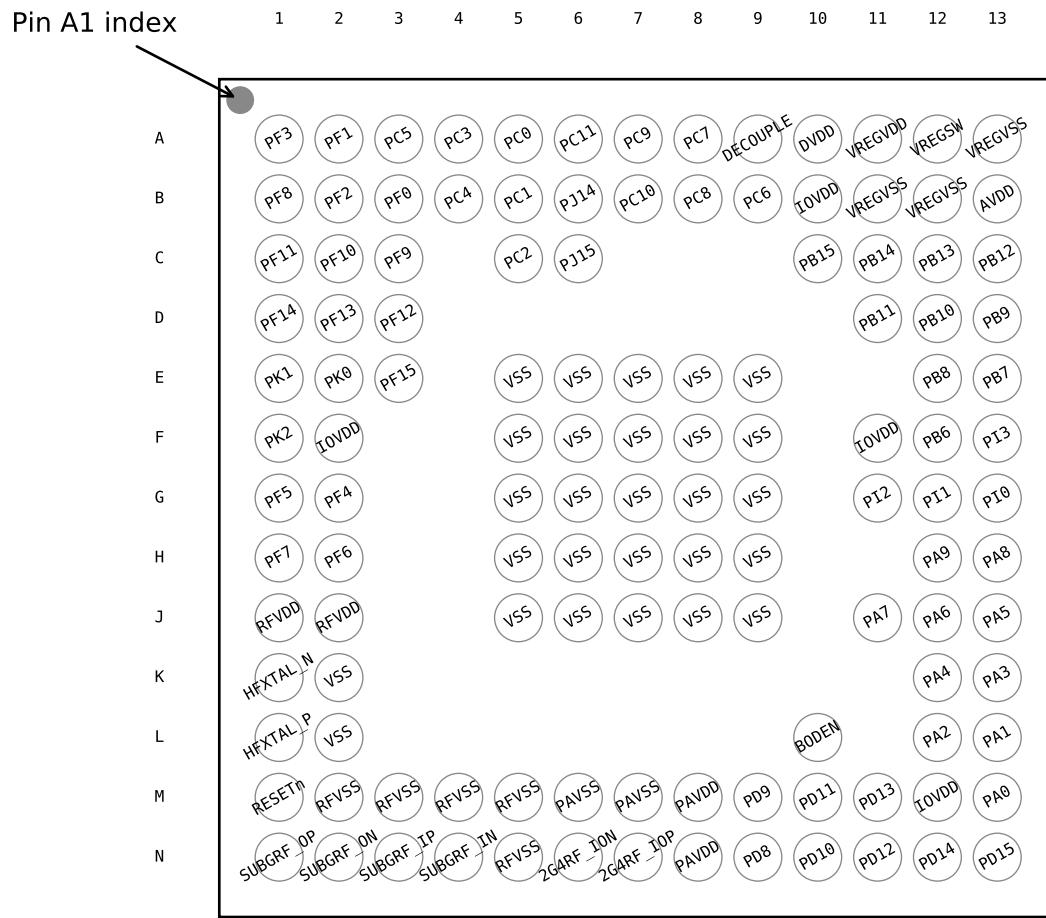


Figure 6.1. BGA125 2.4 GHz and Sub-GHz Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [6.9 GPIO Functionality Table](#) or [6.10 Alternate Functionality Overview](#).

Table 6.1. BGA125 2.4 GHz and Sub-GHz Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF3	A1	GPIO (5V)	PF1	A2	GPIO (5V)
PC5	A3	GPIO (5V)	PC3	A4	GPIO (5V)
PC0	A5	GPIO (5V)	PC11	A6	GPIO (5V)
PC9	A7	GPIO (5V)	PC7	A8	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
DECUPLE	A9	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits.	DVDD	A10	Digital power supply.
VREGVDD	A11	Voltage regulator VDD input	VREGSW	A12	DCDC regulator switching node
VREGVSS	A13 B11 B12	Voltage regulator VSS	PF8	B1	GPIO (5V)
PF2	B2	GPIO (5V)	PF0	B3	GPIO (5V)
PC4	B4	GPIO (5V)	PC1	B5	GPIO (5V)
PJ14	B6	GPIO (5V)	PC10	B7	GPIO (5V)
PC8	B8	GPIO (5V)	PC6	B9	GPIO (5V)
IOVDD	B10 F2 F11 M12	Digital IO power supply.	AVDD	B13	Analog power supply.
PF11	C1	GPIO (5V)	PF10	C2	GPIO (5V)
PF9	C3	GPIO (5V)	PC2	C5	GPIO (5V)
PJ15	C6	GPIO (5V)	PB15	C10	GPIO
PB14	C11	GPIO	PB13	C12	GPIO
PB12	C13	GPIO	PF14	D1	GPIO (5V)
PF13	D2	GPIO (5V)	PF12	D3	GPIO (5V)
PB11	D11	GPIO	PB10	D12	GPIO (5V)
PB9	D13	GPIO (5V)	PK1	E1	GPIO (5V)
PK0	E2	GPIO	PF15	E3	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	E5 E6 E7 E8 E9 F5 F6 F7 F8 F9 G5 G6 G7 G8 G9 H5 H6 H7 H8 H9 J5 J6 J7 J8 J9 K2 L2	Ground	PB8	E12	GPIO (5V)
PB7	E13	GPIO (5V)	PK2	F1	GPIO (5V)
PB6	F12	GPIO (5V)	PI3	F13	GPIO (5V)
PF5	G1	GPIO (5V)	PF4	G2	GPIO (5V)
PI2	G11	GPIO (5V)	PI1	G12	GPIO (5V)
PI0	G13	GPIO (5V)	PF7	H1	GPIO (5V)
PF6	H2	GPIO (5V)	PA9	H12	GPIO (5V)
PA8	H13	GPIO (5V)	RFVDD	J1 J2	Radio power supply
PA7	J11	GPIO (5V)	PA6	J12	GPIO (5V)
PA5	J13	GPIO (5V)	HFXTAL_N	K1	High Frequency Crystal input pin.
PA4	K12	GPIO	PA3	K13	GPIO
HFXTAL_P	L1	High Frequency Crystal output pin.	BODEN	L10	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.
PA2	L12	GPIO	PA1	L13	GPIO
RESETn	M1	Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	RFVSS	M2 M3 M4 M5 N5	Radio Ground
PAVSS	M6 M7	Power Amplifier (PA) voltage regulator VSS	PAVDD	M8 N8	Power Amplifier (PA) voltage regulator VDD input
PD9	M9	GPIO (5V)	PD11	M10	GPIO (5V)
PD13	M11	GPIO	PA0	M13	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
SUBGRF_OP	N1	Sub GHz Differential RF output, positive path.	SUBGRF_ON	N2	Sub GHz Differential RF output, negative path.
SUBGRF_IP	N3	Sub GHz Differential RF input, positive path.	SUBGRF_IN	N4	Sub GHz Differential RF input, negative path.
2G4RF_ION	N6	2.4 GHz Differential RF input/output, negative path. This pin should be externally grounded.	2G4RF_IOP	N7	2.4 GHz Differential RF input/output, positive path.
PD8	N9	GPIO (5V)	PD10	N10	GPIO (5V)
PD12	N11	GPIO (5V)	PD14	N12	GPIO
PD15	N13	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

6.2 BGA125 2.4 GHz Device Pinout

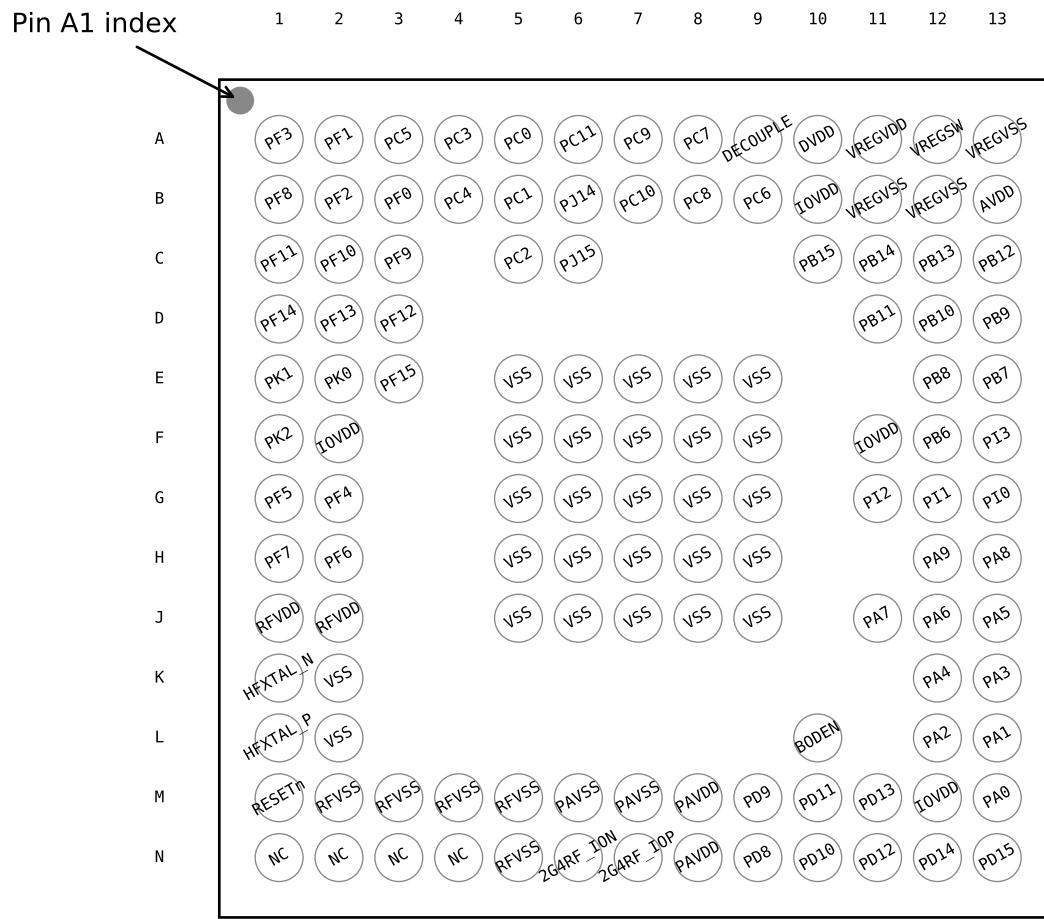


Figure 6.2. BGA125 2.4 GHz Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [6.9 GPIO Functionality Table](#) or [6.10 Alternate Functionality Overview](#).

Table 6.2. BGA125 2.4 GHz Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF3	A1	GPIO (5V)	PF1	A2	GPIO (5V)
PC5	A3	GPIO (5V)	PC3	A4	GPIO (5V)
PC0	A5	GPIO (5V)	PC11	A6	GPIO (5V)
PC9	A7	GPIO (5V)	PC7	A8	GPIO (5V)
DECUPLE	A9	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits.	DVDD	A10	Digital power supply.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVDD	A11	Voltage regulator VDD input	VREGSW	A12	DCDC regulator switching node
VREGVSS	A13 B11 B12	Voltage regulator VSS	PF8	B1	GPIO (5V)
PF2	B2	GPIO (5V)	PF0	B3	GPIO (5V)
PC4	B4	GPIO (5V)	PC1	B5	GPIO (5V)
PJ14	B6	GPIO (5V)	PC10	B7	GPIO (5V)
PC8	B8	GPIO (5V)	PC6	B9	GPIO (5V)
IOVDD	B10 F2 F11 M12	Digital IO power supply.	AVDD	B13	Analog power supply.
PF11	C1	GPIO (5V)	PF10	C2	GPIO (5V)
PF9	C3	GPIO (5V)	PC2	C5	GPIO (5V)
PJ15	C6	GPIO (5V)	PB15	C10	GPIO
PB14	C11	GPIO	PB13	C12	GPIO
PB12	C13	GPIO	PF14	D1	GPIO (5V)
PF13	D2	GPIO (5V)	PF12	D3	GPIO (5V)
PB11	D11	GPIO	PB10	D12	GPIO (5V)
PB9	D13	GPIO (5V)	PK1	E1	GPIO (5V)
PK0	E2	GPIO	PF15	E3	GPIO (5V)
VSS	E5 E6 E7 E8 E9 F5 F6 F7 F8 F9 G5 G6 G7 G8 G9 H5 H6 H7 H8 H9 J5 J6 J7 J8 J9 K2 L2	Ground	PB8	E12	GPIO (5V)
PB7	E13	GPIO (5V)	PK2	F1	GPIO (5V)
PB6	F12	GPIO (5V)	PI3	F13	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF5	G1	GPIO (5V)	PF4	G2	GPIO (5V)
PI2	G11	GPIO (5V)	PI1	G12	GPIO (5V)
PI0	G13	GPIO (5V)	PF7	H1	GPIO (5V)
PF6	H2	GPIO (5V)	PA9	H12	GPIO (5V)
PA8	H13	GPIO (5V)	RFVDD	J1 J2	Radio power supply
PA7	J11	GPIO (5V)	PA6	J12	GPIO (5V)
PA5	J13	GPIO (5V)	HFXTAL_N	K1	High Frequency Crystal input pin.
PA4	K12	GPIO	PA3	K13	GPIO
HFXTAL_P	L1	High Frequency Crystal output pin.	BODEN	L10	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.
PA2	L12	GPIO	PA1	L13	GPIO
RESETn	M1	Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	RFVSS	M2 M3 M4 M5 N5	Radio Ground
PAVSS	M6 M7	Power Amplifier (PA) voltage regulator VSS	PAVDD	M8 N8	Power Amplifier (PA) voltage regulator VDD input
PD9	M9	GPIO (5V)	PD11	M10	GPIO (5V)
PD13	M11	GPIO	PA0	M13	GPIO
NC	N1 N2 N3 N4	No Connect.	2G4RF_ION	N6	2.4 GHz Differential RF input/output, negative path. This pin should be externally grounded.
2G4RF_IOP	N7	2.4 GHz Differential RF input/output, positive path.	PD8	N9	GPIO (5V)
PD10	N10	GPIO (5V)	PD12	N11	GPIO (5V)
PD14	N12	GPIO	PD15	N13	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

6.3 BGA125 Sub-GHz Device Pinout

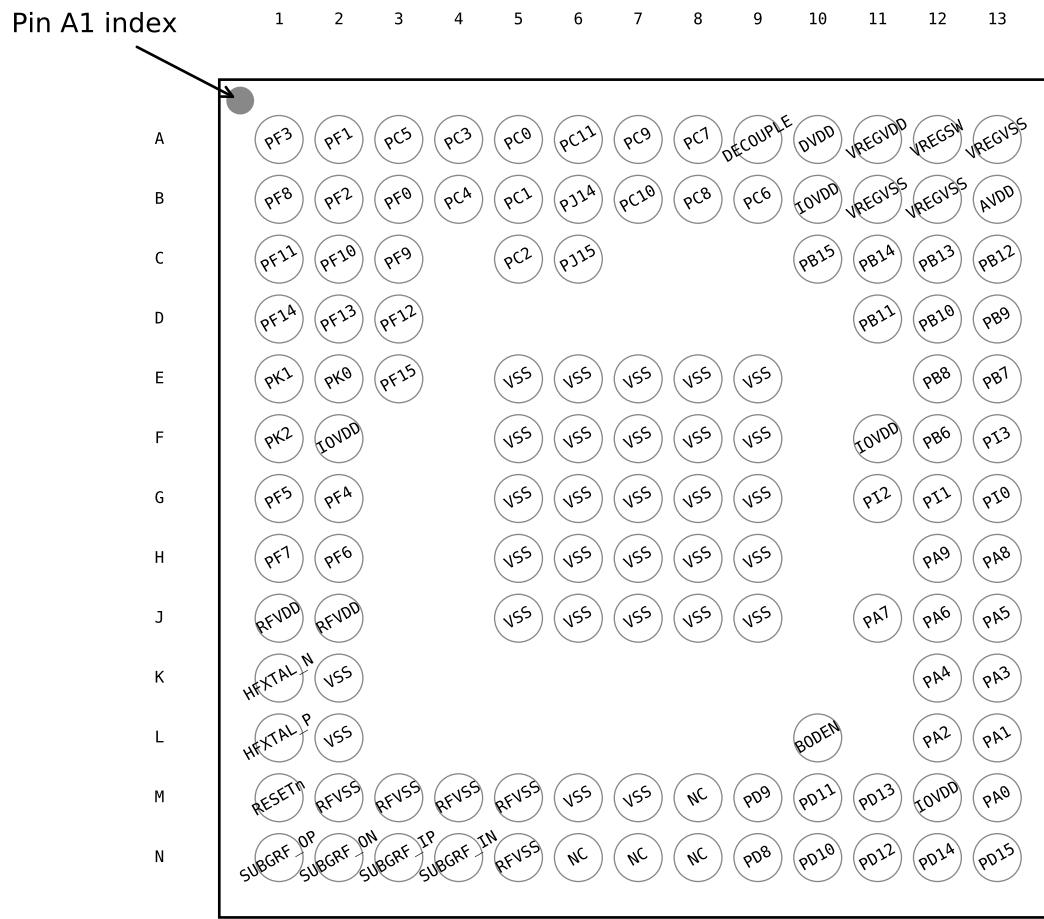


Figure 6.3. BGA125 Sub-GHz Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [6.9 GPIO Functionality Table](#) or [6.10 Alternate Functionality Overview](#).

Table 6.3. BGA125 Sub-GHz Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF3	A1	GPIO (5V)	PF1	A2	GPIO (5V)
PC5	A3	GPIO (5V)	PC3	A4	GPIO (5V)
PC0	A5	GPIO (5V)	PC11	A6	GPIO (5V)
PC9	A7	GPIO (5V)	PC7	A8	GPIO (5V)
DECOPPLE	A9	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits.	DVDD	A10	Digital power supply.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVDD	A11	Voltage regulator VDD input	VREGSW	A12	DCDC regulator switching node
VREGVSS	A13 B11 B12	Voltage regulator VSS	PF8	B1	GPIO (5V)
PF2	B2	GPIO (5V)	PF0	B3	GPIO (5V)
PC4	B4	GPIO (5V)	PC1	B5	GPIO (5V)
PJ14	B6	GPIO (5V)	PC10	B7	GPIO (5V)
PC8	B8	GPIO (5V)	PC6	B9	GPIO (5V)
IOVDD	B10 F2 F11 M12	Digital IO power supply.	AVDD	B13	Analog power supply.
PF11	C1	GPIO (5V)	PF10	C2	GPIO (5V)
PF9	C3	GPIO (5V)	PC2	C5	GPIO (5V)
PJ15	C6	GPIO (5V)	PB15	C10	GPIO
PB14	C11	GPIO	PB13	C12	GPIO
PB12	C13	GPIO	PF14	D1	GPIO (5V)
PF13	D2	GPIO (5V)	PF12	D3	GPIO (5V)
PB11	D11	GPIO	PB10	D12	GPIO (5V)
PB9	D13	GPIO (5V)	PK1	E1	GPIO (5V)
PK0	E2	GPIO	PF15	E3	GPIO (5V)
VSS	E5 E6 E7 E8 E9 F5 F6 F7 F8 F9 G5 G6 G7 G8 G9 H5 H6 H7 H8 H9 J5 J6 J7 J8 J9 K2 L2 M6 M7	Ground	PB8	E12	GPIO (5V)
PB7	E13	GPIO (5V)	PK2	F1	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB6	F12	GPIO (5V)	PI3	F13	GPIO (5V)
PF5	G1	GPIO (5V)	PF4	G2	GPIO (5V)
PI2	G11	GPIO (5V)	PI1	G12	GPIO (5V)
PI0	G13	GPIO (5V)	PF7	H1	GPIO (5V)
PF6	H2	GPIO (5V)	PA9	H12	GPIO (5V)
PA8	H13	GPIO (5V)	RFVDD	J1 J2	Radio power supply
PA7	J11	GPIO (5V)	PA6	J12	GPIO (5V)
PA5	J13	GPIO (5V)	HFXTAL_N	K1	High Frequency Crystal input pin.
PA4	K12	GPIO	PA3	K13	GPIO
HFXTAL_P	L1	High Frequency Crystal output pin.	BODEN	L10	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.
PA2	L12	GPIO	PA1	L13	GPIO
RESETn	M1	Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	RFVSS	M2 M3 M4 M5 N5	Radio Ground
NC	M8 N6 N7 N8	No Connect.	PD9	M9	GPIO (5V)
PD11	M10	GPIO (5V)	PD13	M11	GPIO
PA0	M13	GPIO	SUBGRF_OP	N1	Sub GHz Differential RF output, positive path.
SUBGRF_ON	N2	Sub GHz Differential RF output, negative path.	SUBGRF_IP	N3	Sub GHz Differential RF input, positive path.
SUBGRF_IN	N4	Sub GHz Differential RF input, negative path.	PD8	N9	GPIO (5V)
PD10	N10	GPIO (5V)	PD12	N11	GPIO (5V)
PD14	N12	GPIO	PD15	N13	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

6.4 QFN68 2.4 GHz and Sub-GHz Device Pinout

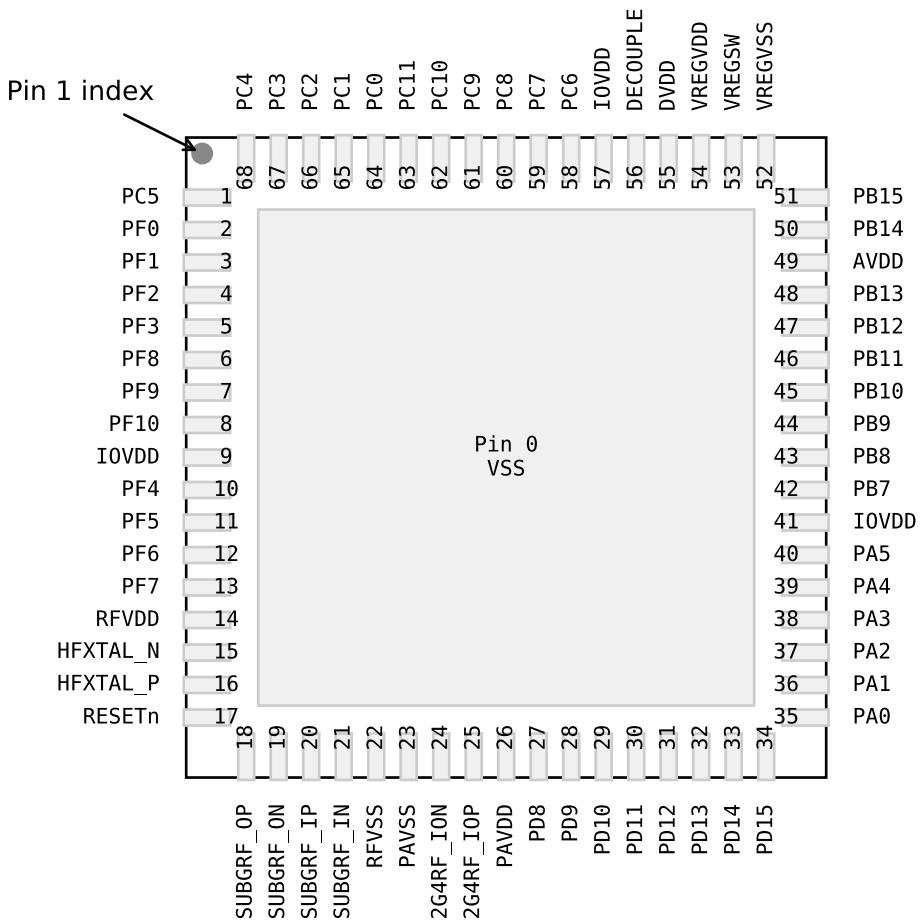


Figure 6.4. QFN68 2.4 GHz and Sub-GHz Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [6.9 GPIO Functionality Table](#) or [6.10 Alternate Functionality Overview](#).

Table 6.4. QFN68 2.4 GHz and Sub-GHz Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PC5	1	GPIO (5V)
PF0	2	GPIO (5V)	PF1	3	GPIO (5V)
PF2	4	GPIO (5V)	PF3	5	GPIO (5V)
PF8	6	GPIO (5V)	PF9	7	GPIO (5V)
PF10	8	GPIO (5V)	IOVDD	9 41 57	Digital IO power supply.
PF4	10	GPIO (5V)	PF5	11	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF6	12	GPIO (5V)	PF7	13	GPIO (5V)
RFVDD	14	Radio power supply	HFXTAL_N	15	High Frequency Crystal input pin.
HFXTAL_P	16	High Frequency Crystal output pin.	RESETn	17	Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
SUBGRF_OP	18	Sub GHz Differential RF output, positive path.	SUBGRF_ON	19	Sub GHz Differential RF output, negative path.
SUBGRF_IP	20	Sub GHz Differential RF input, positive path.	SUBGRF_IN	21	Sub GHz Differential RF input, negative path.
RFVSS	22	Radio Ground	PAVSS	23	Power Amplifier (PA) voltage regulator VSS
2G4RFION	24	2.4 GHz Differential RF input/output, negative path. This pin should be externally grounded.	2G4RF_IOP	25	2.4 GHz Differential RF input/output, positive path.
PAVDD	26	Power Amplifier (PA) voltage regulator VDD input	PD8	27	GPIO (5V)
PD9	28	GPIO (5V)	PD10	29	GPIO (5V)
PD11	30	GPIO (5V)	PD12	31	GPIO (5V)
PD13	32	GPIO	PD14	33	GPIO
PD15	34	GPIO	PA0	35	GPIO
PA1	36	GPIO	PA2	37	GPIO
PA3	38	GPIO	PA4	39	GPIO
PA5	40	GPIO (5V)	PB7	42	GPIO (5V)
PB8	43	GPIO (5V)	PB9	44	GPIO (5V)
PB10	45	GPIO (5V)	PB11	46	GPIO
PB12	47	GPIO	PB13	48	GPIO
AVDD	49	Analog power supply.	PB14	50	GPIO
PB15	51	GPIO	VREGVSS	52	Voltage regulator VSS
VREGSW	53	DCDC regulator switching node	VREGVDD	54	Voltage regulator VDD input
DVDD	55	Digital power supply.	DECOPPLE	56	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits.
PC6	58	GPIO (5V)	PC7	59	GPIO (5V)
PC8	60	GPIO (5V)	PC9	61	GPIO (5V)
PC10	62	GPIO (5V)	PC11	63	GPIO (5V)
PC0	64	GPIO (5V)	PC1	65	GPIO (5V)
PC2	66	GPIO (5V)	PC3	67	GPIO (5V)
PC4	68	GPIO (5V)			

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
Note:					
1. GPIO with 5V tolerance are indicated by (5V).					

6.5 QFN68 Sub-GHz Device Pinout

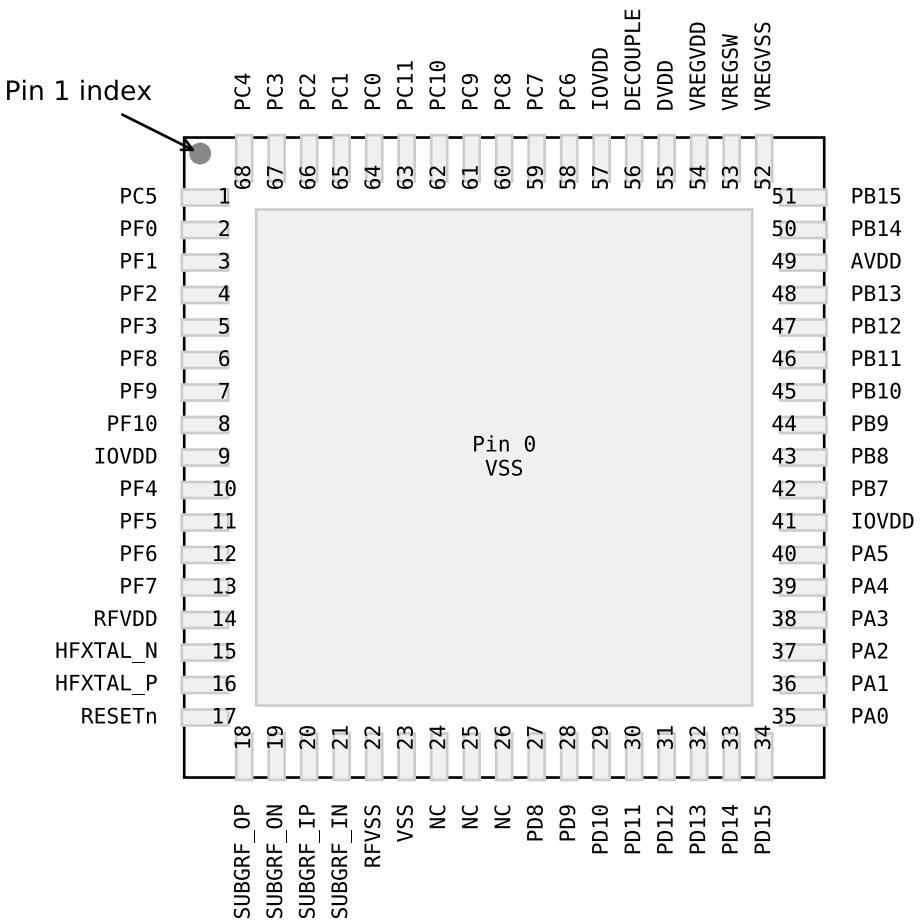


Figure 6.5. QFN68 Sub-GHz Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [6.9 GPIO Functionality Table](#) or [6.10 Alternate Functionality Overview](#).

Table 6.5. QFN68 Sub-GHz Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0 23	Ground	PC5	1	GPIO (5V)
PF0	2	GPIO (5V)	PF1	3	GPIO (5V)
PF2	4	GPIO (5V)	PF3	5	GPIO (5V)
PF8	6	GPIO (5V)	PF9	7	GPIO (5V)
PF10	8	GPIO (5V)	IOVDD	9 41 57	Digital IO power supply.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF4	10	GPIO (5V)	PF5	11	GPIO (5V)
PF6	12	GPIO (5V)	PF7	13	GPIO (5V)
RFVDD	14	Radio power supply	HFXTAL_N	15	High Frequency Crystal input pin.
HFXTAL_P	16	High Frequency Crystal output pin.	RESETn	17	Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
SUBGRF_OP	18	Sub GHz Differential RF output, positive path.	SUBGRF_ON	19	Sub GHz Differential RF output, negative path.
SUBGRF_IP	20	Sub GHz Differential RF input, positive path.	SUBGRF_IN	21	Sub GHz Differential RF input, negative path.
RFVSS	22	Radio Ground	NC	24 25 26	No Connect.
PD8	27	GPIO (5V)	PD9	28	GPIO (5V)
PD10	29	GPIO (5V)	PD11	30	GPIO (5V)
PD12	31	GPIO (5V)	PD13	32	GPIO
PD14	33	GPIO	PD15	34	GPIO
PA0	35	GPIO	PA1	36	GPIO
PA2	37	GPIO	PA3	38	GPIO
PA4	39	GPIO	PA5	40	GPIO (5V)
PB7	42	GPIO (5V)	PB8	43	GPIO (5V)
PB9	44	GPIO (5V)	PB10	45	GPIO (5V)
PB11	46	GPIO	PB12	47	GPIO
PB13	48	GPIO	AVDD	49	Analog power supply.
PB14	50	GPIO	PB15	51	GPIO
VREGVSS	52	Voltage regulator VSS	VREGSW	53	DCDC regulator switching node
VREGVDD	54	Voltage regulator VDD input	DVDD	55	Digital power supply.
DECOPPLE	56	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits.	PC6	58	GPIO (5V)
PC7	59	GPIO (5V)	PC8	60	GPIO (5V)
PC9	61	GPIO (5V)	PC10	62	GPIO (5V)
PC11	63	GPIO (5V)	PC0	64	GPIO (5V)
PC1	65	GPIO (5V)	PC2	66	GPIO (5V)
PC3	67	GPIO (5V)	PC4	68	GPIO (5V)
Note:					
1. GPIO with 5V tolerance are indicated by (5V).					

6.6 QFN48 2.4 GHz and Sub-GHz Device Pinout

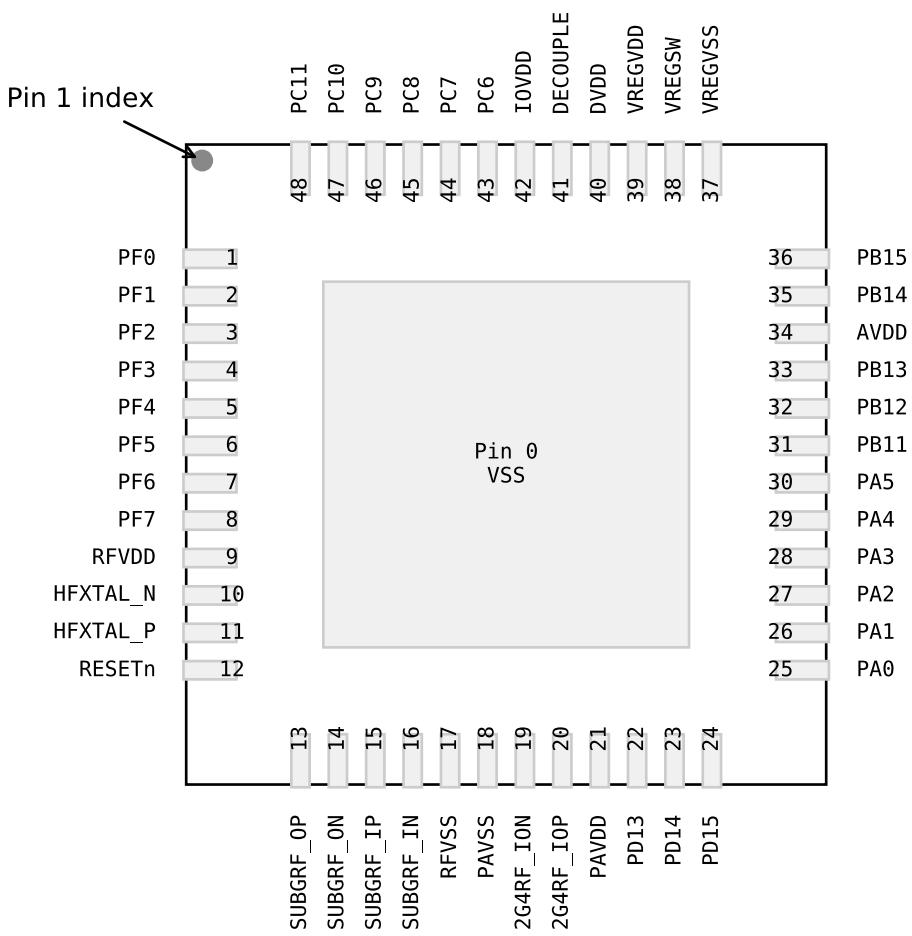


Figure 6.6. QFN48 2.4 GHz and Sub-GHz Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [6.9 GPIO Functionality Table](#) or [6.10 Alternate Functionality Overview](#).

Table 6.6. QFN48 2.4 GHz and Sub-GHz Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PF0	1	GPIO (5V)
PF1	2	GPIO (5V)	PF2	3	GPIO (5V)
PF3	4	GPIO (5V)	PF4	5	GPIO (5V)
PF5	6	GPIO (5V)	PF6	7	GPIO (5V)
PF7	8	GPIO (5V)	RFVDD	9	Radio power supply
HFXTAL_N	10	High Frequency Crystal input pin.	HFXTAL_P	11	High Frequency Crystal output pin.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
RESETn	12	Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	SUBGRF_OP	13	Sub GHz Differential RF output, positive path.
SUBGRF_ON	14	Sub GHz Differential RF output, negative path.	SUBGRF_IP	15	Sub GHz Differential RF input, positive path.
SUBGRF_IN	16	Sub GHz Differential RF input, negative path.	RFVSS	17	Radio Ground
PAVSS	18	Power Amplifier (PA) voltage regulator VSS	2G4RF_ION	19	2.4 GHz Differential RF input/output, negative path. This pin should be externally grounded.
2G4RF_IOP	20	2.4 GHz Differential RF input/output, positive path.	PAVDD	21	Power Amplifier (PA) voltage regulator VDD input
PD13	22	GPIO	PD14	23	GPIO
PD15	24	GPIO	PA0	25	GPIO
PA1	26	GPIO	PA2	27	GPIO
PA3	28	GPIO	PA4	29	GPIO
PA5	30	GPIO (5V)	PB11	31	GPIO
PB12	32	GPIO	PB13	33	GPIO
AVDD	34	Analog power supply.	PB14	35	GPIO
PB15	36	GPIO	VREGVSS	37	Voltage regulator VSS
VREGSW	38	DCDC regulator switching node	VREGVDD	39	Voltage regulator VDD input
DVDD	40	Digital power supply.	DECOPPLE	41	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits.
IOVDD	42	Digital IO power supply.	PC6	43	GPIO (5V)
PC7	44	GPIO (5V)	PC8	45	GPIO (5V)
PC9	46	GPIO (5V)	PC10	47	GPIO (5V)
PC11	48	GPIO (5V)			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

6.7 QFN48 2.4 GHz Device Pinout

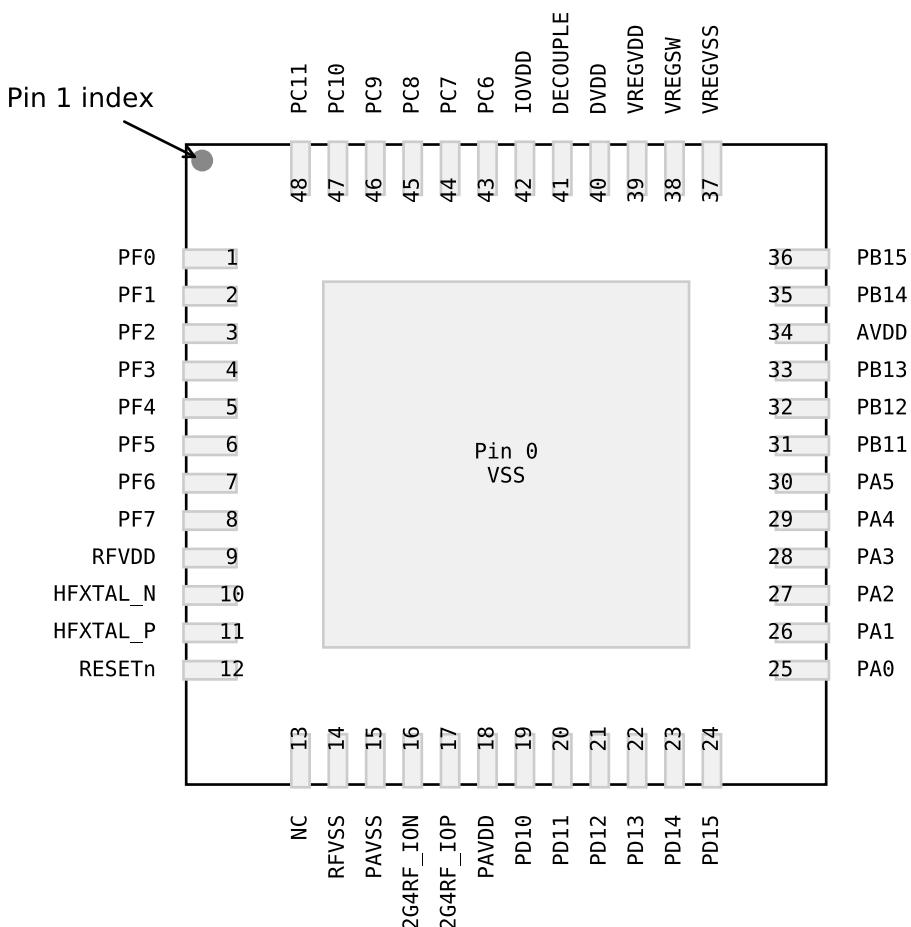


Figure 6.7. QFN48 2.4 GHz Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [6.9 GPIO Functionality Table](#) or [6.10 Alternate Functionality Overview](#).

Table 6.7. QFN48 2.4 GHz Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PF0	1	GPIO (5V)
PF1	2	GPIO (5V)	PF2	3	GPIO (5V)
PF3	4	GPIO (5V)	PF4	5	GPIO (5V)
PF5	6	GPIO (5V)	PF6	7	GPIO (5V)
PF7	8	GPIO (5V)	RFVDD	9	Radio power supply
HFXTAL_N	10	High Frequency Crystal input pin.	HFXTAL_P	11	High Frequency Crystal output pin.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
RESETn	12	Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	NC	13	No Connect.
RFVSS	14	Radio Ground	PAVSS	15	Power Amplifier (PA) voltage regulator VSS
2G4RF_ION	16	2.4 GHz Differential RF input/output, negative path. This pin should be externally grounded.	2G4RF_IOP	17	2.4 GHz Differential RF input/output, positive path.
PAVDD	18	Power Amplifier (PA) voltage regulator VDD input	PD10	19	GPIO (5V)
PD11	20	GPIO (5V)	PD12	21	GPIO (5V)
PD13	22	GPIO	PD14	23	GPIO
PD15	24	GPIO	PA0	25	GPIO
PA1	26	GPIO	PA2	27	GPIO
PA3	28	GPIO	PA4	29	GPIO
PA5	30	GPIO (5V)	PB11	31	GPIO
PB12	32	GPIO	PB13	33	GPIO
AVDD	34	Analog power supply.	PB14	35	GPIO
PB15	36	GPIO	VREGVSS	37	Voltage regulator VSS
VREGSW	38	DCDC regulator switching node	VREGVDD	39	Voltage regulator VDD input
DVDD	40	Digital power supply.	DECUPLE	41	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits.
IOVDD	42	Digital IO power supply.	PC6	43	GPIO (5V)
PC7	44	GPIO (5V)	PC8	45	GPIO (5V)
PC9	46	GPIO (5V)	PC10	47	GPIO (5V)
PC11	48	GPIO (5V)			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

6.8 QFN48 Sub-GHz Device Pinout

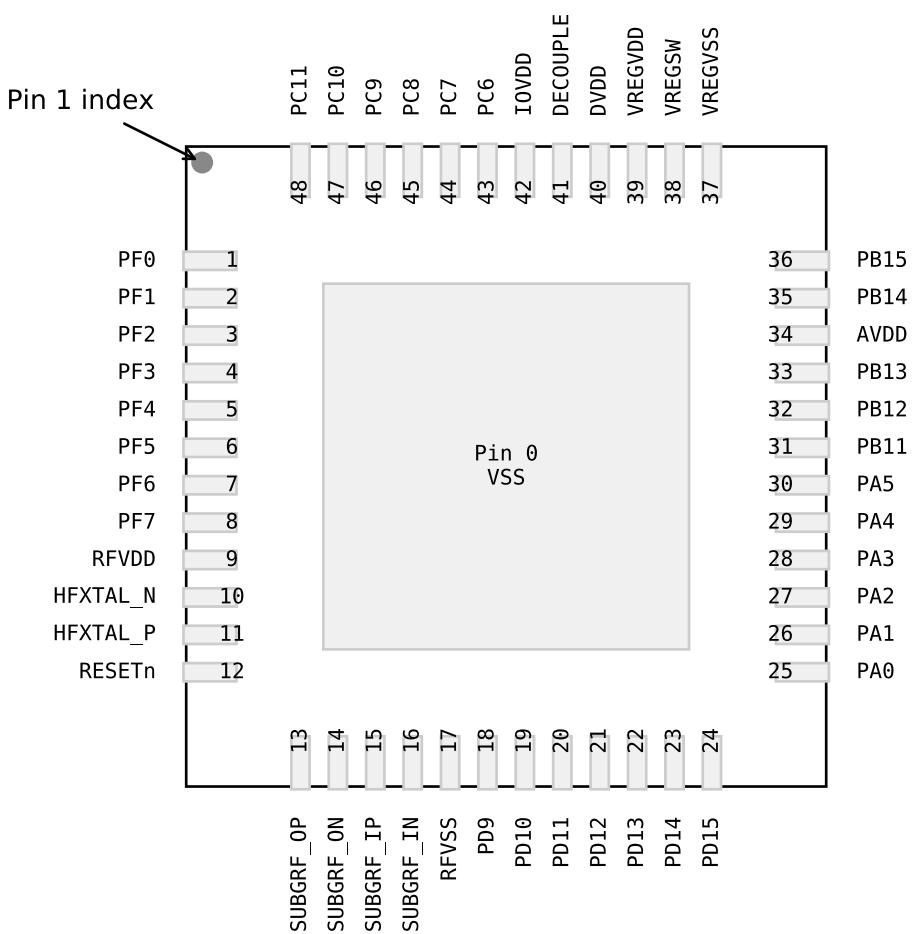


Figure 6.8. QFN48 Sub-GHz Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [6.9 GPIO Functionality Table](#) or [6.10 Alternate Functionality Overview](#).

Table 6.8. QFN48 Sub-GHz Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PF0	1	GPIO (5V)
PF1	2	GPIO (5V)	PF2	3	GPIO (5V)
PF3	4	GPIO (5V)	PF4	5	GPIO (5V)
PF5	6	GPIO (5V)	PF6	7	GPIO (5V)
PF7	8	GPIO (5V)	RFVDD	9	Radio power supply
HFXTAL_N	10	High Frequency Crystal input pin.	HFXTAL_P	11	High Frequency Crystal output pin.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
RESETn	12	Reset input, active low. This pin is internally pulled up to AVDD. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	SUBGRF_OP	13	Sub GHz Differential RF output, positive path.
SUBGRF_ON	14	Sub GHz Differential RF output, negative path.	SUBGRF_IP	15	Sub GHz Differential RF input, positive path.
SUBGRF_IN	16	Sub GHz Differential RF input, negative path.	RFVSS	17	Radio Ground
PD9	18	GPIO (5V)	PD10	19	GPIO (5V)
PD11	20	GPIO (5V)	PD12	21	GPIO (5V)
PD13	22	GPIO	PD14	23	GPIO
PD15	24	GPIO	PA0	25	GPIO
PA1	26	GPIO	PA2	27	GPIO
PA3	28	GPIO	PA4	29	GPIO
PA5	30	GPIO (5V)	PB11	31	GPIO
PB12	32	GPIO	PB13	33	GPIO
AVDD	34	Analog power supply.	PB14	35	GPIO
PB15	36	GPIO	VREGVSS	37	Voltage regulator VSS
VREGSW	38	DCDC regulator switching node	VREGVDD	39	Voltage regulator VDD input
DVDD	40	Digital power supply.	DECOPULE	41	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. This pin should not be used to power any external circuits.
IOVDD	42	Digital IO power supply.	PC6	43	GPIO (5V)
PC7	44	GPIO (5V)	PC8	45	GPIO (5V)
PC9	46	GPIO (5V)	PC10	47	GPIO (5V)
PC11	48	GPIO (5V)			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

6.9 GPIO Functionality Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of each GPIO pin, followed by the functionality available on that pin. Refer to [6.10 Alternate Functionality Overview](#) for a list of GPIO locations available for each function.

Table 6.9. GPIO Functionality Table

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PA0	BUSDY	TIM0_CC0 #0	US0_TX #0		
		TIM0_CC1 #31	US0_RX #31		
		TIM0_CC2 #30	US0_CLK #30		
		TIM0_CDTI0 #29	US0_CS #29		
		TIM0_CDTI1 #28	US0_CTS #28	FRC_DCLK #0	CMU_CLK1 #0
		TIM0_CDTI2 #27	US0_RTS #27	FRC_DOUT #31	PRS_CH6 #0
		TIM1_CC0 #0	US1_TX #0	FRC_DFRAME #30	PRS_CH7 #10
		TIM1_CC1 #31	US1_RX #31	MODEM_DCLK #0	PRS_CH8 #9
		TIM1_CC2 #30	US1_CLK #30	MODEM_DIN #31	PRS_CH9 #8
		TIM1_CC3 #29	US1_CS #29	MODEM_DOUT #30	ACMP0_O #0
	ADC0_EXTN	WTIM0_CC0 #0	US1_CTS #28	MODEM_ANT0 #29	ACMP1_O #0
		LETIM0_OUT0 #0	US1_RTS #27	MODEM_ANT1 #28	LES_CH8
		LETIM0_OUT1 #31	LEU0_TX #0		
		PCNT0_S0IN #0	LEU0_RX #31		
		PCNT0_S1IN #31	I2C0_SDA #0		
			I2C0_SCL #31		

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PA1	BUSCY BUSDX ADC0_EXTP VDAC0_EXT	TIM0_CC0 #1 TIM0_CC1 #0 TIM0_CC2 #31 TIM0_CDTI0 #30 TIM0_CDTI1 #29 TIM0_CDTI2 #28 TIM1_CC0 #1 TIM1_CC1 #0 TIM1_CC2 #31 TIM1_CC3 #30 WTIM0_CC0 #1 LETIM0_OUT0 #1 LETIM0_OUT1 #0 PCNT0_S0IN #1 PCNT0_S1IN #0	US0_TX #1 US0_RX #0 US0_CLK #31 US0_CS #30 US0_CTS #29 US0_RTS #28 US1_TX #1 US1_RX #0 US1_CLK #31 US1_CS #30 US1_CTS #29 US1_RTS #28 LEU0_TX #1 LEU0_RX #0 I2C0_SDA #1 I2C0_SCL #0	FRC_DCLK #1 FRC_DOUT #0 FRC_DFRAME #31 MODEM_DCLK #1 MODEM_DIN #0 MODEM_DOUT #31 MODEM_ANT0 #30 MODEM_ANT1 #29	CMU_CLK0 #0 PRS_CH6 #1 PRS_CH7 #0 PRS_CH8 #10 PRS_CH9 #9 ACMP0_O #1 ACMP1_O #1 LES_CH9
PA2	VDAC0_OUT1ALT / OPA1_OUTALT #1 BUSDY BUSCX OPA0_P	TIM0_CC0 #2 TIM0_CC1 #1 TIM0_CC2 #0 TIM0_CDTI0 #31 TIM0_CDTI1 #30 TIM0_CDTI2 #29 TIM1_CC0 #2 TIM1_CC1 #1 TIM1_CC2 #0 TIM1_CC3 #31 WTIM0_CC0 #2 WTIM0_CC1 #0 LETIM0_OUT0 #2 LETIM0_OUT1 #1 PCNT0_S0IN #2 PCNT0_S1IN #1	US0_TX #2 US0_RX #1 US0_CLK #0 US0_CS #31 US0_CTS #30 US0_RTS #29 US1_TX #2 US1_RX #1 US1_CLK #0 US1_CS #31 US1_CTS #30 US1_RTS #29 LEU0_TX #2 LEU0_RX #1 I2C0_SDA #2 I2C0_SCL #1	FRC_DCLK #2 FRC_DOUT #1 FRC_DFRAME #0 MODEM_DCLK #2 MODEM_DIN #1 MODEM_DOUT #0 MODEM_ANT0 #31 MODEM_ANT1 #30	PRS_CH6 #2 PRS_CH7 #1 PRS_CH8 #0 PRS_CH9 #10 ACMP0_O #2 ACMP1_O #2 LES_CH10

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PA3	BUSCY BUSDX VDAC0_OUT0 / OPA0_OUT	TIM0_CC0 #3 TIM0_CC1 #2 TIM0_CC2 #1 TIM0_CDTI0 #0 TIM0_CDTI1 #31 TIM0_CDTI2 #30	US0_TX #3 US0_RX #2 US0_CLK #1 US0_CS #0 US0_CTS #31 US0_RTS #30		
		TIM1_CC0 #3 TIM1_CC1 #2 TIM1_CC2 #1 TIM1_CC3 #0	US1_TX #3 US1_RX #2 US1_CLK #1 US1_CS #0	FRC_DCLK #3 FRC_DOUT #2 FRC_DFRAME #1	PRS_CH6 #3 PRS_CH7 #2 PRS_CH8 #1
		WTIM0_CC0 #3 WTIM0_CC1 #1	US1_CTS #31 US1_RTS #30	MODEM_DCLK #3 MODEM_DIN #2 MODEM_DOUT #1	PRS_CH9 #0 ACMP0_O #3 ACMP1_O #3
		LETIM0_OUT0 #3 LETIM0_OUT1 #2	LEU0_TX #3 LEU0_RX #2	MODEM_ANT0 #0 MODEM_ANT1 #31	LES_CH11 GPIO_EM4WU8
		PCNT0_S0IN #3 PCNT0_S1IN #2	I2C0_SDA #3 I2C0_SCL #2		
PA4	VDAC0_OUT1ALT / OPA1_OUTALT #2 BUSDY BUSCX OPA0_N	TIM0_CC0 #4 TIM0_CC1 #3 TIM0_CC2 #2 TIM0_CDTI0 #1 TIM0_CDTI1 #0 TIM0_CDTI2 #31	US0_TX #4 US0_RX #3 US0_CLK #2 US0_CS #1 US0_CTS #0 US0_RTS #31		
		TIM1_CC0 #4 TIM1_CC1 #3	US1_TX #4 US1_RX #3	FRC_DCLK #4 FRC_DOUT #3 FRC_DFRAME #2	PRS_CH6 #4 PRS_CH7 #3 PRS_CH8 #2
		TIM1_CC2 #2	US1_CLK #2	MODEM_DCLK #4	PRS_CH9 #1
		TIM1_CC3 #1	US1_CS #1	MODEM_DIN #3	ACMP0_O #4
		WTIM0_CC0 #4 WTIM0_CC1 #2	US1_CTS #0 US1_RTS #31	MODEM_DOUT #2 MODEM_ANT0 #1	ACMP1_O #4
		WTIM0_CC2 #0	LEU0_TX #4	MODEM_ANT1 #0	LES_CH12
		LETIM0_OUT0 #4 LETIM0_OUT1 #3	LEU0_RX #3		
		PCNT0_S0IN #4	I2C0_SDA #4		
		PCNT0_S1IN #3	I2C0_SCL #3		

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PA7	BUSCY BUSDX	WTIM0_CC0 #7 WTIM0_CC1 #5 WTIM0_CC2 #3 PCNT1_S0IN #1 PCNT1_S1IN #0 PCNT2_S0IN #1 PCNT2_S1IN #0	US2_TX #2 US2_RX #1 US2_CLK #0 US2_CS #31 US2_CTS #30 US2_RTS #29 I2C1_SDA #1 I2C1_SCL #0		LES_CH15 ETM_TD1 #1
PA8	BUSACMP0Y BUSACMP0X	WTIM0_CC0 #8 WTIM0_CC1 #6 WTIM0_CC2 #4 WTIM0_CDTI0 #0 PCNT1_S0IN #2 PCNT1_S1IN #1 PCNT2_S0IN #2 PCNT2_S1IN #1	US2_TX #3 US2_RX #2 US2_CLK #1 US2_CS #0 US2_CTS #31 US2_RTS #30 I2C1_SDA #2 I2C1_SCL #1		LES_ALTEX0 ETM_TD2 #1
PA9	BUSACMP0Y BUSACMP0X	WTIM0_CC0 #9 WTIM0_CC1 #7 WTIM0_CC2 #5 WTIM0_CDTI0 #1 PCNT1_S0IN #3 PCNT1_S1IN #2 PCNT2_S0IN #3 PCNT2_S1IN #2	US2_TX #4 US2_RX #3 US2_CLK #2 US2_CS #1 US2_CTS #0 US2_RTS #31 I2C1_SDA #3 I2C1_SCL #2		LES_ALTEX1 ETM_TD3 #1

GPIO Name	Pin Alternate Functionality / Description					
	Analog	Timers	Communication	Radio	Other	
PB6	BUSDY	WTIM0_CC0 #10 WTIM0_CC1 #8 WTIM0_CC2 #6 WTIM0_CDTI0 #2 WTIM0_CDTI1 #0 PCNT1_S0IN #6 PCNT1_S1IN #5 PCNT2_S0IN #6 PCNT2_S1IN #5	US2_TX #9 US2_RX #8 US2_CLK #7 US2_CS #6 US2_CTS #5 US2_RTS #4		CMU_CLKI0 #3 ETM_TD1 #2	
			US3_TX #10 US3_RX #9 US3_CLK #8 US3_CS #7 US3_CTS #6 US3_RTS #5			
			I2C1_SDA #6 I2C1_SCL #5			
			US2_TX #10 US2_RX #9 US2_CLK #8 US2_CS #7 US2_CTS #6 US2_RTS #5			
			US3_TX #11 US3_RX #10 US3_CLK #9 US3_CS #8 US3_CTS #7 US3_RTS #6			
	BUSCY		I2C1_SDA #7 I2C1_SCL #6		ETM_TD2 #2	
			US2_TX #10 US2_RX #9 US2_CLK #8 US2_CS #7 US2_CTS #6 US2_RTS #5			
			US3_TX #11 US3_RX #10 US3_CLK #9 US3_CS #8 US3_CTS #7 US3_RTS #6			
			I2C1_SDA #7 I2C1_SCL #6			
			US2_TX #10 US2_RX #9 US2_CLK #8 US2_CS #7 US2_CTS #6 US2_RTS #5			

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PB8	BUSDY BUSCX	WTIM0_CC0 #12 WTIM0_CC1 #10 WTIM0_CC2 #8 WTIM0_CDTI0 #4 WTIM0_CDTI1 #2 WTIM0_CDTI2 #0 PCNT1_S0IN #8 PCNT1_S1IN #7 PCNT2_S0IN #8 PCNT2_S1IN #7	US2_TX #11 US2_RX #10 US2_CLK #9 US2_CS #8 US2_CTS #7 US2_RTS #6 US3_TX #12 US3_RX #11 US3_CLK #10 US3_CS #9 US3_CTS #8 US3_RTS #7	ETM_TD3 #2	I2C1_SDA #8 I2C1_SCL #7
			US2_TX #12 US2_RX #11 US2_CLK #10 US2_CS #9 US2_CTS #8 US2_RTS #7		
			WTIM0_CC0 #13 WTIM0_CC1 #11 WTIM0_CC2 #9 WTIM0_CDTI0 #5 WTIM0_CDTI1 #3 WTIM0_CDTI2 #1		
			US3_TX #13 US3_RX #12 US3_CLK #11 US3_CS #10 US3_CTS #9 US3_RTS #8		
			I2C1_SDA #9 I2C1_SCL #8		
PB9	OPA2_OUTALT #0 BUSCY BUSDX	WTIM0_CC0 #13 WTIM0_CC1 #11 WTIM0_CC2 #9 WTIM0_CDTI0 #5 WTIM0_CDTI1 #3 WTIM0_CDTI2 #1 PCNT1_S0IN #9 PCNT1_S1IN #8 PCNT2_S0IN #9 PCNT2_S1IN #8	US2_TX #12 US2_RX #11 US2_CLK #10 US2_CS #9 US2_CTS #8 US2_RTS #7 US3_TX #13 US3_RX #12 US3_CLK #11 US3_CS #10 US3_CTS #9 US3_RTS #8	I2C1_SDA #9 I2C1_SCL #8	
			WTIM0_CC0 #13 WTIM0_CC1 #11 WTIM0_CC2 #9 WTIM0_CDTI0 #5 WTIM0_CDTI1 #3 WTIM0_CDTI2 #1		
			US3_TX #13 US3_RX #12 US3_CLK #11 US3_CS #10 US3_CTS #9 US3_RTS #8		
			I2C1_SDA #9 I2C1_SCL #8		

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PB10	OPA2_OUTALT #1 BUSDY BUSCX	WTIM0_CC0 #14 WTIM0_CC1 #12 WTIM0_CC2 #10 WTIM0_CDTI0 #6 WTIM0_CDTI1 #4 WTIM0_CDTI2 #2 PCNT1_S0IN #10 PCNT1_S1IN #9 PCNT2_S0IN #10 PCNT2_S1IN #9	US2_TX #13 US2_RX #12 US2_CLK #11 US2_CS #10 US2_CTS #9 US2_RTS #8 US3_TX #14 US3_RX #13 US3_CLK #12 US3_CS #11 US3_CTS #10 US3_RTS #9 I2C1_SDA #10 I2C1_SCL #9		

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PB11	BUSCY BUSDX OPA2_P		US0_TX #6		
		TIM0_CC0 #6	US0_RX #5		
		TIM0_CC1 #5	US0_CLK #4		
		TIM0_CC2 #4	US0_CS #3		
		TIM0_CDTI0 #3	US0_CTS #2		
		TIM0_CDTI1 #2	US0_RTS #1		
		TIM0_CDTI2 #1	US1_TX #6		
		TIM1_CC0 #6	US1_RX #5	FRC_DCLK #6	
		TIM1_CC1 #5	US1_CLK #4	FRC_DOUT #5	PRS_CH6 #6
		TIM1_CC2 #4	US1_CS #3	FRC_DFRAME #4	PRS_CH7 #5
		TIM1_CC3 #3	US1_CTS #2	MODEM_DCLK #6	PRS_CH8 #4
		WTIM0_CC0 #15	US1_RTS #1	MODEM_DIN #5	PRS_CH9 #3
		WTIM0_CC1 #13	US3_TX #15	MODEM_DOUT #4	ACMP0_O #6
		WTIM0_CC2 #11	US3_RX #14	MODEM_ANT0 #3	ACMP1_O #6
		WTIM0_CDTI0 #7	US3_CLK #13	MODEM_ANT1 #2	
		WTIM0_CDTI1 #5	US3_CS #12		
		WTIM0_CDTI2 #3	US3_CTS #11		
		LETIM0_OUT0 #6	US3_RTS #10		
		LETIM0_OUT1 #5	LEU0_TX #6		
		PCNT0_S0IN #6	LEU0_RX #5		
		PCNT0_S1IN #5	I2C0_SDA #6		
			I2C0_SCL #5		

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PB12	BUSDY	TIM0_CC0 #7			
		TIM0_CC1 #6			
		TIM0_CC2 #5	US0_TX #7		
		TIM0_CDTI0 #4	US0_RX #6		
		TIM0_CDTI1 #3	US0_CLK #5		
		TIM0_CDTI2 #2	US0_CS #4		
		TIM1_CC0 #7	US0_CTS #3	FRC_DCLK #7	
		TIM1_CC1 #6	US0_RTS #2	FRC_DOUT #6	PRS_CH6 #7
		TIM1_CC2 #5	US1_TX #7	FRC_DFRAME #5	PRS_CH7 #6
		TIM1_CC3 #4	US1_RX #6	MODEM_DCLK #7	PRS_CH8 #5
	BUSCX	WTIM0_CC0 #16	US1_CLK #5	MODEM_DIN #6	PRS_CH9 #4
		WTIM0_CC1 #14	US1_CS #4	MODEM_DOUT #5	ACMP0_O #7
		WTIM0_CC2 #12	US1_CTS #3	MODEM_ANT0 #4	ACMP1_O #7
		WTIM0_CDTI0 #8	US1_RTS #2	MODEM_ANT1 #3	
		WTIM0_CDTI1 #6	LEU0_TX #7		
	OPA2_OUT	WTIM0_CDTI2 #4	LEU0_RX #6		
		WTIM1_CC0 #0	I2C0_SDA #7		
		LETIM0_OUT0 #7	I2C0_SCL #6		
		LETIM0_OUT1 #6			
		PCNT0_S0IN #7			
		PCNT0_S1IN #6			

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PB13	BUSCY BUSDX OPA2_N	TIM0_CC0 #8 TIM0_CC1 #7 TIM0_CC2 #6 TIM0_CDTI0 #5 TIM0_CDTI1 #4 TIM0_CDTI2 #3 TIM1_CC0 #8 TIM1_CC1 #7 TIM1_CC2 #6 TIM1_CC3 #5 WTIM0_CC0 #17 WTIM0_CC1 #15 WTIM0_CC2 #13 WTIM0_CDTI0 #9 WTIM0_CDTI1 #7 WTIM0_CDTI2 #5 WTIM1_CC0 #1 LETIM0_OUT0 #8 LETIM0_OUT1 #7 PCNT0_S0IN #8 PCNT0_S1IN #7	US0_TX #8 US0_RX #7 US0_CLK #6 US0_CS #5 US0_CTS #4 US0_RTS #3 US1_TX #8 US1_RX #7 US1_CLK #6 US1_CS #5 US1_CTS #4 US1_RTS #3 LEU0_TX #8 LEU0_RX #7 I2C0_SDA #8 I2C0_SCL #7	FRC_DCLK #8 FRC_DOUT #7 FRC_DFRAME #6 MODEM_DCLK #8 MODEM_DIN #7 MODEM_DOUT #6 MODEM_ANT0 #5 MODEM_ANT1 #4	CMU_CLKI0 #0 PRS_CH6 #8 PRS_CH7 #7 PRS_CH8 #6 PRS_CH9 #5 ACMP0_O #8 ACMP1_O #8 DBG_SW0 #1 GPIO_EM4WU9

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PB14	BUSDY BUSCX LFXTAL_N	TIM0_CC0 #9 TIM0_CC1 #8 TIM0_CC2 #7 TIM0_CDTI0 #6 TIM0_CDTI1 #5 TIM0_CDTI2 #4 TIM1_CC0 #9 TIM1_CC1 #8 TIM1_CC2 #7 TIM1_CC3 #6 WTIM0_CC0 #18 WTIM0_CC1 #16 WTIM0_CC2 #14 WTIM0_CDTI0 #10 WTIM0_CDTI1 #8 WTIM0_CDTI2 #6 WTIM1_CC0 #2 WTIM1_CC1 #0 LETIM0_OUT0 #9 LETIM0_OUT1 #8 PCNT0_S0IN #9 PCNT0_S1IN #8	US0_TX #9 US0_RX #8 US0_CLK #7 US0_CS #6 US0_CTS #5 US0_RTS #4 US1_TX #9 US1_RX #8 US1_CLK #7 US1_CS #6 US1_CTS #5 US1_RTS #4 LEU0_TX #9 LEU0_RX #8 I2C0_SDA #9 I2C0_SCL #8	FRC_DCLK #9 FRC_DOUT #8 FRC_DFRAME #7 MODEM_DCLK #9 MODEM_DIN #8 MODEM_DOUT #7 MODEM_ANT0 #6 MODEM_ANT1 #5	CMU_CLK1 #1 PRS_CH6 #9 PRS_CH7 #8 PRS_CH8 #7 PRS_CH9 #6 ACMP0_O #9 ACMP1_O #9

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PB15	BUSCY BUSDX LFXTAL_P	TIM0_CC0 #10 TIM0_CC1 #9 TIM0_CC2 #8 TIM0_CDTI0 #7 TIM0_CDTI1 #6 TIM0_CDTI2 #5 TIM1_CC0 #10 TIM1_CC1 #9 TIM1_CC2 #8 TIM1_CC3 #7 WTIM0_CC0 #19 WTIM0_CC1 #17 WTIM0_CC2 #15 WTIM0_CDTI0 #11 WTIM0_CDTI1 #9 WTIM0_CDTI2 #7 WTIM1_CC0 #3 WTIM1_CC1 #1 LETIM0_OUT0 #10 LETIM0_OUT1 #9 PCNT0_S0IN #10 PCNT0_S1IN #9	US0_TX #10 US0_RX #9 US0_CLK #8 US0_CS #7 US0_CTS #6 US0_RTS #5 US1_TX #10 US1_RX #9 US1_CLK #8 US1_CS #7 US1_CTS #6 US1_RTS #5 LEU0_TX #10 LEU0_RX #9 I2C0_SDA #10 I2C0_SCL #9	FRC_DCLK #10 FRC_DOUT #9 FRC_DFRAME #8 MODEM_DCLK #10 MODEM_DIN #9 MODEM_DOUT #8 MODEM_ANTO #7 MODEM_ANT1 #6	CMU_CLK0 #1 PRS_CH6 #10 PRS_CH7 #9 PRS_CH8 #8 PRS_CH9 #7 ACMP0_O #10 ACMP1_O #10
		WTIM0_CC0 #20			
		WTIM0_CC1 #18			
		WTIM0_CC2 #16			
		WTIM0_CDTI0 #12	US3_TX #18		
		WTIM0_CDTI1 #10	US3_RX #17		
		WTIM0_CDTI2 #8	US3_CLK #16		
	BUSBY BUSAX	WTIM1_CC0 #4	US3_CS #15		
		WTIM1_CC1 #2	US3_CTS #14		
		WTIM1_CC2 #0	US3_RTS #13		
		PCNT1_S0IN #13	I2C1_SDA #13		
		PCNT1_S1IN #12	I2C1_SCL #12		
		PCNT2_S0IN #13			
		PCNT2_S1IN #12			

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PC1	BUSAY BUSBX	WTIM0_CC0 #21			
		WTIM0_CC1 #19			
		WTIM0_CC2 #17	US3_TX #19		
		WTIM0_CDTI0 #13	US3_RX #18		
		WTIM0_CDTI1 #11	US3_CLK #17		
		WTIM0_CDTI2 #9	US3_CS #16		
		WTIM1_CC0 #5	US3_CTS #15		
		WTIM1_CC1 #3	US3_RTS #14		
		WTIM1_CC2 #1	I2C1_SDA #14		
		PCNT1_S0IN #14	I2C1_SCL #13		
		PCNT1_S1IN #13			
		PCNT2_S0IN #14			
		PCNT2_S1IN #13			
PC2	BUSBY BUSAX	WTIM0_CC0 #22			
		WTIM0_CC1 #20			
		WTIM0_CC2 #18			
		WTIM0_CDTI0 #14	US3_TX #20		
		WTIM0_CDTI1 #12	US3_RX #19		
		WTIM0_CDTI2 #10	US3_CLK #18		
		WTIM1_CC0 #6	US3_CS #17		
		WTIM1_CC1 #4	US3_CTS #16		
		WTIM1_CC2 #2	US3_RTS #15		
		WTIM1_CC3 #0	I2C1_SDA #15		
		PCNT1_S0IN #15	I2C1_SCL #14		
		PCNT1_S1IN #14			
		PCNT2_S0IN #15			
		PCNT2_S1IN #14			

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PC3	BUSAY BUSBX	WTIM0_CC0 #23 WTIM0_CC1 #21 WTIM0_CC2 #19 WTIM0_CDTI0 #15 WTIM0_CDTI1 #13 WTIM0_CDTI2 #11	US3_TX #21 US3_RX #20 US3_CLK #19 US3_CS #18 US3_CTS #17 US3_RTS #16 I2C1_SDA #16 I2C1_SCL #15		
		WTIM1_CC0 #7 WTIM1_CC1 #5 WTIM1_CC2 #3 WTIM1_CC3 #1			
		PCNT1_S0IN #16 PCNT1_S1IN #15 PCNT2_S0IN #16 PCNT2_S1IN #15			
		WTIM0_CC0 #24 WTIM0_CC1 #22 WTIM0_CC2 #20 WTIM0_CDTI0 #16 WTIM0_CDTI1 #14 WTIM0_CDTI2 #12		US3_TX #22 US3_RX #21 US3_CLK #20 US3_CS #19 US3_CTS #18 US3_RTS #17 I2C1_SDA #17 I2C1_SCL #16	
		WTIM1_CC0 #8 WTIM1_CC1 #6 WTIM1_CC2 #4 WTIM1_CC3 #2			
		PCNT1_S0IN #17 PCNT1_S1IN #16 PCNT2_S0IN #17 PCNT2_S1IN #16			

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PC5	BUSAY	WTIM0_CC0 #25			
		WTIM0_CC1 #23			
		WTIM0_CC2 #21			
		WTIM0_CDTI0 #17	US3_TX #23		
		WTIM0_CDTI1 #15	US3_RX #22		
	BUSBX	WTIM0_CDTI2 #13	US3_CLK #21		
		WTIM1_CC0 #9	US3_CS #20		
		WTIM1_CC1 #7	US3_CTS #19		
		WTIM1_CC2 #5	US3_RTS #18		
		WTIM1_CC3 #3	I2C1_SDA #18		
		PCNT1_S0IN #18	I2C1_SCL #17		
		PCNT1_S1IN #17			
		PCNT2_S0IN #18			
		PCNT2_S1IN #17			

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PC6	BUSBY	TIM0_CC0 #11			
		TIM0_CC1 #10			
		TIM0_CC2 #9			
		TIM0_CDTI0 #8			
		TIM0_CDTI1 #7	US0_TX #11		
		TIM0_CDTI2 #6	US0_RX #10		
		TIM1_CC0 #11	US0_CLK #9		
		TIM1_CC1 #10	US0_CS #8		
		TIM1_CC2 #9	US0_CTS #7	FRC_DCLK #11	CMU_CLK0 #2
		TIM1_CC3 #8	US0_RTS #6	FRC_DOUT #10	CMU_CLKI0 #2
		WTIM0_CC0 #26	US1_TX #11	FRC_DFRAME #9	PRS_CH0 #8
		WTIM0_CC1 #24	US1_RX #10	MODEM_DCLK #11	PRS_CH9 #11
		WTIM0_CC2 #22	US1_CLK #9	MODEM_DIN #10	PRS_CH10 #0
		WTIM0_CDTI0 #18	US1_CS #8	MODEM_DOUT #9	PRS_CH11 #5
		WTIM0_CDTI1 #16	US1_CTS #7	MODEM_ANT0 #8	ACMP0_O #11
		WTIM0_CDTI2 #14	US1_RTS #6	MODEM_ANT1 #7	ACMP1_O #11
		WTIM1_CC0 #10	LEU0_TX #11		ETM_TCLK #3
		WTIM1_CC1 #8	LEU0_RX #10		
		WTIM1_CC2 #6	I2C0_SDA #11		
		WTIM1_CC3 #4	I2C0_SCL #10		
		LETIM0_OUT0 #11			
		LETIM0_OUT1 #10			
		PCNT0_S0IN #11			
		PCNT0_S1IN #10			

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PC7	BUSAY	TIM0_CC0 #12			
		TIM0_CC1 #11			
		TIM0_CC2 #10			
		TIM0_CDTI0 #9			
		TIM0_CDTI1 #8	US0_TX #12		
		TIM0_CDTI2 #7	US0_RX #11		
		TIM1_CC0 #12	US0_CLK #10		
		TIM1_CC1 #11	US0_CS #9		
		TIM1_CC2 #10	US0_CTS #8	FRC_DCLK #12	CMU_CLK1 #2
		TIM1_CC3 #9	US0_RTS #7	FRC_DOUT #11	PRS_CH0 #9
	BUSBX	WTIM0_CC0 #27	US1_TX #12	FRC_DFRAME #10	PRS_CH9 #12
		WTIM0_CC1 #25	US1_RX #11	MODEM_DCLK #12	PRS_CH10 #1
		WTIM0_CC2 #23	US1_CLK #10	MODEM_DIN #11	PRS_CH11 #0
		WTIM0_CDTI0 #19	US1_CS #9	MODEM_DOUT #10	ACMP0_O #12
		WTIM0_CDTI1 #17	US1_CTS #8	MODEM_ANT0 #9	ACMP1_O #12
		WTIM0_CDTI2 #15	US1_RTS #7	MODEM_ANT1 #8	ETM_TD0 #3
		WTIM1_CC0 #11	LEU0_TX #12		
		WTIM1_CC1 #9	LEU0_RX #11		
		WTIM1_CC2 #7	I2C0_SDA #12		
		WTIM1_CC3 #5	I2C0_SCL #11		
		LETIM0_OUT0 #12			
		LETIM0_OUT1 #11			
		PCNT0_S0IN #12			
		PCNT0_S1IN #11			

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PC8	BUSBY	TIM0_CC0 #13			
		TIM0_CC1 #12			
		TIM0_CC2 #11			
		TIM0_CDTI0 #10			
		TIM0_CDTI1 #9	US0_TX #13		
		TIM0_CDTI2 #8	US0_RX #12		
		TIM1_CC0 #13	US0_CLK #11		
		TIM1_CC1 #12	US0_CS #10		
		TIM1_CC2 #11	US0_CTS #9	FRC_DCLK #13	PRS_CH0 #10
		TIM1_CC3 #10	US0_RTS #8	FRC_DOUT #12	PRS_CH9 #13
	BUSAX	WTIM0_CC0 #28	US1_TX #13	FRC_DFRAME #11	PRS_CH10 #2
		WTIM0_CC1 #26	US1_RX #12	MODEM_DCLK #13	PRS_CH11 #1
		WTIM0_CC2 #24	US1_CLK #11	MODEM_DIN #12	ACMP0_O #13
		WTIM0_CDTI0 #20	US1_CS #10	MODEM_DOUT #11	ACMP1_O #13
		WTIM0_CDTI1 #18	US1_CTS #9	MODEM_ANT0 #10	ETM_TD1 #3
		WTIM0_CDTI2 #16	US1_RTS #8	MODEM_ANT1 #9	
		WTIM1_CC0 #12	LEU0_TX #13		
		WTIM1_CC1 #10	LEU0_RX #12		
		WTIM1_CC2 #8	I2C0_SDA #13		
		WTIM1_CC3 #6	I2C0_SCL #12		
		LETIM0_OUT0 #13			
		LETIM0_OUT1 #12			
		PCNT0_S0IN #13			
		PCNT0_S1IN #12			

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PC9	BUSAY	TIM0_CC0 #14			
		TIM0_CC1 #13			
		TIM0_CC2 #12			
		TIM0_CDTI0 #11			
		TIM0_CDTI1 #10	US0_TX #14		
		TIM0_CDTI2 #9	US0_RX #13		
		TIM1_CC0 #14	US0_CLK #12		
		TIM1_CC1 #13	US0_CS #11		
		TIM1_CC2 #12	US0_CTS #10	FRC_DCLK #14	PRS_CH0 #11
		TIM1_CC3 #11	US0_RTS #9	FRC_DOUT #13	PRS_CH9 #14
	BUSBX	WTIM0_CC0 #29	US1_TX #14	FRC_DFRAME #12	PRS_CH10 #3
		WTIM0_CC1 #27	US1_RX #13	MODEM_DCLK #14	PRS_CH11 #2
		WTIM0_CC2 #25	US1_CLK #12	MODEM_DIN #13	ACMP0_O #14
		WTIM0_CDTI0 #21	US1_CS #11	MODEM_DOUT #12	ACMP1_O #14
		WTIM0_CDTI1 #19	US1_CTS #10	MODEM_ANT0 #11	ETM_TD2 #3
		WTIM0_CDTI2 #17	US1_RTS #9	MODEM_ANT1 #10	
		WTIM1_CC0 #13	LEU0_TX #14		
		WTIM1_CC1 #11	LEU0_RX #13		
		WTIM1_CC2 #9	I2C0_SDA #14		
		WTIM1_CC3 #7	I2C0_SCL #13		
		LETIM0_OUT0 #14			
		LETIM0_OUT1 #13			
		PCNT0_S0IN #14			
		PCNT0_S1IN #13			

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PC10	BUSY	TIM0_CC0 #15			
		TIM0_CC1 #14			
		TIM0_CC2 #13			
		TIM0_CDTI0 #12			
		TIM0_CDTI1 #11	US0_TX #15		
		TIM0_CDTI2 #10	US0_RX #14		
		TIM1_CC0 #15	US0_CLK #13		
		TIM1_CC1 #14	US0_CS #12		
		TIM1_CC2 #13	US0_CTS #11		
		TIM1_CC3 #12	US0_RTS #10	FRC_DCLK #15	CMU_CLK1 #3
	BUSAX	WTIM0_CC0 #30	US1_TX #15	FRC_DOUT #14	PRS_CH0 #12
		WTIM0_CC1 #28	US1_RX #14	FRC_DFRAME #13	PRS_CH9 #15
		WTIM0_CC2 #26	US1_CLK #13	MODEM_DCLK #15	PRS_CH10 #4
		WTIM0_CDTI0 #22	US1_CS #12	MODEM_DIN #14	PRS_CH11 #3
		WTIM0_CDTI1 #20	US1_CTS #11	MODEM_DOUT #13	ACMP0_O #15
		WTIM0_CDTI2 #18	US1_RTS #10	MODEM_ANT0 #12	ACMP1_O #15
		WTIM1_CC0 #14	LEU0_TX #15	MODEM_ANT1 #11	ETM_TD3 #3
		WTIM1_CC1 #12	LEU0_RX #14		GPIO_EM4WU12
		WTIM1_CC2 #10	I2C0_SDA #15		
		WTIM1_CC3 #8	I2C0_SCL #14		
	PCNT0	LETIM0_OUT0 #15	I2C1_SDA #19		
		LETIM0_OUT1 #14	I2C1_SCL #18		
		PCNT0_S0IN #15			
		PCNT0_S1IN #14			
		PCNT2_S0IN #19			
	PCNT2	PCNT2_S1IN #18			

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PC11		TIM0_CC0 #16			
		TIM0_CC1 #15			
		TIM0_CC2 #14			
		TIM0_CDTI0 #13			
		TIM0_CDTI1 #12	US0_TX #16		
		TIM0_CDTI2 #11	US0_RX #15		
		TIM1_CC0 #16	US0_CLK #14		
		TIM1_CC1 #15	US0_CS #13		
		TIM1_CC2 #14	US0_CTS #12		
		TIM1_CC3 #13	US0_RTS #11	FRC_DCLK #16	CMU_CLK0 #3
		WTIM0_CC0 #31	US1_TX #16	FRC_DOUT #15	PRS_CH0 #13
		WTIM0_CC1 #29	US1_RX #15	FRC_DFRAME #14	PRS_CH9 #16
		BUSAY	WTIM0_CC2 #27	MODEM_DCLK #16	PRS_CH10 #5
		BUSBX	WTIM0_CDTI0 #23	MODEM_DIN #15	PRS_CH11 #4
		WTIM0_CDTI1 #21	US1_CS #13	MODEM_DOUT #14	ACMP0_O #16
		WTIM0_CDTI2 #19	US1_CTS #12	MODEM_ANT0 #13	ACMP1_O #16
		WTIM1_CC0 #15	US1_RTS #11	MODEM_ANT1 #12	DBG_SWO #3
		WTIM1_CC1 #13	LEU0_TX #16		
		WTIM1_CC2 #11	LEU0_RX #15		
		WTIM1_CC3 #9	I2C0_SDA #16		
PD8		LETIM0_OUT0 #16	I2C0_SCL #15		
		LETIM0_OUT1 #15	I2C1_SDA #20		
		PCNT0_S0IN #16	I2C1_SCL #19		
		PCNT0_S1IN #15			
		PCNT2_S0IN #20			
		PCNT2_S1IN #19			
		WTIM0_CC1 #30			
		WTIM0_CC2 #28	US3_TX #0		
		WTIM0_CDTI0 #24	US3_RX #31		
		WTIM0_CDTI1 #22	US3_CLK #30		
PD8		WTIM0_CDTI2 #20	US3_CS #29		
		WTIM1_CC0 #16	US3_CTS #28		
		WTIM1_CC1 #14	US3_RTS #27		
		WTIM1_CC2 #12			
		WTIM1_CC3 #10			
					LES_CH0

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PD9	BUSCY	TIM0_CC0 #17	US0_TX #17		
		TIM0_CC1 #16	US0_RX #16		
		TIM0_CC2 #15	US0_CLK #15		
		TIM0_CDTI0 #14	US0_CS #14		
		TIM0_CDTI1 #13	US0_CTS #13		
		TIM0_CDTI2 #12	US0_RTS #12		
		TIM1_CC0 #17	US1_TX #17		
		TIM1_CC1 #16	US1_RX #16	FRC_DCLK #17	CMU_CLK0 #4
		TIM1_CC2 #15	US1_CLK #15	FRC_DOUT #16	PRS_CH3 #8
		TIM1_CC3 #14	US1_CS #14	FRC_DFRAME #15	PRS_CH4 #0
	BUSDX	WTIM0_CC1 #31	US1_CTS #13	MODEM_DCLK #17	PRS_CH5 #6
		WTIM0_CC2 #29	US1_RTS #12	MODEM_DIN #16	PRS_CH6 #11
		WTIM0_CDTI0 #25	US3_TX #1	MODEM_DOUT #15	ACMP0_O #17
		WTIM0_CDTI1 #23	US3_RX #0	MODEM_ANT0 #14	ACMP1_O #17
		WTIM0_CDTI2 #21	US3_CLK #31	MODEM_ANT1 #13	LES_CH1
		WTIM1_CC0 #17	US3_CS #30		
		WTIM1_CC1 #15	US3_CTS #29		
		WTIM1_CC2 #13	US3_RTS #28		
		WTIM1_CC3 #11	LEU0_TX #17		
		LETIM0_OUT0 #17	LEU0_RX #16		
		LETIM0_OUT1 #16	I2C0_SDA #17		
		PCNT0_S0IN #17	I2C0_SCL #16		
		PCNT0_S1IN #16			

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PD10		TIM0_CC0 #18	US0_TX #18		
		TIM0_CC1 #17	US0_RX #17		
		TIM0_CC2 #16	US0_CLK #16		
		TIM0_CDTI0 #15	US0_CS #15		
		TIM0_CDTI1 #14	US0_CTS #14		
		TIM0_CDTI2 #13	US0_RTS #13		
		TIM1_CC0 #18	US1_TX #18		
		TIM1_CC1 #17	US1_RX #17	FRC_DCLK #18	CMU_CLK1 #4
		TIM1_CC2 #16	US1_CLK #16	FRC_DOUT #17	PRS_CH3 #9
		TIM1_CC3 #15	US1_CS #15	FRC_DFRAME #16	PRS_CH4 #1
	BUSDY	WTIM0_CC2 #30	US1_CTS #14	MODEM_DCLK #18	PRS_CH5 #0
		WTIM0_CDTI0 #26	US1_RTS #13	MODEM_DIN #17	PRS_CH6 #12
		WTIM0_CDTI1 #24	US3_TX #2	MODEM_DOUT #16	ACMP0_O #18
		WTIM0_CDTI2 #22	US3_RX #1	MODEM_ANTO #15	ACMP1_O #18
		WTIM1_CC0 #18	US3_CLK #0	MODEM_ANT1 #14	LES_CH2
		WTIM1_CC1 #16	US3_CS #31		
		WTIM1_CC2 #14	US3_CTS #30		
		WTIM1_CC3 #12	US3_RTS #29		
		LETIM0_OUT0 #18	LEU0_TX #18		
		LETIM0_OUT1 #17	LEU0_RX #17		
		PCNT0_S0IN #18	I2C0_SDA #18		
		PCNT0_S1IN #17	I2C0_SCL #17		

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PD11		TIM0_CC0 #19	US0_TX #19		
		TIM0_CC1 #18	US0_RX #18		
		TIM0_CC2 #17	US0_CLK #17		
		TIM0_CDTI0 #16	US0_CS #16		
		TIM0_CDTI1 #15	US0_CTS #15		
		TIM0_CDTI2 #14	US0_RTS #14		
		TIM1_CC0 #19	US1_TX #19		
		TIM1_CC1 #18	US1_RX #18	FRC_DCLK #19	PRS_CH3 #10
		TIM1_CC2 #17	US1_CLK #17	FRC_DOUT #18	PRS_CH4 #2
		TIM1_CC3 #16	US1_CS #16	FRC_DFRAME #17	PRS_CH5 #1
	BUSCY	WTIM0_CC2 #31	US1_CTS #15	MODEM_DCLK #19	PRS_CH6 #13
		WTIM0_CDTI0 #27	US1_RTS #14	MODEM_DIN #18	ACMP0_O #19
		WTIM0_CDTI1 #25	US3_TX #3	MODEM_DOUT #17	ACMP1_O #19
		WTIM0_CDTI2 #23	US3_RX #2	MODEM_ANT0 #16	LES_CH3
		WTIM1_CC0 #19	US3_CLK #1	MODEM_ANT1 #15	
		WTIM1_CC1 #17	US3_CS #0		
		WTIM1_CC2 #15	US3_CTS #31		
		WTIM1_CC3 #13	US3_RTS #30		
		LETIM0_OUT0 #19	LEU0_TX #19		
		LETIM0_OUT1 #18	LEU0_RX #18		
		PCNT0_S0IN #19	I2C0_SDA #19		
		PCNT0_S1IN #18	I2C0_SCL #18		

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PD12	VDAC0_OUT1ALT / OPA1_OUTALT #0 BUSDY BUSCX	TIM0_CC0 #20 TIM0_CC1 #19 TIM0_CC2 #18 TIM0_CDTI0 #17 TIM0_CDTI1 #16 TIM0_CDTI2 #15 TIM1_CC0 #20 TIM1_CC1 #19 TIM1_CC2 #18 TIM1_CC3 #17 WTIM0_CDTI0 #28 WTIM0_CDTI1 #26 WTIM0_CDTI2 #24 WTIM1_CC0 #20 WTIM1_CC1 #18 WTIM1_CC2 #16 WTIM1_CC3 #14 LETIM0_OUT0 #20 LETIM0_OUT1 #19 PCNT0_S0IN #20 PCNT0_S1IN #19	US0_TX #20 US0_RX #19 US0_CLK #18 US0_CS #17 US0_CTS #16 US0_RTS #15 US1_TX #20 US1_RX #19 US1_CLK #18 US1_CS #17 US1_CTS #16 US3_TX #4 US3_RX #3 US3_CLK #2 US3_CS #1 US3_CTS #0 US3_RTS #31 LEU0_TX #20 LEU0_RX #19 I2C0_SDA #20 I2C0_SCL #19	FRC_DCLK #20 FRC_DOUT #19 FRC_DFRAME #18 MODEM_DCLK #20 MODEM_DIN #19 MODEM_DOUT #18 MODEM_ANTO #17 MODEM_ANT1 #16	PRS_CH3 #11 PRS_CH4 #3 PRS_CH5 #2 PRS_CH6 #14 ACMP0_O #20 ACMP1_O #20 LES_CH4

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PD13	VDAC0_OUT0ALT / OPA0_OUTALT #1	TIM0_CC0 #21	US0_TX #21		
		TIM0_CC1 #20	US0_RX #20		
		TIM0_CC2 #19	US0_CLK #19		
		TIM0_CDTI0 #18	US0_CS #18		
		TIM0_CDTI1 #17	US0_CTS #17		
		TIM0_CDTI2 #16	US0_RTS #16		
		TIM1_CC0 #21	US1_TX #21		
		TIM1_CC1 #20	US1_RX #20	FRC_DCLK #21	PRS_CH3 #12
		TIM1_CC2 #19	US1_CLK #19	FRC_DOUT #20	PRS_CH4 #4
		TIM1_CC3 #18	US1_CS #18	FRC_DFRAME #19	PRS_CH5 #3
	BUSCY	WTIM0_CDTI0 #29	US1_CTS #17	MODEM_DCLK #21	PRS_CH6 #15
		WTIM0_CDTI1 #27	US1_RTS #16	MODEM_DIN #20	ACMP0_O #21
	OPA1_P	WTIM0_CDTI2 #25	US3_TX #5	MODEM_DOUT #19	ACMP1_O #21
		WTIM1_CC0 #21	US3_RX #4	MODEM_ANTO #18	LES_CH5
		WTIM1_CC1 #19	US3_CLK #3	MODEM_ANT1 #17	
		WTIM1_CC2 #17	US3_CS #2		
		WTIM1_CC3 #15	US3_CTS #1		
		LETIM0_OUT0 #21	US3_RTS #0		
		LETIM0_OUT1 #20	LEU0_TX #21		
		PCNT0_S0IN #21	LEU0_RX #20		
		PCNT0_S1IN #20	I2C0_SDA #21		
			I2C0_SCL #20		

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PD14	BUSDY BUSCX VDAC0_OUT1 / OPA1_OUT	TIM0_CC0 #22 TIM0_CC1 #21 TIM0_CC2 #20 TIM0_CDTI0 #19 TIM0_CDTI1 #18 TIM0_CDTI2 #17 TIM1_CC0 #22 TIM1_CC1 #21 TIM1_CC2 #20 TIM1_CC3 #19	US0_TX #22 US0_RX #21 US0_CLK #20 US0_CS #19 US0_CTS #18 US0_RTS #17 US1_TX #22 US1_RX #21 US1_CLK #20 US1_CS #19	FRC_DCLK #22 FRC_DOUT #21 FRC_DFRAME #20 MODEM_DCLK #22 MODEM_DIN #21 MODEM_DOUT #20 MODEM_ANT0 #19 MODEM_ANT1 #18	CMU_CLK0 #5 PRS_CH3 #13 PRS_CH4 #5 PRS_CH5 #4 PRS_CH6 #16 ACMP0_O #22 ACMP1_O #22 LES_CH6 GPIO_EM4WU4
		WTIM0_CDTI0 #30 WTIM0_CDTI1 #28 WTIM0_CDTI2 #26 WTIM1_CC0 #22 WTIM1_CC1 #20 WTIM1_CC2 #18 WTIM1_CC3 #16 LETIM0_OUT0 #22 LETIM0_OUT1 #21 PCNT0_S0IN #22 PCNT0_S1IN #21	US1_CTS #18 US1_RTS #17 US3_TX #6 US3_RX #5 US3_CLK #4 US3_CS #3 US3_CTS #2 US3_RTS #1 LEU0_TX #22 LEU0_RX #21 I2C0_SDA #22 I2C0_SCL #21		

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PD15	VDAC0_OUT0ALT / OPA0_OUTALT #2	TIM0_CC0 #23	US0_TX #23		
		TIM0_CC1 #22	US0_RX #22		
		TIM0_CC2 #21	US0_CLK #21		
		TIM0_CDTI0 #20	US0_CS #20		
		TIM0_CDTI1 #19	US0_CTS #19		
		TIM0_CDTI2 #18	US0_RTS #18		
		TIM1_CC0 #23	US1_TX #23		CMU_CLK1 #5
		TIM1_CC1 #22	US1_RX #22	FRC_DCLK #23	PRS_CH3 #14
		TIM1_CC2 #21	US1_CLK #21	FRC_DOUT #22	PRS_CH4 #6
		TIM1_CC3 #20	US1_CS #20	FRC_DFRAME #21	PRS_CH5 #5
	BUSCY	WTIM0_CDTI0 #31	US1_CTS #19	MODEM_DCLK #23	PRS_CH6 #17
		WTIM0_CDTI1 #29	US1_RTS #18	MODEM_DIN #22	ACMP0_O #23
	OPA1_N	WTIM0_CDTI2 #27	US3_TX #7	MODEM_DOUT #21	ACMP1_O #23
		WTIM1_CC0 #23	US3_RX #6	MODEM_ANTO #20	LES_CH7
		WTIM1_CC1 #21	US3_CLK #5	MODEM_ANT1 #19	DBG_SWO #2
		WTIM1_CC2 #19	US3_CS #4		
		WTIM1_CC3 #17	US3_CTS #3		
		LETIM0_OUT0 #23	US3_RTS #2		
		LETIM0_OUT1 #22	LEU0_TX #23		
		PCNT0_S0IN #23	LEU0_RX #22		
		PCNT0_S1IN #22	I2C0_SDA #23		
			I2C0_SCL #22		

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PF0	BUSBY BUSAX	TIM0_CC0 #24 TIM0_CC1 #23 TIM0_CC2 #22 TIM0_CDTI0 #21 TIM0_CDTI1 #20 TIM0_CDTI2 #19 TIM1_CC0 #24 TIM1_CC1 #23 TIM1_CC2 #22 TIM1_CC3 #21 WTIM0_CDTI1 #30 WTIM0_CDTI2 #28 WTIM1_CC0 #24 WTIM1_CC1 #22 WTIM1_CC2 #20 WTIM1_CC3 #18 LETIM0_OUT0 #24 LETIM0_OUT1 #23 PCNT0_S0IN #24 PCNT0_S1IN #23	US0_TX #24 US0_RX #23 US0_CLK #22 US0_CS #21 US0_CTS #20 US0_RTS #19 US1_TX #24 US1_RX #23 US1_CLK #22 US1_CS #21 US1_CTS #20 US1_RTS #19 US2_TX #14 US2_RX #13 US2_CLK #12 US2_CS #11 US2_CTS #10 US2_RTS #9 LEU0_TX #24 LEU0_RX #23 I2C0_SDA #24 I2C0_SCL #23	FRC_DCLK #24 FRC_DOUT #23 FRC_DFRAME #22 MODEM_DCLK #24 MODEM_DIN #23 MODEM_DOUT #22 MODEM_ANT0 #21 MODEM_ANT1 #20 DBG_SWCLKTCK BOOT_TX	PRS_CH0 #0 PRS_CH1 #7 PRS_CH2 #6 PRS_CH3 #5 ACMP0_O #24 ACMP1_O #24

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PF1			US0_TX #25		
			TIM0_CC0 #25	US0_RX #24	
			TIM0_CC1 #24	US0_CLK #23	
			TIM0_CC2 #23	US0_CS #22	
			TIM0_CDTI0 #22	US0_CTS #21	
			TIM0_CDTI1 #21	US0_RTS #20	
			TIM0_CDTI2 #20	US1_TX #25	
			TIM1_CC0 #25	US1_RX #24	FRC_DCLK #25
			TIM1_CC1 #24	US1_CLK #23	FRC_DOUT #24
			TIM1_CC2 #23	US1_CS #22	FRC_DFRAME #23
	BUSAY	TIM1_CC3 #22	US1_CTS #21	MODEM_DCLK #25	PRS_CH0 #1
		WTIM0_CDTI1 #31	US1_RTS #20	MODEM_DIN #24	PRS_CH1 #0
			WTIM0_CDTI2 #29	US2_TX #15	MODEM_DOUT #23
			WTIM1_CC0 #25	US2_RX #14	MODEM_ANT0 #22
			WTIM1_CC1 #23	US2_CLK #13	MODEM_ANT1 #21
			WTIM1_CC2 #21	US2_CS #12	
			WTIM1_CC3 #19	US2_CTS #11	
			LETIM0_OUT0 #25	US2_RTS #10	
			LETIM0_OUT1 #24	LEU0_TX #25	
			PCNT0_S0IN #25	LEU0_RX #24	
			PCNT0_S1IN #24	I2C0_SDA #25	
				I2C0_SCL #24	

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PF2	BUSBY	TIM0_CC0 #26			
		TIM0_CC1 #25	US0_TX #26		
		TIM0_CC2 #24	US0_RX #25		
		TIM0_CDTI0 #23	US0_CLK #24		
		TIM0_CDTI1 #22	US0_CS #23		CMU_CLK0 #6
		TIM0_CDTI2 #21	US0_CTS #22	FRC_DCLK #26	PRS_CH0 #2
		TIM1_CC0 #26	US0_RTS #21	FRC_DOUT #25	PRS_CH1 #1
		TIM1_CC1 #25	US1_TX #26	FRC_DFRAME #24	PRS_CH2 #0
		TIM1_CC2 #24	US1_RX #25	MODEM_DCLK #26	PRS_CH3 #7
		TIM1_CC3 #23	US1_CLK #24	MODEM_DIN #25	ACMP0_O #26
	BUSAX	WTIM0_CDTI2 #30	US1_CS #23	MODEM_DOUT #24	ACMP1_O #26
		WTIM1_CC0 #26	US1_CTS #22	MODEM_ANT0 #23	DBG_TDO
		WTIM1_CC1 #24	US1_RTS #21	MODEM_ANT1 #22	DBG_SW0 #0
		WTIM1_CC2 #22	LEU0_TX #26		GPIO_EM4WU0
		WTIM1_CC3 #20	LEU0_RX #25		
		LETIM0_OUT0 #26	I2C0_SDA #26		
		LETIM0_OUT1 #25	I2C0_SCL #25		
		PCNT0_S0IN #26			
		PCNT0_S1IN #25			

GPIO Name	Pin Alternate Functionality / Description						
	Analog	Timers	Communication	Radio	Other		
PF3	BUSAY	TIM0_CC0 #27 TIM0_CC1 #26 TIM0_CC2 #25 TIM0_CDTI0 #24 TIM0_CDTI1 #23 TIM0_CDTI2 #22 TIM1_CC0 #27 TIM1_CC1 #26 TIM1_CC2 #25 TIM1_CC3 #24	US0_TX #27 US0_RX #26 US0_CLK #25 US0_CS #24 US0_CTS #23 US0_RTS #22 US1_TX #27 US1_RX #26 US1_CLK #25 US1_CS #24 US1_CTS #23 US1_RTS #22	FRC_DCLK #27 FRC_DOUT #26 FRC_DFRAME #25 MODEM_DCLK #27 MODEM_DIN #26 MODEM_DOUT #25 MODEM_ANT0 #24 MODEM_ANT1 #23	CMU_CLK1 #6 PRS_CH0 #3 PRS_CH1 #2 PRS_CH2 #1 PRS_CH3 #0 ACMP0_O #27 ACMP1_O #27 DBG_TDI		
	BUSBX	WTIM0_CDTI2 #31 WTIM1_CC0 #27 WTIM1_CC1 #25 WTIM1_CC2 #23 WTIM1_CC3 #21 LETIM0_OUT0 #27 LETIM0_OUT1 #26 PCNT0_SOIN #27 PCNT0_SIIN #26	US2_TX #16 US2_RX #15 US2_CLK #14 US2_CS #13 US2_CTS #12 US2_RTS #11 LEU0_TX #27 LEU0_RX #26 I2C0_SDA #27 I2C0_SCL #26				

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PF4	BUSBY BUSAX	TIM0_CC0 #28 TIM0_CC1 #27 TIM0_CC2 #26 TIM0_CDTI0 #25 TIM0_CDTI1 #24 TIM0_CDTI2 #23 TIM1_CC0 #28 TIM1_CC1 #27 TIM1_CC2 #26 TIM1_CC3 #25 WTIM1_CC0 #28 WTIM1_CC1 #26 WTIM1_CC2 #24 WTIM1_CC3 #22 LETIM0_OUT0 #28 LETIM0_OUT1 #27 PCNT0_S0IN #28 PCNT0_S1IN #27	US0_TX #28 US0_RX #27 US0_CLK #26 US0_CS #25 US0_CTS #24 US0_RTS #23 US1_TX #28 US1_RX #27 US1_CLK #26 US1_CS #25 US1_CTS #24 US1_RTS #23 US2_TX #17 US2_RX #16 US2_CLK #15 US2_CS #14 US2_CTS #13 US2_RTS #12 LEU0_TX #28 LEU0_RX #27 I2C0_SDA #28 I2C0_SCL #27	FRC_DCLK #28 FRC_DOUT #27 FRC_DFRAME #26 MODEM_DCLK #28 MODEM_DIN #27 MODEM_DOUT #26 MODEM_ANTO #25 MODEM_ANT1 #24	PRS_CH0 #4 PRS_CH1 #3 PRS_CH2 #2 PRS_CH3 #1 ACMP0_O #28 ACMP1_O #28

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PF5	BUSAY BUSBX	TIM0_CC0 #29 TIM0_CC1 #28 TIM0_CC2 #27 TIM0_CDTI0 #26 TIM0_CDTI1 #25 TIM0_CDTI2 #24 TIM1_CC0 #29 TIM1_CC1 #28 TIM1_CC2 #27 TIM1_CC3 #26 WTIM1_CC0 #29 WTIM1_CC1 #27 WTIM1_CC2 #25 WTIM1_CC3 #23 LETIM0_OUT0 #29 LETIM0_OUT1 #28 PCNT0_S0IN #29 PCNT0_S1IN #28	US0_TX #29 US0_RX #28 US0_CLK #27 US0_CS #26 US0_CTS #25 US0_RTS #24 US1_TX #29 US1_RX #28 US1_CLK #27 US1_CS #26 US1_CTS #25 US1_RTS #24 US2_TX #18 US2_RX #17 US2_CLK #16 US2_CS #15 US2_CTS #14 US2_RTS #13 LEU0_TX #29 LEU0_RX #28 I2C0_SDA #29 I2C0_SCL #28	FRC_DCLK #29 FRC_DOUT #28 FRC_DFRAME #27 MODEM_DCLK #29 MODEM_DIN #28 MODEM_DOUT #27 MODEM_ANTO #26 MODEM_ANT1 #25	PRS_CH0 #5 PRS_CH1 #4 PRS_CH2 #3 PRS_CH3 #2 ACMP0_O #29 ACMP1_O #29

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PF6	BUSBY		US0_TX #30		
		TIM0_CC0 #30	US0_RX #29		
		TIM0_CC1 #29	US0_CLK #28		
		TIM0_CC2 #28	US0_CS #27		
		TIM0_CDTI0 #27	US0_CTS #26		
		TIM0_CDTI1 #26	US0_RTS #25		
		TIM0_CDTI2 #25	US1_TX #30		
		TIM1_CC0 #30	US1_RX #29	FRC_DCLK #30	CMU_CLK1 #7
		TIM1_CC1 #29	US1_CLK #28	FRC_DOUT #29	PRS_CH0 #6
		TIM1_CC2 #28	US1_CS #27	FRC_DFRAME #28	PRS_CH1 #5
	BUSAX	TIM1_CC3 #27	US1_CTS #26	MODEM_DCLK #30	PRS_CH2 #4
		WTIM1_CC0 #30	US1_RTS #25	MODEM_DIN #29	PRS_CH3 #3
		WTIM1_CC1 #28	US2_TX #19	MODEM_DOUT #28	ACMP0_O #30
		WTIM1_CC2 #26	US2_RX #18	MODEM_ANT0 #27	ACMP1_O #30
		WTIM1_CC3 #24	US2_CLK #17	MODEM_ANT1 #26	
		LETIM0_OUT0 #30	US2_CS #16		
		LETIM0_OUT1 #29	US2_CTS #15		
		PCNT0_S0IN #30	US2_RTS #14		
		PCNT0_S1IN #29	LEU0_TX #30		
		PCNT1_S0IN #19	LEU0_RX #29		
		PCNT1_S1IN #18	I2C0_SDA #30		
			I2C0_SCL #29		

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PF7	BUSAY BUSBX	TIM0_CC0 #31 TIM0_CC1 #30 TIM0_CC2 #29 TIM0_CDTI0 #28 TIM0_CDTI1 #27 TIM0_CDTI2 #26 TIM1_CC0 #31 TIM1_CC1 #30 TIM1_CC2 #29 TIM1_CC3 #28 WTIM1_CC0 #31 WTIM1_CC1 #29 WTIM1_CC2 #27 WTIM1_CC3 #25 LETIM0_OUT0 #31 LETIM0_OUT1 #30 PCNT0_S0IN #31 PCNT0_S1IN #30 PCNT1_S0IN #20 PCNT1_S1IN #19	US0_TX #31 US0_RX #30 US0_CLK #29 US0_CS #28 US0_CTS #27 US0 RTS #26 US1_TX #31 US1_RX #30 US1_CLK #29 US1_CS #28 US1_CTS #27 US1 RTS #26 US2_TX #20 US2_RX #19 US2_CLK #18 US2_CS #17 US2_CTS #16 US2_RTS #15 LEU0_TX #31 LEU0_RX #30 I2C0_SDA #31 I2C0_SCL #30	FRC_DCLK #31 FRC_DOUT #30 FRC_DFRAME #29 MODEM_DCLK #31 MODEM_DIN #30 MODEM_DOUT #29 MODEM_ANT0 #28 MODEM_ANT1 #27 ACMP0_O #31 ACMP1_O #31 GPIO_EM4WU1	
PF8	BUSBY BUSAX	WTIM1_CC1 #30 WTIM1_CC2 #28 WTIM1_CC3 #26 PCNT1_S0IN #21 PCNT1_S1IN #20 PCNT2_S0IN #21 PCNT2_S1IN #20	US2_TX #21 US2_RX #20 US2_CLK #19 US2_CS #18 US2_CTS #17 US2_RTS #16 I2C1_SDA #21 I2C1_SCL #20	ETM_TCLK #0	

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PF9	BUSAY BUSBX	WTIM1_CC1 #31 WTIM1_CC2 #29 WTIM1_CC3 #27 PCNT1_S0IN #22 PCNT1_S1IN #21 PCNT2_S0IN #22 PCNT2_S1IN #21	US2_TX #22 US2_RX #21 US2_CLK #20 US2_CS #19 US2_CTS #18 US2_RTS #17 I2C1_SDA #22 I2C1_SCL #21		ETM_TD0 #0
PF10	BUSBY BUSAX	WTIM1_CC2 #30 WTIM1_CC3 #28 PCNT1_S0IN #23 PCNT1_S1IN #22 PCNT2_S0IN #23 PCNT2_S1IN #22	US2_TX #23 US2_RX #22 US2_CLK #21 US2_CS #20 US2_CTS #19 US2_RTS #18 I2C1_SDA #23 I2C1_SCL #22		ETM_TD1 #0
PF11	BUSAY BUSBX		US2_TX #24 US2_RX #23 US2_CLK #22 US2_CS #21 WTIM1_CC2 #31 WTIM1_CC3 #29 PCNT1_S0IN #24 PCNT1_S1IN #23 PCNT2_S0IN #24 PCNT2_S1IN #23		ETM_TD2 #0

GPIO Name	Pin Alternate Functionality / Description					
	Analog	Timers	Communication	Radio	Other	
PF12	BUSBY	WTIM1_CC3 #30 PCNT1_S0IN #25 PCNT1_S1IN #24 PCNT2_S0IN #25 PCNT2_S1IN #24	US2_TX #25 US2_RX #24 US2_CLK #23 US2_CS #22 US2_CTS #21 US2_RTS #20 US3_TX #25 US3_RX #24 US3_CLK #23 US3_CS #22 US3_CTS #21 US3_RTS #20 I2C1_SDA #25 I2C1_SCL #24	ETM_TD3 #0		
	BUSAX					
PF13	BUSAY	WTIM1_CC3 #31 PCNT1_S0IN #26 PCNT1_S1IN #25 PCNT2_S0IN #26 PCNT2_S1IN #25	US2_TX #26 US2_RX #25 US2_CLK #24 US2_CS #23 US2_CTS #22 US2_RTS #21 US3_TX #26 US3_RX #25 US3_CLK #24 US3_CS #23 US3_CTS #22 US3_RTS #21 I2C1_SDA #26 I2C1_SCL #25	ETM_TD3 #0		
	BUSBX					

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PF14	BUSBY		US2_TX #27		
			US2_RX #26		
			US2_CLK #25		
			US2_CS #24		
			US2_CTS #23		
	BUSAX	PCNT1_S0IN #27	US2_RTS #22		
		PCNT1_S1IN #26	US3_TX #27		
		PCNT2_S0IN #27	US3_RX #26		
		PCNT2_S1IN #26	US3_CLK #25		
			US3_CS #24		
PF15	BUSAY		US3_CTS #23		
			US3_RTS #22		
			I2C1_SDA #27		
			I2C1_SCL #26		
			US2_TX #28		
	BUSBX		US2_RX #27		
			US2_CLK #26		
			US2_CS #25		
			US2_CTS #24		
			PCNT1_S0IN #28	US2_RTS #23	
PIO	BUSADC0Y		PCNT1_S1IN #27	US3_TX #28	
			PCNT2_S0IN #28	US3_RX #27	
			PCNT2_S1IN #27	US3_CLK #26	
				US3_CS #25	
				US3_CTS #24	
	BUSADC0X			US3_RTS #23	
				I2C1_SDA #28	
				I2C1_SCL #27	
			US2_TX #5		
			US2_RX #4		
			US2_CLK #3		
			US2_CS #2		
			US2_CTS #1		
			US2_RTS #0		
					LES_ALTEX4

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PI1	BUSADC0Y BUSADC0X		US2_TX #6 US2_RX #5 US2_CLK #4 US2_CS #3 US2_CTS #2 US2_RTS #1		LES_ALTEX5
PI2	BUSADC0Y BUSADC0X	PCNT1_S0IN #4 PCNT1_S1IN #3 PCNT2_S0IN #4 PCNT2_S1IN #3	US2_TX #7 US2_RX #6 US2_CLK #5 US2_CS #4 US2_CTS #3 US2_RTS #2 US3_TX #8 US3_RX #7 US3_CLK #6 US3_CS #5 US3_CTS #4 US3_RTS #3 I2C1_SDA #4 I2C1_SCL #3		LES_ALTEX6 ETM_TCLK #2
PI3	BUSADC0Y BUSADC0X	PCNT1_S0IN #5 PCNT1_S1IN #4 PCNT2_S0IN #5 PCNT2_S1IN #4	US2_TX #8 US2_RX #7 US2_CLK #6 US2_CS #5 US2_CTS #4 US2_RTS #3 US3_TX #9 US3_RX #8 US3_CLK #7 US3_CS #6 US3_CTS #5 US3_RTS #4 I2C1_SDA #5 I2C1_SCL #4		LES_ALTEX7 ETM_TD0 #2

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PJ14	BUSACMP1Y BUSACMP1X	PCNT1_S0IN #11 PCNT1_S1IN #10 PCNT2_S0IN #11 PCNT2_S1IN #10	US3_TX #16 US3_RX #15 US3_CLK #14 US3_CS #13 US3_CTS #12 US3_RTS #11 I2C1_SDA #11 I2C1_SCL #10		LES_ALTEX2
PJ15	BUSACMP1Y BUSACMP1X	PCNT1_S0IN #12 PCNT1_S1IN #11 PCNT2_S0IN #12 PCNT2_S1IN #11	US3_TX #17 US3_RX #16 US3_CLK #15 US3_CS #14 US3_CTS #13 US3_RTS #12 I2C1_SDA #12 I2C1_SCL #11		LES_ALTEX3
PK0	IDAC0_OUT		US2_TX #29 US2_RX #28 US2_CLK #27 US2_CS #26 US2_CTS #25 PCNT1_S0IN #29 PCNT1_S1IN #28 PCNT2_S0IN #29 PCNT2_S1IN #28	US2_RTS #24 US3_TX #29 US3_RX #28 US3_CLK #27 US3_CS #26 US3_CTS #25 US3_RTS #24 I2C1_SDA #29 I2C1_SCL #28	

GPIO Name	Pin Alternate Functionality / Description				
	Analog	Timers	Communication	Radio	Other
PK1			US2_TX #30		
			US2_RX #29		
			US2_CLK #28		
			US2_CS #27		
			US2_CTS #26		
			PCNT1_S0IN #30	US2_RTS #25	
			PCNT1_S1IN #29	US3_TX #30	
			PCNT2_S0IN #30	US3_RX #29	
			PCNT2_S1IN #29	US3_CLK #28	
				US3_CS #27	
PK2			US3_CTS #26		
			US3_RTS #25		
			I2C1_SDA #30		
			I2C1_SCL #29		
			US2_TX #31		
			US2_RX #30		
			US2_CLK #29		
			US2_CS #28		
			US2_CTS #27		
			PCNT1_S0IN #31	US2_RTS #26	
			PCNT1_S1IN #30	US3_TX #31	
			PCNT2_S0IN #31	US3_RX #30	
			PCNT2_S1IN #30	US3_CLK #29	
				US3_CS #28	
			US3_CTS #27		
			US3_RTS #26		
			I2C1_SDA #31		
			I2C1_SCL #30		

6.10 Alternate Functionality Overview

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings and the associated GPIO pin. Refer to [6.9 GPIO Functionality Table](#) for a list of functions available on each GPIO pin.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 6.10. Alternate Functionality Overview

Alternate	LOCATION									
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description	
ACMP0_O	0: PA0	4: PA4	8: PB13	12: PC7	16: PC11	20: PD12	24: PF0	28: PF4	Analog comparator ACMP0, digital output.	
	1: PA1	5: PA5	9: PB14	13: PC8	17: PD9	21: PD13	25: PF1	29: PF5		
	2: PA2	6: PB11	10: PB15	14: PC9	18: PD10	22: PD14	26: PF2	30: PF6		
	3: PA3	7: PB12	11: PC6	15: PC10	19: PD11	23: PD15	27: PF3	31: PF7		
ACMP1_O	0: PA0	4: PA4	8: PB13	12: PC7	16: PC11	20: PD12	24: PF0	28: PF4	Analog comparator ACMP1, digital output.	
	1: PA1	5: PA5	9: PB14	13: PC8	17: PD9	21: PD13	25: PF1	29: PF5		
	2: PA2	6: PB11	10: PB15	14: PC9	18: PD10	22: PD14	26: PF2	30: PF6		
	3: PA3	7: PB12	11: PC6	15: PC10	19: PD11	23: PD15	27: PF3	31: PF7		
ADC0_EXTN	0: PA0								Analog to digital converter ADC0 external reference input negative pin.	
ADC0_EXTP	0: PA1								Analog to digital converter ADC0 external reference input positive pin.	
BOOT_RX	0: PF1								Bootloader RX.	
BOOT_TX	0: PF0								Bootloader TX.	
CMU_CLK0	0: PA1	4: PD9							Clock Management Unit, clock output number 0.	
	1: PB15	5: PD14								
	2: PC6	6: PF2								
	3: PC11	7: PF7								
CMU_CLK1	0: PA0	4: PD10							Clock Management Unit, clock output number 1.	
	1: PB14	5: PD15								
	2: PC7	6: PF3								
	3: PC10	7: PF6								
CMU_CLK10	0: PB13	4: PA5							Clock Management Unit, clock input number 0.	
	1: PF7									
	2: PC6									
	3: PB6									

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
DBG_SWCLKTCK	0: PF0								Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down.
DBG_SWDIOTMS	0: PF1								Debug-interface Serial Wire data input / output and JTAG Test Mode Select. Note that this function is enabled to the pin out of reset, and has a built-in pull up.
DBG_SWO	0: PF2 1: PB13 2: PD15 3: PC11								Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
DBG_TDI	0: PF3								Debug-interface JTAG Test Data In. Note that this function becomes available after the first valid JTAG command is received, and has a built-in pull up when JTAG is active.
DBG_TDO	0: PF2								Debug-interface JTAG Test Data Out. Note that this function becomes available after the first valid JTAG command is received.
ETM_TCLK	0: PF8 1: PA5 2: PI2 3: PC6								Embedded Trace Module ETM clock .

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
ETM_TD0	0: PF9 1: PA6 2: PI3 3: PC7								Embedded Trace Module ETM data 0.
ETM_TD1	0: PF10 1: PA7 2: PB6 3: PC8								Embedded Trace Module ETM data 1.
ETM_TD2	0: PF11 1: PA8 2: PB7 3: PC9								Embedded Trace Module ETM data 2.
ETM_TD3	0: PF12 1: PA9 2: PB8 3: PC10								Embedded Trace Module ETM data 3.
FRC_DCLK	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Frame Controller, Data Sniffer Clock.
FRC_DFRAME	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Frame Controller, Data Sniffer Frame active
FRC_DOUT	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Frame Controller, Data Sniffer Output.
GPIO_EM4WU0	0: PF2								Pin can be used to wake the system up from EM4
GPIO_EM4WU1	0: PF7								Pin can be used to wake the system up from EM4
GPIO_EM4WU4	0: PD14								Pin can be used to wake the system up from EM4

Alternate	LOCATION									
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description	
GPIO_EM4WU8	0: PA3								Pin can be used to wake the system up from EM4	
GPIO_EM4WU9	0: PB13								Pin can be used to wake the system up from EM4	
GPIO_EM4WU12	0: PC10								Pin can be used to wake the system up from EM4	
I2C0_SCL	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	I2C0 Serial Clock Line input / output.	
I2C0_SDA	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	I2C0 Serial Data input / output.	
I2C1_SCL	0: PA7 1: PA8 2: PA9 3: PI2	4: PI3 5: PB6 6: PB7 7: PB8	8: PB9 9: PB10 10: PJ14 11: PJ15	12: PC0 13: PC1 14: PC2 15: PC3	16: PC4 17: PC5 18: PC10 19: PC11	20: PF8 21: PF9 22: PF10 23: PF11	24: PF12 25: PF13 26: PF14 27: PF15	28: PK0 29: PK1 30: PK2 31: PA6	I2C1 Serial Clock Line input / output.	
I2C1_SDA	0: PA6 1: PA7 2: PA8 3: PA9	4: PI2 5: PI3 6: PB6 7: PB7	8: PB8 9: PB9 10: PB10 11: PJ14	12: PJ15 13: PC0 14: PC1 15: PC2	16: PC3 17: PC4 18: PC5 19: PC10	20: PC11 21: PF8 22: PF9 23: PF10	24: PF11 25: PF12 26: PF13 27: PF14	28: PF15 29: PK0 30: PK1 31: PK2	I2C1 Serial Data input / output.	
IDAC0_OUT	0: PK0								IDAC0 output.	
LES_ALTEX0	0: PA8								LESENSE alternate excite output 0.	
LES_ALTEX1	0: PA9								LESENSE alternate excite output 1.	
LES_ALTEX2	0: PJ14								LESENSE alternate excite output 2.	
LES_ALTEX3	0: PJ15								LESENSE alternate excite output 3.	
LES_ALTEX4	0: PI0								LESENSE alternate excite output 4.	
LES_ALTEX5	0: PI1								LESENSE alternate excite output 5.	
LES_ALTEX6	0: PI2								LESENSE alternate excite output 6.	
LES_ALTEX7	0: PI3								LESENSE alternate excite output 7.	

Alternate	LOCATION									
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description	
LES_CH0	0: PD8								LESENSE channel 0.	
LES_CH1	0: PD9								LESENSE channel 1.	
LES_CH2	0: PD10								LESENSE channel 2.	
LES_CH3	0: PD11								LESENSE channel 3.	
LES_CH4	0: PD12								LESENSE channel 4.	
LES_CH5	0: PD13								LESENSE channel 5.	
LES_CH6	0: PD14								LESENSE channel 6.	
LES_CH7	0: PD15								LESENSE channel 7.	
LES_CH8	0: PA0								LESENSE channel 8.	
LES_CH9	0: PA1								LESENSE channel 9.	
LES_CH10	0: PA2								LESENSE channel 10.	
LES_CH11	0: PA3								LESENSE channel 11.	
LES_CH12	0: PA4								LESENSE channel 12.	
LES_CH13	0: PA5								LESENSE channel 13.	
LES_CH14	0: PA6								LESENSE channel 14.	
LES_CH15	0: PA7								LESENSE channel 15.	
LETIM0_OUT0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Low Energy Timer LETIM0, output channel 0.	
LETIM0_OUT1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Low Energy Timer LETIM0, output channel 1.	

Alternate	LOCATION									
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description	
LEU0_RX	0: PA1	4: PA5	8: PB14	12: PC8	16: PD9	20: PD13	24: PF1	28: PF5	LEUART0 Receive input.	
	1: PA2	5: PB11	9: PB15	13: PC9	17: PD10	21: PD14	25: PF2	29: PF6		
	2: PA3	6: PB12	10: PC6	14: PC10	18: PD11	22: PD15	26: PF3	30: PF7		
	3: PA4	7: PB13	11: PC7	15: PC11	19: PD12	23: PF0	27: PF4	31: PA0		
LEU0_TX	0: PA0	4: PA4	8: PB13	12: PC7	16: PC11	20: PD12	24: PF0	28: PF4	LEUART0 Transmit output. Also used as receive input in half duplex communication.	
	1: PA1	5: PA5	9: PB14	13: PC8	17: PD9	21: PD13	25: PF1	29: PF5		
	2: PA2	6: PB11	10: PB15	14: PC9	18: PD10	22: PD14	26: PF2	30: PF6		
	3: PA3	7: PB12	11: PC6	15: PC10	19: PD11	23: PD15	27: PF3	31: PF7		
LFXTAL_N	0: PB14								Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.	
LFXTAL_P	0: PB15								Low Frequency Crystal (typically 32.768 kHz) positive pin.	
MODEM_ANT0	0: PA3	4: PB12	8: PC6	12: PC10	16: PD11	20: PD15	24: PF3	28: PF7	MODEM antenna control output 0, used for antenna diversity.	
	1: PA4	5: PB13	9: PC7	13: PC11	17: PD12	21: PF0	25: PF4	29: PA0		
	2: PA5	6: PB14	10: PC8	14: PD9	18: PD13	22: PF1	26: PF5	30: PA1		
	3: PB11	7: PB15	11: PC9	15: PD10	19: PD14	23: PF2	27: PF6	31: PA2		
MODEM_ANT1	0: PA4	4: PB13	8: PC7	12: PC11	16: PD12	20: PF0	24: PF4	28: PA0	MODEM antenna control output 1, used for antenna diversity.	
	1: PA5	5: PB14	9: PC8	13: PD9	17: PD13	21: PF1	25: PF5	29: PA1		
	2: PB11	6: PB15	10: PC9	14: PD10	18: PD14	22: PF2	26: PF6	30: PA2		
	3: PB12	7: PC6	11: PC10	15: PD11	19: PD15	23: PF3	27: PF7	31: PA3		
MODEM_DCLK	0: PA0	4: PA4	8: PB13	12: PC7	16: PC11	20: PD12	24: PF0	28: PF4	MODEM data clock out.	
	1: PA1	5: PA5	9: PB14	13: PC8	17: PD9	21: PD13	25: PF1	29: PF5		
	2: PA2	6: PB11	10: PB15	14: PC9	18: PD10	22: PD14	26: PF2	30: PF6		
	3: PA3	7: PB12	11: PC6	15: PC10	19: PD11	23: PD15	27: PF3	31: PF7		
MODEM_DIN	0: PA1	4: PA5	8: PB14	12: PC8	16: PD9	20: PD13	24: PF1	28: PF5	MODEM data in.	
	1: PA2	5: PB11	9: PB15	13: PC9	17: PD10	21: PD14	25: PF2	29: PF6		
	2: PA3	6: PB12	10: PC6	14: PC10	18: PD11	22: PD15	26: PF3	30: PF7		
	3: PA4	7: PB13	11: PC7	15: PC11	19: PD12	23: PF0	27: PF4	31: PA0		
MODEM_DOUT	0: PA2	4: PB11	8: PB15	12: PC9	16: PD10	20: PD14	24: PF2	28: PF6	MODEM data out.	
	1: PA3	5: PB12	9: PC6	13: PC10	17: PD11	21: PD15	25: PF3	29: PF7		
	2: PA4	6: PB13	10: PC7	14: PC11	18: PD12	22: PF0	26: PF4	30: PA0		
	3: PA5	7: PB14	11: PC8	15: PD9	19: PD13	23: PF1	27: PF5	31: PA1		

Alternate	LOCATION									
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description	
OPA0_N	0: PA4								Operational Amplifier 0 external negative input.	
OPA0_P	0: PA2								Operational Amplifier 0 external positive input.	
OPA1_N	0: PD15								Operational Amplifier 1 external negative input.	
OPA1_P	0: PD13								Operational Amplifier 1 external positive input.	
OPA2_N	0: PB13								Operational Amplifier 2 external negative input.	
OPA2_OUT	0: PB12								Operational Amplifier 2 output.	
OPA2_OUTALT	0: PB9 1: PB10								Operational Amplifier 2 alternative output.	
OPA2_P	0: PB11								Operational Amplifier 2 external positive input.	
PCNT0_S0IN	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Pulse Counter PCNT0 input number 0.	
PCNT0_S1IN	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Pulse Counter PCNT0 input number 1.	
PCNT1_S0IN	0: PA6 1: PA7 2: PA8 3: PA9	4: PI2 5: PI3 6: PB6 7: PB7	8: PB8 9: PB9 10: PB10 11: PJ14	12: PJ15 13: PC0 14: PC1 15: PC2	16: PC3 17: PC4 18: PC5 19: PF6	20: PF7 21: PF8 22: PF9 23: PF10	24: PF11 25: PF12 26: PF13 27: PF14	28: PF15 29: PK0 30: PK1 31: PK2	Pulse Counter PCNT1 input number 0.	
PCNT1_S1IN	0: PA7 1: PA8 2: PA9 3: PI2	4: PI3 5: PB6 6: PB7 7: PB8	8: PB9 9: PB10 10: PJ14 11: PJ15	12: PC0 13: PC1 14: PC2 15: PC3	16: PC4 17: PC5 18: PF6 19: PF7	20: PF8 21: PF9 22: PF10 23: PF11	24: PF12 25: PF13 26: PF14 27: PF15	28: PK0 29: PK1 30: PK2 31: PA6	Pulse Counter PCNT1 input number 1.	

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
PCNT2_S0IN	0: PA6	4: PI2	8: PB8	12: PJ15	16: PC3	20: PC11	24: PF11	28: PF15	Pulse Counter PCNT2 input number 0.
	1: PA7	5: PI3	9: PB9	13: PC0	17: PC4	21: PF8	25: PF12	29: PK0	
	2: PA8	6: PB6	10: PB10	14: PC1	18: PC5	22: PF9	26: PF13	30: PK1	
	3: PA9	7: PB7	11: PJ14	15: PC2	19: PC10	23: PF10	27: PF14	31: PK2	
PCNT2_S1IN	0: PA7	4: PI3	8: PB9	12: PC0	16: PC4	20: PF8	24: PF12	28: PK0	Pulse Counter PCNT2 input number 1.
	1: PA8	5: PB6	9: PB10	13: PC1	17: PC5	21: PF9	25: PF13	29: PK1	
	2: PA9	6: PB7	10: PJ14	14: PC2	18: PC10	22: PF10	26: PF14	30: PK2	
	3: PI2	7: PB8	11: PJ15	15: PC3	19: PC11	23: PF11	27: PF15	31: PA6	
PRS_CH0	0: PF0	4: PF4	8: PC6	12: PC10					Peripheral Reflex System PRS, channel 0.
	1: PF1	5: PF5	9: PC7	13: PC11					
	2: PF2	6: PF6	10: PC8						
	3: PF3	7: PF7	11: PC9						
PRS_CH1	0: PF1	4: PF5							Peripheral Reflex System PRS, channel 1.
	1: PF2	5: PF6							
	2: PF3	6: PF7							
	3: PF4	7: PF0							
PRS_CH2	0: PF2	4: PF6							Peripheral Reflex System PRS, channel 2.
	1: PF3	5: PF7							
	2: PF4	6: PF0							
	3: PF5	7: PF1							
PRS_CH3	0: PF3	4: PF7	8: PD9	12: PD13					Peripheral Reflex System PRS, channel 3.
	1: PF4	5: PF0	9: PD10	13: PD14					
	2: PF5	6: PF1	10: PD11	14: PD15					
	3: PF6	7: PF2	11: PD12						
PRS_CH4	0: PD9	4: PD13							Peripheral Reflex System PRS, channel 4.
	1: PD10	5: PD14							
	2: PD11	6: PD15							
	3: PD12								
PRS_CH5	0: PD10	4: PD14							Peripheral Reflex System PRS, channel 5.
	1: PD11	5: PD15							
	2: PD12	6: PD9							
	3: PD13								
PRS_CH6	0: PA0	4: PA4	8: PB13	12: PD10	16: PD14				Peripheral Reflex System PRS, channel 6.
	1: PA1	5: PA5	9: PB14	13: PD11	17: PD15				
	2: PA2	6: PB11	10: PB15	14: PD12					
	3: PA3	7: PB12	11: PD9	15: PD13					

Alternate	LOCATION									
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description	
PRS_CH7	0: PA1	4: PA5	8: PB14						Peripheral Reflex System PRS, channel 7.	
	1: PA2	5: PB11	9: PB15							
	2: PA3	6: PB12	10: PA0							
	3: PA4	7: PB13								
PRS_CH8	0: PA2	4: PB11	8: PB15						Peripheral Reflex System PRS, channel 8.	
	1: PA3	5: PB12	9: PA0							
	2: PA4	6: PB13	10: PA1							
	3: PA5	7: PB14								
PRS_CH9	0: PA3	4: PB12	8: PA0	12: PC7	16: PC11				Peripheral Reflex System PRS, channel 9.	
	1: PA4	5: PB13	9: PA1	13: PC8						
	2: PA5	6: PB14	10: PA2	14: PC9						
	3: PB11	7: PB15	11: PC6	15: PC10						
PRS_CH10	0: PC6	4: PC10							Peripheral Reflex System PRS, channel 10.	
	1: PC7	5: PC11								
	2: PC8									
	3: PC9									
PRS_CH11	0: PC7	4: PC11							Peripheral Reflex System PRS, channel 11.	
	1: PC8	5: PC6								
	2: PC9									
	3: PC10									
TIM0_CC0	0: PA0	4: PA4	8: PB13	12: PC7	16: PC11	20: PD12	24: PF0	28: PF4	Timer 0 Capture Compare input / output channel 0.	
	1: PA1	5: PA5	9: PB14	13: PC8	17: PD9	21: PD13	25: PF1	29: PF5		
	2: PA2	6: PB11	10: PB15	14: PC9	18: PD10	22: PD14	26: PF2	30: PF6		
	3: PA3	7: PB12	11: PC6	15: PC10	19: PD11	23: PD15	27: PF3	31: PF7		
TIM0_CC1	0: PA1	4: PA5	8: PB14	12: PC8	16: PD9	20: PD13	24: PF1	28: PF5	Timer 0 Capture Compare input / output channel 1.	
	1: PA2	5: PB11	9: PB15	13: PC9	17: PD10	21: PD14	25: PF2	29: PF6		
	2: PA3	6: PB12	10: PC6	14: PC10	18: PD11	22: PD15	26: PF3	30: PF7		
	3: PA4	7: PB13	11: PC7	15: PC11	19: PD12	23: PF0	27: PF4	31: PA0		
TIM0_CC2	0: PA2	4: PB11	8: PB15	12: PC9	16: PD10	20: PD14	24: PF2	28: PF6	Timer 0 Capture Compare input / output channel 2.	
	1: PA3	5: PB12	9: PC6	13: PC10	17: PD11	21: PD15	25: PF3	29: PF7		
	2: PA4	6: PB13	10: PC7	14: PC11	18: PD12	22: PF0	26: PF4	30: PA0		
	3: PA5	7: PB14	11: PC8	15: PD9	19: PD13	23: PF1	27: PF5	31: PA1		
TIM0_CDT10	0: PA3	4: PB12	8: PC6	12: PC10	16: PD11	20: PD15	24: PF3	28: PF7	Timer 0 Complementary Dead Time Insertion channel 0.	
	1: PA4	5: PB13	9: PC7	13: PC11	17: PD12	21: PF0	25: PF4	29: PA0		
	2: PA5	6: PB14	10: PC8	14: PD9	18: PD13	22: PF1	26: PF5	30: PA1		
	3: PB11	7: PB15	11: PC9	15: PD10	19: PD14	23: PF2	27: PF6	31: PA2		

Alternate	LOCATION									
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description	
TIM0_CDTI1	0: PA4	4: PB13	8: PC7	12: PC11	16: PD12	20: PF0	24: PF4	28: PA0	Timer 0 Complementary Dead Time Insertion channel 1.	
	1: PA5	5: PB14	9: PC8	13: PD9	17: PD13	21: PF1	25: PF5	29: PA1		
	2: PB11	6: PB15	10: PC9	14: PD10	18: PD14	22: PF2	26: PF6	30: PA2		
	3: PB12	7: PC6	11: PC10	15: PD11	19: PD15	23: PF3	27: PF7	31: PA3		
TIM0_CDTI2	0: PA5	4: PB14	8: PC8	12: PD9	16: PD13	20: PF1	24: PF5	28: PA1	Timer 0 Complementary Dead Time Insertion channel 2.	
	1: PB11	5: PB15	9: PC9	13: PD10	17: PD14	21: PF2	25: PF6	29: PA2		
	2: PB12	6: PC6	10: PC10	14: PD11	18: PD15	22: PF3	26: PF7	30: PA3		
	3: PB13	7: PC7	11: PC11	15: PD12	19: PF0	23: PF4	27: PA0	31: PA4		
TIM1_CC0	0: PA0	4: PA4	8: PB13	12: PC7	16: PC11	20: PD12	24: PF0	28: PF4	Timer 1 Capture Compare input / output channel 0.	
	1: PA1	5: PA5	9: PB14	13: PC8	17: PD9	21: PD13	25: PF1	29: PF5		
	2: PA2	6: PB11	10: PB15	14: PC9	18: PD10	22: PD14	26: PF2	30: PF6		
	3: PA3	7: PB12	11: PC6	15: PC10	19: PD11	23: PD15	27: PF3	31: PF7		
TIM1_CC1	0: PA1	4: PA5	8: PB14	12: PC8	16: PD9	20: PD13	24: PF1	28: PF5	Timer 1 Capture Compare input / output channel 1.	
	1: PA2	5: PB11	9: PB15	13: PC9	17: PD10	21: PD14	25: PF2	29: PF6		
	2: PA3	6: PB12	10: PC6	14: PC10	18: PD11	22: PD15	26: PF3	30: PF7		
	3: PA4	7: PB13	11: PC7	15: PC11	19: PD12	23: PF0	27: PF4	31: PA0		
TIM1_CC2	0: PA2	4: PB11	8: PB15	12: PC9	16: PD10	20: PD14	24: PF2	28: PF6	Timer 1 Capture Compare input / output channel 2.	
	1: PA3	5: PB12	9: PC6	13: PC10	17: PD11	21: PD15	25: PF3	29: PF7		
	2: PA4	6: PB13	10: PC7	14: PC11	18: PD12	22: PF0	26: PF4	30: PA0		
	3: PA5	7: PB14	11: PC8	15: PD9	19: PD13	23: PF1	27: PF5	31: PA1		
TIM1_CC3	0: PA3	4: PB12	8: PC6	12: PC10	16: PD11	20: PD15	24: PF3	28: PF7	Timer 1 Capture Compare input / output channel 3.	
	1: PA4	5: PB13	9: PC7	13: PC11	17: PD12	21: PF0	25: PF4	29: PA0		
	2: PA5	6: PB14	10: PC8	14: PD9	18: PD13	22: PF1	26: PF5	30: PA1		
	3: PB11	7: PB15	11: PC9	15: PD10	19: PD14	23: PF2	27: PF6	31: PA2		
US0_CLK	0: PA2	4: PB11	8: PB15	12: PC9	16: PD10	20: PD14	24: PF2	28: PF6	USART0 clock input / output.	
	1: PA3	5: PB12	9: PC6	13: PC10	17: PD11	21: PD15	25: PF3	29: PF7		
	2: PA4	6: PB13	10: PC7	14: PC11	18: PD12	22: PF0	26: PF4	30: PA0		
	3: PA5	7: PB14	11: PC8	15: PD9	19: PD13	23: PF1	27: PF5	31: PA1		
US0_CS	0: PA3	4: PB12	8: PC6	12: PC10	16: PD11	20: PD15	24: PF3	28: PF7	USART0 chip select input / output.	
	1: PA4	5: PB13	9: PC7	13: PC11	17: PD12	21: PF0	25: PF4	29: PA0		
	2: PA5	6: PB14	10: PC8	14: PD9	18: PD13	22: PF1	26: PF5	30: PA1		
	3: PB11	7: PB15	11: PC9	15: PD10	19: PD14	23: PF2	27: PF6	31: PA2		
US0_CTS	0: PA4	4: PB13	8: PC7	12: PC11	16: PD12	20: PF0	24: PF4	28: PA0	USART0 Clear To Send hardware flow control input.	
	1: PA5	5: PB14	9: PC8	13: PD9	17: PD13	21: PF1	25: PF5	29: PA1		
	2: PB11	6: PB15	10: PC9	14: PD10	18: PD14	22: PF2	26: PF6	30: PA2		
	3: PB12	7: PC6	11: PC10	15: PD11	19: PD15	23: PF3	27: PF7	31: PA3		

Alternate	LOCATION									
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description	
US0_RTS	0: PA5	4: PB14	8: PC8	12: PD9	16: PD13	20: PF1	24: PF5	28: PA1	USART0 Request To Send hardware flow control output.	
	1: PB11	5: PB15	9: PC9	13: PD10	17: PD14	21: PF2	25: PF6	29: PA2		
	2: PB12	6: PC6	10: PC10	14: PD11	18: PD15	22: PF3	26: PF7	30: PA3		
	3: PB13	7: PC7	11: PC11	15: PD12	19: PF0	23: PF4	27: PA0	31: PA4		
US0_RX	0: PA1	4: PA5	8: PB14	12: PC8	16: PD9	20: PD13	24: PF1	28: PF5	USART0 Asynchronous Receive.	
	1: PA2	5: PB11	9: PB15	13: PC9	17: PD10	21: PD14	25: PF2	29: PF6	USART0 Synchronous mode Master Input / Slave Output (MISO).	
	2: PA3	6: PB12	10: PC6	14: PC10	18: PD11	22: PD15	26: PF3	30: PF7		
	3: PA4	7: PB13	11: PC7	15: PC11	19: PD12	23: PF0	27: PF4	31: PA0		
US0_TX	0: PA0	4: PA4	8: PB13	12: PC7	16: PC11	20: PD12	24: PF0	28: PF4	USART0 Asynchronous Transmit. Also used as receive input in half duplex communication.	
	1: PA1	5: PA5	9: PB14	13: PC8	17: PD9	21: PD13	25: PF1	29: PF5	USART0 Synchronous mode Master Output / Slave Input (MOSI).	
	2: PA2	6: PB11	10: PB15	14: PC9	18: PD10	22: PD14	26: PF2	30: PF6		
	3: PA3	7: PB12	11: PC6	15: PC10	19: PD11	23: PD15	27: PF3	31: PF7		
US1_CLK	0: PA2	4: PB11	8: PB15	12: PC9	16: PD10	20: PD14	24: PF2	28: PF6	USART1 clock input / output.	
	1: PA3	5: PB12	9: PC6	13: PC10	17: PD11	21: PD15	25: PF3	29: PF7		
	2: PA4	6: PB13	10: PC7	14: PC11	18: PD12	22: PF0	26: PF4	30: PA0		
	3: PA5	7: PB14	11: PC8	15: PD9	19: PD13	23: PF1	27: PF5	31: PA1		
US1_CS	0: PA3	4: PB12	8: PC6	12: PC10	16: PD11	20: PD15	24: PF3	28: PF7	USART1 chip select input / output.	
	1: PA4	5: PB13	9: PC7	13: PC11	17: PD12	21: PF0	25: PF4	29: PA0		
	2: PA5	6: PB14	10: PC8	14: PD9	18: PD13	22: PF1	26: PF5	30: PA1		
	3: PB11	7: PB15	11: PC9	15: PD10	19: PD14	23: PF2	27: PF6	31: PA2		
US1_CTS	0: PA4	4: PB13	8: PC7	12: PC11	16: PD12	20: PF0	24: PF4	28: PA0	USART1 Clear To Send hardware flow control input.	
	1: PA5	5: PB14	9: PC8	13: PD9	17: PD13	21: PF1	25: PF5	29: PA1		
	2: PB11	6: PB15	10: PC9	14: PD10	18: PD14	22: PF2	26: PF6	30: PA2		
	3: PB12	7: PC6	11: PC10	15: PD11	19: PD15	23: PF3	27: PF7	31: PA3		
US1_RTS	0: PA5	4: PB14	8: PC8	12: PD9	16: PD13	20: PF1	24: PF5	28: PA1	USART1 Request To Send hardware flow control output.	
	1: PB11	5: PB15	9: PC9	13: PD10	17: PD14	21: PF2	25: PF6	29: PA2		
	2: PB12	6: PC6	10: PC10	14: PD11	18: PD15	22: PF3	26: PF7	30: PA3		
	3: PB13	7: PC7	11: PC11	15: PD12	19: PF0	23: PF4	27: PA0	31: PA4		
US1_RX	0: PA1	4: PA5	8: PB14	12: PC8	16: PD9	20: PD13	24: PF1	28: PF5	USART1 Asynchronous Receive.	
	1: PA2	5: PB11	9: PB15	13: PC9	17: PD10	21: PD14	25: PF2	29: PF6	USART1 Synchronous mode Master Input / Slave Output (MISO).	
	2: PA3	6: PB12	10: PC6	14: PC10	18: PD11	22: PD15	26: PF3	30: PF7		
	3: PA4	7: PB13	11: PC7	15: PC11	19: PD12	23: PF0	27: PF4	31: PA0		

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
US1_TX	0: PA0	4: PA4	8: PB13	12: PC7	16: PC11	20: PD12	24: PF0	28: PF4	USART1 Asynchronous Transmit. Also used as receive input in half duplex communication.
	1: PA1	5: PA5	9: PB14	13: PC8	17: PD9	21: PD13	25: PF1	29: PF5	
	2: PA2	6: PB11	10: PB15	14: PC9	18: PD10	22: PD14	26: PF2	30: PF6	
	3: PA3	7: PB12	11: PC6	15: PC10	19: PD11	23: PD15	27: PF3	31: PF7	USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	0: PA7	4: PI1	8: PB7	12: PF0	16: PF5	20: PF9	24: PF13	28: PK1	
	1: PA8	5: PI2	9: PB8	13: PF1	17: PF6	21: PF10	25: PF14	29: PK2	USART2 clock input / output.
	2: PA9	6: PI3	10: PB9	14: PF3	18: PF7	22: PF11	26: PF15	30: PA5	
	3: PI0	7: PB6	11: PB10	15: PF4	19: PF8	23: PF12	27: PK0	31: PA6	
US2_CS	0: PA8	4: PI2	8: PB8	12: PF1	16: PF6	20: PF10	24: PF14	28: PK2	
	1: PA9	5: PI3	9: PB9	13: PF3	17: PF7	21: PF11	25: PF15	29: PA5	USART2 chip select input / output.
	2: PI0	6: PB6	10: PB10	14: PF4	18: PF8	22: PF12	26: PK0	30: PA6	
	3: PI1	7: PB7	11: PF0	15: PF5	19: PF9	23: PF13	27: PK1	31: PA7	
US2_CTS	0: PA9	4: PI3	8: PB9	12: PF3	16: PF7	20: PF11	24: PF15	28: PA5	
	1: PI0	5: PB6	9: PB10	13: PF4	17: PF8	21: PF12	25: PK0	29: PA6	USART2 Clear To Send hardware flow control input.
	2: PI1	6: PB7	10: PF0	14: PF5	18: PF9	22: PF13	26: PK1	30: PA7	
	3: PI2	7: PB8	11: PF1	15: PF6	19: PF10	23: PF14	27: PK2	31: PA8	
US2_RTS	0: PI0	4: PB6	8: PB10	12: PF4	16: PF8	20: PF12	24: PK0	28: PA6	
	1: PI1	5: PB7	9: PF0	13: PF5	17: PF9	21: PF13	25: PK1	29: PA7	USART2 Request To Send hardware flow control output.
	2: PI2	6: PB8	10: PF1	14: PF6	18: PF10	22: PF14	26: PK2	30: PA8	
	3: PI3	7: PB9	11: PF3	15: PF7	19: PF11	23: PF15	27: PA5	31: PA9	
US2_RX	0: PA6	4: PI0	8: PB6	12: PB10	16: PF4	20: PF8	24: PF12	28: PK0	USART2 Asynchronous Receive.
	1: PA7	5: PI1	9: PB7	13: PF0	17: PF5	21: PF9	25: PF13	29: PK1	
	2: PA8	6: PI2	10: PB8	14: PF1	18: PF6	22: PF10	26: PF14	30: PK2	USART2 Synchronous mode Master Input / Slave Output (MISO).
	3: PA9	7: PI3	11: PB9	15: PF3	19: PF7	23: PF11	27: PF15	31: PA5	
US2_TX	0: PA5	4: PA9	8: PI3	12: PB9	16: PF3	20: PF7	24: PF11	28: PF15	USART2 Asynchronous Transmit. Also used as receive input in half duplex communication.
	1: PA6	5: PI0	9: PB6	13: PB10	17: PF4	21: PF8	25: PF12	29: PK0	
	2: PA7	6: PI1	10: PB7	14: PF0	18: PF5	22: PF9	26: PF13	30: PK1	USART2 Synchronous mode Master Output / Slave Input (MOSI).
	3: PA8	7: PI2	11: PB8	15: PF1	19: PF6	23: PF10	27: PF14	31: PK2	

Alternate	LOCATION									
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description	
US3_CLK	0: PD10	4: PD14	8: PB6	12: PB10	16: PC0	20: PC4	24: PF13	28: PK1	USART3 clock input / output.	
	1: PD11	5: PD15	9: PB7	13: PB11	17: PC1	21: PC5	25: PF14	29: PK2		
	2: PD12	6: PI2	10: PB8	14: PJ14	18: PC2	22: PF11	26: PF15	30: PD8		
	3: PD13	7: PI3	11: PB9	15: PJ15	19: PC3	23: PF12	27: PK0	31: PD9		
US3_CS	0: PD11	4: PD15	8: PB7	12: PB11	16: PC1	20: PC5	24: PF14	28: PK2	USART3 chip select input / output.	
	1: PD12	5: PI2	9: PB8	13: PJ14	17: PC2	21: PF11	25: PF15	29: PD8		
	2: PD13	6: PI3	10: PB9	14: PJ15	18: PC3	22: PF12	26: PK0	30: PD9		
	3: PD14	7: PB6	11: PB10	15: PC0	19: PC4	23: PF13	27: PK1	31: PD10		
US3_CTS	0: PD12	4: PI2	8: PB8	12: PJ14	16: PC2	20: PF11	24: PF15	28: PD8	USART3 Clear To Send hardware flow control input.	
	1: PD13	5: PI3	9: PB9	13: PJ15	17: PC3	21: PF12	25: PK0	29: PD9		
	2: PD14	6: PB6	10: PB10	14: PC0	18: PC4	22: PF13	26: PK1	30: PD10		
	3: PD15	7: PB7	11: PB11	15: PC1	19: PC5	23: PF14	27: PK2	31: PD11		
US3 RTS	0: PD13	4: PI3	8: PB9	12: PJ15	16: PC3	20: PF12	24: PK0	28: PD9	USART3 Request To Send hardware flow control output.	
	1: PD14	5: PB6	9: PB10	13: PC0	17: PC4	21: PF13	25: PK1	29: PD10		
	2: PD15	6: PB7	10: PB11	14: PC1	18: PC5	22: PF14	26: PK2	30: PD11		
	3: PI2	7: PB8	11: PJ14	15: PC2	19: PF11	23: PF15	27: PD8	31: PD12		
US3_RX	0: PD9	4: PD13	8: PI3	12: PB9	16: PJ15	20: PC3	24: PF12	28: PK0	USART3 Asynchronous Receive.	
	1: PD10	5: PD14	9: PB6	13: PB10	17: PC0	21: PC4	25: PF13	29: PK1	USART3 Synchronous mode Master Input / Slave Output (MISO).	
	2: PD11	6: PD15	10: PB7	14: PB11	18: PC1	22: PC5	26: PF14	30: PK2		
	3: PD12	7: PI2	11: PB8	15: PJ14	19: PC2	23: PF11	27: PF15	31: PD8		
US3_TX	0: PD8	4: PD12	8: PI2	12: PB8	16: PJ14	20: PC2	24: PF11	28: PF15	USART3 Asynchronous Transmit. Also used as receive input in half duplex communication.	
	1: PD9	5: PD13	9: PI3	13: PB9	17: PJ15	21: PC3	25: PF12	29: PK0		
	2: PD10	6: PD14	10: PB6	14: PB10	18: PC0	22: PC4	26: PF13	30: PK1		
	3: PD11	7: PD15	11: PB7	15: PB11	19: PC1	23: PC5	27: PF14	31: PK2		
VDAC0_EXT	0: PA1								Digital to analog converter VDAC0 external reference input pin.	
VDAC0_OUT0 / OPA0_OUT	0: PA3								Digital to Analog Converter DAC0 output channel number 0.	
VDAC0_OUT0ALT / OPA0_OUT-ALT	0: PA5								Digital to Analog Converter DAC0 alternative output for channel 0.	

Alternate	LOCATION									
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description	
VDAC0_OUT1 / OPA1_OUT	0: PD14								Digital to Analog Converter DAC0 output channel number 1.	
VDAC0_OUT1ALT / OPA1_OUT-ALT	0: PD12 1: PA2 2: PA4								Digital to Analog Converter DAC0 alternative output for channel 1.	
WTIM0_CC0	0: PA0	4: PA4	8: PA8	12: PB8	16: PB12	20: PC0	24: PC4	28: PC8	Wide timer 0 Capture Compare input / output channel 0.	
	1: PA1	5: PA5	9: PA9	13: PB9	17: PB13	21: PC1	25: PC5	29: PC9		
	2: PA2	6: PA6	10: PB6	14: PB10	18: PB14	22: PC2	26: PC6	30: PC10		
	3: PA3	7: PA7	11: PB7	15: PB11	19: PB15	23: PC3	27: PC7	31: PC11		
WTIM0_CC1	0: PA2	4: PA6	8: PB6	12: PB10	16: PB14	20: PC2	24: PC6	28: PC10	Wide timer 0 Capture Compare input / output channel 1.	
	1: PA3	5: PA7	9: PB7	13: PB11	17: PB15	21: PC3	25: PC7	29: PC11		
	2: PA4	6: PA8	10: PB8	14: PB12	18: PC0	22: PC4	26: PC8	30: PD8		
	3: PA5	7: PA9	11: PB9	15: PB13	19: PC1	23: PC5	27: PC9	31: PD9		
WTIM0_CC2	0: PA4	4: PA8	8: PB8	12: PB12	16: PC0	20: PC4	24: PC8	28: PD8	Wide timer 0 Capture Compare input / output channel 2.	
	1: PA5	5: PA9	9: PB9	13: PB13	17: PC1	21: PC5	25: PC9	29: PD9		
	2: PA6	6: PB6	10: PB10	14: PB14	18: PC2	22: PC6	26: PC10	30: PD10		
	3: PA7	7: PB7	11: PB11	15: PB15	19: PC3	23: PC7	27: PC11	31: PD11		
WTIM0_CDTI0	0: PA8	4: PB8	8: PB12	12: PC0	16: PC4	20: PC8	24: PD8	28: PD12	Wide timer 0 Complimentary Dead Time Insertion channel 0.	
	1: PA9	5: PB9	9: PB13	13: PC1	17: PC5	21: PC9	25: PD9	29: PD13		
	2: PB6	6: PB10	10: PB14	14: PC2	18: PC6	22: PC10	26: PD10	30: PD14		
	3: PB7	7: PB11	11: PB15	15: PC3	19: PC7	23: PC11	27: PD11	31: PD15		
WTIM0_CDTI1	0: PB6	4: PB10	8: PB14	12: PC2	16: PC6	20: PC10	24: PD10	28: PD14	Wide timer 0 Complimentary Dead Time Insertion channel 1.	
	1: PB7	5: PB11	9: PB15	13: PC3	17: PC7	21: PC11	25: PD11	29: PD15		
	2: PB8	6: PB12	10: PC0	14: PC4	18: PC8	22: PD8	26: PD12	30: PF0		
	3: PB9	7: PB13	11: PC1	15: PC5	19: PC9	23: PD9	27: PD13	31: PF1		
WTIM0_CDTI2	0: PB8	4: PB12	8: PC0	12: PC4	16: PC8	20: PD8	24: PD12	28: PF0	Wide timer 0 Complimentary Dead Time Insertion channel 2.	
	1: PB9	5: PB13	9: PC1	13: PC5	17: PC9	21: PD9	25: PD13	29: PF1		
	2: PB10	6: PB14	10: PC2	14: PC6	18: PC10	22: PD10	26: PD14	30: PF2		
	3: PB11	7: PB15	11: PC3	15: PC7	19: PC11	23: PD11	27: PD15	31: PF3		
WTIM1_CC0	0: PB12	4: PC0	8: PC4	12: PC8	16: PD8	20: PD12	24: PF0	28: PF4	Wide timer 1 Capture Compare input / output channel 0.	
	1: PB13	5: PC1	9: PC5	13: PC9	17: PD9	21: PD13	25: PF1	29: PF5		
	2: PB14	6: PC2	10: PC6	14: PC10	18: PD10	22: PD14	26: PF2	30: PF6		
	3: PB15	7: PC3	11: PC7	15: PC11	19: PD11	23: PD15	27: PF3	31: PF7		

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
WTIM1_CC1	0: PB14	4: PC2	8: PC6	12: PC10	16: PD10	20: PD14	24: PF2	28: PF6	Wide timer 1 Capture Compare input / output channel 1.
	1: PB15	5: PC3	9: PC7	13: PC11	17: PD11	21: PD15	25: PF3	29: PF7	
	2: PC0	6: PC4	10: PC8	14: PD8	18: PD12	22: PF0	26: PF4	30: PF8	
	3: PC1	7: PC5	11: PC9	15: PD9	19: PD13	23: PF1	27: PF5	31: PF9	
WTIM1_CC2	0: PC0	4: PC4	8: PC8	12: PD8	16: PD12	20: PF0	24: PF4	28: PF8	Wide timer 1 Capture Compare input / output channel 2.
	1: PC1	5: PC5	9: PC9	13: PD9	17: PD13	21: PF1	25: PF5	29: PF9	
	2: PC2	6: PC6	10: PC10	14: PD10	18: PD14	22: PF2	26: PF6	30: PF10	
	3: PC3	7: PC7	11: PC11	15: PD11	19: PD15	23: PF3	27: PF7	31: PF11	
WTIM1_CC3	0: PC2	4: PC6	8: PC10	12: PD10	16: PD14	20: PF2	24: PF6	28: PF10	Wide timer 1 Capture Compare input / output channel 3.
	1: PC3	5: PC7	9: PC11	13: PD11	17: PD15	21: PF3	25: PF7	29: PF11	
	2: PC4	6: PC8	10: PD8	14: PD12	18: PF0	22: PF4	26: PF8	30: PF12	
	3: PC5	7: PC9	11: PD9	15: PD13	19: PF1	23: PF5	27: PF9	31: PF13	

6.11 Analog Port (APORT) Client Maps

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, DACs, etc. The APORT consists of a set of shared buses, switches, and control logic needed to configurally implement the signal routing. [Figure 6.9 APORT Connection Diagram on page 199](#) shows the APORT routing for this device family (note that available features may vary by part number). A complete description of APORT functionality can be found in the Reference Manual.

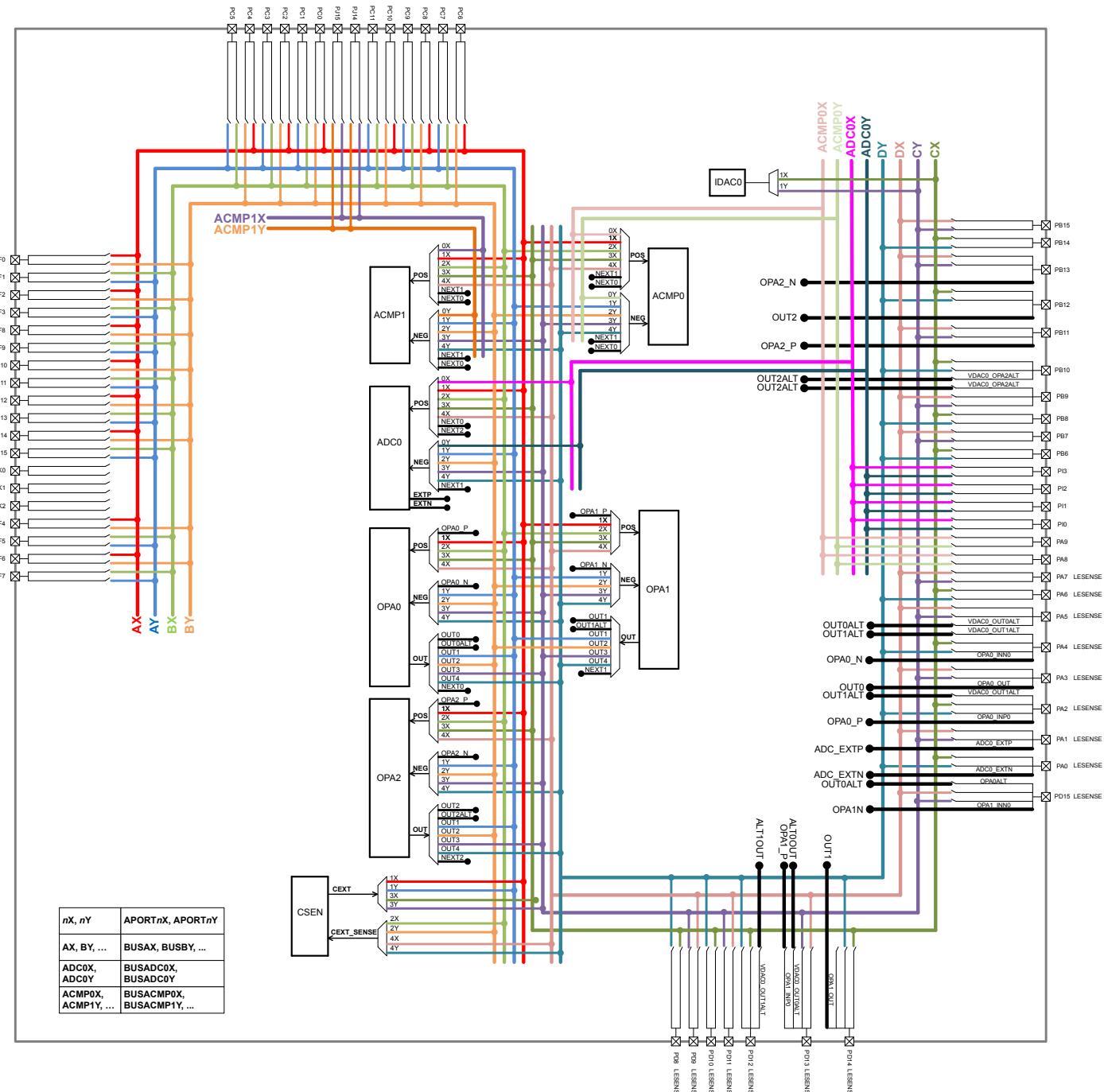


Figure 6.9. APORT Connection Diagram

Client maps for each analog circuit using the APORT are shown in the following tables. The maps are organized by bus, and show the peripheral's port connection, the shared bus, and the connection from specific bus channel numbers to GPIO pins.

In general, enumerations for the pin selection field in an analog peripheral's register can be determined by finding the desired pin connection in the table and then combining the value in the Port column (APORT $_{_}$), and the channel identifier (CH $_{_}$). For example, if pin

PF7 is available on port APOR2X as CH23, the register field enumeration to connect to PF7 would be APOR2XCH23. The shared bus used by this connection is indicated in the Bus column.

Table 6.11. ACMP0 Bus and Pin Mapping

Table 6.12. ACMP1 Bus and Pin Mapping

APORT4Y	APORT4X	APORT3Y	APORT3X	APORT2Y	APORT2X	APORT1Y	APORT1X	APORT0Y	APORT0X	Port
BUSDY	BUSDX	BUSCY	BUSCX	BUSBY	BUSBX	BUSAY	BUSAX	BUSACMP1Y	BUSACMP1X	Bus
PB15	PB15			PF15						CH31
PB14		PB14	PF14			PF14				CH30
PB13	PB13			PF13	PF13					CH29
PB12		PB12	PF12			PF12				CH28
PB11	PB11			PF11	PF11					CH27
PB10		PB10	PF10			PF10				CH26
PB8	PB9	PB9		PF9	PF9	PF9				CH25
PB7	PB7	PB8	PF8			PF8				CH24
PB6		PB6	PF6		PF7	PF7				CH23
PB5				PF5	PF5	PF5	PF6			CH22
PB4				PF4		PF4	PF4			CH21
PB3				PF3	PF3	PF3	PF2			CH20
PB2				PF2		PF1	PF1			CH19
PB1				PF0			PF0			CH18
PA7	PA7									CH17
PA6		PA6								CH16
PA5	PA5									CH15
PA4		PA4								CH14
PA3	PA3				PC11	PC11				CH13
PA2		PA2	PC10				PC10			CH12
PA1	PA1			PC9	PC9	PC9				CH11
PA0		PA0	PC8			PC8				CH10
PD15	PD15			PC7	PC7	PC7				CH9
PD14		PD14	PC6			PC6		PJ15	PJ15	CH8
PD13	PD13			PC5	PC5	PC5		PJ14	PJ14	CH7
PD12		PD12	PC4			PC4				CH6
PD11	PD11			PC3	PC3	PC3				CH5
PD10		PD10	PC2			PC2				CH4
PD9	PD9			PC1	PC1	PC1				CH3
PD8		PD8	PC0			PC0				CH2
										CH1
										CH0

Table 6.13. ADC0 Bus and Pin Mapping

APORT4Y	APORT4X	APORT3Y	APORT3X	APORT2Y	APORT2X	APORT1Y	APORT1X	APORT0Y	APORT0X	Port
BUSDY	BUSDX	BUSCY	BUSCX	BUSBY	BUSBX	BUSAY	BUSAX	BUSADC0Y	BUSADC0X	Bus
PB15	PB15			PF15	PF15					CH31
PB14	PB13	PB13	PB14	PF14		PF14				CH30
PB12	PB11	PB11	PB12	PF12		PF13				CH29
PB10	PB9	PB9	PB10	PF10		PF11				CH28
PB8	PB7	PB7	PB8	PF8		PF9				CH27
PB6			PB6	PF6		PF7				CH26
				PF4		PF5				CH25
				PF2		PF3				CH24
				PF0		PF1				CH23
						PF1				CH22
						PF0				CH21
							PF4			CH20
							PF3			CH19
							PF2			CH18
							PF1			CH17
							PF0			CH16
										CH15
PA6	PA7	PA7	PA6							CH14
PA5	PA5		PA5							CH13
PA4	PA3	PA3	PA4							CH12
PA2	PA1	PA1	PA2	PC10		PC11	PC11			CH11
PA0	PD15	PD15	PA0	PC8		PC9	PC9			CH10
PD14	PD13	PD13	PD14	PC6		PC7	PC7			CH9
PD12	PD11	PD11	PD12	PC4		PC5	PC5			CH8
PD10	PD9	PD9	PD10	PC2		PC3	PC3			CH7
PD8			PD8	PC0		PC1	PC1			CH6
						PC0	PC0			CH5
							PC4			CH4
							PC2	PC2		CH3
							PC1	PC1		CH2
							PC0	PC0		CH1
								PI0	PI0	CH0

Table 6.14. CSEN Bus and Pin Mapping

Port	CEXT	CEXT_SENSE	CEXT	Port
APORT1Y	APORT1X		APORT4Y	APORT4X
BUSCY	BUSCX	Bus	BUSDY	BUSBX
PB15	CH31		PB15	PF15
PB14	CH30		PB14	PF14
PB13	CH29		PB13	PF13
PB11	CH28		PB12	PF12
PB10	CH27		PB11	PF11
PB9	CH26		PB10	PF10
PB8	CH25		PB9	PF9
PB7	CH24		PB8	PF8
PB6	CH23		PB7	PF7
PB6	CH22		PB6	PF6
	CH21		PB5	PF5
	CH20		PB4	PF4
	CH19		PB3	PF3
	CH18		PB2	PF2
	CH17		PB1	PF1
	CH16		PF0	PF0
	CH15		PA7	
PA7	CH14		PA6	PA6
PA5	CH13		PA5	
PA4	CH12		PA4	
PA3	CH11		PA3	PC11
PA2	CH10		PA2	PC10
PA1	CH9		PA1	PC9
PA0	CH8		PA0	PC8
PD15	CH7		PD15	PC7
PD14	CH6		PD14	PC6
PD13	CH5		PD13	PC5
PD12	CH4		PD12	PC4
PD11	CH3		PD11	PC3
PD10	CH2		PD10	PC2
PD9	CH1		PD9	PC1
PD8	CH0		PD8	PC0

Table 6.15. IDAC0 Bus and Pin Mapping

PA6	CH14	PA5	PA5	PA6	CH14
PA4	CH12	PA4	PA4	PA4	CH12
PA3	CH11	PA3	PA3	PA3	CH11
PA2	CH10	PA2	PA2	PA2	CH10
PA1	CH9	PA1	PA1	PA1	CH9
PA0	CH8	PA0	PA0	PA0	CH8
PD15	CH7	PD15	PC7	PD15	CH7
PD14	CH6	PD14	PC6	PD14	CH6
PD13	CH5	PD13	PC5	PD13	CH5
PD12	CH4	PD12	PC4	PD12	CH4
PD11	CH3	PD11	PC3	PD11	CH3
PD10	CH2	PD10	PC2	PD10	CH2
PD9	CH1	PD9	PC1	PD9	CH1
PD8	CH0	PD8	PC0	PD8	CH0

Table 6.16. VDAC0 / OPA Bus and Pin Mapping

APORT4Y	APORT3Y	APORT2Y	APORT1Y	APORT1X	APORT3X	APORT2X	APORT1X	APORT4Y	APORT3Y	APORT2Y	APORT1Y	Port
BUSDY	BUSCY	BUSBY	BUSAY	BUSDX	BUSCX	BUSBX	BUSAX	BUSDY	BUSCY	BUSBY	BUSAY	Bus
PB15		PF15		PB15		PF15		PB15		PF15		CH31
PB14		PF14		PB14		PF14		PB14		PF14		CH30
PB13		PF13		PB13		PF13		PB13		PF13		CH29
PB12		PF12		PB12		PF12		PB12		PF12		CH28
PB11		PF11		PB11		PF11		PB11		PF11		CH27
PB10		PF10		PB10		PF10		PB10		PF10		CH26
PB9		PF9		PB9		PF9		PB9		PF9		CH25
PB8		PF8		PB8		PF8		PB8		PF8		CH24
PB7		PF7		PB7		PF7		PB7		PF7		CH23
PB6		PF6		PB6		PF6		PB6		PF6		CH22
		PF5				PF5				PF5		CH21
		PF4				PF4				PF4		CH20
		PF3				PF3				PF3		CH19
		PF2				PF2				PF2		CH18
		PF1				PF1				PF1		CH17
		PF0				PF0				PF0		CH16
		PA7				PA7				PA7		CH15
PA6		PA5				PA6				PA6		CH14
PA4		PA3				PA4				PA5		CH13
PA2		PC10				PA3		PC11		PA4		CH12
PA1		PC9				PA2		PC10		PA3		CH11
PA0		PC8				PA1		PC9		PA2		CH10
PD14		PC6				PD15		PC7		PA1		CH9
PD13		PC5				PD14		PC6		PA0		CH8
PD12		PC4				PD13		PC5		PD15		CH7
PD11		PC3				PD12		PC4		PD13		CH6
PD10		PC2				PD11		PC3		PD12		CH5
PD9		PC1				PD10		PC2		PD11		CH4
PD8		PC0				PD9		PC1		PD10		CH3
						PD8		PC0		PD9		CH2
										PD8		CH1
										PD8		CH0

APORT4Y	APORT3Y	APORT2Y	APORT1Y	APORT14X	APORT3X	APORT2X	APORT1X	APORT4Y	APORT3Y	APORT2Y	APORT1Y	Port
BUSDY	BUSCY	BUSBY	BUSAY	BUSDX	BUSCX	BUSBX	BUSAX	BUSDY	BUSCY	BUSBY	BUSAY	Bus
PB15		PF15		PB15		PF15		PB15		PF15		CH31
PB14		PF14		PB14		PF14		PB14		PF14		CH30
PB13		PF13		PB13		PF13		PB13		PF13		CH29
PB12		PF12		PB12		PF12		PB12		PF12		CH28
PB11		PF11		PB11		PF11		PB11		PF11		CH27
PB10		PF10		PB10		PF10		PB10		PF10		CH26
PB9		PF9		PB9		PF9		PB9		PF9		CH25
PB8		PF8		PB8		PF8		PB8		PF8		CH24
PB7		PF7		PB7		PF7		PB7		PF7		CH23
PB6		PF6		PB6		PF6		PB6		PF6		CH22
		PF5				PF5				PF5		CH21
		PF4				PF4				PF4		CH20
		PF3				PF3				PF3		CH19
		PF2				PF2				PF2		CH18
		PF1				PF1				PF1		CH17
		PF0				PF0				PF0		CH16
		PA7				PA7				PA7		CH15
PA6		PA5				PA6				PA6		CH14
PA4		PA3				PA4				PA5		CH13
PA2		PC10				PA3		PC11		PA4		CH12
PA1		PC9				PA2		PC10		PA3		CH11
PA0		PC8				PA1		PC9		PA2		CH10
PD14		PC6				PD15		PC7		PA1		CH9
PD13		PC5				PD14		PC6		PA0		CH8
PD12		PC4				PD13		PC5		PD15		CH7
PD11		PC3				PD12		PC4		PD13		CH6
PD10		PC2				PD11		PC3		PD12		CH5
PD9		PC1				PD10		PC2		PD11		CH4
PD8		PC0				PD9		PC1		PD10		CH3
						PD8		PC0		PD9		CH2
										PD8		CH1
										PD8		CH0

					Port
VDAC0_OUT1 / OPA1_OUT					
APORT4Y	APORT3Y	APORT2Y	APORT1Y		Bus
BUSDY	BUSCY	BUSBY	BUSAY		CH31
	PB15		PF15		CH30
PB14		PF14			CH29
PB12		PF12			CH28
PB11		PF11			CH27
PB10		PF10			CH26
PB8	PB9	PF9			CH25
PB7	PB8	PF8			CH24
PB6	PB7	PF7			CH23
PB6		PF6			CH22
		PF5			CH21
		PF4			CH20
			PF3		CH19
			PF2		CH18
			PF1		CH17
			PF0		CH16
			PA7		CH15
PA6					CH14
PA4	PA5				CH13
PA4					CH12
PA2	PA3	PC11			CH11
PA0		PC10			CH10
PD14		PA1	PC9		CH9
PD12		PD15	PC8		CH8
PD10			PC7		CH7
PD8				PC6	CH6
				PD13	CH5
				PD11	CH4
				PC2	CH3
				PD9	CH2
				PC0	CH1
					CH0

7. BGA125 Package Specifications

7.1 BGA125 Package Dimensions

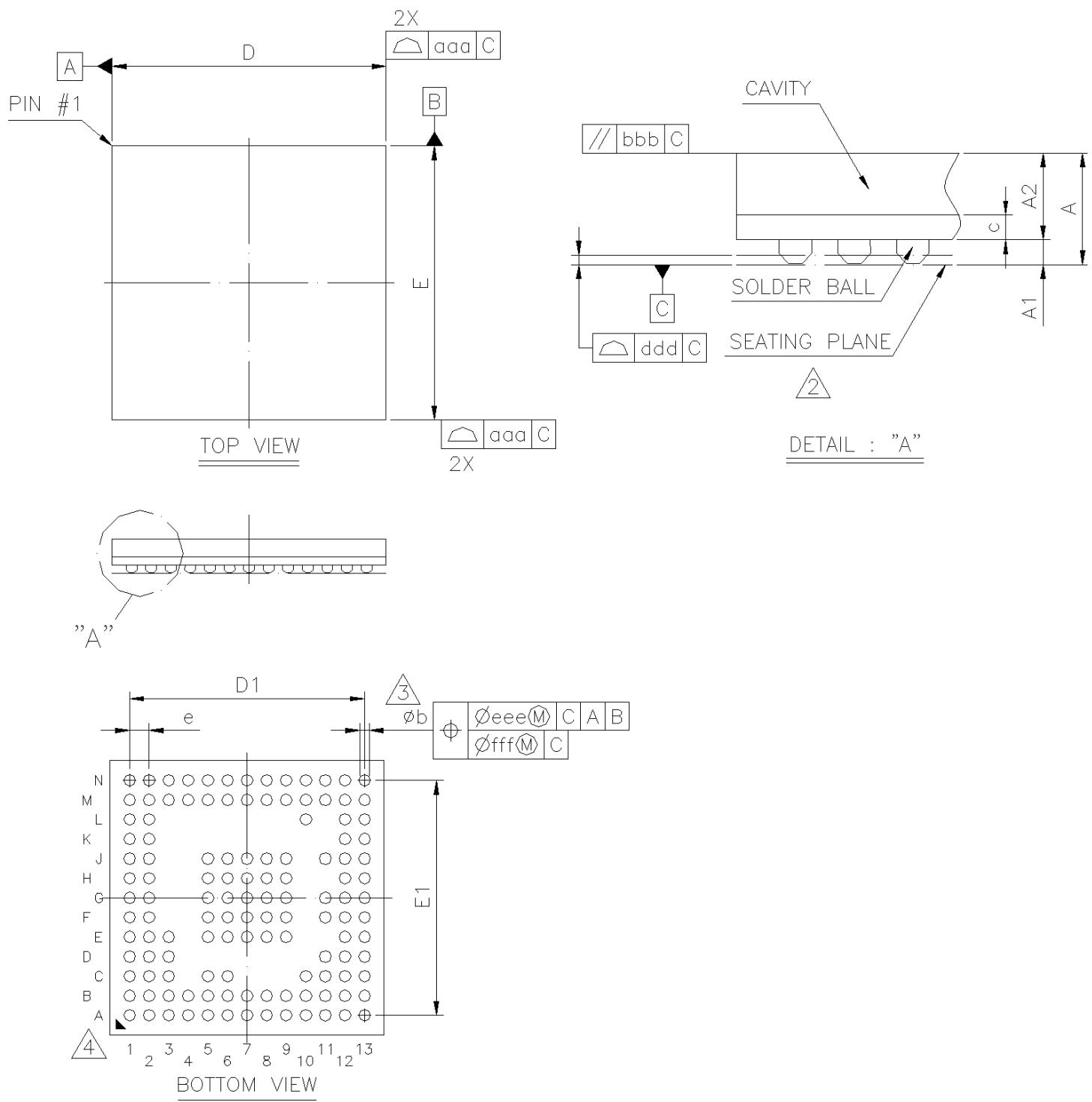


Figure 7.1. BGA125 Package Drawing

Table 7.1. BGA125 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.87	0.94
A1	0.16	0.21	0.26
A2	0.61	0.66	0.71
c	0.17	0.21	0.25
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D1	—	6.00	—
E1	—	6.00	—
e	—	0.50	—
b	0.25	0.30	0.35
aaa		0.10	
bbb		0.10	
ddd		0.08	
eee		0.15	
fff		0.05	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

7.2 BGA125 PCB Land Pattern

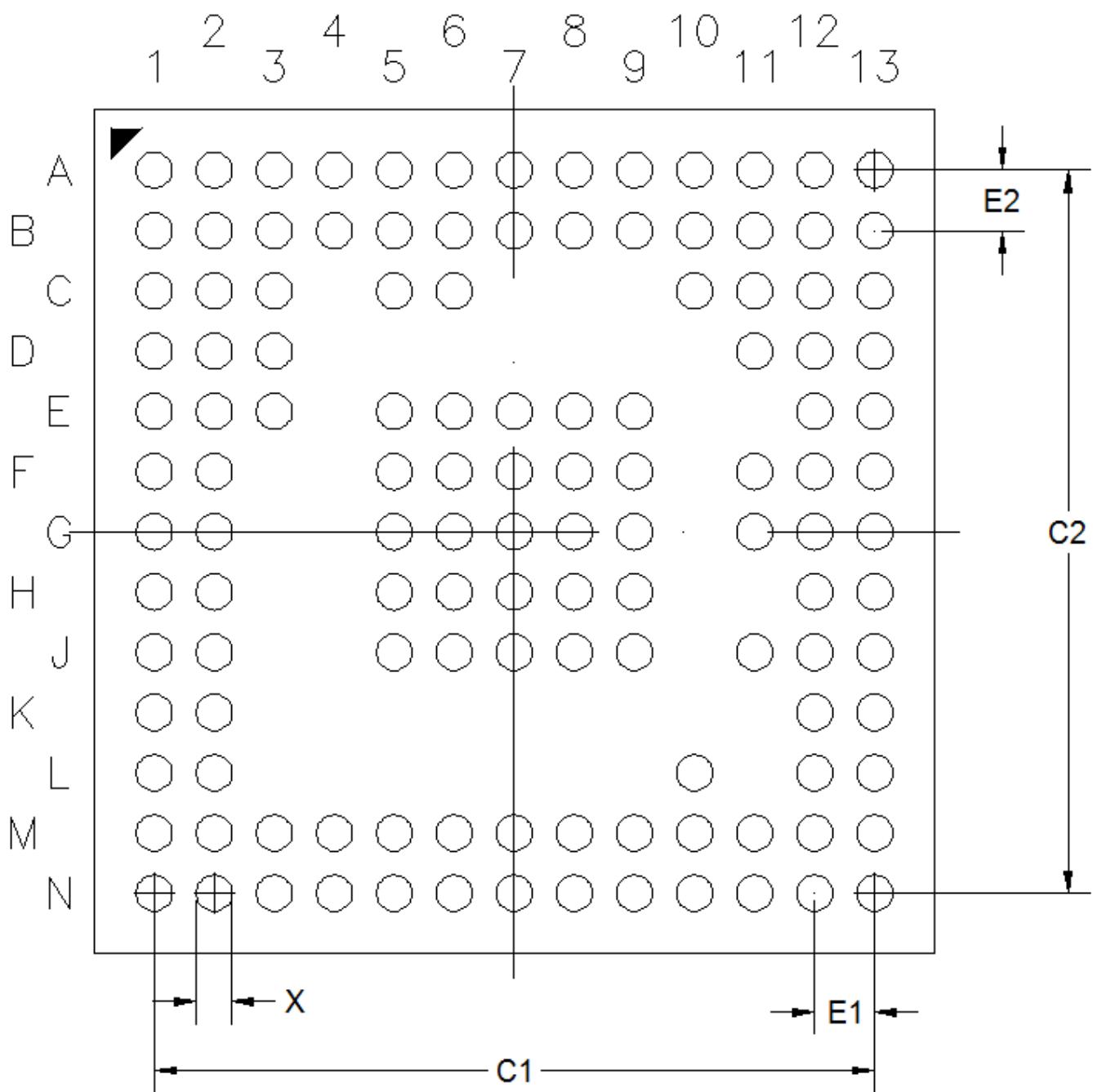


Figure 7.2. BGA125 PCB Land Pattern Drawing

Table 7.2. BGA125 PCB Land Pattern Dimensions

Dimension	Min	Nom	Max
X		0.25	
C1		6.00	
C2		6.00	
E1		0.5	
E2		0.5	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7.3 BGA125 Package Marking



Figure 7.3. BGA125 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
 1. Family Code (B | M | F)
 2. G (Gecko)
 3. Series (1, 2,...)
 4. Device Configuration (1, 2,...)
 5. Performance Grade (P | B | V)
 6. Feature Code (1, 2,...)
 7. TRX Code (3 = TXRX | 2 = RX | 1 = TX)
 8. Band (1 = Sub-GHz | 2 = 2.4 GHz | 3 = Dual-band)
 9. Flash (J = 1024K | H = 512K | G = 256K | F = 128K | E = 64K | D = 32K)
 10. Temperature Grade (G = -40 to 85 | I = -40 to 125)
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.

8. QFN48 Package Specifications

8.1 QFN48 Package Dimensions

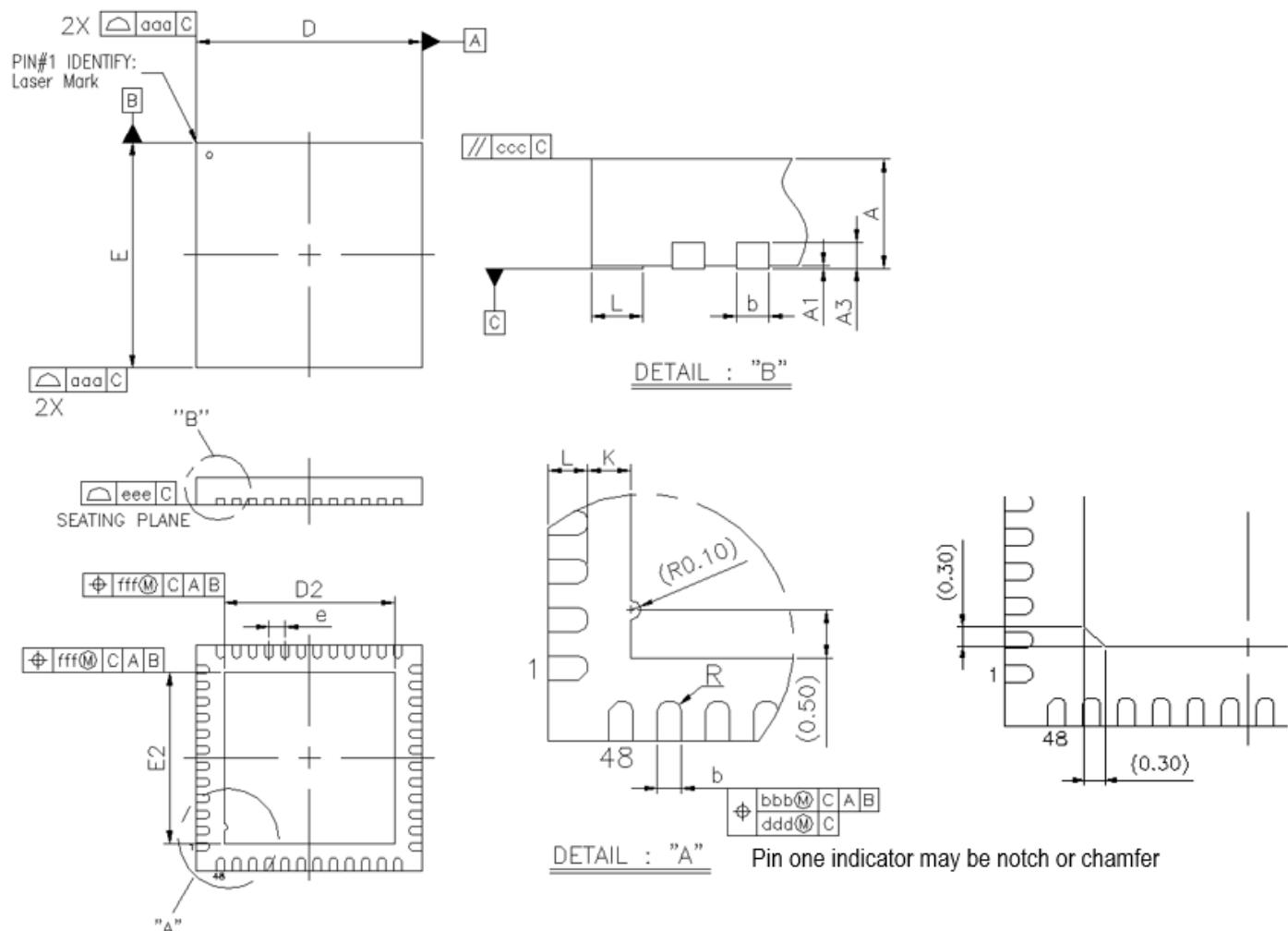


Figure 8.1. QFN48 Package Drawing

Table 8.1. QFN48 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.18	0.25	0.30
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	5.15	5.30	5.45
E2	5.15	5.30	5.45
e	0.50 BSC		
L	0.30	0.40	0.50
K	0.20	—	—
R	0.09	—	—
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2 QFN48 PCB Land Pattern

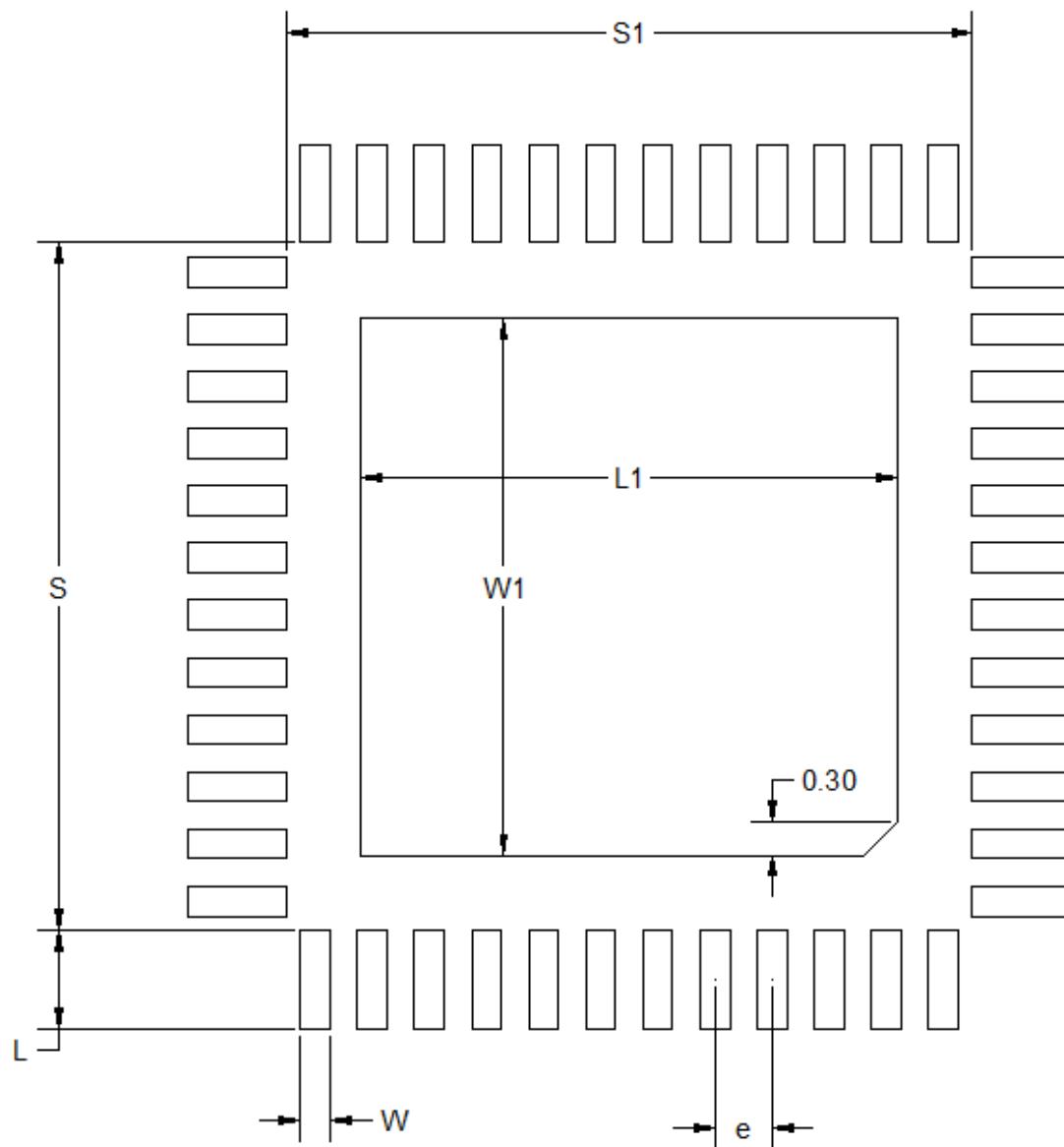


Figure 8.2. QFN48 PCB Land Pattern Drawing

Table 8.2. QFN48 PCB Land Pattern Dimensions

Dimension	Typ
S1	6.01
S	6.01
L1	4.70
W1	4.70
e	0.50
W	0.26
L	0.86

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
7. A 4x4 array of 0.75 mm square openings on a 1.00 mm pitch can be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.3 QFN48 Package Marking



Figure 8.3. QFN48 Package Marking

The package marking consists of:

- PPPPPPPP – The part number designation.
 1. Family Code (B | M | F)
 2. G (Gecko)
 3. Series (1, 2,...)
 4. Device Configuration (1, 2,...)
 5. Performance Grade (P | B | V)
 6. Feature Code (1, 2,...)
 7. TRX Code (3 = TXRX | 2 = RX | 1 = TX)
 8. Band (1 = Sub-GHz | 2 = 2.4 GHz | 3 = Dual-band)
 9. Flash (J = 1024K | H = 512K | G = 256K | F = 128K | E = 64K | D = 32K)
 10. Temperature Grade (G = -40 to 85 | I = -40 to 125)
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.

9. QFN68 Package Specifications

9.1 QFN68 Package Dimensions

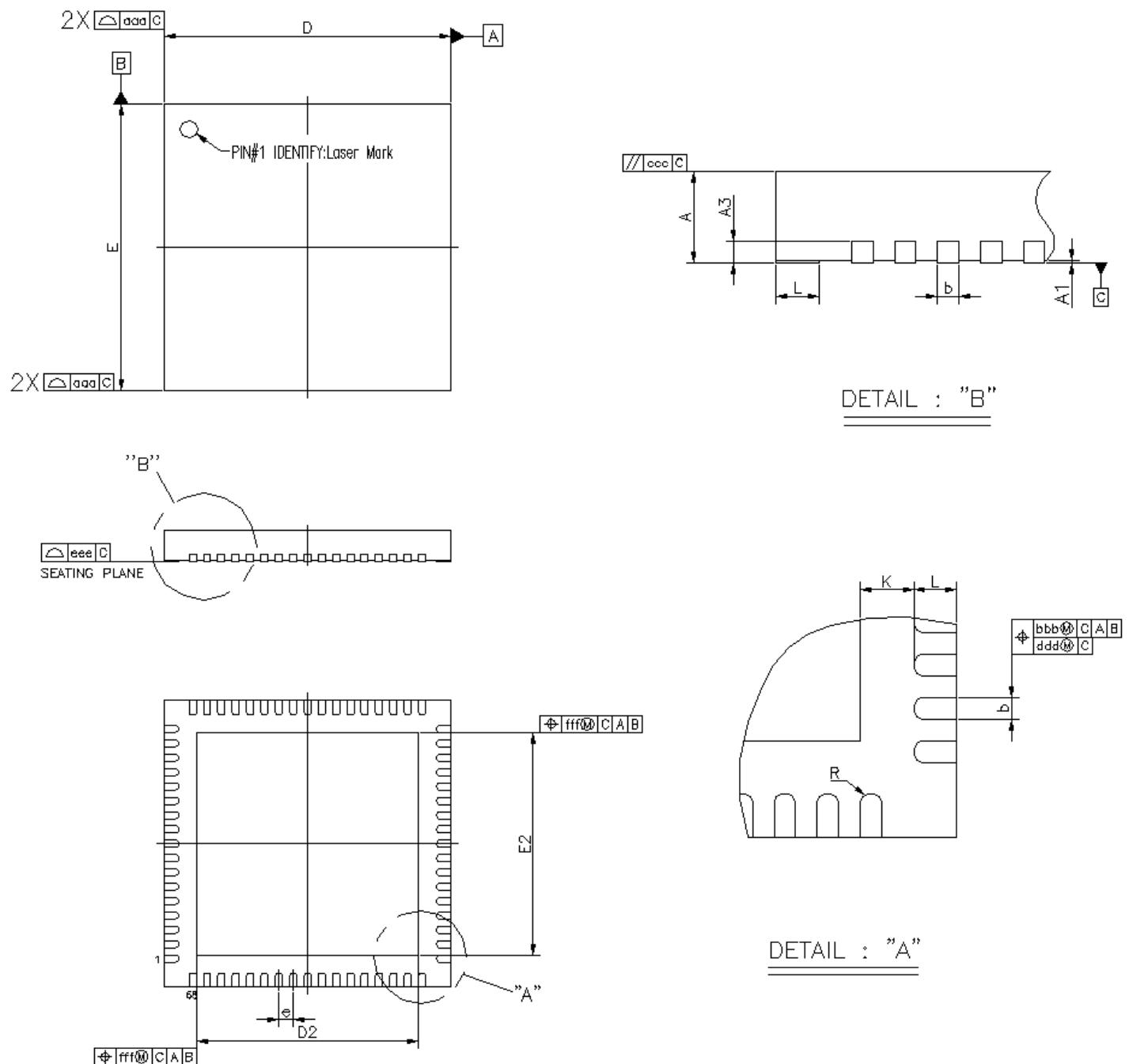


Figure 9.1. QFN68 Package Drawing

Table 9.1. QFN68 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.15	0.20	0.25
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	6.05	6.20	6.35
E2	6.05	6.20	6.35
e	0.40 BSC		
L	0.30	0.40	0.50
K	0.20	—	—
R	0.075	—	—
aaa	0.10		
bbb	0.07		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.2 QFN68 PCB Land Pattern

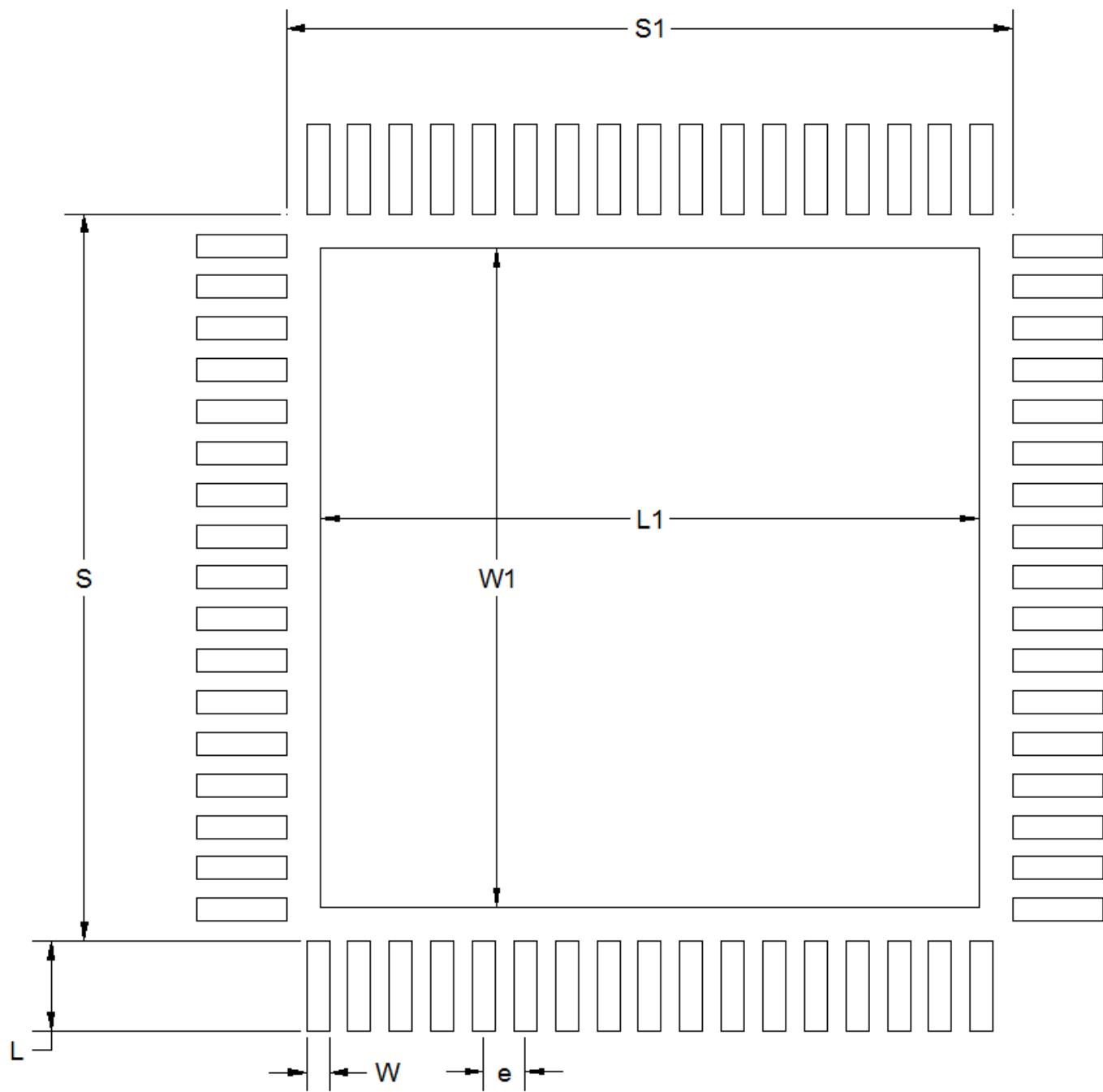


Figure 9.2. QFN68 PCB Land Pattern Drawing

Table 9.2. QFN68 PCB Land Pattern Dimensions

Dimension	Typ
L	0.86
W	0.22
e	0.40
S	7.01
S1	7.01
L1	6.35
W1	6.35

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.100 mm (4 mils).
7. The ratio of stencil aperture to land pad size can be 1:1 for all pads.
8. A 3x3 array of 1.50 mm square openings on a 1.80 mm pitch can be used for the center ground pad.
9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.3 QFN68 Package Marking

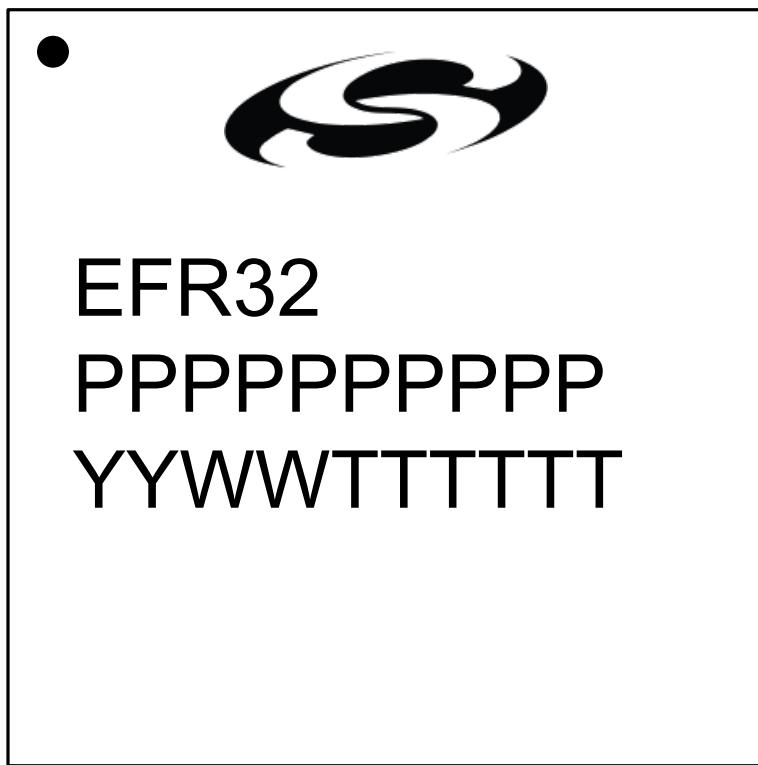


Figure 9.3. QFN68 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

10. Revision History

Revision 1.5

December, 2019

- In the front page block diagram, updated the lowest energy mode for LETIMER.
- Updated [3.6.4 Low Energy Timer \(LETIMER\)](#) lowest energy mode.
- In [5.2 RF Matching Networks](#), corrected document references for component values and added document reference to IPD solutions.
- Corrected the max value of the Absolute voltage on 2G4RF_IOP, 2G4RF_ION, SUBGRF_OP and SUBGRF_ON pins in Absolute Maximum Ratings table in [4.1.1 Absolute Maximum Ratings](#).
- Added a Note about the operating voltage in [3.8.3 True Random Number Generator \(TRNG\)](#).

Revision 1.4

July, 2019

- In Feature List, removed wake on radio.
- In System Overview:
 - Replaced reference to "modules" with "peripherals" or "blocks"
 - Renamed GPCRC section
- In Electrical Specifications, reordered footnotes according to order of appearance in the table.
- In General Operating Conditions for f_{CORE} :
 - Added conditions for all usable wait state settings
 - Corrected maximum specification from 20 MHz to 7 MHz for test condition VSCALE0, MODE = WS0
- In sub-GHz specifications, replaced references to "PAVDD" with "External PA Supply" for clarity.
- In RF Transmitter Characteristics for 802.15.4 DSSS-OQPSK in the 2.4GHz Band, updated parameter for EVM.
- In Sub-GHz RF Transmitter characteristics for 915 MHz Band:
 - Corrected test conditions for:
 - $SPUR_{HARM_FCC_14}$, in non-restricted bands
 - $SPUR_{OOB_FCC_14}$, in non-restricted bands
 - $SPUR_{HARM_FCC_20}$, in non-restricted bands
 - $SPUR_{OOB_FCC_20}$, in non-restricted bands
 - Updated typical specification from -52 dBm to -62 dBm and maximum specification from -46 dBm to -56 dBm for:
 - $SPUR_{OOB_FCC_20}$, in restricted bands (30-88 MHz)
 - $SPUR_{OOB_FCC_14}$, in restricted bands (30-88 MHz)
 - Added footnote to PSD.
- In [4.1.10.2 Sub-GHz RF Receiver Characteristics for 915 MHz Band](#), updated typical specification from -60 dBm to -61 dBm and maximum specification from -54 dBm to -55 dBm for $SPUR_{RX_ARIB}$, 930-1000 MHz, RBW=100 kHz.
- Corrected units for F_{RANGE} in:
 - Sub-GHz RF Receiver Characteristics for 490 MHz Band
 - Sub-GHz RF Receiver Characteristics for 315 MHz Band
 - Sub-GHz RF Receiver Characteristics for 169 MHz Band
- In LFRCO, updated test conditions for f_{LFRCO} .
- In GPIO, added footnotes to V_{IL} and V_{IH} .
- In VMON, updated test conditions for I_{VMON} .
- In VDAC, updated test conditions for I_{DAC} , 200 Hz refresh rate.
- In CSEN, updated test conditions for:
 - C_{EXTMAX}
 - I_{CSEN_BOND}
 - I_{CSEN_EM2}
 - I_{CSEN_ACTIVE}
- In Pin Definitions, updated pin descriptions for DECOUPLE and RESETn.
- Updated feature code in:
 - [7.3 BGA125 Package Marking](#)
 - [8.3 QFN48 Package Marking](#)

Revision 1.3

June, 2018

- [4.1.5.4 Current Consumption Using Radio 3.3 V with DC-DC](#): Updated typical 802.15.4 receive current specifications.
- [Table 6.9 GPIO Functionality Table on page 141](#): Changed presentation to order table by pin name instead of pin location.

Revision 1.2

February, 2018

- Added new orderable part numbers for QFN68 variants and associated packaging and pinout information.
- Absolute Maximum Ratings Table:** Added footnote to clarify IOVDD over-voltage operation conditions.
- APORT Connection Diagram:** Corrected OPA output connections to route through "Y" buses.

Revision 1.1

October, 2017

- Updated **Ordering Table** to revision-C OPNs.
- Added high-temperature part numbers to **Ordering Table** and added associated specifications / content throughout document.
- Updated product highlights on **Front Page** and **Feature List** for consistency across EFR32xG1x family documentation.
- System Overview Updates**
 - Expanded Receiver Architecture section.
 - Clarified / corrected energy mode mentions in RTCC and Opamp sections.
 - Memory maps updated with LE peripherals and new formatting.
- Absolute Maximum Ratings Table:**
 - Removed redundant I_{VSSMAX} line.
 - Added footnote to clarify V_{DIGPIN} specification for 5V tolerant GPIO.
- General Operating Conditions Table:**
 - Removed redundant footnote about shorting VREGVDD and AVDD together.
 - Added footnote about IOVDD voltage restriction when CSEN peripheral is used with chopping enabled.
 - Added footnote for additional information on peak current during voltage scaling operations.
- RF Receiver Characteristics for 2GFSK in the 2.4GHz Band, 1 Mbps Data Rate Table:**
 - Sensitivity, Co-channel interferer and Selectivity typical numbers updated to latest phy characterization data.
 - BLOCK_{OOB} specifications changed to show Min values instead of Typ.
- RF Receiver Characteristics for 2GFSK in the 2.4GHz Band, 2 Mbps Data Rate Table:**
 - SAT Typical value corrected from 5 to 10 dBm.
 - BLOCK_{OOB} specifications removed.
- RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band Table:** Footnote added to BLOCK_{80211G} specification to clarify blocker signal definition.
- Sub-GHz RF Receiver Characteristics for 915 MHz Band Table:** Added O-QPSK DSSS phy specifications.
- Sub-GHz RF Transmitter Characteristics for 868 MHz Band Table:** SPUR_{OOB_ESI} below 1 GHz Typ corrected from -60 to -42 dBm.
- Sub-GHz RF Receiver Characteristics for 490 MHz Band Table:** Corrected 10 kbps 2GFSK reference signal bandwidth to 20.038 kHz.
- Flash Memory Characteristics Table:**
 - Added timing measurement clarification for Device Erase and Mass Erase.
 - Device Erase Time typical values corrected from 69 to 82 ms.
- Analog to Digital Converter (ADC) Table:**
 - Added header text for general specification conditions.
 - Added footnote for clarification of input voltage limits.
- Digital to Analog Converter (VDAC) Table:** Gain Error min/max specifications relaxed for REFSEL on 1V25LN, VDD, and EXT settings.
- Current Digital to Analog Converter (IDAC) Table:** Total accuracy STEPSEL value setting corrected from 0x80 to 0x10.
- Analog Port (APORT) Table:** Operation in EM2/EM3 supply current changed from 915 to 67 nA (silicon fix from rev B to C).
- 2.4 GHz RF Transmitter Output Power Figure:** Extended temperature range to 125 C.
- 2.4 GHz RF Receiver Sensitivity Figure:** Updated with latest characterization data and added 125 C operational plots.
- Typical Sub-GHz Impedance-matching network circuits Figure:** Corrected split between two examples from 450 MHz to 500 MHz.
- Minor typographical corrections, including capitalization, mis-spellings and punctuation marks, throughout document.
- Minor formatting and styling updates, including table formats, TOC location, and boilerplate information throughout document.

Revision 1.0

2017-04-14

- Added Thermal Characteristics table.
- Finalized specification tables. All tables were updated with latest characterization data and production test limits.
- Updated typical performance graphs for DC-DC.
- Minor typographical, clarity, and consistency improvements.
- Condensed pin function tables with new formatting.

Revision 0.6

2017-02-23

- Updated 2 Mbps 2GFSK receiver specifications with latest characterization data.
- Added table-wide conditions to 2GFSK 1 Mbps and 2 Mbps receiver tables.
- Clarified opamp noise measurement conditions in electrical spec table.

Revision 0.5

2017-02-03

- New corporate stylesheet applied.
- Updated device block diagrams on front page and in System Overview.
- Updated Feature List with latest characterization numbers.
- "Bluetooth Smart" changed to "Bluetooth Low Energy" throughout document.
- All OPNs changed to revision B.
- Minor typographical corrections and clarifications in System Overview.
- Electrical Characteristics Table Changes
 - All specification tables updated with latest characterization data and production test limits.
 - Split 2.4 GHz 2GFSK tables into separate tables for 1 Mbps and 2 Mbps data rates.
 - Split HFRCO/AUXHFRCO table into separate tables for HFRCO and AUXHFRCO.
 - OPAMP, CSEN, and VDAC specification line items updated to match test conditions.
 - Added tables for Analog Port (APORT) and Pulse Counter (PCNT).
- Added Typical Performance Curves for supply current, DCDC, and RF parameters.
- Added missing alternate functions and descriptions to Pinout and Alternate Function tables.
- Added APORT Connection Diagram.
- Corrected Package Marking description for QFN48 and BGA125.
- Corrected Package Marking diagram for QFN48.

Revision 0.2

2016-09-21

Initial release.

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