TPS22949x Current-Limited Load Switch With Low Noise Regulation Capability

1 Features

- Integrated Current Limiter
  - Input Voltage Range: 1.62 V to 4.5 V
  - Low ON-Resistance
    - r_{ON} = 300-mΩ at V_{IN} = 4.5 V
    - r_{ON} = 350-mΩ at V_{IN} = 3.3 V
    - r_{ON} = 400-mΩ at V_{IN} = 2.5 V
    - r_{ON} = 600-mΩ at V_{IN} = 1.8 V
  - Integrated 100-mA Minimum Current Limit
  - Undervoltage Lockout
  - Fast-Current Limit Response Time
  - Integrated Fault Blanking and Auto Restart
- Stable Without Current Limiter Output Capacitor (TPS22949A Only)
- Integrated Low-Noise RF LDO
  - Input Voltage Range: 1.62 V to 4.5 V
  - Low Noise: 50 µVrms (10 Hz to 100 kHz)
  - 80-dB V_{IN} PSRR (10 Hz to 10 kHz)
  - Fast Start-Up Time: 130 µs
  - Low Dropout 100 mV at I_{load} =100 mA
  - Integrated Output Discharge
  - Stable With 2.2-µF Output Capacitor
- 1.8-V Compatible Control Input Threshold
- ESD Performance Tested Per JESD 22
  - 3500 V Human Body Model (A114-B, Class II)
  - 1000 V Charged Device Model (C101)
- Tiny 8-Terminal YZP Package (1.9 mm × 0.9 mm, 0.5-mm Pitch, 0.5-mm Height) and WSON-8 (DRG) 3.0 mm × 3.0 mm

2 Applications

- Fingerprint Module Protection
- Portable Consumer Electronics
- Smart Phones
- Notebooks
- Control Access Systems

3 Description

The TPS22949 and TPS22949A are devices that provide protection to systems and loads in high-current conditions. The device contains a 500-mΩ current-limited P-channel MOSFET that can operate over an input voltage range of 1.62 V to 4.5 V as well as a low-dropout (LDO) regulator with a fixed output voltage of 1.8 V.

The switch is controlled by an on/off input (EN1), which can interface directly with low-voltage control signals. When the switch current reaches the maximum limit, the TPS22949/TPS22949A operates in a constant-current mode to prohibit excessive currents from causing damage. If the constant current condition persists after 12 ms, these devices shut off the switch and pull the fault signal pin (OC) low. The TPS22949/TPS22949A has an auto-restart feature that turns the switch on again after 70 ms if the EN1 pin is still active.

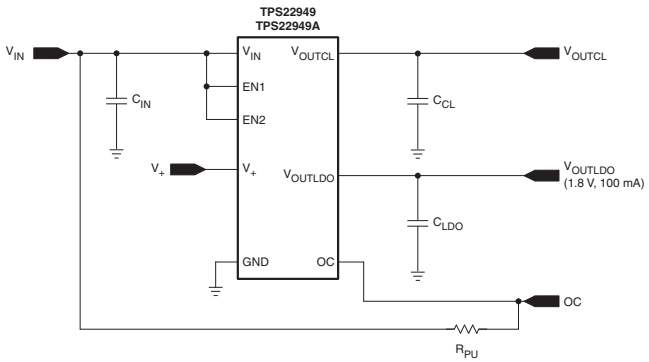
The output of the current limiter is internally connected to an RF low-dropout (LDO) regulator that offers good AC performance with very low ground current, good power supply rejection ratio (PSRR), low noise, fast start-up, and excellent line and load transient response. The output of the regulator is stable with ceramic capacitors. This LDO uses a precision voltage reference and feedback loop to achieve overall accuracy of 2% over all load, line, process, and temperature variations.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22949	DSBGA (8)	1.90 mm × 0.90 mm
TPS22949A	DSBGA (8)	1.90 mm × 0.90 mm
	WSON (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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4 Revision History

Changes from Revision C (January 2010) to Revision D **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Dissipation Ratings* table ... 5

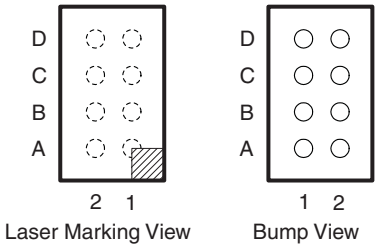
5 Description (continued)

The TPS22949A integrates additional internal circuitry that increases the current limit of the switch during the power-up sequence. This feature allows the TPS22949A to operate without a storage capacitor at the input of the LDO.

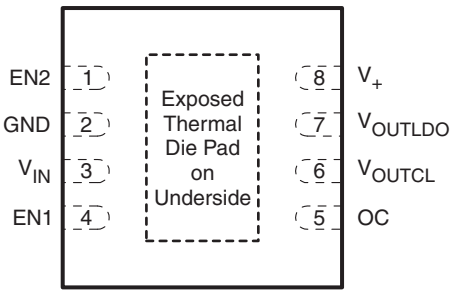
The TPS22949 and TPS22949A are available in a space-saving 8-terminal WCSP (YZP) or in an 8-pin WSON package (DRG). Both devices are characterized for operation over the free-air temperature range of –40°C to 85°C.

6 Pin Configuration and Functions

YZP Package
8-Pin DSBGA
Top View



DRG Package
8-Pin WSON
Top View



The exposed center pad, if used, must be connected as a secondary GND or left electrically open.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	DSBGA	WSON		
EN1	D2	4	I	Power switch control input. Active high. Do not leave floating.
EN2	A2	1	I	LDO control input. Active high. Do not leave floating.
GND	B2	2	—	Ground
OC	D1	5	O	Overcurrent output flag. Active low, open-drain output that indicates an overcurrent, supply undervoltage, or overtemperature state.
V_+	A1	8	I	Supply voltage
V_{IN}	C2	3	I	Supply input. Input to the power switch; bypass this input with a ceramic capacitor to ground.
V_{OUTCL}	C1	6	O	Switch output. Output of the power switch
V_{OUTLDO}	B1	7	O	LDO output. Output of the RF LDO fixed to 1.8 V(1).

(1) Output voltages from 0.9 V to 3.6 V in 50-mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.

YZP Package Pin Assignments

D	EN1	OC
C	V_{IN}	V_{OUTCL}
B	GND	V_{OUTLDO}
A	EN2	V_+
	2	**1**

7 Specifications

7.1 Absolute Maximum Ratings(1)

			MIN	MAX	UNIT
V_I	Input voltage	V_{IN}, EN1, EN2, V_+	–0.3	6	V
V_{OUTCL}	Current limiter output voltage			V_{IN} + 0.3	V
T_J	Operating junction temperature		–40	105	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage(1)	1.62		4.5	V
V_{OUTCL}	Current limiter output voltage			V_{IN}	V
V_+	Supply voltage	2.6		5.5	V
C_{IN}	Input capacitor	1			µF
T_A	Ambient free-air temperature	–40		85	°C
CONTROL INPUTS (EN1, EN2)					
V_{IH}	High-level input voltage	1.4		5.5	V
V_{IL}	Low-level input voltage			0.4	V

(1) See the *Application and Implementation*.

7.4 Thermal Information

THERMAL METRIC(1)		TPS22949x		UNIT
		YZP [DSBGA]	DRG [WSON]	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.8	51.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.6	65.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.8	25.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.1	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.8	26	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	6.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{GND}	Ground pin current	EN1 and EN2 = V_+ V_+ = V_{OUT} + 1.4 V or 2.5, whichever > 5.5 V, V_{OUTCL} ≥ V_{OUTLDO} + 0.5 V I_{OUT2} = 0 mA			85	110	µA
I_{GNDCL}	Ground pin current (current limiter only)	EN1 = V_+ and EN2 = 0			40	75	µA
$I_{GND(OFF)}$	OFF-state ground pin current	EN1 and EN2 = GND, V_{OUTCL} = Open, V_{OUTLDO} = Open	V_{IN} = V_+ = 3.3 V			2	µA
			V_{IN} = 3.6 V, V_+ = 5.5 V			6	
I_{EN2}	Enable pin 2 current, enabled	VEN2 = V_+ =5.5 V, V_{IN} = 4.5 V				1	µA
I_{EN1}	Enable pin 1 current, enabled	VEN1 = V_+ = 5.5 V, V_{IN} = 4.5 V				1	µA
Thermal shutdown	Shutdown threshold (T_A)	TPS22949			122		°C
		TPS22949A			135		
	Return from shutdown	TPS22949			112		
		TPS22949A			120		
	Hysteresis	TPS22949			10		
		TPS22949A			10		

(1) Typical values are at V_{IN} = 3.3 V and T_A = 25°C.

7.6 Current Limiter Electrical Characteristics

over operating free-air temperature range, V_+ = 3.3 V, EN1 = V_+, EN2 = GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	YZP PACKAGE			DRG PACKAGE			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
r_{ON}	ON-state resistance	I_{OUT} = 20 mA	V_{IN} = 4.5 V	25°C		0.3	0.4		0.4	0.5	Ω
				Full			0.5			0.6	
			V_{IN} = 3.3 V	25°C		0.35	0.6		0.45	0.7	
				Full			0.7			0.8	
			V_{IN} = 2.5 V	25°C		0.4	0.7		0.5	0.8	
				Full			0.8			0.9	
			V_{IN} = 1.8 V	25°C		0.6	0.9		0.7	1	
				Full			1.0			1.1	
			V_{IN} = 1.62 V	25°C		0.7	1.0		0.8	1.1	
				Full			1.1			1.2	
I_{LIM}	Current limit	V_{OUT} = 3 V	V_{IN} = 3.3 V	Full	100	150	200	100	150	200	mA
$I_{LIM\ (INRUSH)}$	Power-ON inrush current limit (TPS22949A only)	V_{OUT} = 3 V	V_{IN} = 3.3 V	Full		750			750		
UVLO-CL	Undervoltage shutdown	V_{IN} increasing			1.39	1.49	1.59	1.39	1.49	1.59	V
	Undervoltage shutdown hysteresis					30			30		mV
	OC output logic low voltage	I_{SINK} = 10 mA	V_{IN} = 4.5 V	Full		0.1	0.3		0.1	0.3	V
			V_{IN} = 1.8 V			0.2	0.4		0.2	0.4	

7.7 Low-Noise LDO Regulator Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OUTLDO}	Output voltage(1)			1.76	1.8	1.84	V
$\Delta V_{OUTLDO}/\Delta V_{IN}$	V_{IN} line regulation	V_{IN} = V_{OUTLDO} + 0.5 V to 4.5 V, I_{OUT} = 1 mA			±0.1		%/V
	V_{IN} line transient	ΔV_{IN} = 400 mV, t_r = t_f = 1 µs			±2		mV
$\Delta V_{OUTLDO}/\Delta V_+$	V_+ line regulation	V_{IN} = V_{OUTLDO} + 1.4 V or 2.5 V, whichever is > 5.5 V, I_{OUT} = 1 mA			±0.1		%/V
	V_+ line transient	ΔV_{IN} = 600 mV, t_r = t_f = 1 µs			±5		mV
$\Delta V_{OUTLDO}/\Delta I_{OUT2}$	Load regulation	I_{OUT2} = 0 to 100 mA (no load to full load)			±0.01		%/V
	Load transient	I_{OUT2} = 0 to 100 mA, t_r = t_f = 1 µs			±35		mV
V_{DO}	Dropout voltage (V_{DO} = V_{IN} – V_{OUTLDO})	V_{IN} = $V_{OUTLDO(NOM)}$ – 0.1 V, V_+ – $V_{OUTLDO(NOM)}$ = 1.4 V, I_{OUT} = 100 mA			110	200	mV
V_{IN} PSRR	Power supply rejection ratio	V_{OUTCL} – V_{OUTLDO} ≥ 0.5 V, V_+ = V_{OUTLDO} + 1.4 V, I_{OUT} = 100 mA,	f = 10 Hz		75		dB
			f = 100 Hz		75		
			f = 1 kHz		80		
			f = 10 kHz		80		
			f = 100 kHz		85		
			f = 1 MHz		85		
V_+ PSRR	Power supply rejection ratio	V_{OUTCL} – V_{OUTLDO} ≥ 0.5 V, V_+ = V_{OUTLDO} + 1.4 V, I_{OUT} = 100 mA,	f = 10 Hz		80		dB
			f = 100 Hz		80		
			f = 1 kHz		75		
			f = 10 kHz		65		
			f = 100 kHz		55		
			f = 1 MHz		35		
V_N	Output noise voltage	V_+ ≥2.5 V, V_{OUTLDO} = V_{OUTCL} + 0.5 V	BW = 10 Hz to 100 kHz		50		µVrms
t_{STR}	Start-up time	V_{OUT} = 95%, $V_{OUT(NOM)}$, I_{OUT} = 100 mA, C_{OUT} = 2.2 µF			130	250	µs
UVLO-V_+	Undervoltage lockout	V_+ rising		2.3	2.45	2.55	V
	Hysteresis	V_+ falling			150		mV

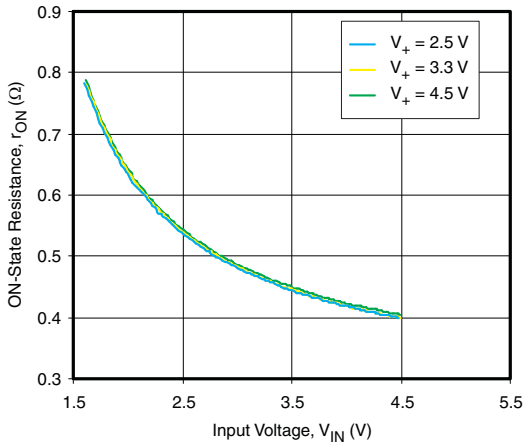
(1) LDO output voltage is fixed at 1.8 V. However, output voltages from 0.9 V to 3.6 V in 50-mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.

7.8 Current Limiter Switching Characteristics

V_{IN} = 3.3 V, T_A = 25°C, R_L = 500 Ω, C_L = 0.1 µF (unless otherwise noted)

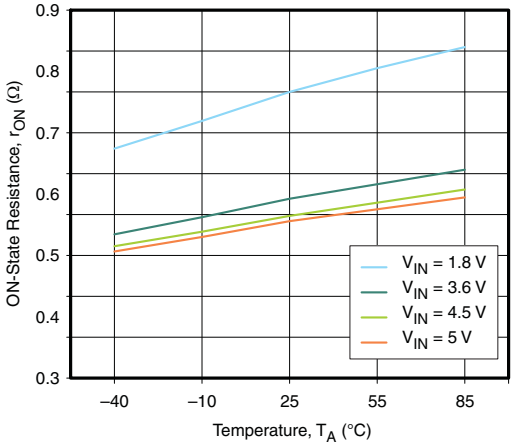
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	R_L = 500 Ω, C_{CL} = 0.1 µF		95		µs
t_{OFF}	Turnoff time	R_L = 500 Ω, C_{CL} = 0.1 µF		2		µs
t_r	V_{OUT} rise time	R_L = 500 Ω, C_{CL} = 0.1 µF		25		µs
t_f	V_{OUT} fall time	R_L = 500 Ω, C_{CL} = 0.1 µF		10		µs
t_{BLANK}	Overcurrent blanking time		6	12	18	ms
t_{RSTRT}	Auto-restart time		40	80	120	ms
t_{INRUSH}	Power-ON inrush current limit time (TPS22949A only)	R_L = 500 Ω, C_{CL} = 0.1 µF		150		µs
	Short-circuit response time	V_{IN} = V_{EN1} = 3.3 V, moderate overcurrent condition		11		µs
		V_{IN} = V_{EN1} = 3.3 V, hard short		5		

7.9 Typical Characteristics



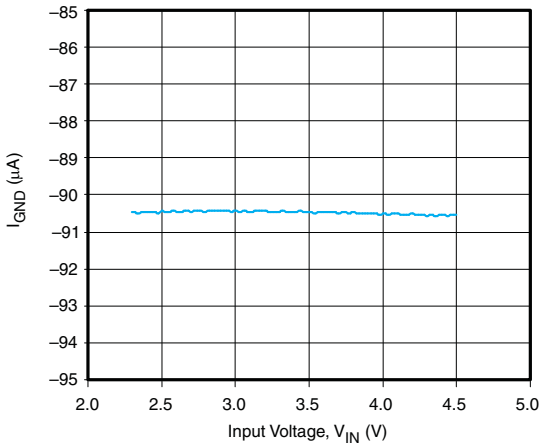
T_A = 25°C

Figure 1. ON-State Resistance vs Input Voltage



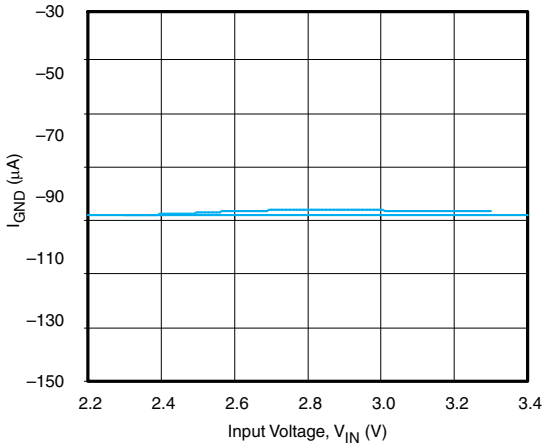
V_+ = 5.5 V

Figure 2. ON-State Resistance vs Temperature,



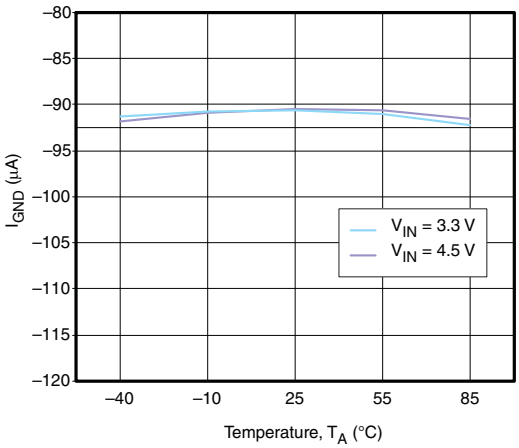
V_+ = 5.5 V

Figure 3. Ground Pin Current vs Input Voltage



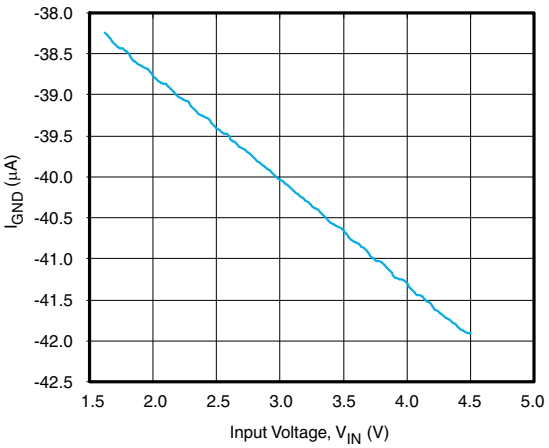
V_+ = 3.3 V

Figure 4. Ground Pin Current vs Input Voltage



V_+ = 5.5 V

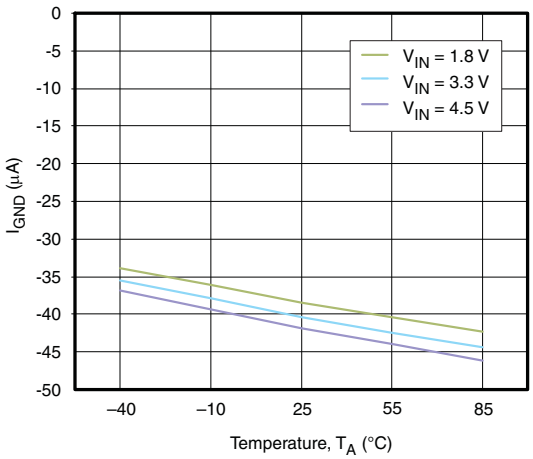
Figure 5. Ground Pin Current vs Temperature



V_+ = 5.5 V

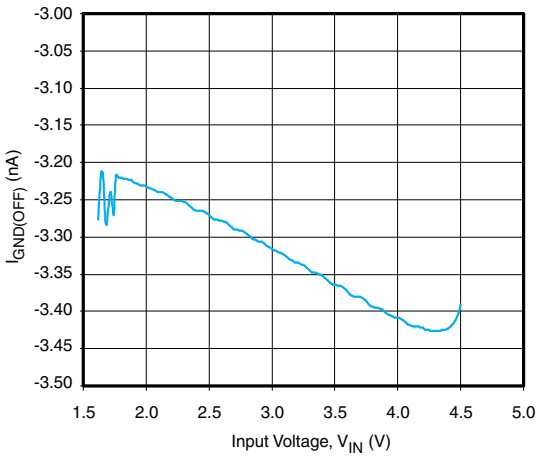
Figure 6. Ground Pin Current vs Input Voltage (Current Limiter Only)

Typical Characteristics (continued)



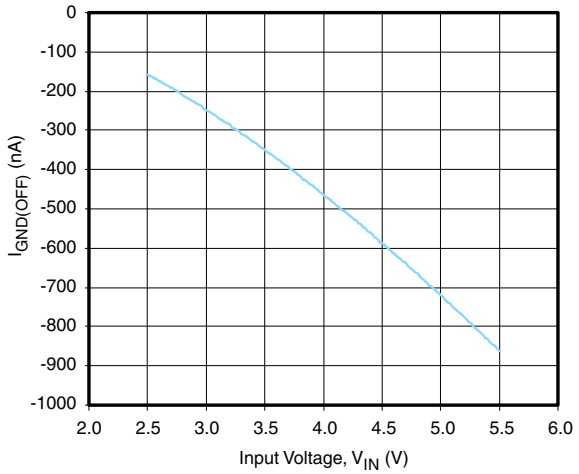
V_+ = 5.5 V

Figure 7. Ground Pin Current vs Temperature (Current Limiter Only)



V_+ = 5.5 V

Figure 8. OFF-State Ground Current vs Input Voltage



V_{IN} = V_+

Figure 9. OFF-State Ground Current vs Input Voltage

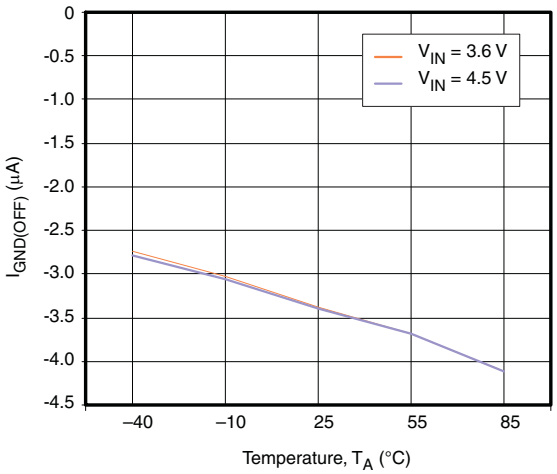


Figure 10. OFF-State Ground Current vs Temperature

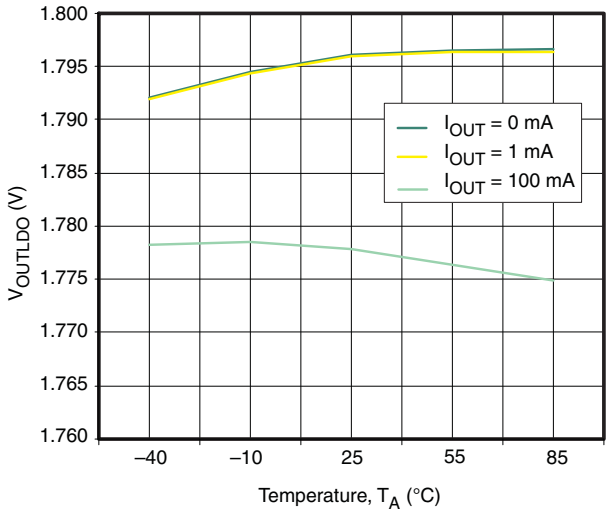


Figure 11. Output Voltage vs Temperature

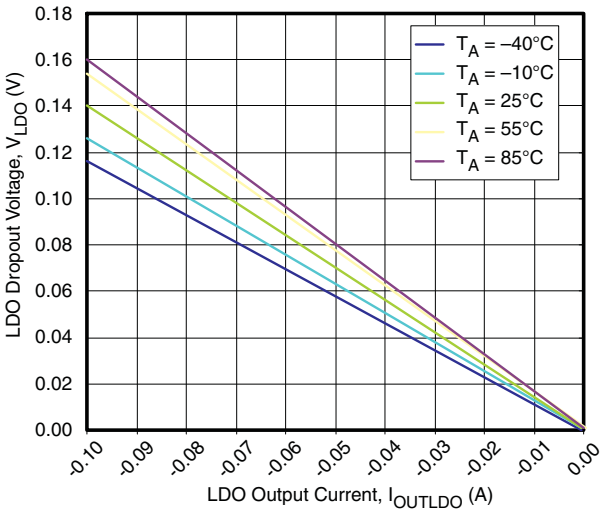
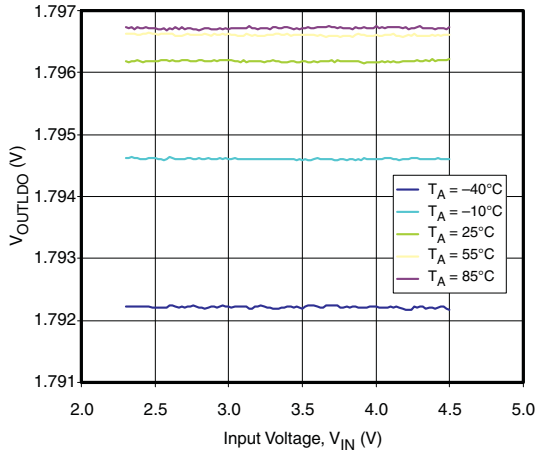


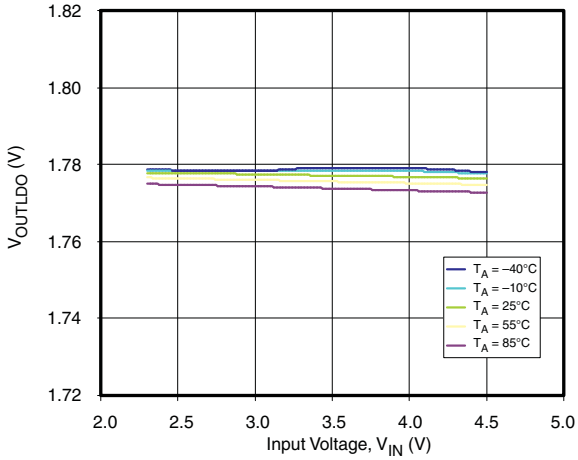
Figure 12. LDO Dropout Voltage vs Output Current

Typical Characteristics (continued)



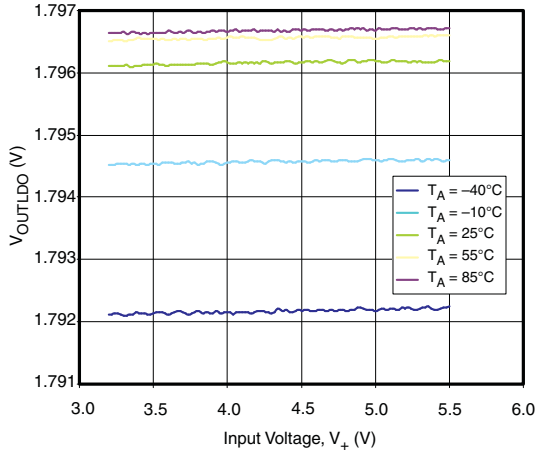
I_{OUT} = 0 mA

Figure 13. Input Voltage, V_{IN}, Line Regulation



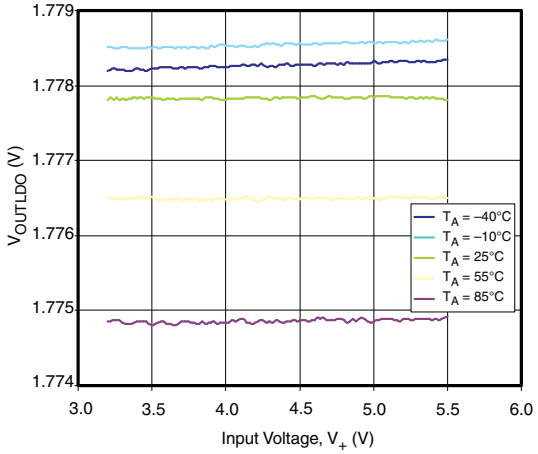
I_{OUT} = 100 mA

Figure 14. Input Voltage, V_{IN}, Line Regulation



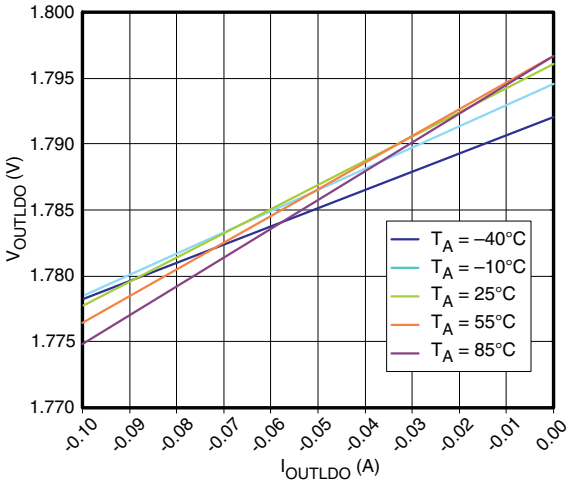
I_{OUT} = 0 mA

Figure 15. Input Voltage, V_+, Line Regulation



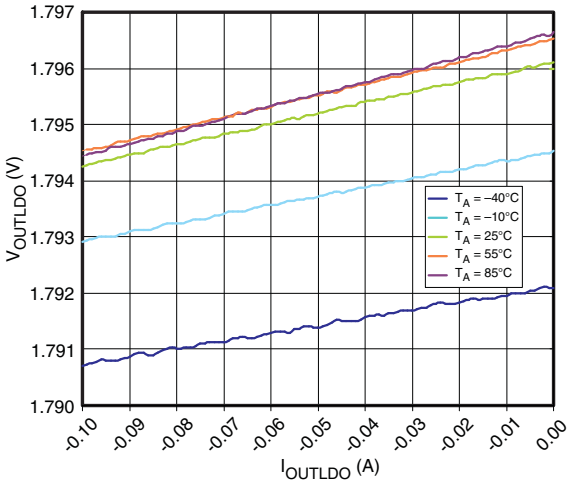
I_{OUT} = 100 mA

Figure 16. Input Voltage, V_+, Line Regulation



I_{OUT} = 100 mA

Figure 17. Load Regulation



I_{OUT} = 10 mA

Figure 18. Load Regulation Under Light Loads

Typical Characteristics (continued)

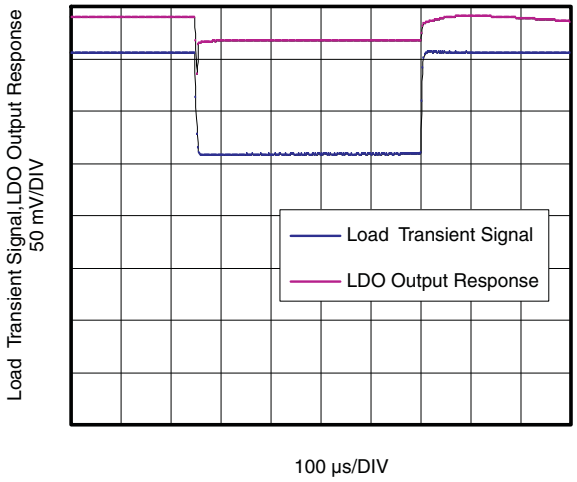


Figure 19. Load Transient

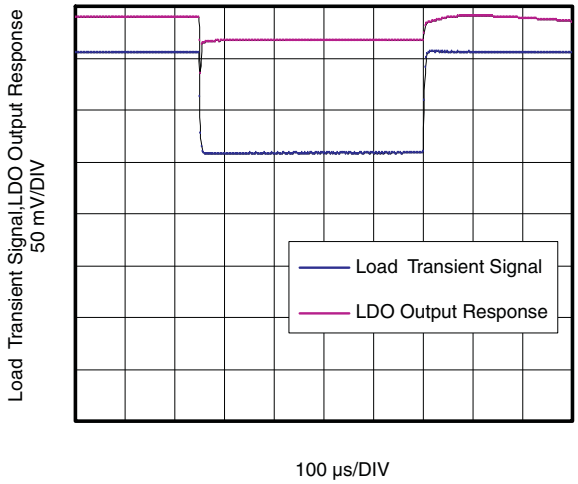


Figure 20. V_{IN} Load Transient

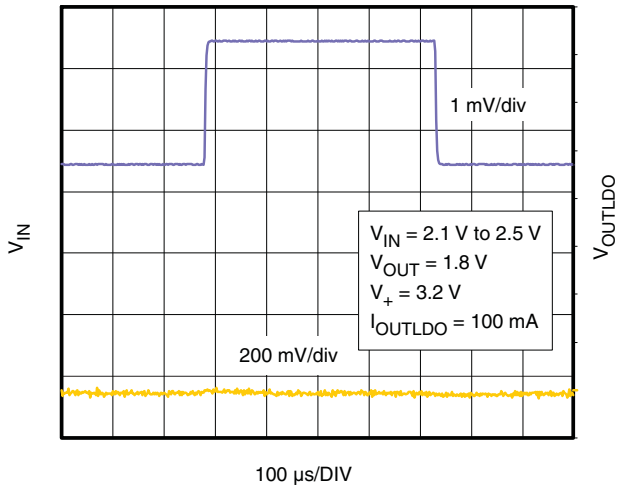


Figure 21. V_+ Load Transient

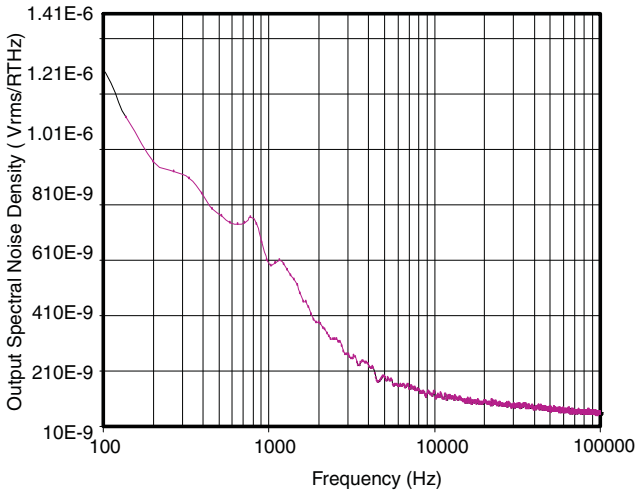


Figure 22. Output Spectral Noise Density vs Frequency

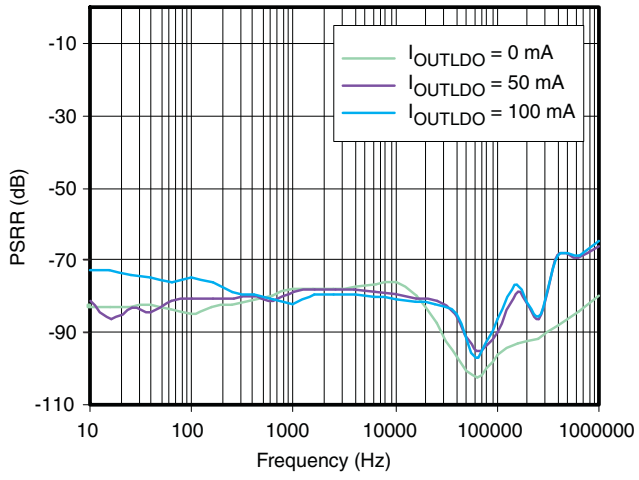


Figure 23. PSRR vs Frequency

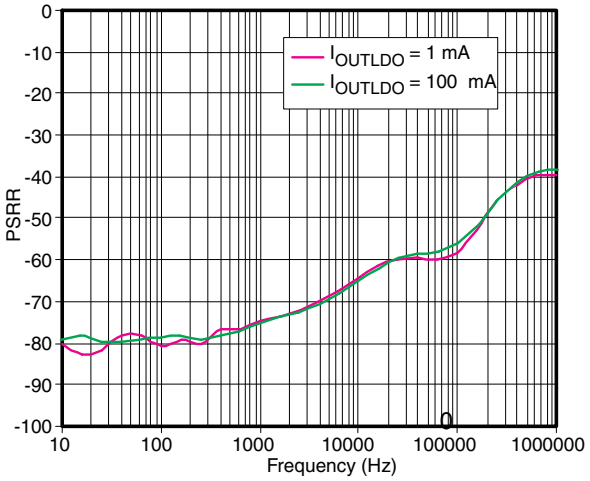


Figure 24. V_+ PSRR vs Frequency

Typical Characteristics (continued)

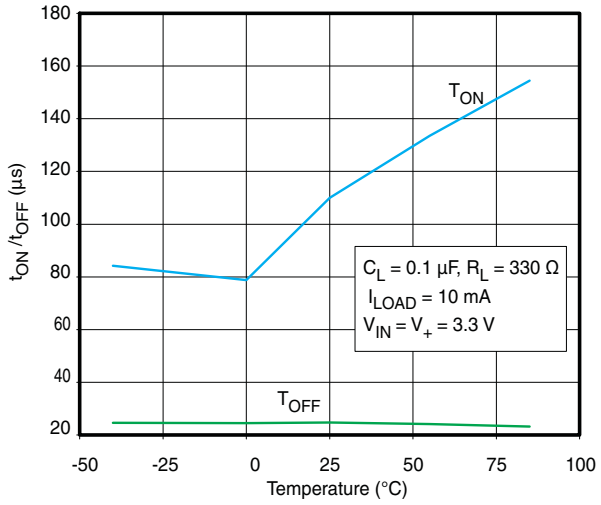


Figure 25. t_{ON}/t_{OFF} vs Temperature

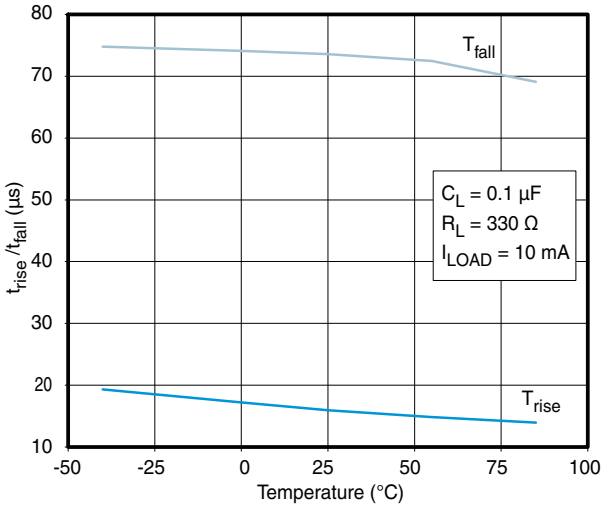
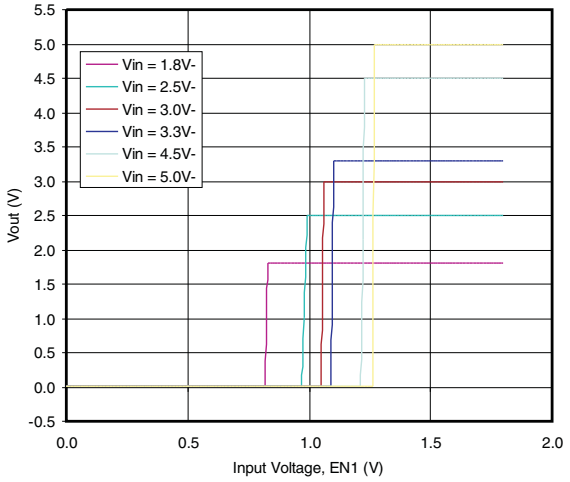
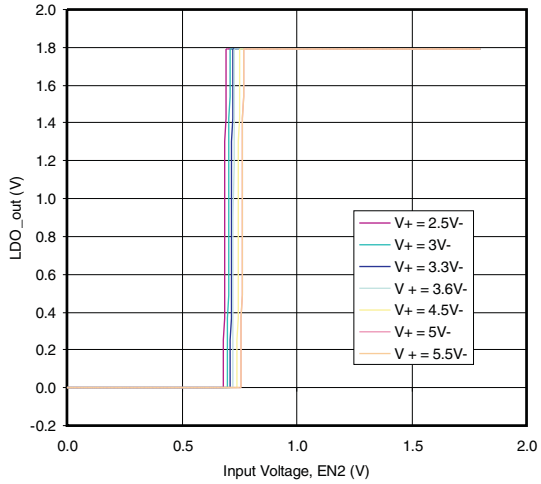


Figure 26. t_{rise}/t_{fall} vs Temperature



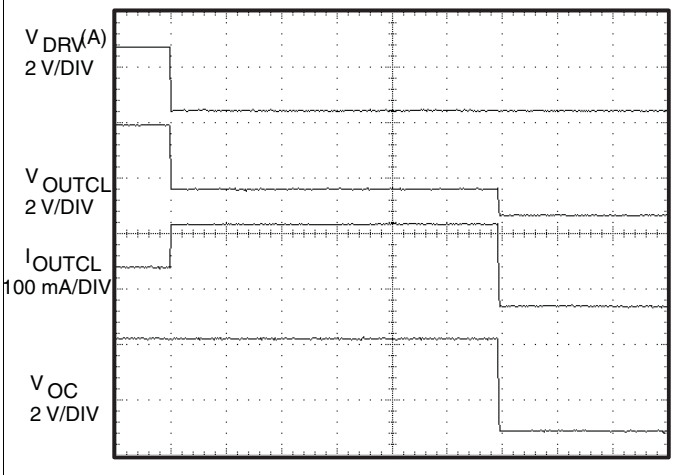
V_+ = 5.5 V

Figure 27. EN1 (Current Limiter) Input Thresholds



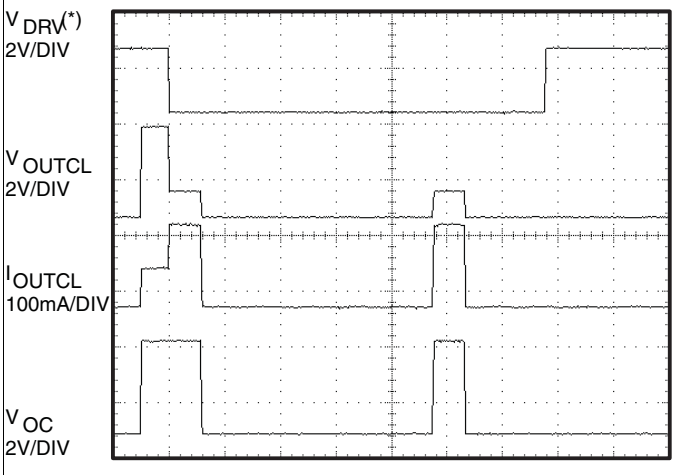
V_{IN} = 3.3 V

Figure 28. EN2 (LDO) Input Thresholds



V_{DRV} signal forces the device to go into overcurrent mode.

Figure 29. t_{BLANK} Response



V_{DRV} signal forces the device to go into overcurrent mode.

Figure 30. $t_{RESTART}$ Response

Typical Characteristics (continued)

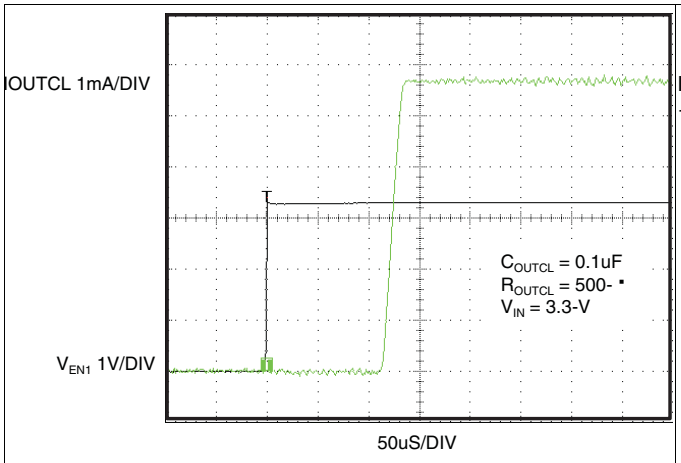


Figure 31. Current Limiter t_{ON} Response

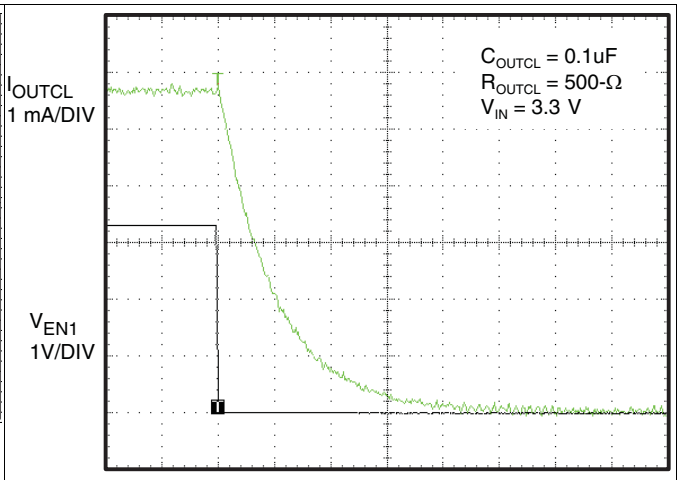


Figure 32. Current Limiter t_{OFF} Response

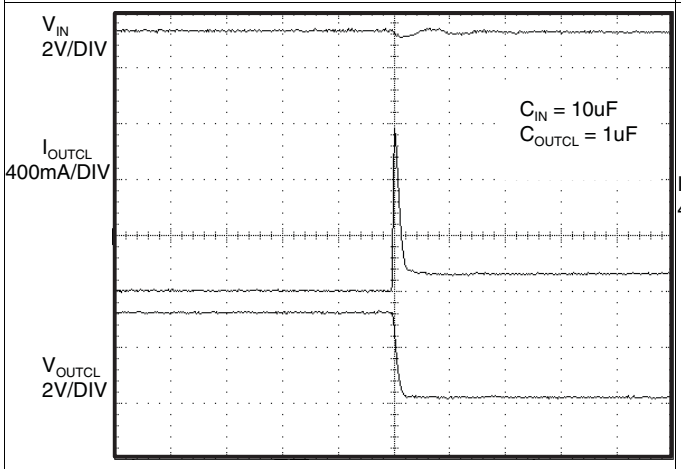


Figure 33. Short-Circuit Response Time (V_{OUTCL} Shorted to GND)

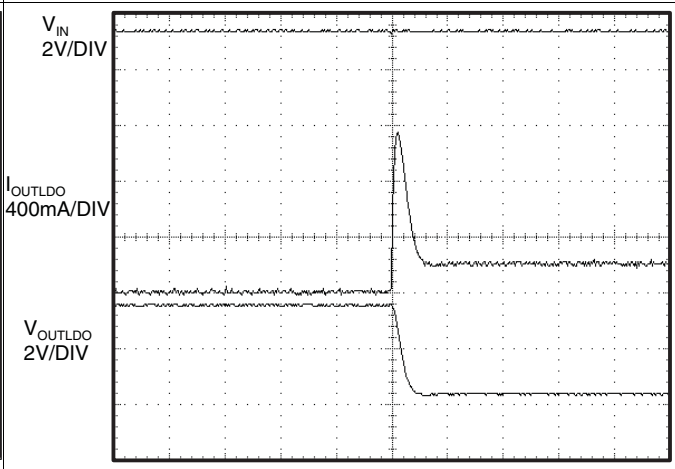


Figure 34. Short-Circuit Response Time (V_{OUTLDO} Shorted to GND)

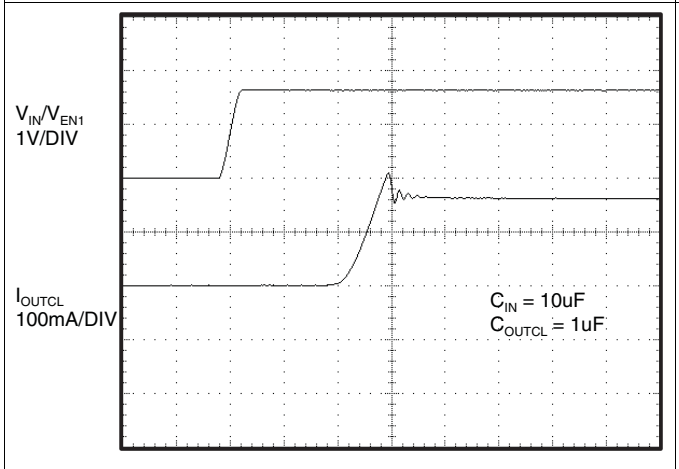


Figure 35. Short-Circuit Response Time (Switch Power Up to Hard Short) (TPS22949)

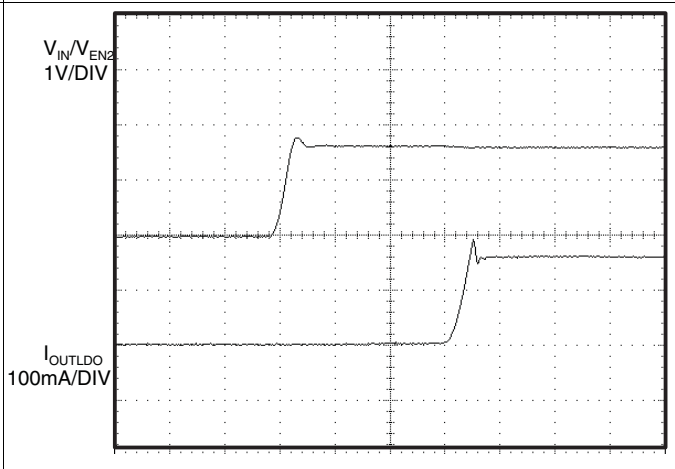


Figure 36. Short-Circuit Response Time (LDO Power Up to Hard Short) (TPS22949)

Typical Characteristics (continued)

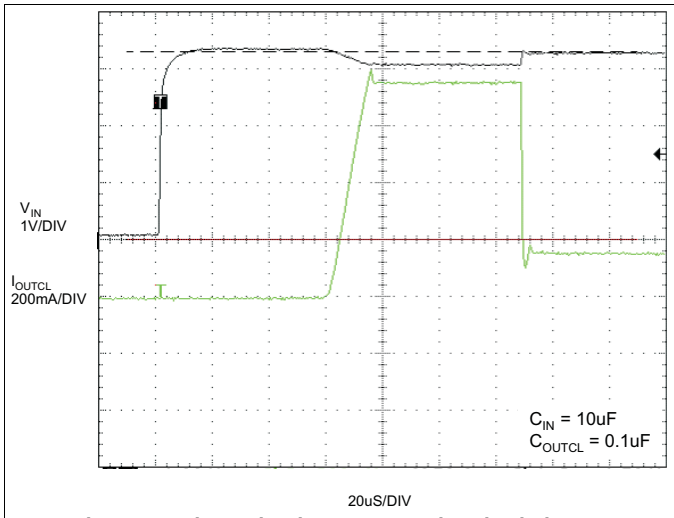


Figure 37. Short-Circuit Response Time (Switch Power Up to Hard Short) (TPS22949A)

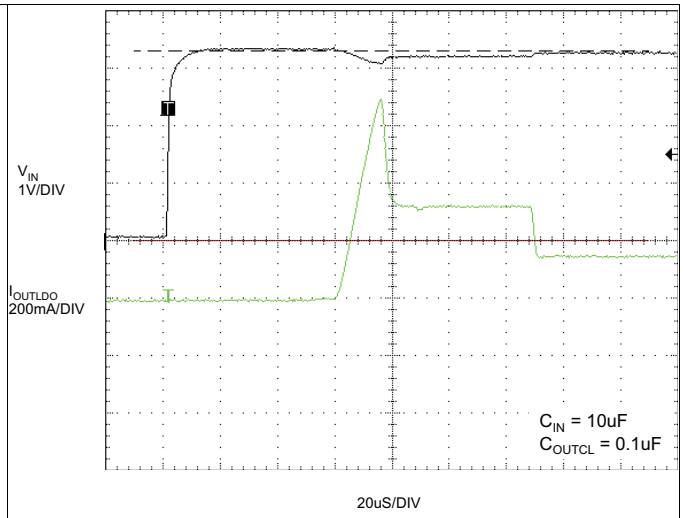


Figure 38. Short-Circuit Response Time (LDO Power Up to Hard Short) (TPS22949A)

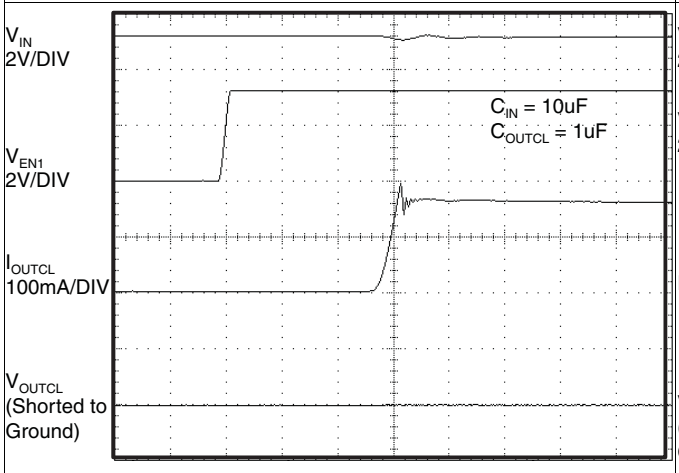


Figure 39. Current Limit Response Time (Current Limiter)

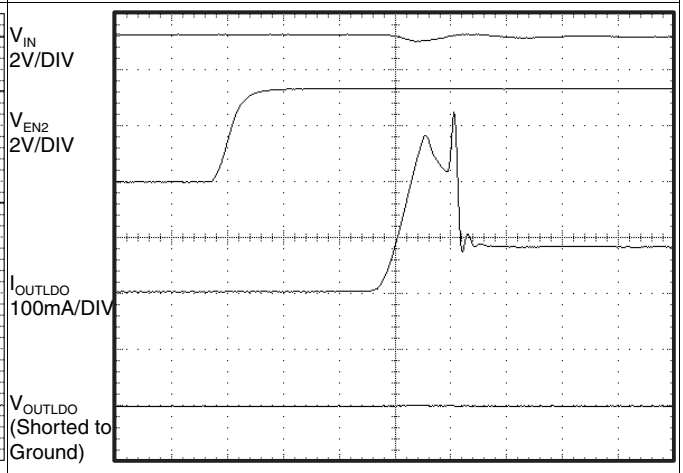


Figure 40. Current Limit Response Time (LDO)

8 Detailed Description

8.1 Overview

The TPS22949 and TPS22949A are devices that provide protection to systems and loads in high-current conditions. The device contains a 500-mΩ current-limited P-channel MOSFET that can operate over an input voltage range of 1.62 V to 4.5 V. In addition, these devices feature a low-dropout regulator (LDO) with a fixed output voltage of 1.8 V. When the switch current reaches the maximum limit, the TPS22949/TPS22949A operates in a constant-current mode to prohibit excessive currents from causing damage. The fault signal pin (OC) will signal the constant current condition if it persists after 12 ms. The output of the current limiter is internally connected to the LDO.

8.2 Functional Block Diagram

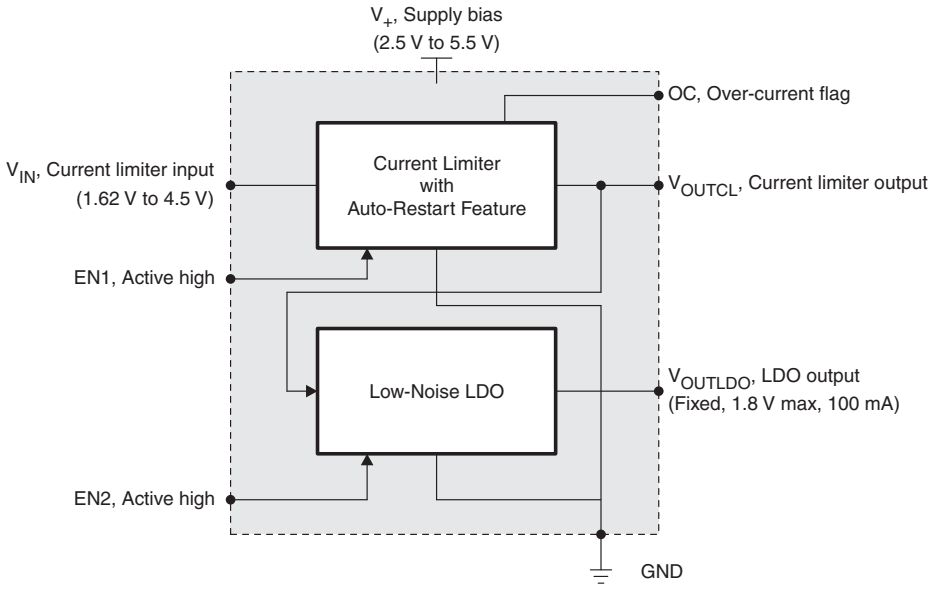


Figure 41. Simplified Block Diagram

Functional Block Diagram (continued)

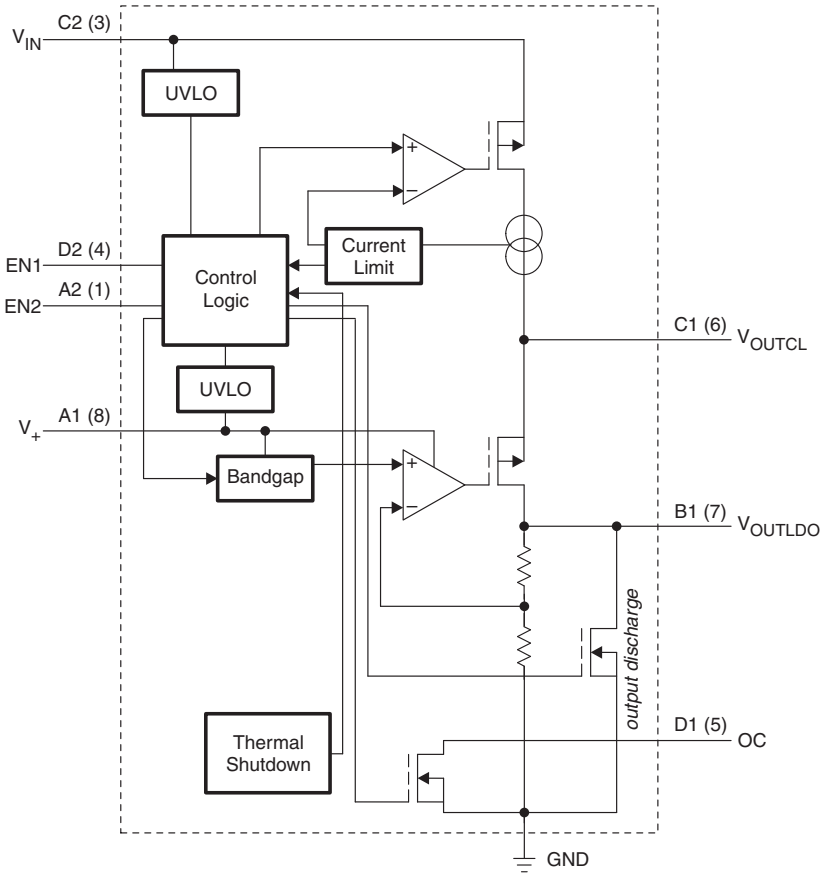


Figure 42. Detailed Block Diagram

8.3 Feature Description

8.3.1 Undervoltage Lockout (UVLO)

The undervoltage lockout turns off the switch if the input voltage drops below the undervoltage lockout threshold. With the ON pin active, the input voltage rising above the undervoltage lockout threshold causes a controlled turnon of the switch, which limits current overshoots. The TPS22949 and TPS22949A also have a UVLO on the V_+ bias voltage and keep the output of the LDO shut off until the internal circuitry is operating properly.

8.3.2 Fault Reporting

When an overcurrent, input undervoltage, or overtemperature condition is detected, OC is set active low to signal the fault mode. OC is an open-drain MOSFET and requires a pullup resistor between V_{IN} and OC. During shutdown, the pulldown on OC is disabled, thus reducing current draw from the supply.

8.3.3 Current Limiting

When the switch current reaches the maximum limit, the TPS22949/TPS22949A operates in a constant-current mode to prohibit excessive currents from causing damage. TPS22949/TPS22949A has a minimum current limit of 100 mA.

8.4 Device Functional Modes

Table 1 summarizes the LDO state as determined by the EN1 and EN2 pins.

Table 1. Function Table

STATE OF THE DEVICE	EN1	EN2
Current limiter and LDO disabled	0	X
Current limiter enabled and LDO disabled	1	0
Current limiter and LDO enabled	1	1

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This application illustrates the TPS22949 and TPS22949A configured with a 100-mA sinking load with both enables tied to the same input voltage.

9.1.1 Input Voltage

The input voltage (V_{IN}) of the current limiter is set from 1.62 V to 4.5 V, however if both the current limiter and the LDO are enabled, the user must be careful to keep the input voltage (V_{IN}) greater than 1.8 V + (voltage drop through the switch) + (voltage drop through the LDO); otherwise, the LDO does not have a high enough internal input signal to operate properly.

A current limiter input voltage ramp time less than the blanking time (approximately 10 ms typical) is recommended. If the ramp time extends beyond the blanking period, then the current limiter goes into recycle, and the system may not start or operate properly.

9.1.2 Input/Output Capacitors

Although an input capacitor is not required for stability of on the input pin (V_{IN}), it is good analog design practice to connect a 0.1-µF to 1-µF low equivalent series resistance (ESR) capacitor across the IN pin input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher value capacitor may be necessary if large, fast rise time load transients are anticipated, or if the device is located close to the power source. If source impedance is not sufficiently low, a 0.1-µF input capacitor may be necessary to ensure stability. The V_+ bias pin does not require an input capacitor because it does not source high currents. However, if source impedance is not sufficiently low, a small 0.1-µF bypass capacitor is recommended.

A 0.1-µF capacitor C_{CL}, must be placed between V_{OUTCL} and GND. This capacitor prevents parasitic board inductances from forcing V_{OUTCL} below GND when the switch turns off.

9.2 Typical Application

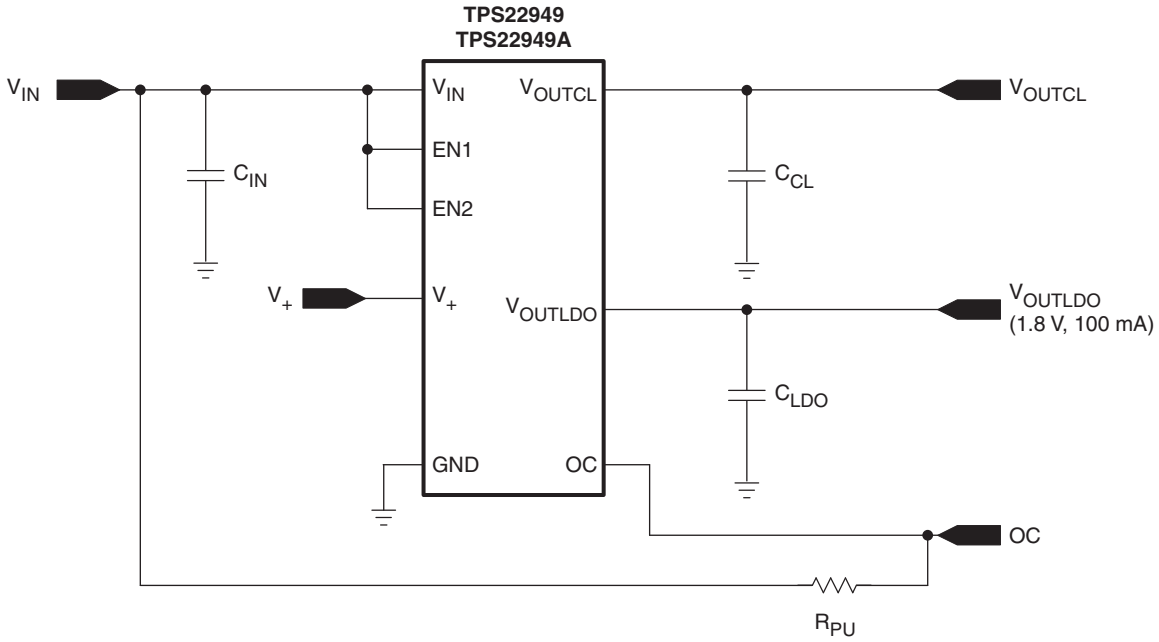


Figure 43. TPS22949/TPS22949A Typical Application With Both Enable Pins Tied to the Input Voltage

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.3 V
V+	3.3 V
C_{IN}	4.7 µF
C_{LDO}	2.2 µF

9.2.2 Detailed Design Procedure

9.2.2.1 Start-Up Sequence

For the TPS22949, the total output capacitance must be kept below a maximum value, $C_{CL(max)}$, to prevent the part from registering an overcurrent condition and turning off the switch. The maximum output capacitance can be determined from Equation 1:

$$C_{CL} = I_{LIM(MAX)} \times t_{BLANK(MIN)} \div V_{IN} \quad (1)$$

Due to the integral body diode in the PMOS switch, a C_{IN} greater than C_{CL} is highly recommended. A C_{CL} greater than C_{IN} can cause V_{OUTCL} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUTCL} to V_{IN}.

On TPS22949, a storage capacitor (C_{CL}) at the output of the current limiter is recommended to provide enough current to the LDO during the start-up sequence. The storage capacitor is needed to reduce the amount of inrush current supplied through the current-limited load switch to the LDO during the power-up sequence (see Figure 44). If the C_{CL} capacitor is too small, the inrush current needed to start the LDO and charge C_{LDO} could be interpreted by the current limiter as an overcurrent and, therefore, trigger the current-limiting feature of the switch. The switch would then try to limit the current to the 100-mA limit, and the user would see an undesired drop on the supply line (see Figure 45).

On TPS22949A, the storage capacitor (C_{CL}) is not required. TPS22949A integrates an additional internal circuitry that increases the current limit of the switch to approximately 750 mA (that is, $I_{LIM(INRUSH)}$) for about 250 µs (that is, t_{INRUSH}), initiated when the internal circuitry of the LDO is operating properly (that is, when the UVLO of the LDO bias (V_+) is disabled (V_+ > 2.6 V). Because the current limit is increased during the power-up sequence, a potential inrush current through the LDO is not interpreted by the current limiter as an overcurrent. The current needed by the LDO is then be supplied by the input capacitor (C_{IN}) of the current limiter (see Figure 45).

The TPS22949 LDO (V_{OUTLDO}) is designed to be stable with standard ceramic capacitors with values of 2.2 µF or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR must be less than 250 mΩ. Figure 43, Figure 44, and Figure 45 illustrate the behavior of the TPS22949 and TPS22949A with a 100-mA sinking load and different capacitor values for a typical application where both enables are tied to the same input voltage (see Figure 43).

9.2.3 Application Curves

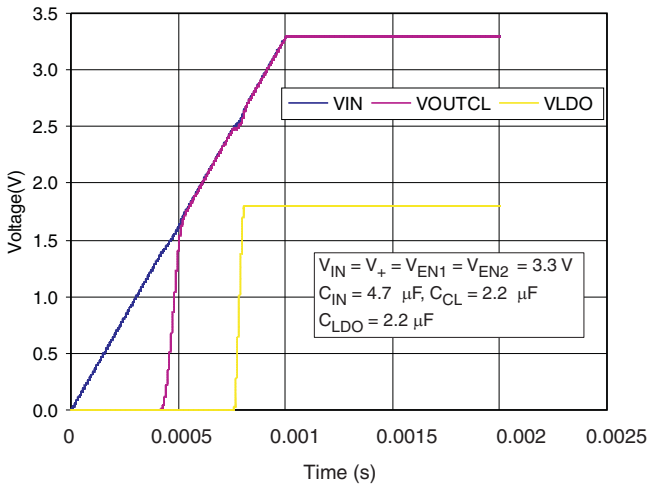


Figure 44. TPS22949 Power-Up Sequence

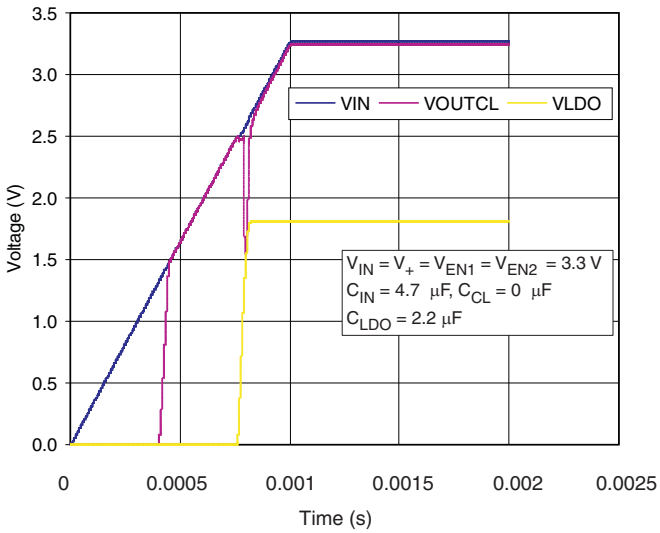


Figure 45. TPS22949 Power-Up Sequence

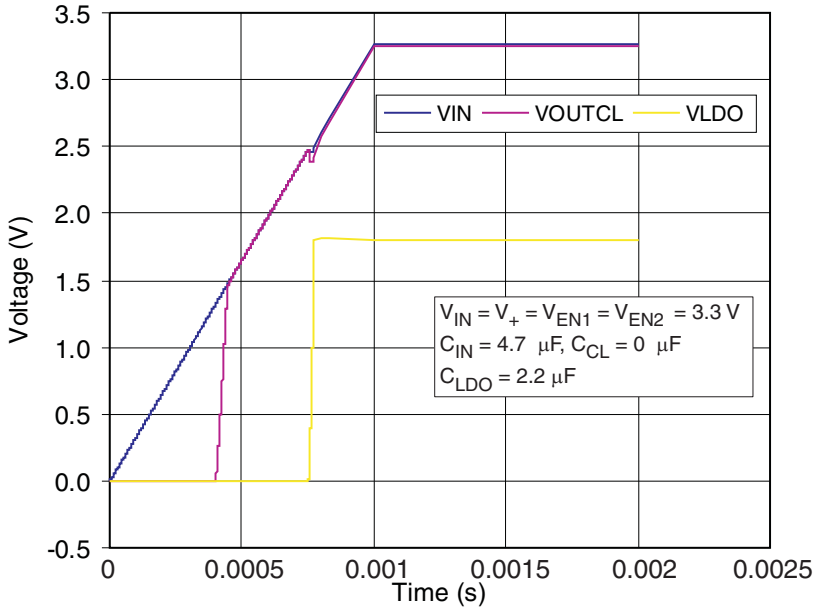


Figure 46. TPS22949A Power-Up Sequence

9.3 System Examples

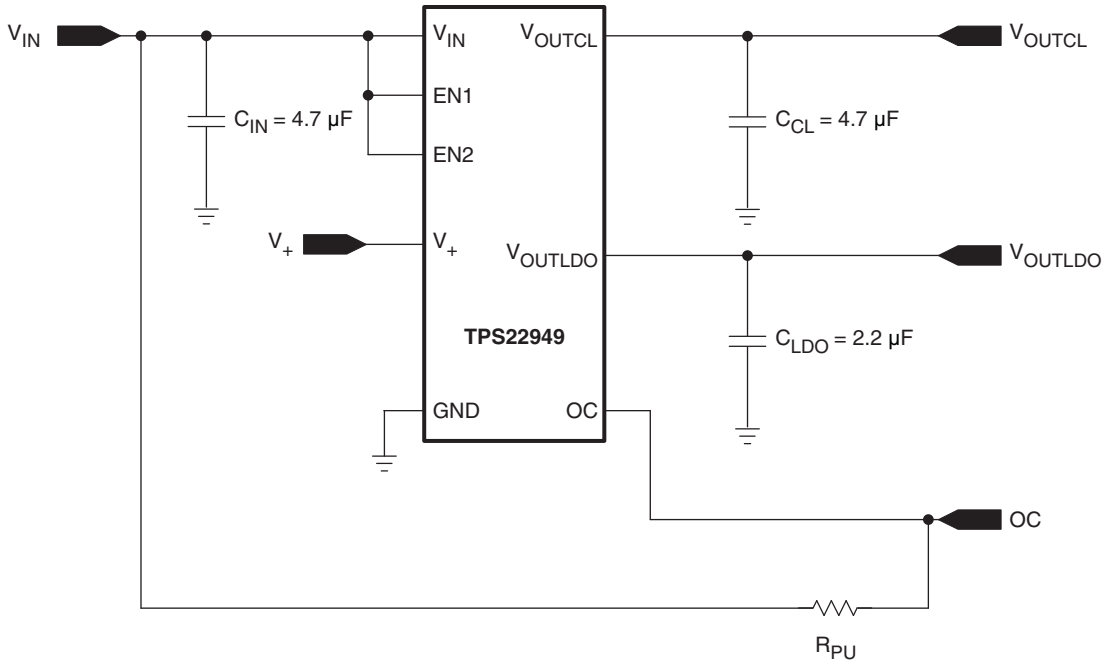


Figure 47. TPS22949 Typical Application Schematic

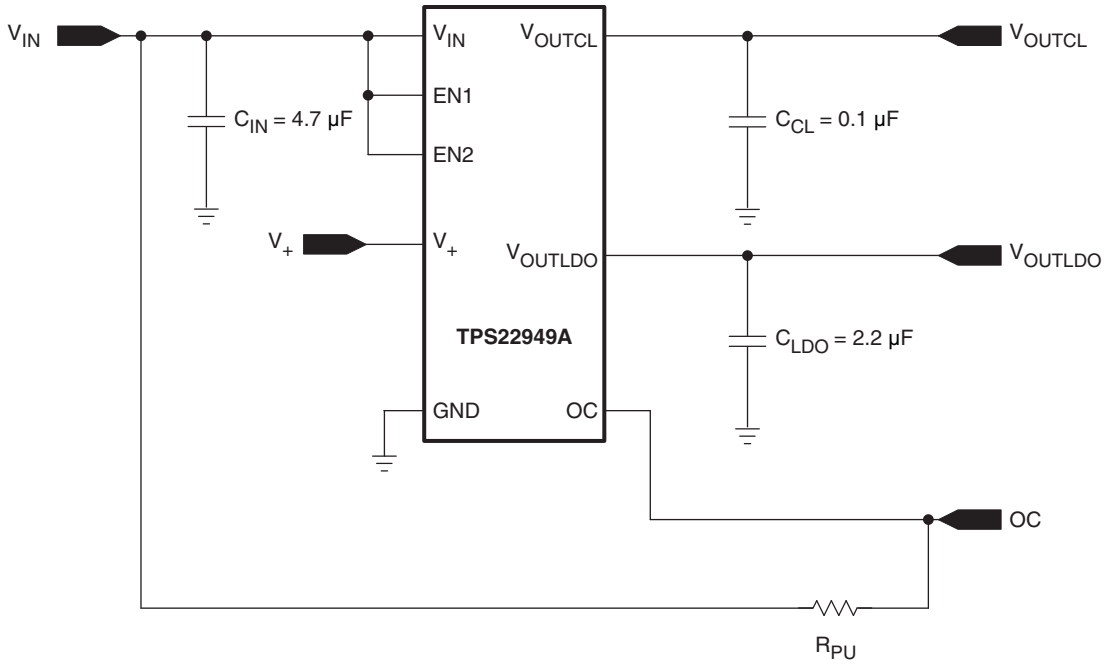


Figure 48. TPS22949A Typical Application Schematic

10 Power Supply Recommendations

The device is designed to operate from a V+ range of 2.6 V to 5.5 V and VIN range of 1.62 V to 4.5 V (without using the LDO) or >1.8 V to 4.5 V (when using the LDO). This supply must be placed as close to the device pin as possible with the recommended input bypass capacitor. If the supply is located more than a few inches from the device pins, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10 µF may be sufficient.

11 Layout

11.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, V+, VOUTLDO, VOUTCL, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

11.2 Layout Example

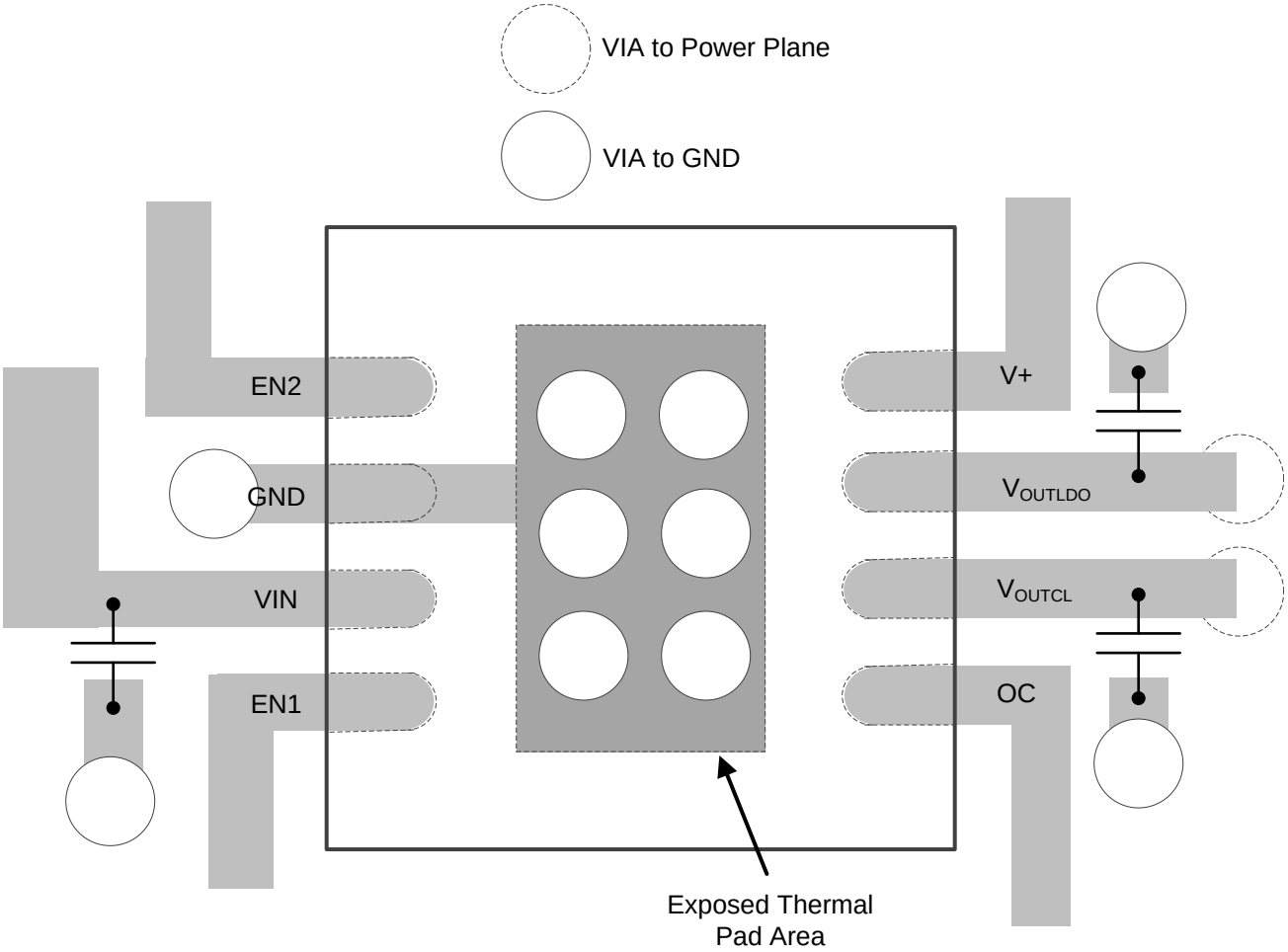


Figure 49. Layout Schematic

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS22949	Click here	Click here	Click here	Click here	Click here
TPS22949A	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22949ADRGR	ACTIVE	SON	DRG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZUG	Samples
TPS22949AYZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(4Z ~ 4Z2)	Samples
TPS22949YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(4Y ~ 4Y2)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

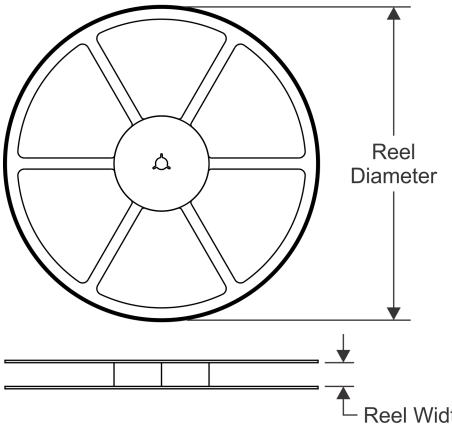
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

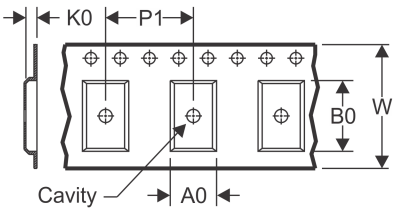
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

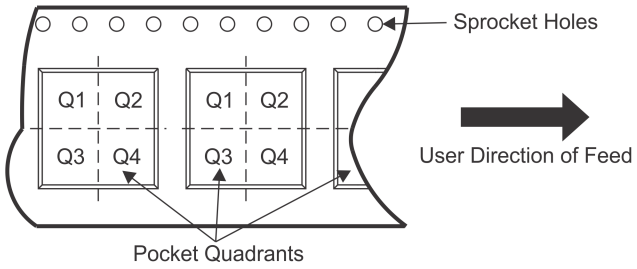


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

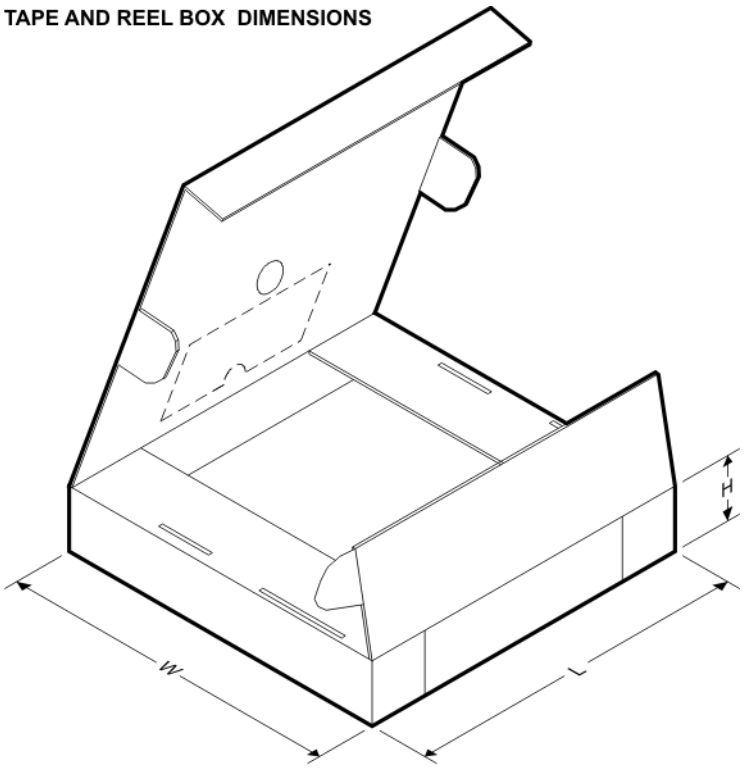
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22949ADRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS22949AYZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1
TPS22949YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

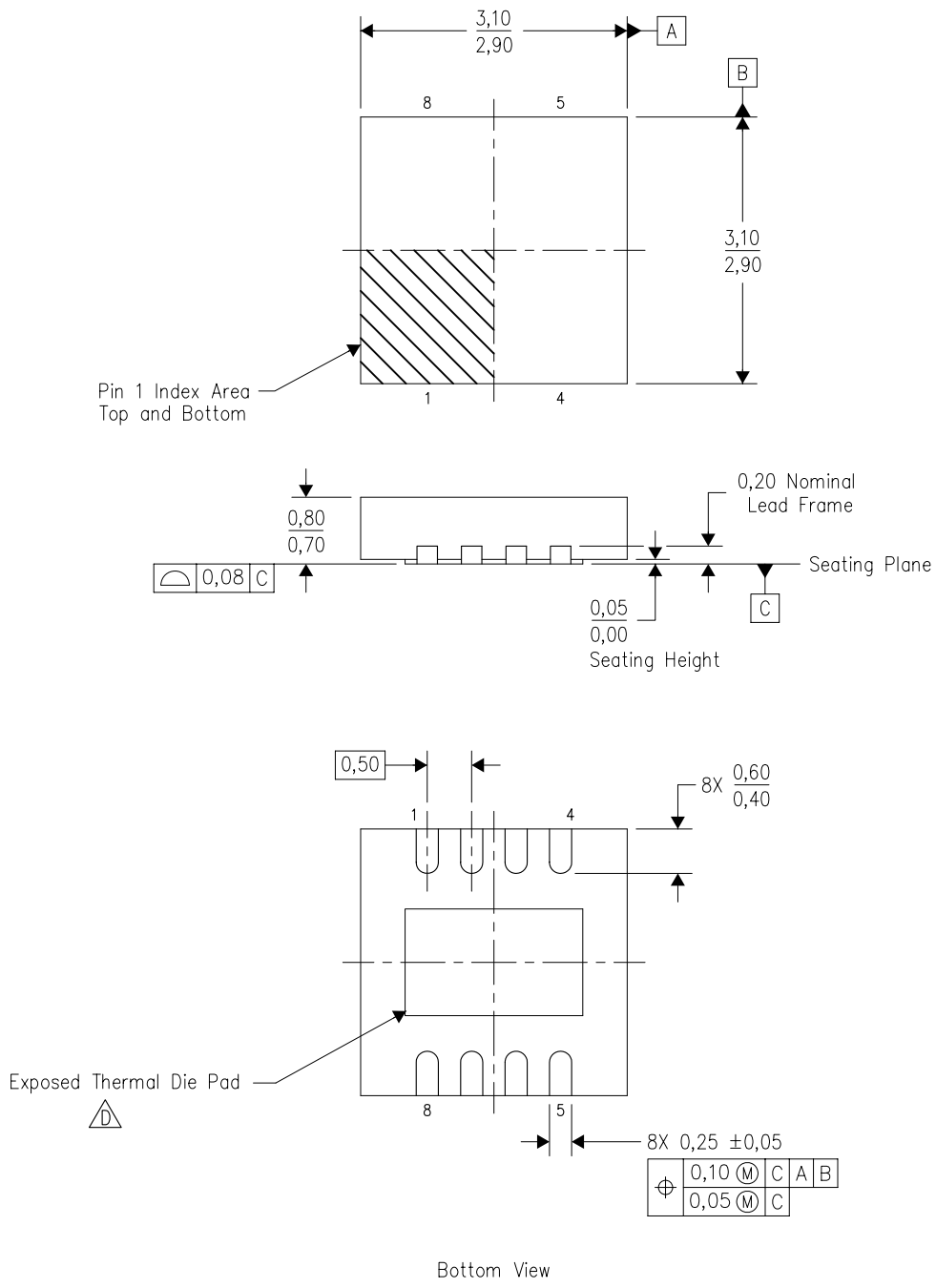
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22949ADRGR	SON	DRG	8	3000	367.0	367.0	35.0
TPS22949AYZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0
TPS22949YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. JEDEC MO–229 package registration pending.

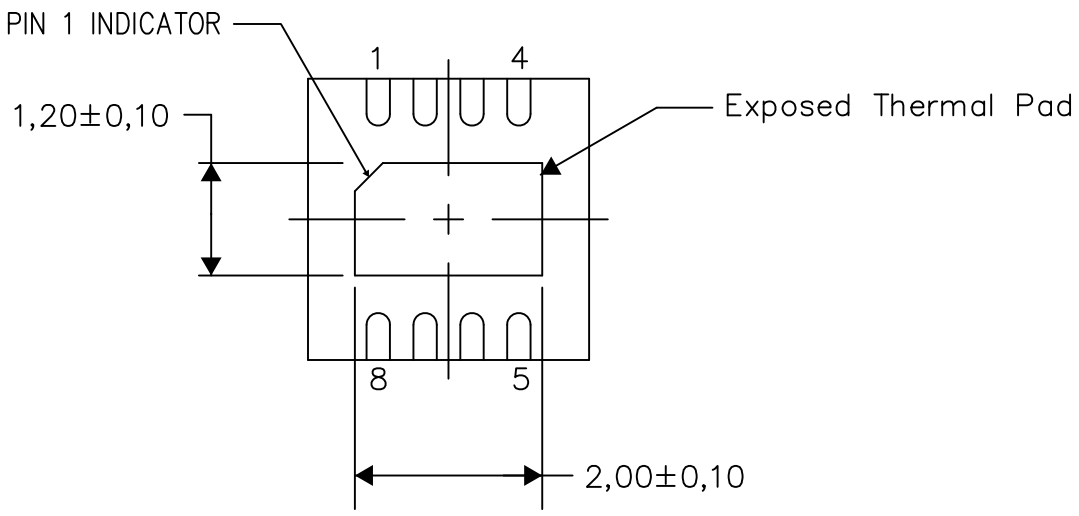
DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



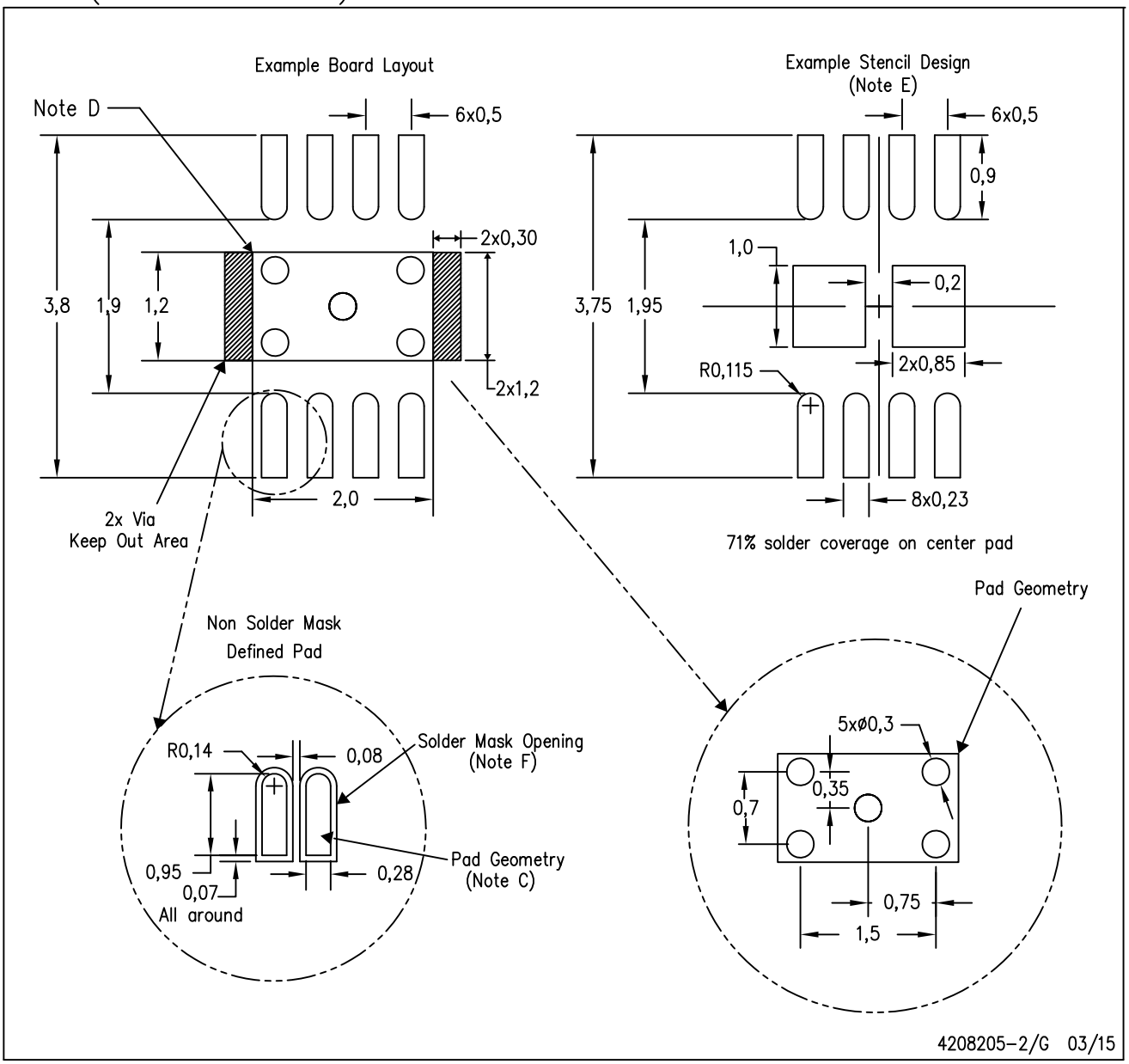
Bottom View

Exposed Thermal Pad Dimensions

4206881–2/I 03/15

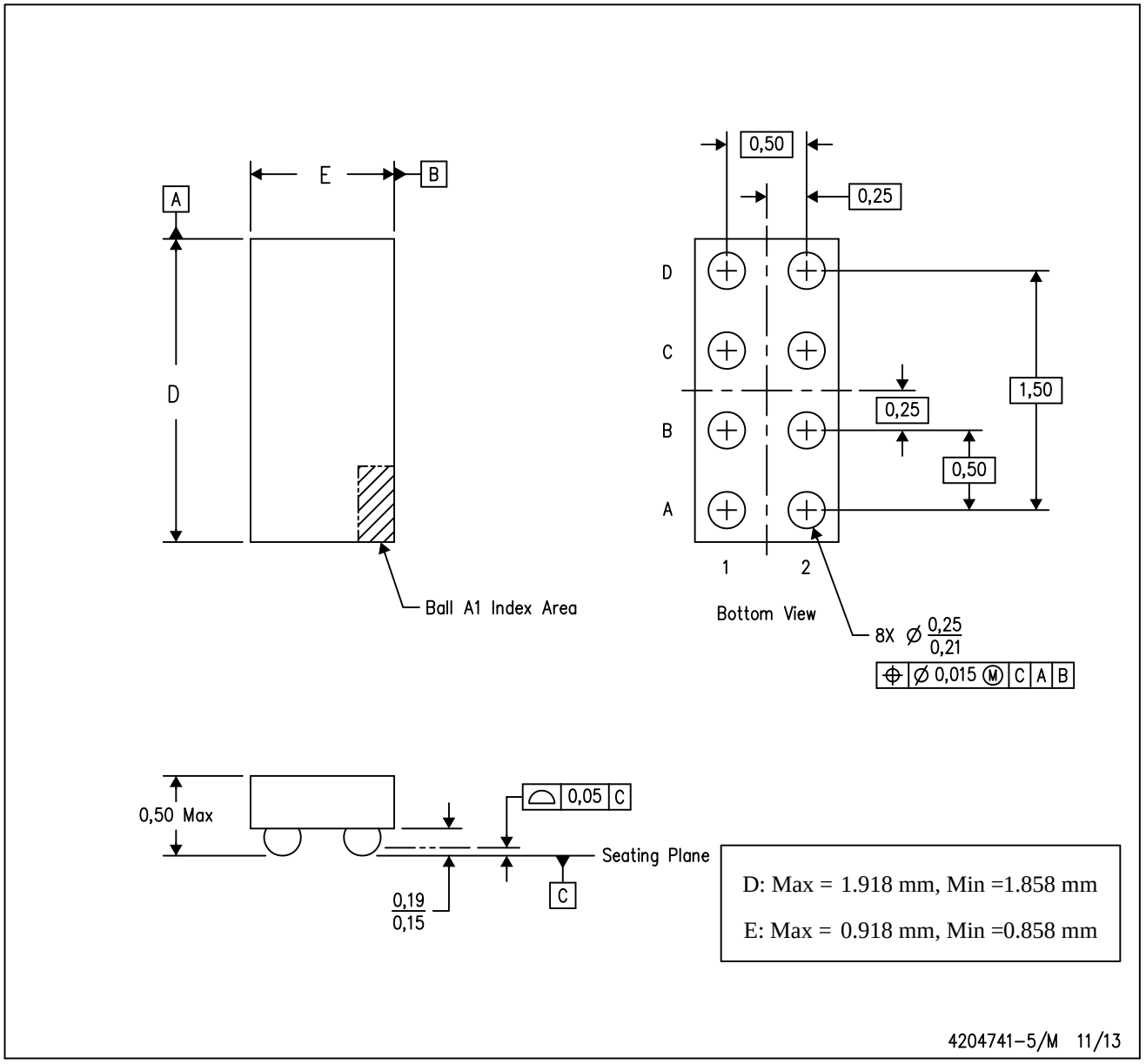
NOTE: All linear dimensions are in millimeters

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

YZP (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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