

Dual Mode CircLink™ Controller

Datasheet

PRODUCT FEATURES

- Low Power CMOS, 3.3 Volt Power Supply with 5 Volt Tolerant I/O
- Supports 8/16-Bit Data Bus
 - Both 86xx and 68hxx Platforms
- 1K On-chip Dual Port Buffer Memory
 - Sequential I/O Mapped Access
- Enhanced Token Passing Protocol from ARCNET
 - Maximum 31 Nodes per Network
 - Token Retry Mechanism
 - Maximum 256 Bytes per Packet
 - Consecutive Node ID Assignment
- Memory Mirror
 - Shared Memory within Network
- Network Standard Time
 - Network Time Synchronization
 - Automatic Time Stamping
- Coded Mark Inversion
 - Intelligent 1-Bit Error Correction
 - Magnetic Saturation Prevention
- Dual Operation Modes
 - Peripheral (Host) Mode Operates with MCU
 - Standalone (I/O) Mode Operates without MCU
- Supports 8 Bit Programmable General Purpose I/O at peripheral Mode
- Supports 16 Bit Input and 16 Bit Output at Standalone Mode
- Dual Communication Modes (with Peripheral Mode)
 - Free Format Mode
 - Remote Buffer Mode
- 3 Port Hub Integrated
 - 1 Internal and 2 External
- Flexible Topologies
 - Bus, Star and Tree
- Low Cost Media can be Used
 - RS485 Differential Driver
- Fiber Optics and Twisted Pair Cable Supported
- 128-Pin, VTQFP Lead-free RoHS Compliant Package
- Temperature Range from 0 to 70 Degrees C

ORDERING INFORMATION

Order Number(s):

TMC2074-NU for 128 Pin, VTQFP Lead-Free RoHS Compliant Package



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Table of Contents

| | | |
|------------------|--|-----------|
| Chapter 1 | General Description | 6 |
| 1.1 | About CirLink | 6 |
| 1.2 | About TMC2074 | 7 |
| 1.3 | Internal Block Diagram | 8 |
| 1.4 | Pin Configuration | 9 |
| 1.5 | Pin Description by Functions | 13 |
| 1.5.1 | CPU Interface Pins (27) | 13 |
| 1.5.2 | Transceiver Interface Pins (5) | 13 |
| 1.5.3 | Setup Pins (37) | 14 |
| 1.5.4 | External Output or I/O Pins (10) | 14 |
| 1.5.5 | Test Pins (5) | 15 |
| 1.5.6 | Clock Pins (3) | 15 |
| 1.6 | Setup Pins | 16 |
| 1.6.1 | CPU Type Selection | 16 |
| 1.6.2 | Address Multiplex Selection | 17 |
| 1.6.3 | Write Timing Selection | 18 |
| 1.6.4 | Read Timing Selection | 19 |
| 1.6.5 | Data Bus Width Selection | 20 |
| 1.6.6 | Data Bus Byte Swap | 20 |
| 1.6.7 | Data Strobe Polarity Specification | 20 |
| 1.6.8 | Page Size Selection | 21 |
| 1.6.9 | Maximum Node (MAXID) Number Setup | 21 |
| 1.6.10 | Node ID Setup | 21 |
| 1.6.11 | NST Resolution Setup | 22 |
| 1.6.12 | Standalone Mode Specification | 22 |
| 1.6.13 | Warning Timer Resolution/Standalone Sending Schedule Setup | 22 |
| 1.6.14 | Diagnosis Mode | 22 |
| 1.6.15 | Prescaler Setup for Communication Speed | 22 |
| 1.6.16 | NST Carry Output Digit Select | 23 |
| 1.6.17 | CMI Bypass Specification | 23 |
| 1.6.18 | HUB Function ON/OFF | 23 |
| 1.6.19 | Optical Transceiver Mode | 23 |
| 1.6.20 | TXEN Polarity Select | 24 |
| 1.6.21 | Extension Timer Setting 1 | 24 |
| 1.6.22 | Test Pins | 24 |
| Chapter 2 | Functional Description | 25 |
| 2.1 | Communication Specification | 25 |
| 2.2 | Message Class | 25 |
| 2.3 | CirLink Network Communication Protocol Overview | 26 |
| 2.4 | CirLink Protocol Enhancement | 27 |
| 2.4.1 | Reducing Token Loss | 27 |
| 2.4.2 | Reduction of Network Reconfiguration Time | 27 |
| 2.4.3 | Reduction of Reconfiguration Burst Signal Send Time | 28 |
| 2.5 | RAM Page Expansion | 28 |
| 2.5.1 | RAM Access | 29 |
| 2.5.2 | Packet Buffer Structure | 31 |
| 2.5.3 | Packet Data Structure | 32 |
| 2.6 | CPU Interface | 33 |
| 2.6.1 | CPU Identification and Compatibility between Intel and Motorola Processors | 33 |

| | | |
|------------------|---|-----------|
| 2.6.2 | Interface Restrictions | 34 |
| 2.7 | CircLink Operation and Communication Modes | 35 |
| 2.7.1 | Operational Mode | 35 |
| 2.7.2 | Communication Mode | 36 |
| 2.8 | Sending in Peripheral Mode | 38 |
| 2.8.1 | Example of Sending Control from CPU in Free Format Mode | 38 |
| 2.8.2 | TX Control from CPU in Remote Buffer Mode | 39 |
| 2.9 | Receive in Peripheral Mode | 39 |
| 2.9.1 | Temporary Receive and Direct Receive | 40 |
| 2.9.2 | Example of Receive Flow in Free Format Mode | 43 |
| 2.9.3 | Example of Receive Flow in Remote Buffer Mode | 44 |
| 2.9.4 | Warning Timer (WT) at Remote Buffer Receive | 44 |
| 2.10 | Standalone Mode | 47 |
| 2.10.1 | General Description of Standalone Mode | 47 |
| 2.10.2 | Sending in Standalone Mode | 47 |
| 2.10.3 | Reception in Standalone Mode | 50 |
| 2.11 | Diagnostic Mode | 54 |
| 2.12 | Network Standard Time (NST) | 55 |
| 2.12.1 | Functions Provided by NST | 55 |
| 2.12.2 | Time-synchronous Sequence | 56 |
| 2.12.3 | Phase Error | 57 |
| 2.12.4 | nNSTCOUT Pulse Generation Cycle | 60 |
| 2.13 | CMI Modem | 62 |
| 2.14 | HUB Function | 62 |
| 2.14.1 | Operation Example of HUB Function | 64 |
| 2.14.2 | Timer Expansion in Multi-stage Cascade Connection | 65 |
| 2.15 | 8-Bit General-purpose I/O Port (New function) | 66 |
| Chapter 3 | Description of Registers | 67 |
| 3.1 | Register Map | 67 |
| 3.2 | Details of Register | 70 |
| 3.2.1 | COMR0 Register: Status/interrupt Mask Register | 70 |
| 3.2.2 | COMR1 Register: Diagnostic/Command Register | 72 |
| 3.2.3 | COMR2 Register: Page Register | 74 |
| 3.2.4 | COMR3 Register: Page-internal Address Register | 75 |
| 3.2.5 | COMR5 Register: Sub-address Register | 77 |
| 3.2.6 | COMR6 Register: Configuration Register | 78 |
| 3.2.7 | COMR7 Register | 80 |
| 3.2.8 | NST Register: Network Standard Time | 84 |
| 3.2.9 | INTSTA Register: EC Interrupt Status | 84 |
| 3.2.10 | INTMSK Register: EC Interrupt Mask | 87 |
| 3.2.11 | ECCMD Register: EC Command Register | 88 |
| 3.2.12 | RSID Register: Receive SID | 89 |
| 3.2.13 | SSID Register: SID | 89 |
| 3.2.14 | RXFH Register: Receive Flag (higher side) | 90 |
| 3.2.15 | RXFL Register: Receive Flag (lower side) | 91 |
| 3.2.16 | CMID Register: Clock Master Node ID | 92 |
| 3.2.17 | MODE Register: Operation Mode Setup Register | 93 |
| 3.2.18 | CARRY Register: Carry Selection for External Output | 95 |
| 3.2.19 | RXMH register: Receive mode (higher side) | 96 |
| 3.2.20 | RXML Register: Receive Mode (lower side) | 97 |
| 3.2.21 | MAXID Register: Selection of Max. ID | 98 |
| 3.2.22 | NID Register: Selection of the Node ID | 98 |
| 3.2.23 | PS Register: Page Size Selection | 99 |

Datasheet

| | | |
|--|---|------------|
| 3.2.24 | CKP Register: Communication Rate Selection..... | 99 |
| 3.2.25 | NSTDIF Register: NST Phase Difference | 100 |
| 3.2.26 | PININFO Register: Pin Setup Information | 101 |
| 3.2.27 | ERRINFO Register: Error Information | 102 |
| A-1 Outline | | 104 |
| A-2 CMI Code | | 104 |
| A-3 CMI Modem Configuration | | 105 |
| A-4 CMITX Block | | 106 |
| A-5 CMIRX Block | | 107 |
| A-6 Details Regarding Reception | | 108 |

List of Figures

| | | |
|-----------|--|-----|
| Figure 1 | - TMC2074 Block Diagram | 8 |
| Figure 2 | - Pin Names: Pin Name in Peripheral Mode/Pin Name in Standalone Mode | 9 |
| Figure 3 | - Motorola CPU Mode (68hxx) | 16 |
| Figure 4 | - Intel CPU Mode (86xx) | 16 |
| Figure 5 | - Non-Multiplex Bus | 17 |
| Figure 6 | - Multiplex (Ale Falling-Edge Type) | 17 |
| Figure 7 | - Multiplex (Ale Rising-Edge Type) | 18 |
| Figure 8 | - Packet Structure of Free Format Mode (Example of 32 bytes/page) | 36 |
| Figure 9 | - Packet Structure of Remote Buffer Mode (Example of 32 bytes/page) | 37 |
| Figure 10 | - Data Import Timing in Standalone Mode and External Trigger Mode (Mode 3) | 49 |
| Figure 11 | - Transmission Packet Buffer Configuration (Mode 1, 2) | 49 |
| Figure 12 | - Transmission Packet Buffer Configuration (Mode 3) | 50 |
| Figure 13 | - Strobe Output Timing in Standalone Mode, External Trigger Mode (Mode 3) | 51 |
| Figure 14 | - Reception Packet Buffer Configuration (SPRE [2:0] = other than 111) | 52 |
| Figure 15 | - Reception Packet Buffer Configuration (SPRE [2:0]=111) | 53 |
| Figure 16 | - Internal 3 Port HUB Block Diagram | 63 |
| Figure 17 | - CMI Coding State transition diagram | 104 |
| Figure 18 | - CMI Modem Block Diagram | 105 |
| Figure 19 | - Example of Unstable Comparator Output | 108 |
| Figure 20 | - TMC2074 128 Pin Package Outline | 111 |
| Figure 21 | - Timing Measurement Points | 115 |

List of Tables

| | | |
|---------|--|-----|
| Table 1 | - Pin Lists Sorted by Function | 10 |
| Table 2 | - The Number of Nodes and RAM Page Size | 28 |
| Table 3 | - CPU Type | 33 |
| Table 4 | - Distinction and Matching of the CPU Type | 33 |
| Table 5 | - Page Format of Packet Buffer | 42 |
| Table 6 | - Transmission Period According to Timer Setup | 48 |
| Table 7 | - CirLink Register Map | 67 |
| Table 8 | - TMC2074 128 Pin Package Parameters | 111 |

Chapter 1 General Description

1.1 About Circlink

The Circlink networking controller was developed for small control-oriented local network data communication based on ARCNET's token-passing protocol that guarantees message integrity and calculatable maximum cycle time.

In a Circlink network, when a node receives the token it becomes the temporary master of the network for a fixed, short period of time. No node can dominate the network since token control must be relinquished when transmission is complete. Once a transmission is completed the token is passed on to the next node (logical neighbor), allowing it to become the master.

Because of this token passing scheme, maximum waiting time for network access can be calculated and the time performance of the network is predictable or deterministic. Control networking applications require predictable performance to ensure that controlled events occur when required. However, reconfiguration of a regular ARCNET network becomes necessary when the token is missed due to electronic and magnetic noise. In these cases, the maximum wait time for sending datagrams cannot be guaranteed and the real-time characteristic is impaired. Circlink makes several modifications to the original ARCNET protocol (such as maximum and consecutive node ID assignment) to avoid token missing as much as possible and reduce the network reconfiguration time.

Circlink implements other enhancements to the ARCNET protocol including a smaller-sized network, shorter packet size, and remote buffer mode operation that enable more efficient and reliable small, control-oriented LANs. In addition, Circlink introduces several unique features for reducing overall system cost while increasing system reliability.

Circlink can operate under a special mode called "Standalone" or "I/O" mode. In this mode, Circlink does not need an administrating CPU for each node. Only one CPU is needed to manage a Circlink network composed up to maximum 31 nodes, reducing cost and complexity.

In a Circlink network, the data sent by the source node is received by all other nodes in the network and stored according to node source ID. For the target node the received data is executed per ARCNET flow control and the data is stored in its buffer RAM. The receiving node processes the data while the remaining nodes on the network discard the data when the receiving node has completed. This memory-mirroring function assures higher reliability and significantly reduces network traffic.

Network Standard Time (NST) is also a unique Circlink feature. NST is realized by synchronizing the individual local time on each network node to the clock master in the designated node from which the packet is sent. Circlink also uses CMI code for transmitting signals, rather than the dipulse or bipolar signals that are the standard ARCNET signals. Since CMI encoding eliminates the DC element, a simple combination of a standard RS485 IC and a pulse transformer can be used to implement a transformer-coupled network.



1.2 About TMC2074

The TMC2074 network controller is CirLink technology's flagship product. The TMC2074's flexibility and rich feature set enable a high-reliability and high-performance, real-time and control-oriented network without the cumbersome middle layer protocol stacks and complex packet prioritization schemes typically required.

TMC2074 operates at network data transfer rates up to 5 Mbps. Its embedded 1 kByte RAM can be configured into a maximum of 32 pages to implement a 31-node network where each node in the network has the same local memory.

The TMC2074 has two operational modes: "Peripheral Mode" and "Standalone Mode". It can operate with or without the existence of a system CPU on a network node. In Peripheral Mode, the TMC2074 has two selectable communication modes, "Free Format Mode" and "Remote Buffer Mode". Free Format mode, retained from ARCNET, is "packet oriented" communication. Remote Buffer mode communication is a CirLink-specific feature, and is a token oriented communication, which includes automatic data transmission when the token arrives.

The TMC2074 has a flexible 8-bit or 16-bit databus to interface various CPU types including X86, 68XX, and SHX with multiplexed or non-multiplexed address/data. When operating in Peripheral mode, the TMC2074 has 8-bit programmable I/O available. When operating in Standalone mode, the TMC2074's I/O configuration is 16-bit. The TMC2074 also integrates a 3-port hub (two ports for external connection) to accommodate various network topologies (Bus, Star, etc.) and combinations.

1.3 Internal Block Diagram

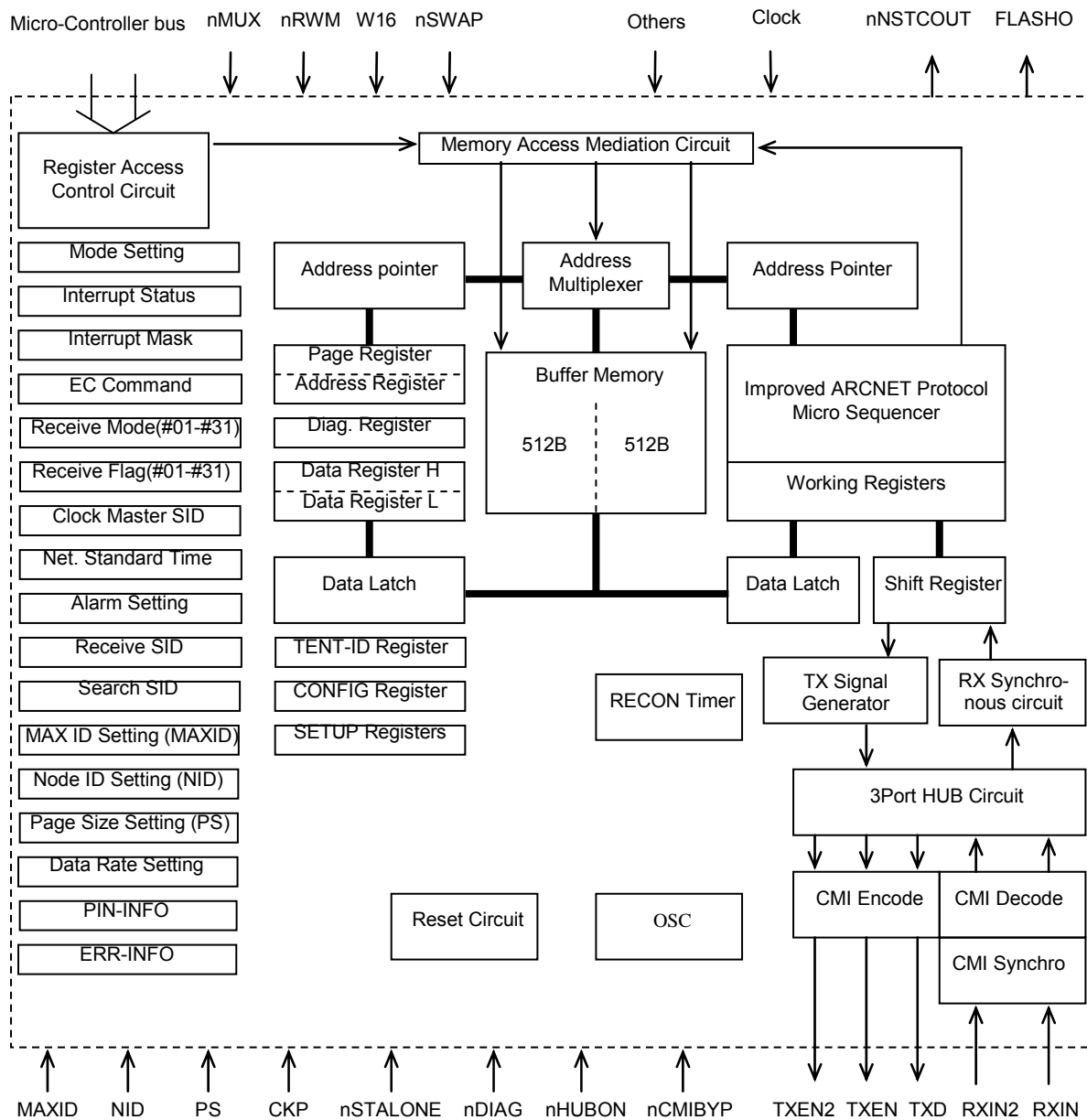


Figure 1 - TMC2074 Block Diagram

1.4 Pin Configuration

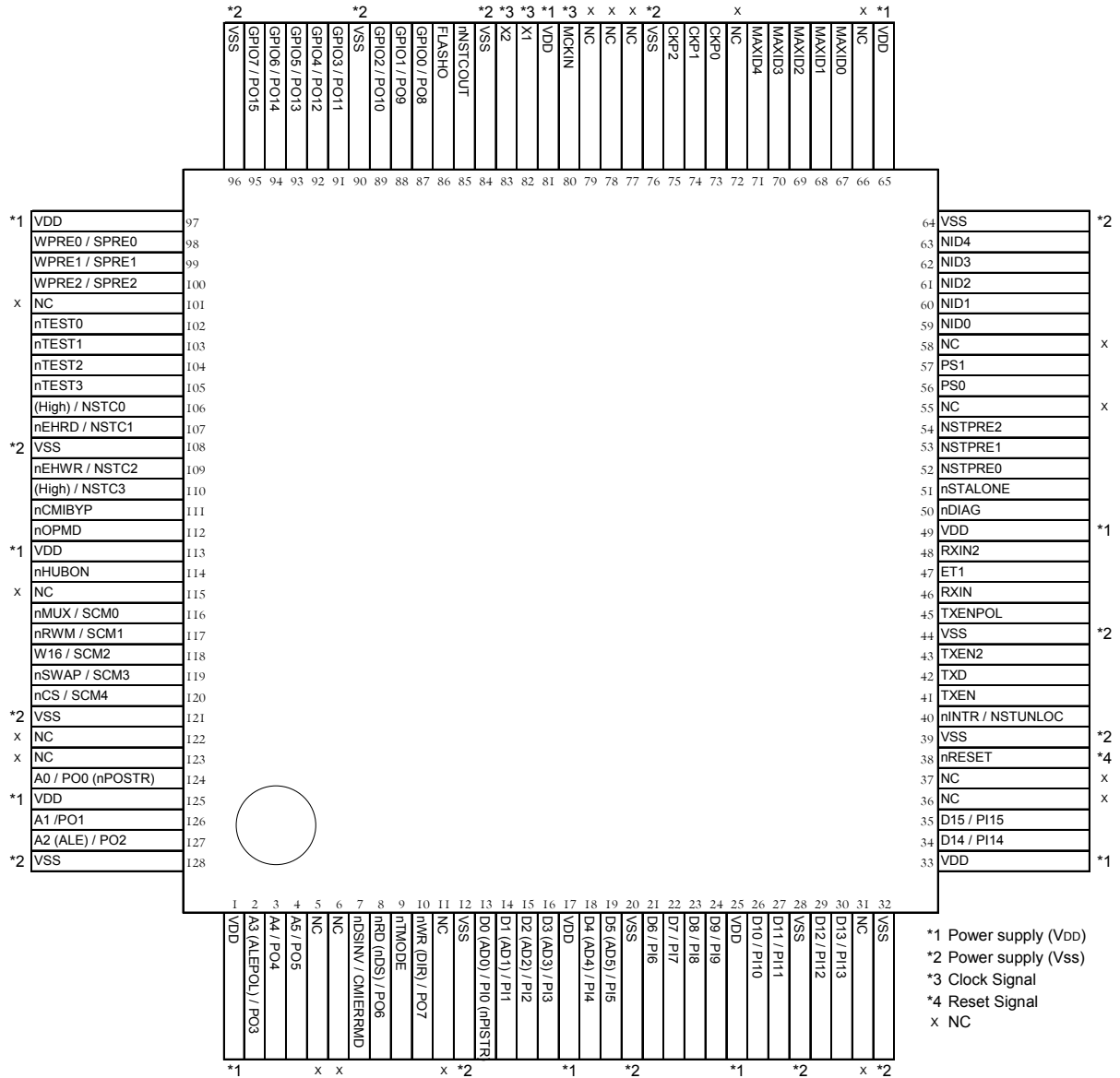


Figure 2 - Pin Names: Pin Name in Peripheral Mode/Pin Name in Standalone Mode

Table 1- Pin Lists Sorted by Function

| Pin | | Peripheral Mode | | Standalone Mode | | Input Buffer | | Output Buffer | |
|------------------------------|---------|-----------------|-----------|-----------------|-----------|--------------|-------|---------------|------|
| Count | Pin NO. | Pin Name | Direction | Pin Name | Direction | Pull-Up | Type | Drive | Type |
| CPU Interface | | | | | | | | | |
| 1 | 38 | nRESET | IN | nRESET | IN | Internal | T-NRM | --- | --- |
| 2 | 120 | nCS | IN | SCM4 | IN | Internal | T-NRM | --- | --- |
| 3 | 124 | A0 | IN | PO0/nPOSTR | 3s/O | Internal | T-NRM | 4mA | |
| 4 | 126 | A1 | IN | PO1 | 3s.O | Internal | T-NRM | 4mA | |
| 5 | 127 | A2/ALE | IN | PO2 | 3s.O | Internal | T-NRM | 4mA | |
| 6 | 2 | A3/ALEPOL | IN | PO3 | 3s.O | Internal | T-NRM | 4mA | |
| 7 | 3 | A4 | IN | PO4 | 3s.O | Internal | T-NRM | 4mA | |
| 8 | 4 | A5 | IN | PO5 | 3s.O | Internal | T-NRM | 4mA | |
| 9 | 8 | nRD/nDS | IN | PO6 | 3s.O | Internal | T-NRM | 4mA | |
| 10 | 10 | nWR/DIR | IN | PO7 | 3s.O | Internal | T-NRM | 4mA | |
| 11 | 13 | D0/AD0 | BI | PI0/nPISTR | IN | Internal | T-NRM | 4mA | |
| 12 | 14 | D1/AD1 | BI | PI1 | IN | Internal | T-NRM | 4mA | |
| 13 | 15 | D2/AD2 | BI | PI2 | IN | Internal | T-NRM | 4mA | |
| 14 | 16 | D3/AD3 | BI | PI3 | IN | Internal | T-NRM | 4mA | |
| 15 | 18 | D4/AD4 | BI | PI4 | IN | Internal | T-NRM | 4mA | |
| 16 | 19 | D5/AD5 | BI | PI5 | IN | Internal | T-NRM | 4mA | |
| 17 | 21 | D6 | BI | PI6 | IN | Internal | T-NRM | 4mA | |
| 18 | 22 | D7 | BI | PI7 | IN | Internal | T-NRM | 4mA | |
| 19 | 23 | D8 | BI | PI8 | IN | Internal | T-NRM | 4mA | |
| 20 | 24 | D9 | BI | PI9 | IN | Internal | T-NRM | 4mA | |
| 21 | 26 | D10 | BI | PI10 | IN | Internal | T-NRM | 4mA | |
| 22 | 27 | D11 | BI | PI11 | IN | Internal | T-NRM | 4mA | |
| 23 | 29 | D12 | BI | PI12 | IN | Internal | T-NRM | 4mA | |
| 24 | 30 | D13 | BI | PI13 | IN | Internal | T-NRM | 4mA | |
| 25 | 34 | D14 | BI | PI14 | IN | Internal | T-NRM | 4mA | |
| 26 | 35 | D15 | BI | PI15 | IN | Internal | T-NRM | 4mA | |
| 27 | 40 | nINTR | OUT | NSTUNLOC | OUT | --- | --- | 4mA | |
| Total:27 | | | | | | | | | |
| Transceiver Interface | | | | | | | | | |
| 1 | 46 | RXIN | IN | RXIN | IN | Internal | T-NRM | --- | --- |
| 2 | 41 | TXEN | OUT | TXEN | OUT | --- | --- | 4mA | |
| 3 | 42 | TXD | OUT | TXD | OUT | --- | --- | 4mA | |
| 4 | 48 | RXIN2 | IN | RXIN2 | IN | Internal | T-NRM | --- | --- |
| 5 | 43 | TXEN2 | OUT | TXEN2 | OUT | --- | --- | 4mA | |
| Total:5 | | | | | | | | | |
| Clock | | | | | | | | | |
| 1 | 82 | X1 | IN | X1 | IN | --- | --- | --- | --- |
| 2 | 83 | X2 | OUT | X2 | OUT | --- | --- | --- | --- |
| 3 | 80 | MCKIN | IN | MCKIN | IN | Internal | T-NRM | --- | --- |
| Total:3 | | | | | | | | | |

| Pin | | Peripheral Mode | | Standalone Mode | | Input Buffer | | Output Buffer | |
|-------------------|---------|-----------------|-----------|-----------------|-----------|--------------|-------|---------------|------|
| Count | Pin NO. | Pin Name | Direction | Pin Name | Direction | Pull-Up | Type | Drive | Type |
| Setup Pins | | | | | | | | | |
| 1 | 116 | nMUX | IN | SCM0 | IN | Internal | T-NRM | — | — |
| 2 | 117 | nRWM | IN | SCM1 | IN | Internal | T-NRM | — | — |
| 3 | 118 | W16 | IN | SCM2 | IN | Internal | T-NRM | — | — |
| 4 | 119 | nSWAP | IN | SCM3 | IN | Internal | T-NRM | — | — |
| 5 | 52 | NSTPRE0 | IN | NSTPRE0 | IN | Internal | T-NRM | — | — |
| 6 | 53 | NSTPRE1 | IN | NSTPRE1 | IN | Internal | T-NRM | — | — |
| 7 | 54 | NSTPRE2 | IN | NSTPRE2 | IN | Internal | T-NRM | — | — |
| 8 | 56 | PS0 | IN | PS0 | IN | Internal | T-NRM | — | — |
| 9 | 57 | PS1 | IN | PS1 | IN | Internal | T-NRM | — | — |
| 10 | 59 | ND0 | IN | ND0 | IN | Internal | T-NRM | — | — |
| 11 | 60 | ND1 | IN | ND1 | IN | Internal | T-NRM | — | — |
| 12 | 61 | ND2 | IN | ND2 | IN | Internal | T-NRM | — | — |
| 13 | 62 | ND3 | IN | ND3 | IN | Internal | T-NRM | — | — |
| 14 | 63 | ND4 | IN | ND4 | IN | Internal | T-NRM | — | — |
| 15 | 67 | MAXID0 | IN | MAXID0 | IN | Internal | T-NRM | — | — |
| 16 | 68 | MAXID1 | IN | MAXID1 | IN | Internal | T-NRM | — | — |
| 17 | 69 | MAXID2 | IN | MAXID2 | IN | Internal | T-NRM | — | — |
| 18 | 70 | MAXID3 | IN | MAXID3 | IN | Internal | T-NRM | — | — |
| 19 | 71 | MAXID4 | IN | MAXID4 | IN | Internal | T-NRM | — | — |
| 20 | 73 | CKP0 | IN | CKP0 | IN | Internal | T-NRM | — | — |
| 21 | 74 | CKP1 | IN | CKP1 | IN | Internal | T-NRM | — | — |
| 22 | 75 | CKP2 | IN | CKP2 | IN | Internal | T-NRM | — | — |
| 23 | 51 | nSTALONE+H | IN | nSTALONE+L | IN | Internal | T-NRM | — | — |
| 24 | 50 | nDIAG | IN | nDIAG | IN | Internal | T-NRM | — | — |
| 25 | 45 | TXENPOL | IN | TXENPOL | IN | Internal | T-NRM | — | — |
| 26 | 98 | WPRE0 | IN | SPRE0 | IN | Internal | T-NRM | — | — |
| 27 | 99 | WPRE1 | IN | SPRE1 | IN | Internal | T-NRM | — | — |
| 28 | 100 | WPRE2 | IN | SPRE2 | IN | Internal | T-NRM | — | — |
| 29 | 106 | Un-USE(Hgh) | IN | NSTC0 | IN | Internal | T-NRM | — | — |
| 30 | 107 | nEHRD | IN | NSTC1 | IN | Internal | T-NRM | — | — |
| 31 | 109 | nEHRV | IN | NSTC2 | IN | Internal | T-NRM | — | — |
| 32 | 110 | Un-USE(Hgh) | IN | NSTC3 | IN | Internal | T-NRM | — | — |
| 33 | 7 | nDSINV | IN | CMERRMD | IN | Internal | T-NRM | — | — |
| 34 | 111 | nCMBYP | IN | nCMBYP | IN | Internal | T-NRM | — | — |
| 35 | 114 | nHLBON | IN | nHLBON | IN | Internal | T-NRM | — | — |
| 36 | 112 | nOPMD | IN | nOPMD | IN | Internal | T-NRM | — | — |
| 37 | 47 | ET1 | IN | ET1 | IN | Internal | T-NRM | — | — |
| Total:37 | | | | | | | | | |

| Pin | | Peripheral Mode | | Standalone Mode | | Input Buffer | | Output Bufer | |
|---------------------------|--|-----------------|-----------|-----------------|-----------|--------------|-------|--------------|------|
| Count | Pin NO. | Pin Name | Direction | Pin Name | Direction | Pull-Up | Type | Drive | Type |
| Output or I/O Pins | | | | | | | | | |
| 1 | 85 | nNSTCOUT | OUT | nNSTCOUT | OUT | --- | --- | 4mA | |
| 2 | 86 | FLASHO | 3s.O | FLASHO | 3s.O | --- | --- | 4mA | |
| 3 | 87 | GPIO0 | 3s.O | PO8 | 3s.O | Internal | T-NRM | 4mA | |
| 4 | 88 | GPIO1 | 3s.O | PO9 | 3s.O | Internal | T-NRM | 4mA | |
| 5 | 89 | GPIO2 | 3s.O | PO10 | 3s.O | Internal | T-NRM | 4mA | |
| 6 | 91 | GPIO3 | 3s.O | PO11 | 3s.O | Internal | T-NRM | 4mA | |
| 7 | 92 | GPIO4 | 3s.O | PO12 | 3s.O | Internal | T-NRM | 4mA | |
| 8 | 93 | GPIO5 | 3s.O | PO13 | 3s.O | Internal | T-NRM | 4mA | |
| 9 | 94 | GPIO6 | 3s.O | PO14 | 3s.O | Internal | T-NRM | 4mA | |
| 10 | 95 | GPIO7 | 3s.O | PO15 | 3s.O | Internal | T-NRM | 4mA | |
| Total:10 | | | | | | | | | |
| Test Pins | | | | | | | | | |
| 1 | 102 | nTEST0 | IN | nTEST0 | IN | Nothing | T-NRM | --- | --- |
| 2 | 103 | nTEST1 | IN | nTEST1 | IN | Nothing | T-NRM | --- | --- |
| 3 | 104 | nTEST2 | IN | nTEST2 | IN | Nothing | T-NRM | --- | --- |
| 4 | 105 | nTEST3 | IN | nTEST3 | IN | Nothing | T-NRM | --- | --- |
| 5 | 9 | nTMODE | IN | nTMODE | IN | Internal | T-NRM | --- | --- |
| Total 5 | | | | | | | | | |
| Power Pins | | | | | | | | | |
| 1-10 | 1,17,25, 33,49,65 ,81,97, 113,125 | VDD | PWR | VDD | PWR | --- | --- | --- | --- |
| 11-24 | 12,20,28, 32,39,44, 64,76,84, 90,96,108 ,121,128 | VSS | PWR | VSS | PWR | --- | --- | --- | --- |
| Total 24 | | | | | | | | | |
| NC Pins | | | | | | | | | |
| 1-17 | 5,6,11,31, 36,37,55, 58,66,72, 77,78,79, 101,115, 122,123 | NC (Open) | --- | NC (Open) | --- | --- | --- | --- | --- |
| Total 17 | | | | | | | | | |

Total Pin = 128

(High) : Connect to VDD

(Open) : Not Connect

T-NRM TTL Level Input w/o schmitt

3s/O Tri-state Output or Normal Output

3s.O Tri-state Output

1.5 Pin Description by Functions

* A pin name starting with “n” indicates an active-low pin.

1.5.1 CPU Interface Pins (27)

| | |
|-------------------------|---|
| D[15:6]/PI[15:6] | Data Bus / Standalone Input Port (bit15-6) |
| D[5:1]/AD[5:1]/PI[5:1] | Data Bus / Address Data Bus / Standalone Input Port (bit5-1) |
| D[0]/AD[0]/PI[0]/nPISTR | Data Bus / Address Data Bus / Standalone Input Port (bit5-0) /Standalone strobe Input Port |
| nCS/SCM[4] | Chip Select Input / Standalone Designate CMID (bit4) |
| nWR/DIR/PO[7] | Write Signal Input / Access Direction / Standalone Input Port (bit7) |
| nRD/nDS/PO[6] | Read Signal Input / Data strobe / Standalone Input Port (bit6) |
| A[5:4]/PO[5:4] | Address Input / Standalone Input Port (bit5-4) |
| A[3]/ALEPOL/PO[3] | Address Input / ALE Designate Polarity / Standalone Output Port (bit3) |
| A[2]/ALE/PO[2] | Address Input / ALE / Standalone Output Port (bit2) |
| A[1]/PO[1] | Address Input / Standalone Output Port (bit1) |
| A[0]/PO[0]/nPOSTR | Address Input / Standalone Output Port (bit0) / Standalone strobe Input Port |
| nINTR/NSTUNLOC | Interrupt Output / NSTUNLOC Flag Output for Standalone |
| nRESET | Reset Input (Active Low) |

1.5.2 Transceiver Interface Pins (5)

| | |
|-------|---|
| RXIN | Port1 Receive Data Input |
| TXEN | Port1 Transmit Enable Output |
| TXD | Transmit Data Output (Port1 & 2 Common) |
| RXIN2 | Port2 Receive Data Input |
| TXEN2 | Port2 Transmit Enable Output |

1.5.3 Setup Pins (37)

| | |
|---------------------|---|
| nMUX/SCM[0] | Select Address Multiplex Mode/Standalone Designate CMID (bit0) |
| nRWM/SCM[1] | Select R/W Mode / Standalone Designate CMID (bit1) |
| W16/SCM[2] | Select Data Bus Width / Standalone Designate CMID (bit2) |
| nSWAP/SCM[3] | Select Swap Mode / Standalone Designate CMID (bit3) |
| nDSINV/CMIERMD | nDS Designate Polarity / Standalone CMI Receive Error Mode |
| PS[1:0] | Determine Page Size (*1) |
| NID[4:0] | Determine MyID Number (*1) |
| MAXID[4:0] | Determine MAXID Number (*1) |
| CKP[2:0] | Determine Data Rate (*1) |
| NSTPRE[2:0] | NST Resolution |
| nSTALONE | Select Standalone Mode |
| WPRE[2:0]/SPRE[2:0] | Select Warning Timer Resolution / Standalone TX Schedule |
| nDIAG | Select Diagnostics Mode |
| ET 1 | Determine ARCNET Extended Timer (*1) |
| NSTC[3] | Select NST Carry Output Digit in Standalone Mode bit[3] |
| nEHWR/NSTC[2] | Enhanced Write / NST Carry Output Digit in Standalone Mode bit[2] |
| nEHRD/NSTC[1] | Enhanced Read / NST Carry Output Digit in Standalone Mode bit[1] |
| NSTC[0] | NST Carry Output Digit in Standalone Mode bit[0] |
| TXENPOL | TXEN, TXEN2 Designate Polarity |
| nOPMD | Select Optical Transceiver Mode |
| nCMIBYP | Bypass CMI Modem |
| nHUBON | ON/OFF Determine of Internal HUB function |

(*1) Could be also determined by the register at the Peripheral Mode

1.5.4 External Output or I/O Pins (10)

| | |
|----------|--------------------------|
| nNSTCOUT | NST Carry Output |
| FLASHO | Outside Output for FLASH |

Datasheet

GPIO[7:0]/PO[15:8]

General-purpose I/O port (bit7-0) / Standalone Output Port (bit15-8)

1.5.5 Test Pins (5)

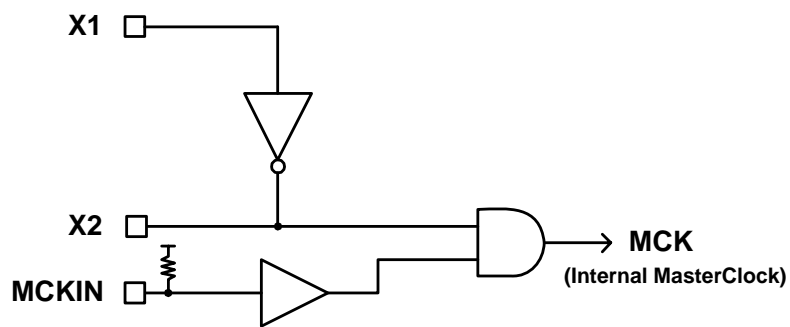
nTEST[3:0]

Test Pins

nTMODE

Test Mode

1.5.6 Clock Pins (3)



- Using an external clock :

X1 is connected to GND with MCKIN connected to the input of the external clock

- Using XTAL:

MCKIN is connected to VDD with X1 , X2 connected to the Crystal Oscillator

1.6 Setup Pins

Setup pins are strapped high or low to configure options according to system design. For low, strap to ground. Many pins have internal pullups on their input buffers. These pins can be left unconnected to keep them in high state.

1.6.1 CPU Type Selection

(nRWM/SCM[1]: Pin)

- Peripheral mode: This pin selects the CPU type; in this case, the definition of nWR/DIR (pin) and nRD/nDS (pin) are selected (refer to Figure 3 - Motorola CPU Mode (68hxx)).
- Standalone mode: This pin is the clock –master-ID-specification input SCM[1].

[nRWM=H, nDSINV=H]

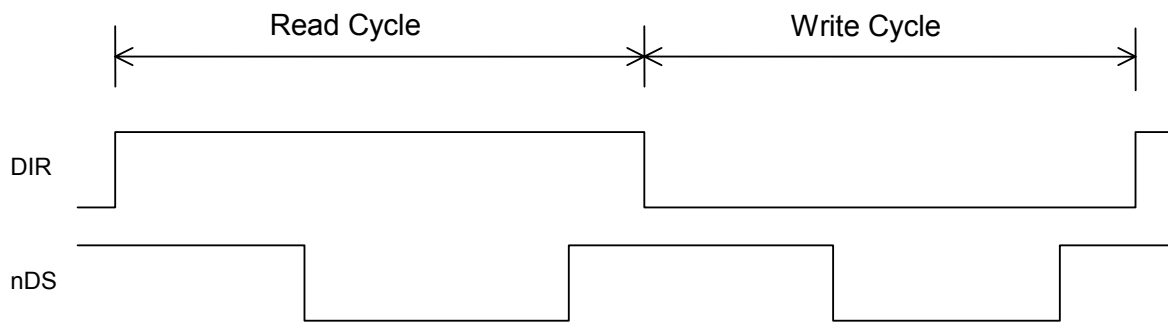


Figure 3- Motorola CPU Mode (68hxx)

[nRWM=L, nDSINV=L or H]

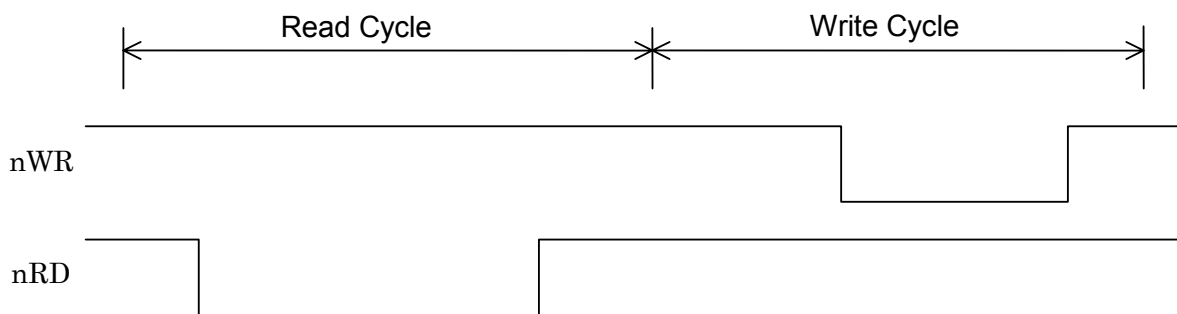


Figure 4 - Intel CPU Mode (86xx)

1.6.2 Address Multiplex Selection

(nMUX/SCM[0]: Pin)

In peripheral mode, this pin specifies the system data bus from bit5 to 0 and whether or not the addresses are multiplexed (Refer to Figure 5 - Non-Multiplex Bus). When the multiplexing bus option is selected, the polarity of A2/ALE is specified based on A3/ALEPOL. In standalone mode, this pin is the clock-master-ID-specification input SCM[0].

[In case of nMUX=H]

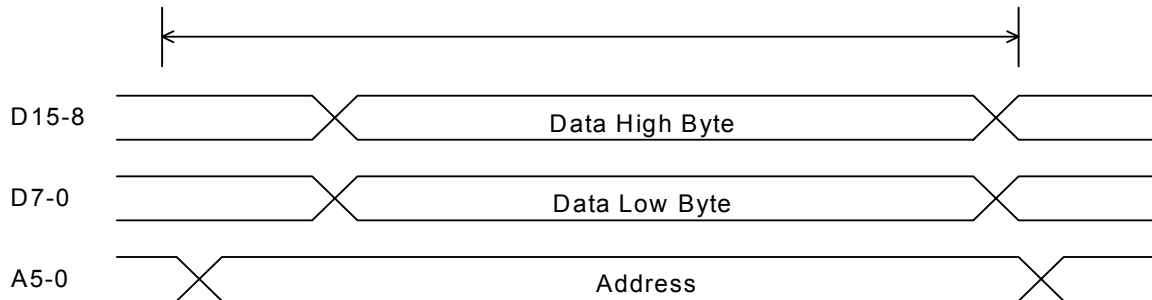


Figure 5 - Non-Multiplex Bus

[In Case of nMUX=L, ALEPOL=H]

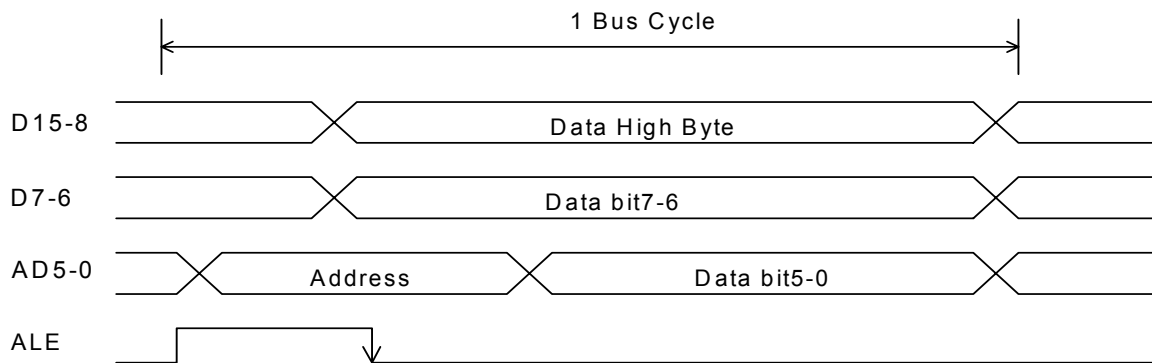


Figure 6 - Multiplex (Ale Falling-Edge Type)

[In case of nMUX=L, ALEPOL=L]

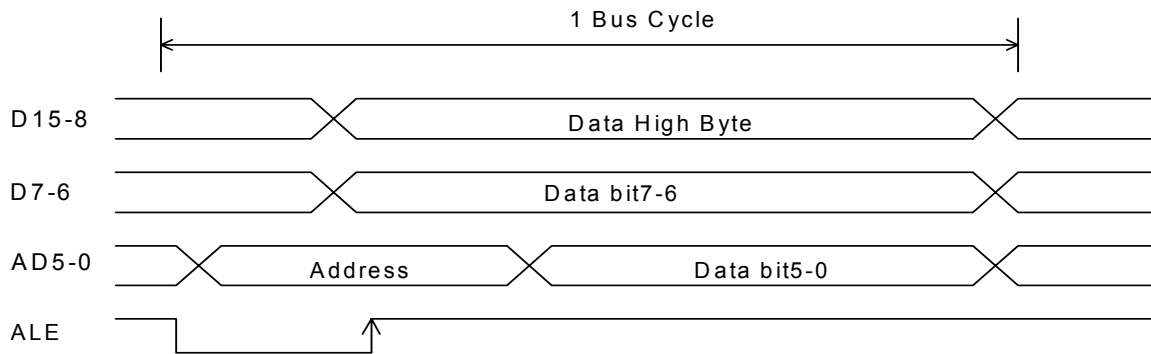


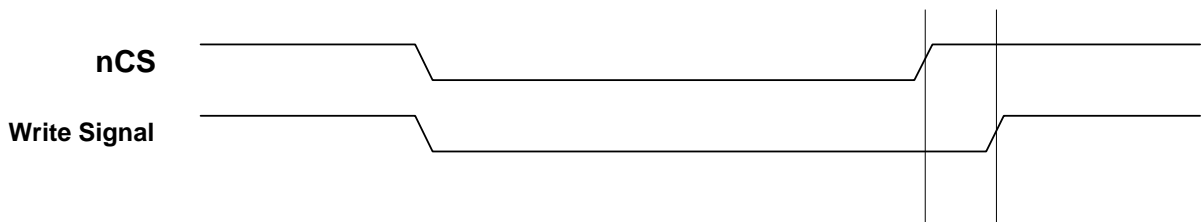
Figure 7 - Multiplex (Ale Rising-Edge Type)

1.6.3 Write Timing Selection

(nEHWR/NSTC[2]: Pin)

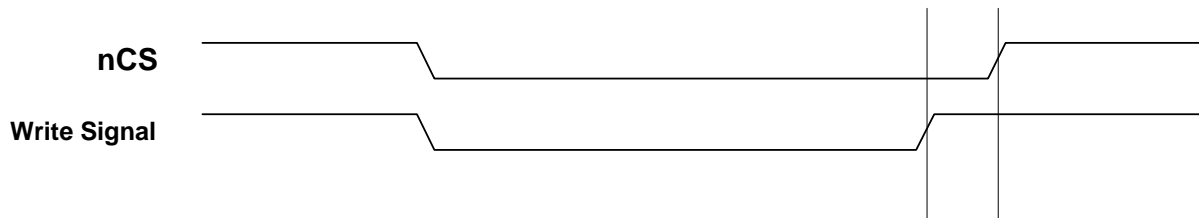
- Peripheral mode: This pin selects the write timing.
- Standalone mode: This pin is NST- carry-output-digit-selection NSTC[2].

[Example: nMUX=H,nEHWR=H]



Tie to Hi for CPU's where nCS goes Hi before the write signal goes Hi.

[Example: nMUX=H,nEHWR=L]



Tie to Low for CPUs where nCS goes Hi after the write signal goes Hi.

Datasheet

The write signal differs depending on the CPU type:

nRWM = H: nDS signal at DIR = L

nRWM = L: nWR signal

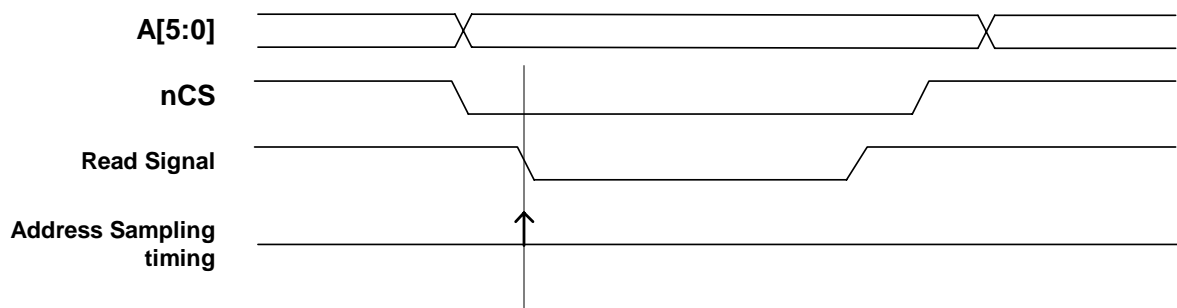
NOTE: Refer to the AC timing specifications (in another document) for details (setup time, hold time, etc.). Compare timing specifications for nEHWR=L and nEHWR=H.

1.6.4 Read Timing Selection

(nEHRD/NSTC[1]: Pin)

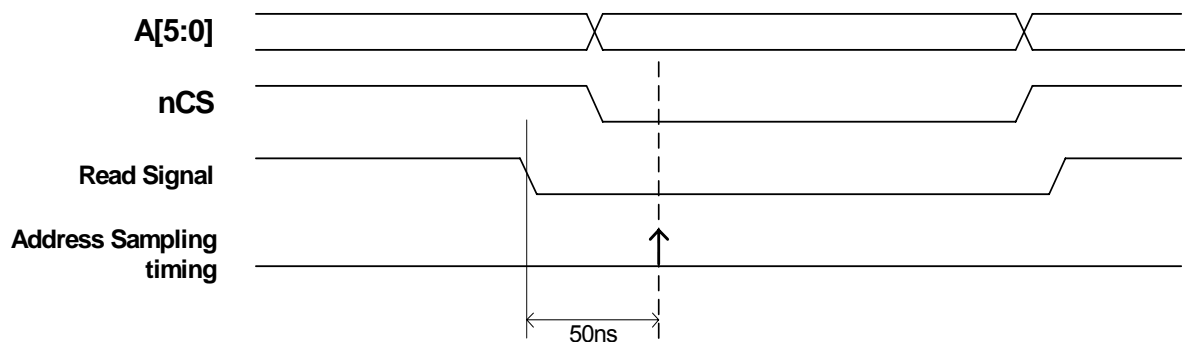
- Peripheral mode: This pin selects the read timing type.
- Standalone mode: This is NST- carry-output-digit selection NSTC[1].

[In case of nMUX=H,nEHRD=H]



Tie to Hi for CPUs with valid address before nCS and the read signal go low.

[Example: nMUX = H and nEHRD = L]



Tie to L for the CPU's where nCS is enabled and addresses are valid after the read signal goes low.

NOTE: Address acquisition timing in the CirLink delays about 50 ns (with 20 MHz-XTAL).

The read signal differs depending on the CPU type:

nRWM = H: nDS signal at DIR = H

nRWM = L: nRD signal

NOTE: Refer to the AC timing specifications (in another document) for details (setup time, hold time, etc.). Compare timing specifications for nEHRD=L and nEHRD=H.

1.6.5 Data Bus Width Selection

(W16/SCM[2]: Pin)

This pin selects the width of the data bus in the peripheral mode; H: 16-bit mode, L: 8-bit mode. In the 16-bit mode, the LSB address in the CirLink is fixed to 0. In the standalone mode, this pin is the clock-master-ID input pin SCM[2].

1.6.6 Data Bus Byte Swap

(nSWAP/SCM[3]: Pin)

In peripheral mode, this pin selects the data order at 8-bit access. Although the registers in the CirLink are defined as 16-bit width, 8-bit access is available, and in this case, the assignment of lower/upper byte of the register and odd/even number of addresses can be changed. The nSWAP=L assigns the lower byte to even number address/ upper byte to odd number address, and the nSWAP=H assigns the lower byte to odd number address /upper byte to even number address. In standalone mode, this pin is the clock master ID input SCM[3].

1.6.7 Data Strobe Polarity Specification

(nDSINV/CMIERRMD: pin)

In peripheral mode, this pin selects the pin polarity of data strobe (nDS). It is active low with nDSINV = H and active high with nDSINV = L. In standalone mode, this pin is equivalent to CMIERRMD (bit 12) in Mode Register. The packet receive stops upon the occurrence of a CMI receive error correction (CMIECC) with CMIERRMD = H.

1.6.8 Page Size Selection

(PS[1:0]: Pin/Register)

Select page size per packet. The maximum number of nodes depends on the page size selection since the packet buffer size is limited to 1 kByte. Page size can be selected by settings using register bits INIMODE (bit 9); 0: selects pin, 1: selects register (The default is 0).

| PS[1:0] | Page Size | Max Node Number |
|---------|-----------|-----------------|
| 00 | 256 Byte | 3 Node |
| 01 | 128 Byte | 7 Node |
| 10 | 64 Byte | 15 Node |
| 11 | 32 Byte | 31 Node |

1.6.9 Maximum Node (MAXID) Number Setup

(MAXID[4:0]: Pin/Register)

The maximum node ID is set based on the number of nodes on the network. All nodes in each CirLink network, therefore, should have the same maximum node ID. This minimizes the time required to reconfigure the network. There are two methods to specify the maximum node ID, Either through pin or register settings depending on INIMODE (bit 9); 0: selects pin, 1: selects register (The default is 0). If the nDIAG pin is set to L as the exception, however, the maximum node ID is automatically set to the largest value. For more details, refer to section 2.11 - Diagnostic Mode.

1.6.10 Node ID Setup

(NID[4:0]: Pin/Register)

Set node ID. A unique number must be assigned to each node in the network with ascending order starting from ID=01. ID = 00 and an ID larger than the maximum node ID are not valid. There are two methods to assign the node ID, either through pin or register, settings depending on INIMODE (bit 7) 0: selects pin, 1: select register (default is 0).

MAXID[4:0] determines the maximum node ID value. The token will be passed only around the nodes whose IDs are equal to or less than the maximum ID value. . In the CirLink network, a node whose MAXID[4:0] and NID[4:0] matches is the node initiating the token passing.. Even if this particular node is absent from the network, the network reconfiguration time is greatly reduced because the network will be only reconfigured by the nodes with IDs less than MAXID[4:0]. Since the maximum number of nodes is fixed to MAXID[4:0] in a CirLink network, the original priority timer of ARCNET, $(255 - ID) \times 146 \mu s^*$, which determines the time required for network reconfiguration, is modified to $(MAXID[4:0]-ID) \times 146 \mu s$, greatly reducing network reconfiguration time. Refer to section 2.4.2 - Reduction of Network Reconfiguration Time for more details.

* $146 \mu s$ is defined under operation at 2.5 Mbps based on ARCNET protocol. That number is half at 5 Mbps.

1.6.11 NST Resolution Setup

(NSTPRE[2:0]: Pin)

Select resolution of network standard time counter(NST) . Refer to section 2.12 - Network Standard Time (NST) for details.

1.6.12 Standalone Mode Specification

(nSTALONE: Pin)

This pin enables the Standalone mode operation of CirLink. Refer to section 2.10 - Standalone Mode for the details

1.6.13 Warning Timer Resolution/Standalone Sending Schedule Setup

(WPRE/SPRE[2:0]: Pin)

These pins select the warning timer resolution in peripheral mode and the transmit Schedule (include setup trigger mode) in standalone mode. Refer to sections 2.9.4 and 2.10 for more details.

1.6.14 Diagnosis Mode

(nDIAG: Pin)

This pin places CirLink in Diagnostic mode. It pulls nDIAG low, and sets the MAXID to “1Fh”. Refer to section 2.11 - Diagnostic Mode for the details.

1.6.15 Prescaler Setup for Communication Speed

Communication speed can be selected either through pin or register, depending on the specification of INIMODE (bit 9); 0: pin, 1: register (default is 0).

(CKP[2:0]: Pin/Register)

| CKP2-0 | Prescale | Communication Speed | | | |
|--------|----------|---------------------|------------|------------|------------|
| | | 40MHz XTAL | 20MHz XTAL | 32MHz XTAL | 16MHz XTAL |
| 000 | 8 | 5Mbps | 2.5Mbps | 4Mbps | 2Mbps |
| 001 | 16 | 2.5Mbps | 1.25Mbps | 2Mbps | 1Mbps |
| 010 | 32 | 1.25Mbps | 625Kbps | 1Mbps | 500Kbps |
| 011 | 64 | 625Kbps | 312.5Kbps | 500Kbps | 250Kbps |
| 100 | 128 | 312.5Kbps | 156.25Kbps | 250Kbps | 125Kbps |
| 101 | 256 | 156.25Kbps | 78.125Kbps | 125Kbps | 62.5Kbps |
| 110 | reserved | reserved | reserved | reserved | reserved |
| 111 | reserved | reserved | reserved | reserved | reserved |

1.6.16 NST Carry Output Digit Select

(NSTC[3], nEHWR/NSTC[2], nEHRD/NSTC[1], NSTC[0]: Pin)

These pins are equivalent to the same-symbol signal NSTC[3:0] (bit 7-4) of the carry register in Standalone mode. The output timing of external pulse nNSTCOUT is specified as an NST digit position. For the functions using Peripheral mode, refer to sections 1.6.3 and 1.6.4.

1.6.17 CMI Bypass Specification

(nCMIBYP: Pin)

Selects bypassing the CMI code/encoding. nCMIBYP = L bypasses the CMI coding/decoding circuit so that encoding is RZ form signal interface, equivalent to the ARCNET back plane mode.

1.6.18 HUB Function ON/OFF

(nHUBON: Pin)

Selects ON/OFF ; nHUBON=H selects HUB function OFF, nHUBON=L selects HUB function ON and enables port 2 (RXIN2 and TXEN2) (in nHUBON = H, RXIN2 should be fixed to High).

Refer to section 2.14 - HUB Function for the detailed operations.

1.6.19 Optical Transceiver Mode

(nOPMD: Pin)

Selects the output mode of the sending-enable; nOPMD = H makes the optical transceiver mode unavailable and allows the TXEN and TXEN2 output pins to function as “sending-enable”. Setting nOPMD = L allows TXEN and TXEN2 output pins to function as “sending-enable and sending pulse” to be able to be directly connected to the TTL input pin of the optical transceiver.

1.6.20 TXEN Polarity Select

(TXENPOL: Pin)

Selects the output polarities of the TXEN and TXEN2 signal. TXENPOL = L selects negative logic and TXENPOL = H positive logic.

1.6.21 Extension Timer Setting 1

(ET1: Pin/Register)

Refer to section 2.14 - HUB Function for operational details.

1.6.22 Test Pins

(nTEST[3:0], nTMODE: Pin)

All the pins must be connected to VDD.

Chapter 2 Functional Description

2.1 Communication Specification

- Data transfer bit rate 78.125 kbps to 2.5 Mbps (with 20 MHz Xtal, 5 Mbps with 40 MHz Xtal).
- The max. number of nodes 31 (ID = 00 is not available for use)
- Data transfer check Only the destination node can check data transfer. Other nodes, however, can receive (monitor) the same data.
- Protocol Enhanced version of ARCNET (token passing)
- Packet size 256 bytes max. (User area: 253 bytes max.)

2.2 Message Class

The following five classes of messages are identical to those in the ARCNET protocol. Refer to the ARCNET Controller COM20020 Rev. D datasheet for more information.

ITT (Token)

| | | | |
|-------|-----|-----|-----|
| ALERT | EOT | DID | DID |
|-------|-----|-----|-----|

FBE (Free Buffer Enquiries)

| | | | |
|-------|-----|-----|-----|
| ALERT | ENQ | DID | DID |
|-------|-----|-----|-----|

ACK (Acknowledgements)

| | |
|-------|-----|
| ALERT | ACK |
|-------|-----|

NAK (Negative Acknowledgements)

| | |
|-------|-----|
| ALERT | NAK |
|-------|-----|

PACKET (Data Packets)

| | | | | | | | | |
|-------|-----|-----|-----|-----|----|-------------------|-----|-----|
| ALERT | SOH | SID | DID | DID | CP | DATA X n | CRC | CRC |
|-------|-----|-----|-----|-----|----|-------------------|-----|-----|

N : MAX253
(ARCNET Layer)

2.3 CircLink Network Communication Protocol Overview

CircLink Protocol is derived from the ARCNET protocol. This section explains the ARCNET basic communication protocol.

A token (ITT: Invitation to Transmit) is a unique signaling sequence that is passed in an orderly fashion among all the active nodes in the network. When a particular node receives the token, it has the sole right to initiate a transmission sequence or it must pass the token to its logical neighbor. This neighbor can be physically located anywhere on the network and has the 2nd highest address. Once the token is passed to the recipient, it has the right to initiate transmission. This token-passing sequence continues in a logical ring fashion serving all nodes equally. Node addresses must be unique and can range from 0 – 255 with 0 reserved for broadcast messages. In a transmission sequence the node with the token becomes the source node and any other node selected becomes the destination node. First the source node inquires if the destination node is in a mode to receive a transmission by sending out a free buffer enquiry (FBE). The destination node responds by returning an Acknowledgement (ACK) meaning that the buffer is available or by returning a negative Acknowledgement (NAK) meaning that no buffer is available. Upon receiving the ACK, the source node sends out the data transmission (PAC) with either 0 – 507 bytes of data (PAC). If the data was properly received by the destination node as evidenced by a successful CRC test, the destination node sends another ACK. If the transmission was unsuccessful, the destination node does nothing causing the source node to timeout. The source node will therefore, infer that the transmission failed and will retry after it receives the token on the next token pass. The transmission sequence terminates and the token is passed to the next node. If the desired message exceeds 507 bytes the message is sent in a series of packets-one packet every token pass.

The ARCNET protocol comprises the reconfiguration process to ensure the complete token passing for every node linked to the network.

ARCNET has the ability to reconfigure the network automatically if a node is either added or removed from the network. If a node joins the network it does not automatically participate in the token passing sequence. Being excluded from receiving the token, the new node will generate a reconfiguration burst that destroys the token passing sequence. Once the token is lost all nodes will cease transmitting and begin a timeout sequence (Priority Timer, $(255-ID) \times 146 \mu s$), based on their own node address. The node (Node ID=N) with the highest address will timeout first and pass the token to the next higher address (Node ID=N+1). If that node does not respond, it is assumed that node does not exist. Then the node address is incremented (Node ID=N+2) and the token resent. This process is repeated until a node responds. At that time the token is released to the responding node and the address of the responding node is noted as the logical neighbor of the originating node. This process is repeated by all nodes until each node learns its logical neighbor. This eliminates wasting time in sending datagrams to absent addresses once the network has been re-established.

When a node leaves the network the reconfiguration process is slightly different. When a node releases the token to its logical neighbor, it expects its logical neighbor will respond within the response time out window (78 μs). If no response within the response time out window, it assumes that its neighbor has left the network and immediately begins a search for a new logical neighbor by incrementing the node address of its logical neighbor and initiating a token pass. Network activity is again monitored and the increment process and resending of the token continues until a new logical neighbor is found. Once found the network returns to the normal logical ring routine of passing token to logical neighbors.

These reconfiguration sequences of the network are automatic and seamless without software intervention required.



2.4 CirLink Protocol Enhancement

Since ARCNET communication is controlled by a token, token loss and the corresponding network reconfiguration significantly reduce network throughput. The CirLink controller design includes enhancements to and modifications of the ARCNET protocol to increase reliability and performance.

2.4.1 Reducing Token Loss

The burst signal is the primary cause of token loss. The burst signal is part of the sequence for new nodes joining the network as described in section 2.3. but with CirLink all nodes join the network at system start-up. If a node leaves the network due to token loss it can readily rejoin the network in the next polling with no burst necessary. In order to avoid this burst signal, the ARCNET protocol has been modified to specify node IDs as consecutive numbers starting from 01. When a node other than the node having the largest node ID (NID [4:0] and MAXID[4:0]) sends a token with the starting address being the node ID +1, the token can be received in the next polling, even if the node had previously dropped out of the network.

The token retry function added to CirLink greatly reduces the possibility of not receiving the response from the logical neighbor due to token corruption. CirLink node IDs are consecutive and since the retry does not occur under normal conditions, the token retry function does not degrade the total performance. This function can be set to ON or OFF using software settings (default is ON).

Another cause of token loss is the corruption of ACK/NAK. In the ARCNET flow control (refer to page 12 in the ARCNET controller COM20020I datasheet), if the source node receives signals other than the anticipated ACK/NAK response (such as noise or, data-deformed ACK/NAK and the like) from the destination node, the source node returns to the receive-wait state with a token being held by the node. The network considers this token loss because the token disappears from the network. To avoid this problem, the ARCNET protocol has been modified in CirLink to send a token even after the detection of ACK/NAK corruption. This function can be set to ON or OFF (default is ON).

2.4.2 Reduction of Network Reconfiguration Time

To reduce the required time of $(255 - ID) \times 146 \mu\text{s}^*$ during network reconfiguration, CirLink designates a node with the maximum ID as the maximum node (MAX_NODE). This node immediately starts sending tokens with destination numbers starting from 00. The token sent to 00 is not received by any node but triggers the other nodes to enter into the receive state after the $(255 - ID) \times 146 \mu\text{s}^*$ time is over. In addition, The $(255 - ID) \times 146 \mu\text{s}^*$ timer formula, derived from ARCNET, is modified to $(\text{The maximum number of nodes} - ID) \times 146 \mu\text{s}$ depending on the maximum number of nodes, which is specified by the MAXID [4:0] pin. This modification makes significantly reduces the time required for network reconfiguration even in the absence of the node designated as MAX_NODE.

* $146 \mu\text{s}$ is defined under operation at 2.5 Mbps based on ARCNET protocol. The time is half at 5 Mbps..

2.4.3 Reduction of Reconfiguration Burst Signal Send Time

Since the CirLink maximum packet size is smaller than ARCNET, the reconfiguration burst signal is of shorter duration, thus reducing the time required for network reconfiguration (as listed in the table below).

| CirLink | | |
|---------|-----------------|---------------------------|
| PS[1:0] | MAX Packet Size | Burst Signal Sending Time |
| 00 | 256(253)Byte | 1.63ms |
| 01 | 128(125)Byte | 1.07ms |
| 10 | 64(61)Byte | 0.79ms |
| 11 | 32(29)Byte | 0.65ms |

| ARCNET | | |
|--------|-----------------|---------------------------|
| -- | MAX Packet Size | Burst Signal Sending Time |
| -- | 512(508)Byte | 2.75ms |

() : Data Size

NOTE: "Burst Signal Sending Time" is the time under operation at 2.5 Mbps. The time is half at 5 Mbps.

2.5 RAM Page Expansion

The original ARCNET buffer RAM is divided into 256 or 512-bytes per page. This configuration has a maximum of four pages available in 1 kByte increments, leaving the majority of the RAM unused when small data packets are used. CirLink RAM addressing has been modified to significantly expand the number of pages available in RAM and to store pages corresponding to the node IDs on the network as listed in Table 2.

Table 2 - The Number of Nodes and RAM Page Size

| PAGE SIZE | PS[1:0] | NODE ID(MIN) ^{*1} | NODE ID(MAX) | PAGE ADDRESS |
|-----------|---------|----------------------------|--------------|--------------|
| 256 Byte | 00 | 01h | 03h | 100h X ID |
| 128 Byte | 01 | 01h | 07h | 80h X ID |
| 64 Byte | 10 | 01h | 0Fh | 40h X ID |
| 32 Byte | 11 | 01h | 1Fh | 20h X ID |

NOTE: ^{*1} : Node ID = 00 is used only for the system development and is not available for users.

2.5.1 RAM Access

The CPU accesses the packet buffer (RAM) through the COMR4 register. Prior to access, a read or write and the page number need to be specified using the COMR2 register, as well as the address specification in the page using the COMR3 register. The accessing method varies depending on the bit width of the data bus, word mode, and swap mode.

(1) Data bus = 16 bits (W16 pin=H)

COMR2 Register : RDDATA, AUTOINC, nWRAPAR, PAGE[4:0]

A/AD[5:0] = 04h

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|-----|------|------|---|---|---|---|---|
| - | - | - | - | - | - | - | - | RD. | A.I. | nW.A | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|-----|------|------|---|---|---|---|---|

COMR3 Register : Address Within a page RAMADR[7:0]

A/AD[5:0] = 06h

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| - | - | - | - | - | - | - | - | 7 | 6 | 5 | 4 | 3 | 2 | 1 | X |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

Bit0 is fixed in 0 in the inside.

COM4 Register : Packet Data RAMDT[15:0]

A/AD[5:0] = 08h

| | | | | | | | | | | | | | | | |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|

(2-a) Data bus = 8 bits , Word mode=OFF

(W16 pin=L, WDMD=0 in MODE REG.)

COMR2 Register : RDDATA AUTOINC nWRAPAR PAGE[4:0]

A/AD[5:0] = 04h (05h) *

| | | | | | | | |
|-----|------|------|---|---|---|---|---|
| RD. | A.I. | nW.A | 4 | 3 | 2 | 1 | 0 |
|-----|------|------|---|---|---|---|---|

COMR3 Register : Address within a page RAMADR[7:0]

A/AD[5:0] = 06h (07h) *

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|

COMR4 Register : Packet Data RAMDT[7:0]

A/AD[5:0] = 08h or 09h

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|

(*) : nSWAP=L

(2-b) Data bus = 8 bits , Word mode=ON

(W16 pin=L, WDMD=1 in MODE REG.)

COMR2 Register : RDDATA AUTOINC nWRAPAR PAGE[4:0]

A/AD[5:0] = 04h (05h) *

| | | | | | | | |
|-----|------|------|---|---|---|---|---|
| RD. | A.I. | nW.A | 4 | 3 | 2 | 1 | 0 |
|-----|------|------|---|---|---|---|---|

COMR3 Register : Address within a page RAMADR[7:0]

A/AD[5:0] = 06h (07h) *

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | X |
|---|---|---|---|---|---|---|---|

Bit0 is fixed in 0 in the inside.

COMR4 Register : Packet Data RAMDT[15:0]

A/AD[5:0] = 08h (09h) *

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|

A/AD[5:0] = 09h (08h) *

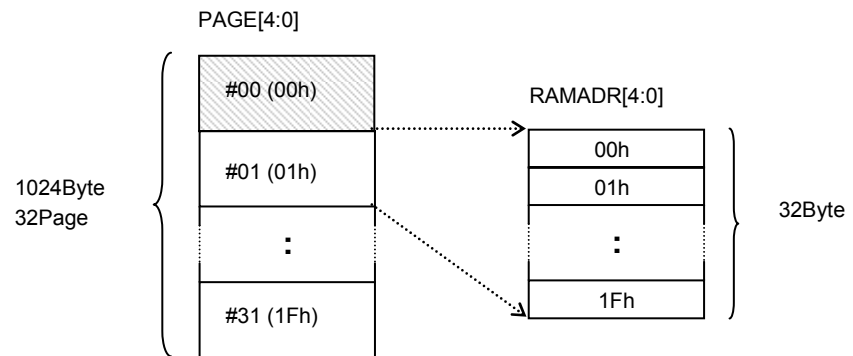
| | | | | | | | |
|----|----|----|----|----|----|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|----|----|----|----|----|----|---|---|

():nSWAP=L

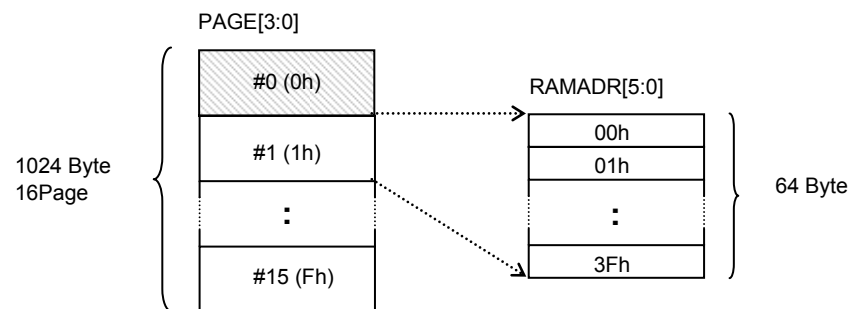
NOTE: In word mode = ON, to preserve the upper and lower bytes of word data, COMR4 must be accessed in order of 08h first and 09h second. This restriction applies to both read and write. Also, it is impossible to independently access the Continuation Pointer (CP address = 02h) in RAM independently To access the CP, a dummy cycle is necessary. Refer to section 2.5.3 - Packet Data Structure for detail.

2.5.2 Packet Buffer Structure

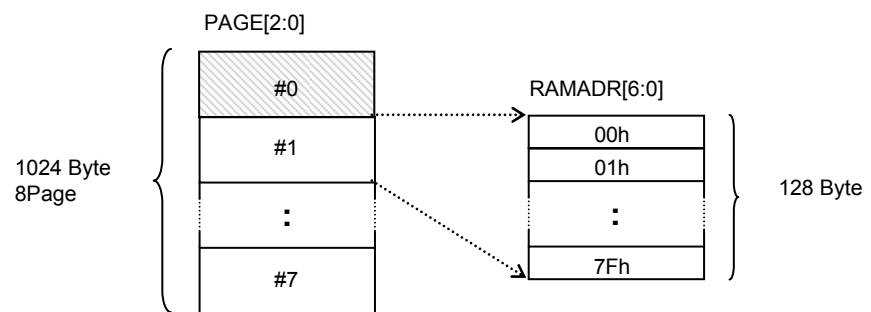
32 Byte Mode



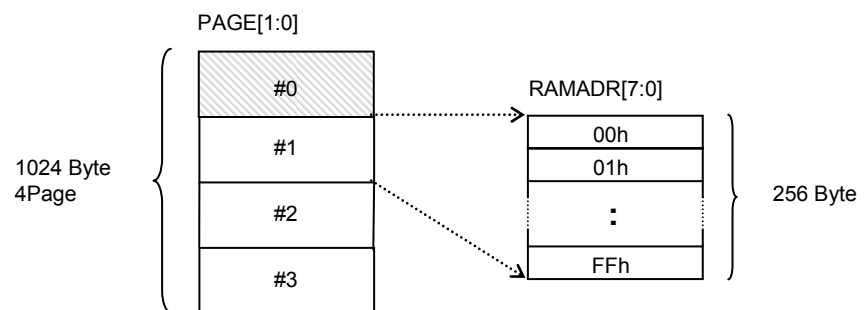
64 Byte Mode



128 Byte Mode



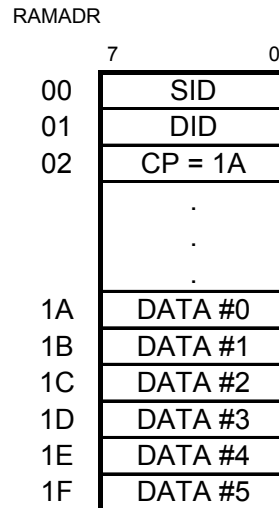
256 Byte Mode



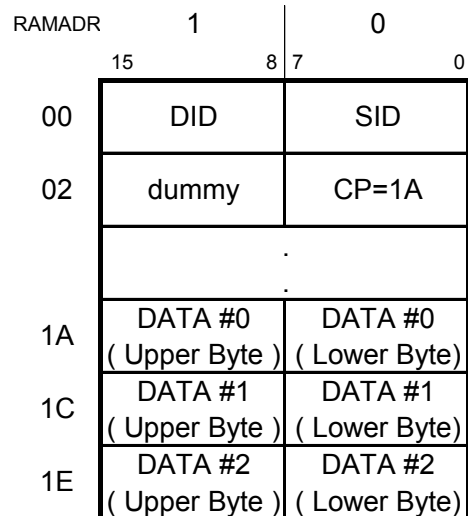
2.5.3 Packet Data Structure

PS = [1:0] = Example of 11 (32-byte mode)

8 bit constitution
(W16=L, WDMD=0)



16 bit constitution
(W16=L, WDMD=1 OR W16=H)



SID: Source-ID (Source node ID)

DID: Destination-ID (Destination node ID): DID=0 means the broadcast packet.

CP: Continuation pointer

Writes the value (Page size - N) for sending N-byte data. That is, it indicates the top position of data in the page. The example shows the value is 1Ah (32 - 6 bytes = 26 bytes = 1Ah).

NOTE: Limitations on the specifiable values for CP.

32B Mode (PS [1:0] = 11) : Values from 03h to 1Fh

64B Mode (PS [1:0] = 10) : Values from 03h to 3Fh

128B Mode (PS [1:0] = 01) : Values from 03h to 7Fh

256B Mode (PS [1:0] = 00) : Values from 03h to FFh

If a packet is sent with CP other than the specified value the destination node rejects the packet, and the session closes with a sending error (TXERR). Simultaneously the CP error (CPERR) flag of the EC status register is set, which can issue an interrupt. The error flag, however, means a setup or CP specification error to the CirLink, and does not indicate a network error.

Sender:

Sending error (TXERR) and CP error (CPERR) flags are set and a token is passed to the next node. Since TA flag is reset to 1 except in the remote buffer mode (TXM = 1) as well as the continuous send mode (RTO = 0), a send command must be issued for re-sending.

Receiver:

The receiver rejects the packet and goes back to idle state.

2.6 CPU Interface

2.6.1 CPU Identification and Compatibility between Intel and Motorola Processors

The CirLink controller can be connected to any combination of CPUs listed in Table 3 - CPU Type. For more information on setup, refer to section 1.6 - Setup Pins.

Table 3 - CPU Type

| ITEM | CONNECTION CPU TYPE | |
|---------------------|-------------------------------------|----------------------------------|
| | 16 BIT CPU | 8 BIT CPU |
| Address Multiplexed | Non-MUX / Multiplexed | Non-MUX / Multiplexed |
| Data Bus width | 8 bit/16 bit | 8 bit |
| Read / Write | nRD , nWRL OR DIR , nLDS(LDS) | nRD , nWR OR DIR , nDS(DS) |

Table 4 - Distinction and Matching of the CPU Type describes setup of pin functions of address bus/data, bus/read write controls by nRWM and nMUX pins.

Table 4- Distinction and Matching of the CPU Type

| Pin Name | Intel (80XX) Type | | Motorola (68XX) Type | |
|---------------|-------------------|--------|----------------------|---------|
| | nRWM = 0 | | nRWM=1 | |
| | nMUX=0 | nMUX=1 | nMUX=0 | nMUX=1 |
| D15 - D6 | D15-D6 | D15-D6 | D15-D6 | D15-D6 |
| D/AD5 - D/AD0 | AD5-AD0 | D5-D0 | AD5-AD0 | D5-D0 |
| A5-A4 | - | A5-A4 | - | A5-A4 |
| A3 | ALEPOL | A3 | ALEPOL | A3 |
| A2 | ALE | A2 | ALE | A2 |
| A1-A0 | - | A1-A0 | - | A1-A0 |
| nWR/DIR | nWR | nWR | DIR | DIR |
| nRD/nDS | nRD | nRD | nDS(DS) | nDS(DS) |

NOTE: Symbol definition in Table 4:

| | |
|---------|--|
| D | Data Bus |
| A | Address Bus |
| AD | Address / Data Bus |
| nWR | Write Signal (16 Bit CPU is nWRL) |
| nRD | Read Signal |
| DIR | Read / Write Signal |
| nDS(DS) | Data Strobe Signal (16 Bit CPU is nLDS) (Polarity is designated by nDSINV pin) |
| ALE | Address Latch Enable Signal |
| ALEPOL | Designate ALE polarity |

2.6.2 Interface Restrictions

Data Strobe signal using Motorola 16-bit CPU

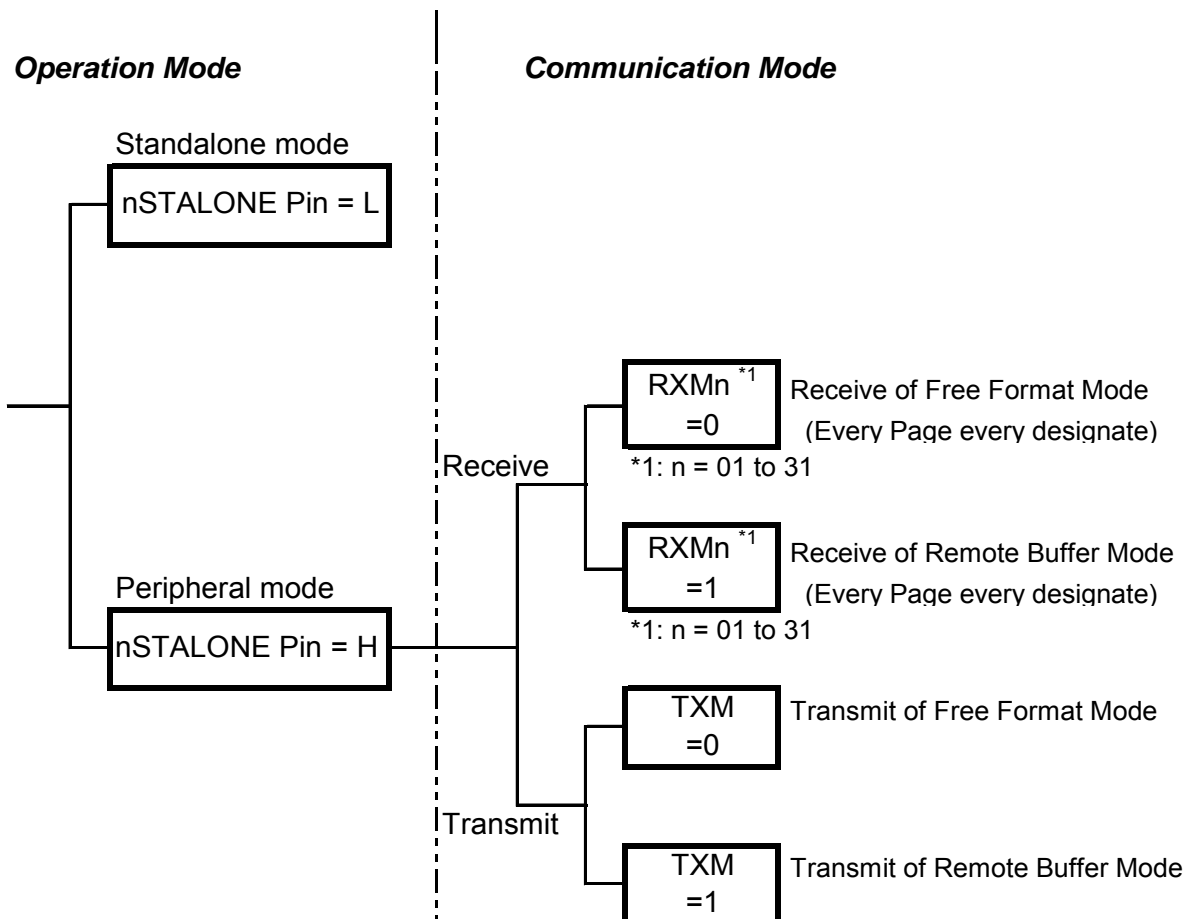
When executing word (16 bit) access to odd addresses by DIR and data strobe signals, the Motorola CPU does not discriminate between upper and lower data strobe signals. Because of this, it is necessary to OR the upper and lower data strobe signals to provide the data strobe input.

Data Transmission

When transmitting and receiving data of 8 bits and 16 bits, the transmitter node can send odd-numbered bytes but the receiving node can only implement word access (which is 16-bit), the word is read with one invalid upper data byte. To use the receive data function in a system, special care must be taken. This problem occurs only when the CP field value in the packet is an odd number.

2.7 CirLink Operation and Communication Modes

CirLink has two operation modes: Peripheral mode, which carries out communications in partnership with a system CPU, and Standalone mode, which enables communications by CirLink without a CPU. These modes can be switched by the nSTALONE pin. In the standalone mode, the pins for interfacing CPU are switched as ports for the external input/output and internal registers cannot be accessed. There are two communication modes in peripheral mode: Free format mode, which is capable of handling a free format packet, and Remote Buffer mode, which uses CirLink RAM as a simple buffer. The register bits RXM01 to RXM31 specify the RX mode of each page and TXM specifies the mode for TX mode.



2.7.1 Operational Mode

Peripheral mode

Peripheral mode acts as the system CPU's peripheral circuit and has two communication modes, Free Format mode and Remote Buffer mode. The communication mode is independently selectable for send and receive; TXM of mode register for sender and RXM01 to RXM31 of receive mode register for receive. The communication mode for sender and receiver must be identical and the communication mode of the receiver page should be adjusted to match the communication mode of the sender.

Standalone mode

In Standalone mode, Circlink independently executes send and receive sequences without a CPU. Refer to section 2.10 - Standalone Mode for more details.

2.7.2 Communication Mode

Free format mode

Free format mode is retained from the original ARCNET specification. This mode is optimal for transferring large amounts of data at once. CPU controls a series of sequence such as "Packet preparation → Issuing TX command → Interruption handling after the end of TX" at sender and "Receive command issuing → Interrupt handling after the end of RX → Packet read" at receiver.

Since Circlink initiates the actual TX upon receipt of a token addressed to the node, the time between a TX command being issued and TX starting varies depending on the line status. The free format mode is a "packet-oriented" transfer mode that assumes a completion of packet preparation before issuing a TX CMD, so its real-time performance is not as high as that of the remote buffer mode "token-oriented" mode. On the other hand, the free format mode has no limitation on the packet data structure, and it can handle free format packets. Moreover, communications in this mode are initiated only by writing a TX CMD, thereby reducing traffic on the network.

8 bit constitution
(W16=L, WDMD=0)

16 bit constitution
(W16=L, WDMD=1 OR W16=H)

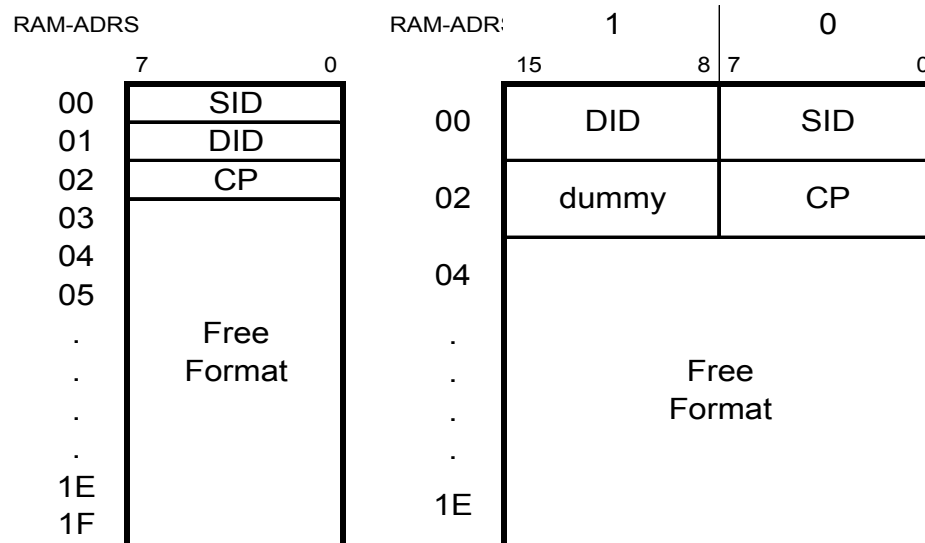


Figure 8 - Packet Structure of Free Format Mode (Example of 32 bytes/page)

Remote buffer mode

Remote Buffer mode, a Circlink enhancement, optimizes real-time performance. In this mode Circlink can be handled as a simple data buffer like "write data into the Circlink at any time" at a transmit node and "read data from the Circlink at any time" at a receiver node ".

Since the remote buffer mode is a "token-oriented" mode that features automatic transmission each time a node receives a token (= sending right), preparation of the packet header portion (SID, DID, and CP) is



required prior to issuing a TX CMD. The data portion of a packet must be valid in 8 or 16 bits. This mode restricts the data structure, but it is optimized in its real-time performance when compared to Free Format mode since it can always communicate with the packet data.

Setting RTO to 1 (Default = 0) in the mode register limits CirLink to one packet per TX CMD write. If RTO is switched to 1 while operating under RTO = 0, the automatic send operation is disabled immediately after the completion of the packet delivery.

8 bit constitution
(W16=L,WDMD=0)

| RAM-ADRS | 7 | 0 |
|----------|--------|---|
| 00 | SID | |
| 01 | DID | |
| 02 | CP=1A | |
| : | : | |
| : | : | |
| : | : | |
| 1A | BYTE#0 | |
| 1B | BYTE#1 | |
| 1C | BYTE#2 | |
| 1D | BYTE#3 | |
| 1E | BYTE#4 | |
| 1F | BYTE#5 | |

16bit constitution
(W16=L,WDMD=1 OR W16=H)

| RAM-ADR: | 1 | 0 |
|----------|--------------------------|--------------------------|
| | 15 | 8 7 0 |
| 00 | DID | SID |
| 02 | dummy | CP=1A |
| : | : | : |
| : | : | : |
| 1A | WORD#0 (Upper Byte) | WORD#0 (Lower Byte) |
| 1C | WORD#1 (Upper Byte) | WORD#1 (Lower Byte) |
| 1E | WORD#2 (Upper Byte) | WORD#2 (Lower Byte) |

Figure 9 - Packet Structure of Remote Buffer Mode (Example of 32 bytes/page)

In 16-bit constitution, upper and lower bytes in the same word are preserved as the same packet data (Refer to section 3.2.5 - COMR5 Register: Sub-address Register).

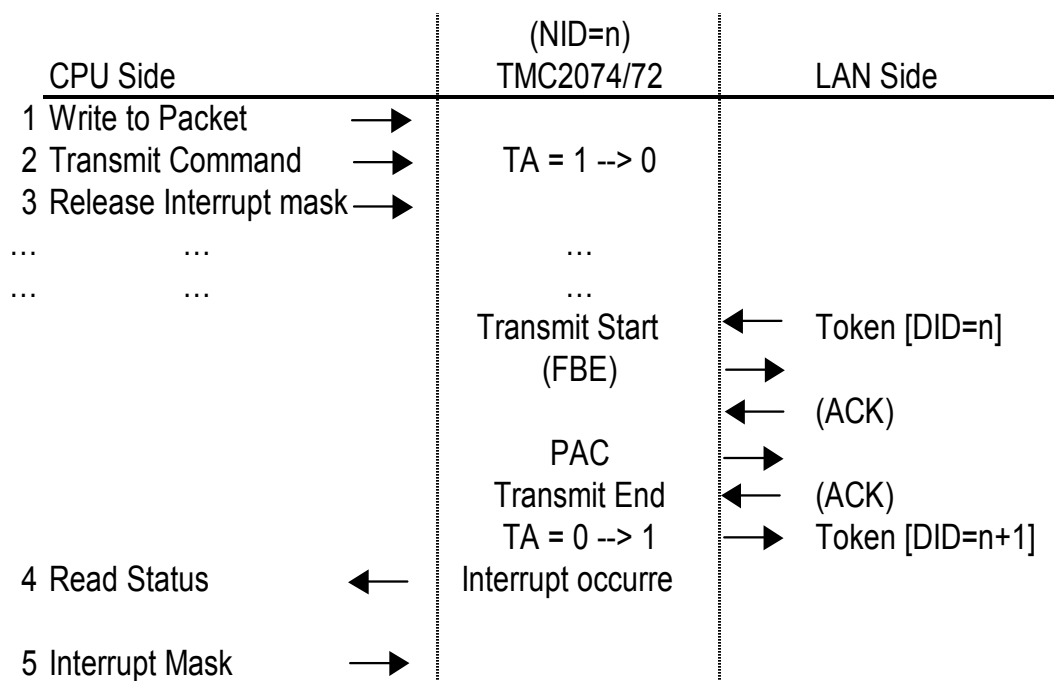
2.8 Sending in Peripheral Mode

To send data using CirLink, it is necessary to write data being transmitted in the packet buffer regardless of the communication mode. For TX, the page corresponding to its node ID in the packet buffer is assigned as the TX buffer. The CPU writes TX data on this page.

2.8.1 Example of Sending Control from CPU in Free Format Mode

(MODE REGISTER: TXM = 0)

The CPU manages all communication sequences such as "Packet preparation → Issuing TX CMD → Handling interrupt after the end of TX".



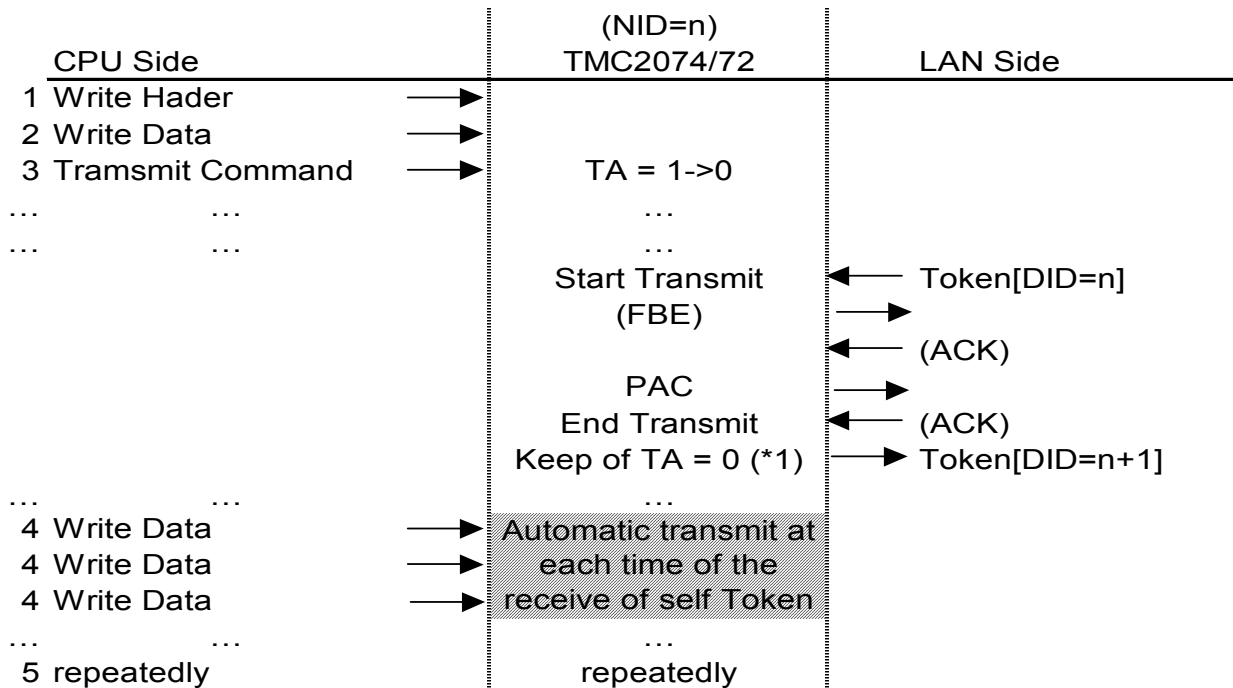
(): Not executed in the case of broadcast transmit.

NOTE: When DID set to 00h, it becomes the broadcast packet.

2.8.2 TX Control from CPU in Remote Buffer Mode

(MODE REGISTER: TXM = 1)

CirLink can be treated as a simple data buffer so that the system CPU can write data to the CirLink at any time.



(): Not done for broadcast transmission

NOTE: When DID is set to 00h, it becomes the broadcast packet.

(*1)

If the RTO bit is 0 in the mode register, CirLink continues sending packets with a single TX CMD. The TA bit that represents TX end, continues to be 0 unless RTO is set to 1 (constant TX status).

If the RTO bit is 1, the TA bit returns to 1 after each packet is transmitted, as in Free Format mode. TX CMD must be issued every time but this does not significantly increase traffic on the network, making it suitable for applications such as handling sensor information that remains fairly constant.

2.9 Receive in Peripheral Mode

CirLink receives all packet data on the network. After receiving a packet without any errors, CirLink stores the packets in the relevant page in RAM according to the source ID (SID) included in the packet. Receiving the data packet addressed to the node has four steps: Receiving FBE → Sending ACK → Receiving PACKET → Sending ACK. For receiving a data packet addressed to another node in the network, the packet is stored in the relevant page without sending an ACK.

As described above, Circlink constantly receives packets, with one exception: It abandons the received packets when the receive mode of the corresponding page is Free Format mode and the receive flag is set to 1 (Receive Inhibited). In this case, Circlink does not return an ACK even if the packet is addressed to the node (this case is handled as a receive error).

If the receive mode of the corresponding page is set to Remote Buffer mode, Circlink unconditionally stores packets in the corresponding page in the packet RAM as long as the received data is valid. The previous packet is overwritten and the newest packet is always stored in the packet RAM.

The meaning of the receive flag varies depending on the receive mode:

(1) Free Format receive mode

0: Receive wait or receiving

1: Receive is inhibited or receives is completed

(2) Remote Buffer receive mode

0: No receive in a certain period

1: One or more receive in a certain period

2.9.1 Temporary Receive and Direct Receive

Packets received are stored in the pages partitioned by the received source ID (received SID). There are two methods for storing packets: storing after error checking through a temporary buffer (#00), and storing directly. The decision of which process is used is automatically selected in Circlink based on the combination of page size and communication speed prescaler setting. The smaller the page size or the larger the division ratio of the transfer rate prescaler, the more data packets will be received through the temporary buffer.

| Prescale | | | Page Size Setting? PS[1:0] | | | |
|----------|------------------------|-------------------------|----------------------------|--------|---------|---------|
| CKP[2:0] | Bit Rate : Input clock | Communication Speed | 11:32B | 10:64B | 01:128B | 00:256B |
| 000 | 1:8 | 2.5 Mbps : 20 MHz Xtal | 0 | 0 | % | X |
| 001 | 1:16 | 1.25 Mbps : 20 MHz Xtal | 0 | 0 | 0 | % |
| 010 | 1:32 | 625 kbps : 20 MHz Xtal | 0 | 0 | 0 | 0 |
| CKP>=011 | 1:64 over | Omission | 0 | 0 | 0 | 0 |

0 : Receive through temporary buffer available

X : Receive through temporary buffer not available

% : Receive through temporary buffer available with condition

see paragraph below.

In the table above, “ % ” indicates “Temporary Relay Reception is not available in the default setting. However, by setting the FARB Bit = 1 in register, Setup 2 temporary relay reception is available. The FARB Bit = 1 setting is possible when the FARB bit default is 0 and only when the input clock is below 20 MHz.”

Datasheet

When the clock exceeds 20 MHz, it should not be set to 1. Also, FARB Bit renewal must be carried out during software reset.

In temporary buffer receive mode, the packet data containing any errors is left at page 00 if the receive terminates abnormally (CRC error, etc.). The copy to "SID page" corresponding to the received source ID (Receive SID) is not executed (the received data is discarded).

In direct receive mode, the packet data containing errors is left at "SID page" even if the receive terminates abnormally (CRC error, etc.).

Regardless of whether the receive is done through temporary buffer or direct receive, the RXF# flag upon abnormal termination of receive is set to 0 (not completed). It does not matter which receive process is being used because free format mode assumes that the receive is always checked with the RXF# flag. *¹

On the contrary, the receive process is important in the remote buffer receive mode with direct receive. *²
In the worst case, if SID is corrupted in the received packet, the packet data may be written to the wrong page.

| Receive structure | Receive Mode RXM[31:01] | |
|---------------------------|-------------------------|------------------|
| | 0: Free Format | 1: Remote Buffer |
| Temporary routing receive | ○ | ○ |
| Direct receive | ○ * ¹ | X * ² |

○: receive data reliable

X: receive data unreliable

Table 5 - Page Format of Packet Buffer

[NID[4:0]=11110, PS[1:0]=11 : 32Byte/Page]

| RAM Address | Page | Usage |
|-------------|------|------------------------------|
| 000 – 01F | #01 | Temporary buffer for receive |
| 020 – 03F | #01 | Data from Node01 |
| : | : | : |
| 3A0 – 3BF | #29 | Data from Node29 |
| 3C0 – 3DF | #30 | Buffer for transmit |
| 3E0 – 3FF | #31 | Data from Node31 |

[NID[4:0]=X1110, PS[1:0]=10 : 64Byte /Page]

| RAM Address | Page | Usage |
|-------------|------|------------------------------|
| 000 - 03F | #00 | Temporary buffer for receive |
| 040 - 07F | #01 | Data from Node01 |
| : | : | : |
| 340 – 37F | #13 | Data from Node13 |
| 380 – 3BF | #14 | Buffer for transmit |
| 3C0 – 3FF | #15 | Data from Node15 |

[NID[4:0]=XX110, PS[1:0]=01 : 128Byte/Page]

| RAM Address | Page | Usage |
|-------------|------|------------------------------|
| 000 – 07F | #00 | Temporary buffer for receive |
| 080 – 0FF | #01 | Data from Node01 |
| : | : | : |
| 280 – 2FF | #05 | Data from Node05 |
| 300 – 37F | #06 | Buffer for transmit |
| 380 – 3FF | #07 | Data from Node07 |

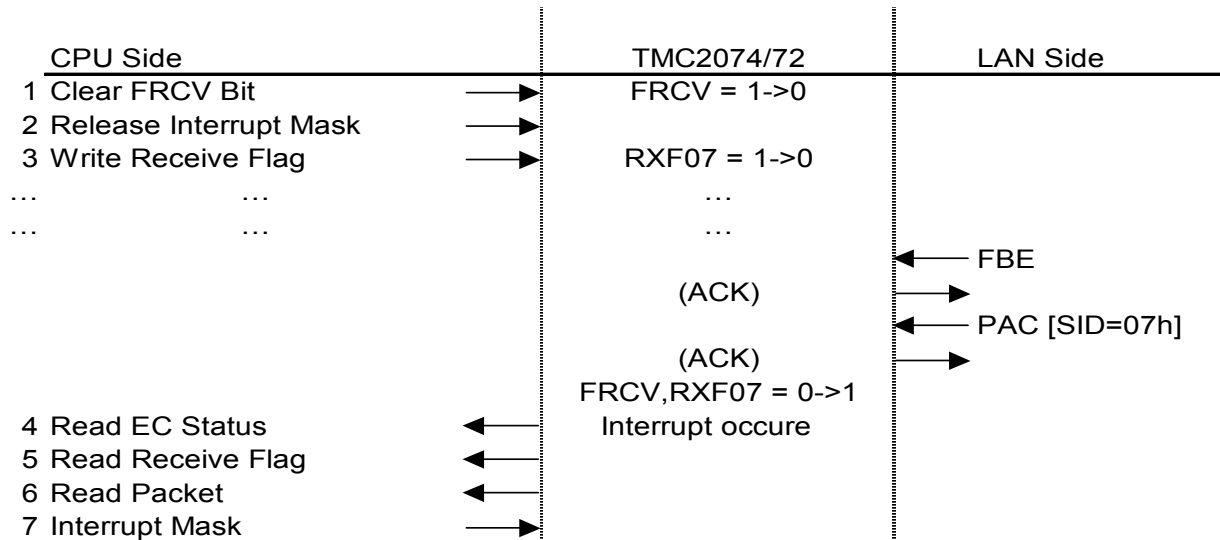
[NID[4:0]=XXX10, PS[1:0]=00 : 256Byte/Page]

| RAM Address | Page | Usage |
|-------------|------|------------------------------|
| 000 – 0FF | #00 | Temporary buffer for receive |
| 100 – 1FF | #01 | Data from Node01 |
| 200 – 2FF | #02 | Buffer for transmit |
| 300 – 3FF | #03 | Data from Node03 |

2.9.2 Example of Receive Flow in Free Format Mode

(RXMH/RXML REGISTER: When in RXM07 = 0)

A CPU controls a series of sequence such as "Issuing RX CMD → Handling interrupt after RX → Packet read":



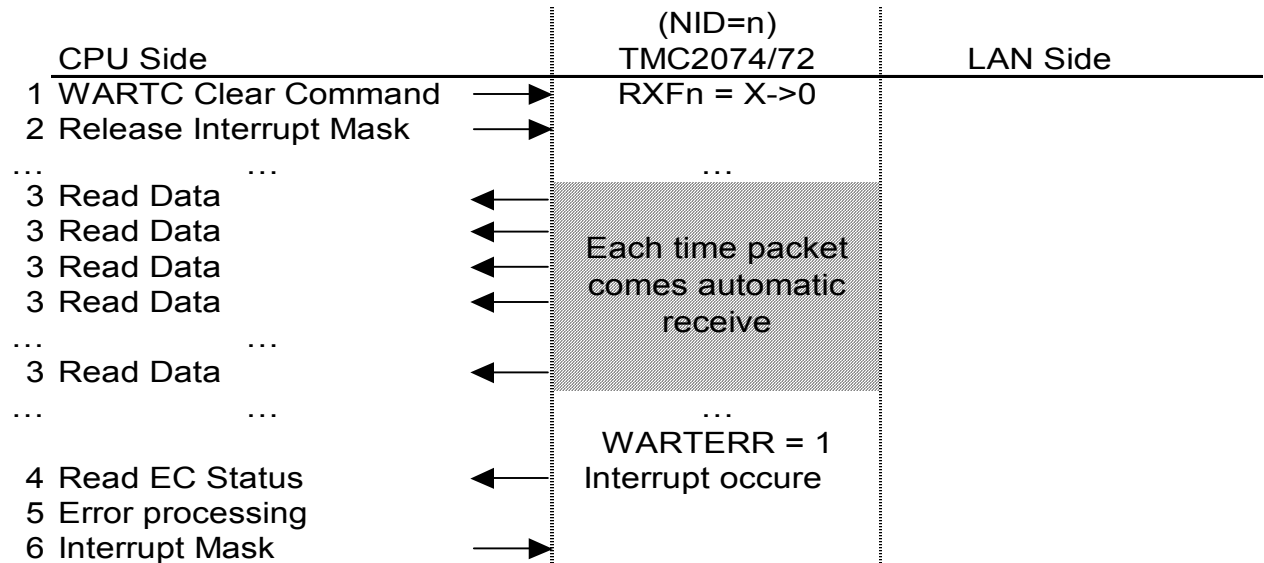
(): it is FBE, PAC addressed to self

After the receive completion in the free format mode, the FRCV (Free format receive end flag) in the EC interruption status register (INTSTA) changes from 0 to 1, permitting the flag to be an interrupt source.

2.9.3 Example of Receive Flow in Remote Buffer Mode

(RXMH/RXML REGISTER: When in RXM07 = 1)

CirLink can be treated as a simple data buffer such as "read data from the CirLink at any timing".



After completing the receive of remote buffer mode, RRCV (Remote buffer receive end flag) in the EC interrupts the status register (INTSTA) and changes from 0 to 1, permitting the flag to be an interrupt source. This mode also monitors if a packet comes from applicable nodes within a certain period. If there is a non-responsive node, the WARTERR flag changes from 0 to 1, permitting this change to be an interrupt source. Refer to section 3.2.9 - INTSTA Register: EC Interrupt Status.

2.9.4 Warning Timer (WT) at Remote Buffer Receive

CirLink checks the logical AND RXF flags of all pages that are set to remote buffer mode. A result of 1 during a cycle indicates a normal state in which there is no silent node on the network. In this case the object flags are cleared after a certain period of time (see table below).

In contrast, if the result retains a 0, the condition is not in a normal state, and WATERR in the EC interrupt status register changes from 0 to 1. This condition will generate an interrupt..

This function is initialized by writing a warning timer clear command into the EC Command register. The monitoring time is set by the warning timer resolution setup pins: WPRE [2:0] and WARTC3-0 in the Carry Selection register.

Actually, the warning timer clear command only clears WATERR flag. The Warning timer function starts automatically after releasing software reset. So some initial settings for this function set before releasing software reset.

Procedure:

Step-1: Turn on software reset (RESET bit = 1 in COMR6 register)

Step-2: Set initial settings (Rx-Mode, CARRY-Selection, etc..)

Datasheet

Step-3: Set WARTERR flag = 0 in the EC interrupt mask register

Step-4: Release software reset (RESET bit = 0 in COMR6 register)

Step-5: Start the Warning Timer function automatically

Step-6: Write the warning timer clear command into the EC Command register.

Step-7: Set WARTERR flag = 1 in the EC Interrupt Mask register

Step-8: After step-7, an interrupt occurs when a warning timer error occurs.

CARRY Selection

| WARTC3-0 | CARRY Digit | Check Period |
|----------|-------------|---------------------------------|
| 0000 | ----- | ILLEGAL Setting |
| 0001 | WT[1] | WT Resolution * 2 ¹ |
| 0010 | WT[2] | WT Resolution * 2 ² |
| : | : | : |
| 1111 | WT[15] | WT Resolution * 2 ¹⁵ |

Resolution Selection

| WPRE2:0 | Resolution | | | |
|---------|---------------------|------------|------------|------------|
| | 40MHz XTAL | 20MHz XTAL | 32MHz XTAL | 16MHz XTAL |
| 000 | 12.8us | 25.6us | 16.0us | 32.0us |
| 001 | 25.60us | 51.2us | 32.0us | 64.0us |
| 010 | 51.2us | 102.4us | 64.0us | 128.0us |
| 011 | 102.40us | 204.8us | 128.0us | 256.0us |
| 1xx | Setting prohibition | | | |

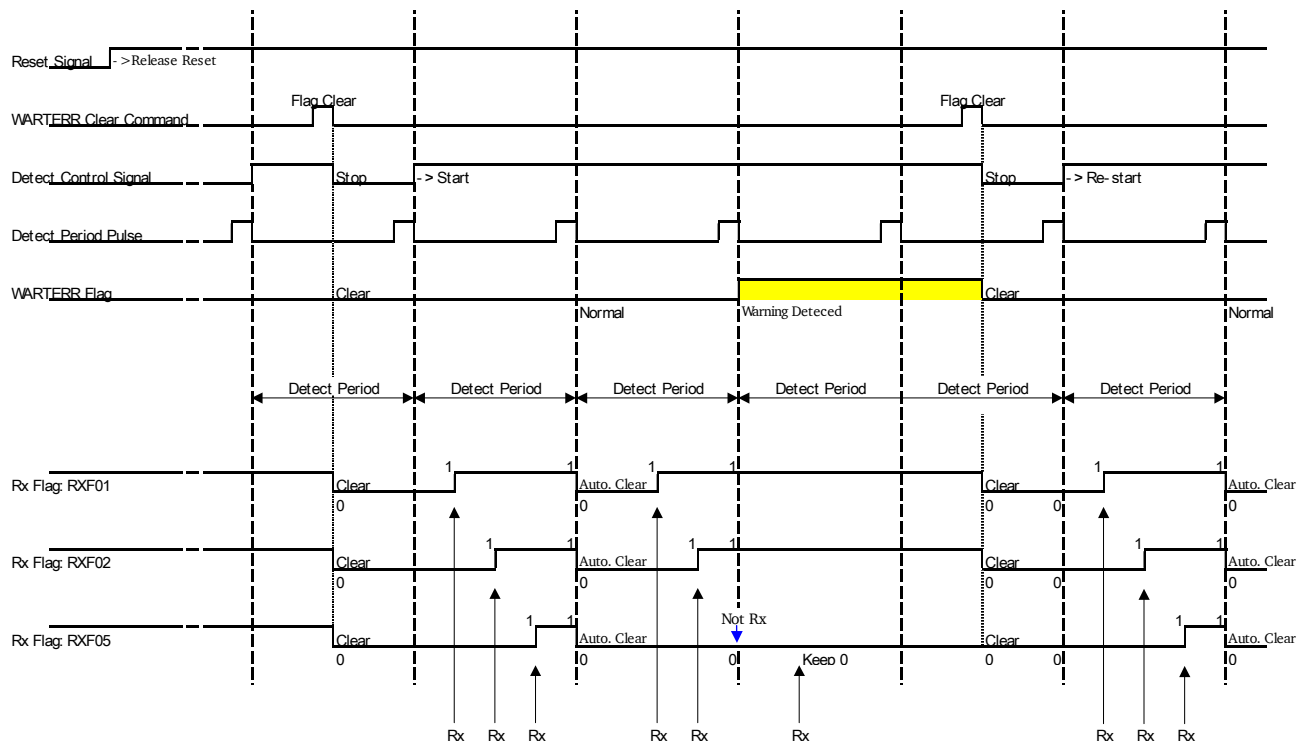
Action of the receive flag(RXFxx) at the remote buffer mode

| Occure event | | Communication Mode / Receive flag name | | | | |
|--|----------------|--|------------------------|----------------------|------------------------|------------------------|
| | | Remote Buffer RXF01 | Remote Buffer RXF02 | Free Format RXF03 | Remote Buffer RXF04 | Remote Buffer RXF05 |
| 1 Clear Command | HOST | 0 | 0 | X | 0 | 0 |
| . | | . | . | . | . | . |
| 2 Receive #01 | LAN | 1 | 0 | X | 0 | 0 |
| 3 Receive #05 | LAN | 1 | 0 | X | 0 | 1 |
| 4 Receive #02 | LAN | 1 | 1 | X | 0 | 1 |
| . | | . | . | . | . | . |
| 5 Warning Timer C.O. WARTERR = 0 -> 1 | TMC 2074/72 | 1 | 1 | X | 0 | 1 |
| . | | . | . | . | . | . |
| . | | . | . | . | . | . |

Until the clear command is issued hold of condition

 Example : Case of MAXID=05
 X = Don't Care

Waning Timer function : Timing chart example



2.10 Standalone Mode

2.10.1 General Description of Standalone Mode

The standalone mode allows CirLink to execute send/receive commands without CPU support. The functions of the CPU interface signals need to be set as listed below. Setting the nSTALONE pin to Low (0) enables Standalone mode.

| Pin | Peripheral mode | Operation Mode | | |
|------------------------|-----------------|----------------|-----------------------|-----------|
| | | Direction | Standalone Mode | Direction |
| D[15:6]/PI[15:6] | D[15:6] | I/O | Input Port PI[15:6] | I |
| D[5:0]/AD[5:0]/PI[5:0] | D/AD[5:0] | I/O | Input Port PI[5:0] | I |
| PO[15:8] | Hi-Impedance | --- | Output Port PO[15:8] | O |
| nWR/DIR/PO[7] | nWR/DIR | I | Output Port PO[7] | O |
| nRD/nDS/PO[6] | nRD/nCS | I | Output Port PO[6] | O |
| A[5:4]/PO[5:4] | A[5:4] | I | Output Port PO[5:4] | O |
| A[3]/ALEPOL/PO[3] | A3/ALEPOL | I | Output Port PO[3] | O |
| A[2]/ALE/PO[2] | A2/ALE | I | Output Port PO[2] | O |
| A[1:0]/PO[1:0] | A[1:0] | I | Output Port PO[1:0] | O |
| nCS/SCM[4] | nCS | I | CMID Designate (bit4) | I |
| nSWAP/SCM[3] | nSWAP | I | CMID Designate (bit3) | I |
| W16/SCM[2] | W16 | I | CMID Designate (bit2) | I |
| nRWN/SCM[1] | nRWM | I | CMID Designate (bit1) | I |
| nMUX/SCM[0] | nMUX | I | CMID Designate (bit0) | I |
| WPRE[2:0]/SPRE[2:0] | WPRE[2:0] | I | SPRE[2:0] | I |
| nINTR/NSTUNLOC | nINTR | O | NSTUNLOC | O |
| FLASHO | FLASHO | O | FLASHO | O |
| (High) /NSTC[3] | Fix High | I | NSTC[3] | I |
| nEHWR/NSTC[2] | nEHWR | I | NSTC[2] | I |
| nEHRD/NSTC[1] | nEHRD | I | NSTC[1] | I |
| (High) NSTC[0] | Fix High | I | NSTC[0] | I |
| nDSINV/CMERRMD | nDSINV | I | CMERRMD | I |

In standalone mode, internal registers cannot be accessed. The TXEN bit in the standalone mode defaults to 1, allowing nodes to automatically join the network upon start-up (reset). Since the default parameters such as page size, max. node ID, and the node ID are set with pins, this mode does not provide any software solutions for network malfunction caused by any improper pin settings.

2.10.2 Sending in Standalone Mode

In standalone mode the contents of input port can be sent as a broadcast packet. Sending starts automatically upon any of the following events.

- (1) When the received packets are normally received with no CRC error. The packet format does not have to be an output port controller packet (as stated later).
- (2) Timer Setup.
- (3) When tokens are received.

(4) When external trigger is entered.

The scenarios above (transmission triggers) can be set in accordance with the SPRE2-0 pin as below.

| SPRE2-0 | Transmission Trigger Setting | Trigger Mode name |
|---------|--|-------------------|
| 000 | (1) After receiving self-addressed packets, or (2) Timer Setup | Mode 1 |
| 001 | | |
| 010 | | |
| 011 | | |
| 100 | | |
| 101 | (3) After receiving Self-addressed tokens | Mode 2 |
| 110 | Reserved | |
| 111 | (4) External trigger (Word data security) | Mode 3 |

- Mode 1 (After receiving self-addressed packet + Timer setup)

In this mode, when self-addressed packets are normally received with no CRC error and the timer has timed-out, the transmission trigger is activated. Namely, the “OR” of these two conditions is removed. The transmission period during Timer set-up is selected in accordance with the SPRE2-0 pin as shown in Table 6.

Table 6 - Transmission Period According to Timer Setup

| SPRE2-0 | @40MHZ XTAL | @20MHZ XTAL | @32MHZ XTAL | @16MHZ XTAL |
|---------|-------------|-------------|-------------|-------------|
| 000 | 1.6mS | 3.3mS | 2.0mS | 4.1mS |
| 001 | 3.3mS | 6.6mS | 4.1mS | 8.2mS |
| 010 | 6.6mS | 13.1mS | 8.2mS | 16.4mS |
| 011 | 13.1mS | 26.2mS | 16.4mS | 32.8mS |
| 100 | 52.4mS | 108.4mS | 65.6mS | 131.2mS |

- Mode 2 (After receiving self-addressed tokens)

This mode carries out a transmission whenever tokens are received . It is the same procedure used in Remote Buffer mode as in Peripheral mode. Since self-addressed tokens are transmitted once received, it is an effective method for transmitting at frequent intervals.

- Mode 3 (External Trigger)

In this mode, the input port status is latched internally when transmission strobes are entered from an external source, thus activating the transmission trigger. The transmission strobe input pin is the input port's least significant pin PI0 (nPISTR). At the beginning, it activates the data latch and transmission

trigger. Accordingly, data entered through the input port is 15-bit and the least significant bit (bit 0) is fixed at 0.

Transmission data in this mode is secured at 15-bit word units. The external strobe generator is needed. It is an effective mode when transmitting A/D converter or counter output. (In the above-mentioned Mode 1 and Mode 2, only bit unit data security can be obtained).

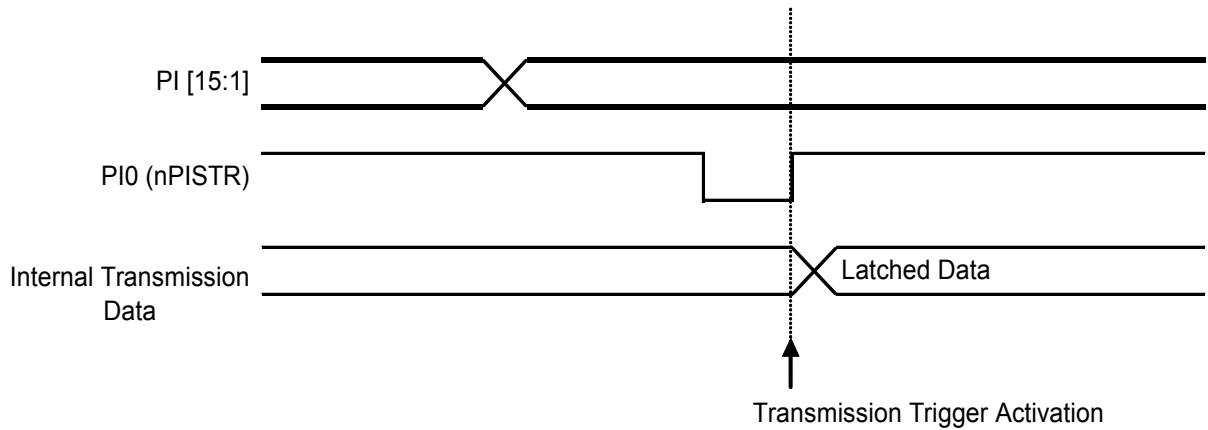


Figure 10 - Data Import Timing in Standalone Mode and External Trigger Mode (Mode 3)

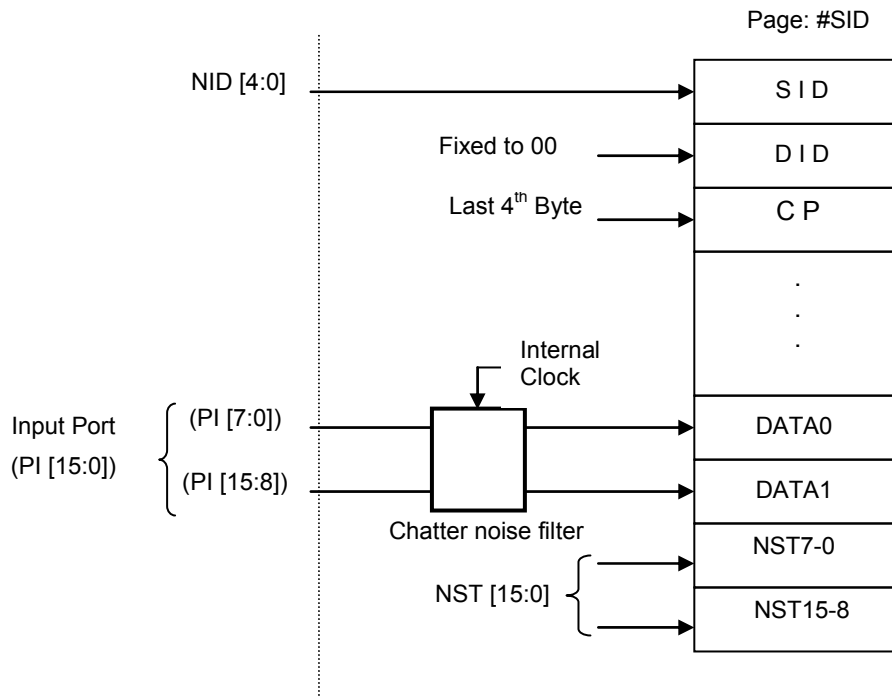


Figure 11 - Transmission Packet Buffer Configuration (Mode 1, 2)

In Modes 1 and 2, data from the input port is sampled by the internal clock in each port (bit unit) in the chatter noise filter. Accordingly, when data from the input port is imported into the transmission packet buffer, data is not secured in byte units or word units. Only bit unit security is available. Neither the A/D converter nor the counter output can be connected to the input port.

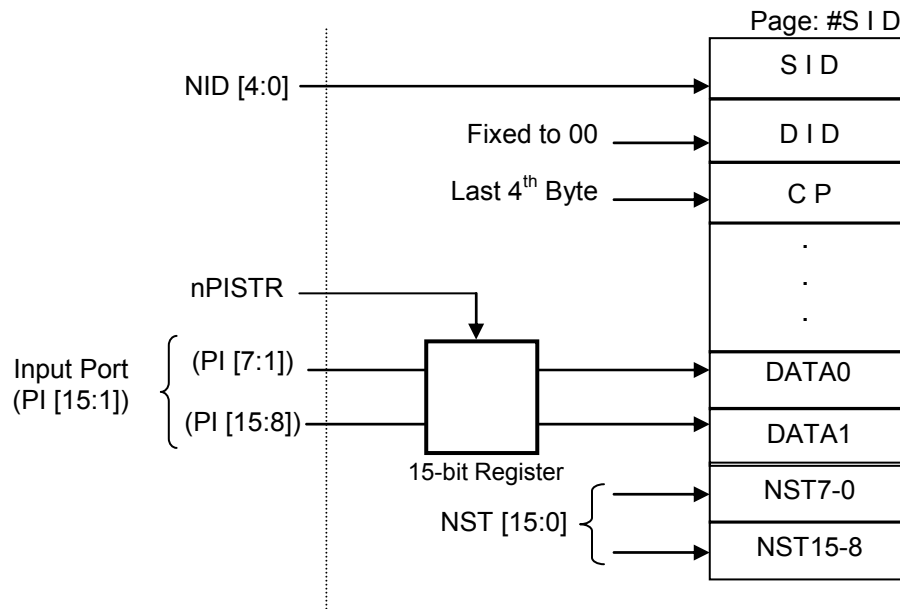


Figure 12 - Transmission Packet Buffer Configuration (Mode 3)

In Mode 3 the chatter noise filter is bypassed and a 15-bit register is connected to the input port. The input port's least significant pin (nPISTR) is used in this register clock. When nPISTR starts, data from the input port (15-bit) is imported into the register and is used as transmission data. Immediately after importing, data security in the word units (15-bit) is available due to the transmission trigger being activated. Accordingly, output from the A/D converter or counter can be connected to the input port, and bit 0 of the transmission data is fixed to 0.

2.10.3 Reception in Standalone Mode

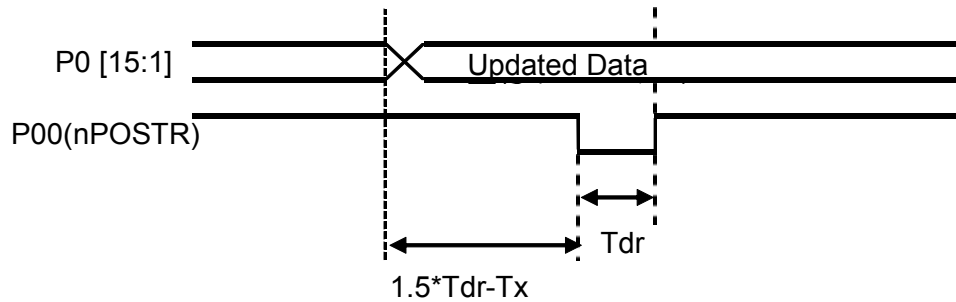
The Standalone mode has the function of exporting the contents of received data packets to the Output port. To prevent unnecessary updating of output port contents, there are restrictions for the format of received packets as discussed below:

Received Packet Format Restrictions for Data Port:

- 1) Packet's self-address should be (DID = NID);
- 2) The contents of the final 5th and 6th byte word data (DATA 1) should be in accordance with the contents of the final 3rd and 4th byte word data.

When the above requirements are met, as well as normal reception without CRC errors, the word data is latched to the output latch. Latch output is exported as it is in a normal way as external output. The initial high-impedance setting after Hardware Reset is maintained at high-impedance until the packet is received as normal.

When the transmission trigger mode is set to External Trigger (Mode 3, SPRE2-0=111), the output port's least significant pin is converted to the function of Strobe output (nPOSTR). When the requirements of (1) and (2) (listed above) are met, as well as normal reception without CRC errors, Word data is latched to the output latch. When the output status is updated, a strobe signal is transmitted by the nPOSTR pin. As with reception of data, only the higher order 15-bits are effective. The PO15-1 output port's initial high-impedance setting immediately after Hardware Reset is maintained at high-impedance until the packet is received as normal. Strobe output nPOSTR has regular output status, and the initial setting after Hardware Reset is 'high'.



Tdr: Transmission Rate Cycle (400 ns when 2.5 Mbps)
Tx: Input Clock Cycle (50 ns when 20 MHz)

Figure 13 - Strobe Output Timing in Standalone Mode, External Trigger Mode (Mode 3)

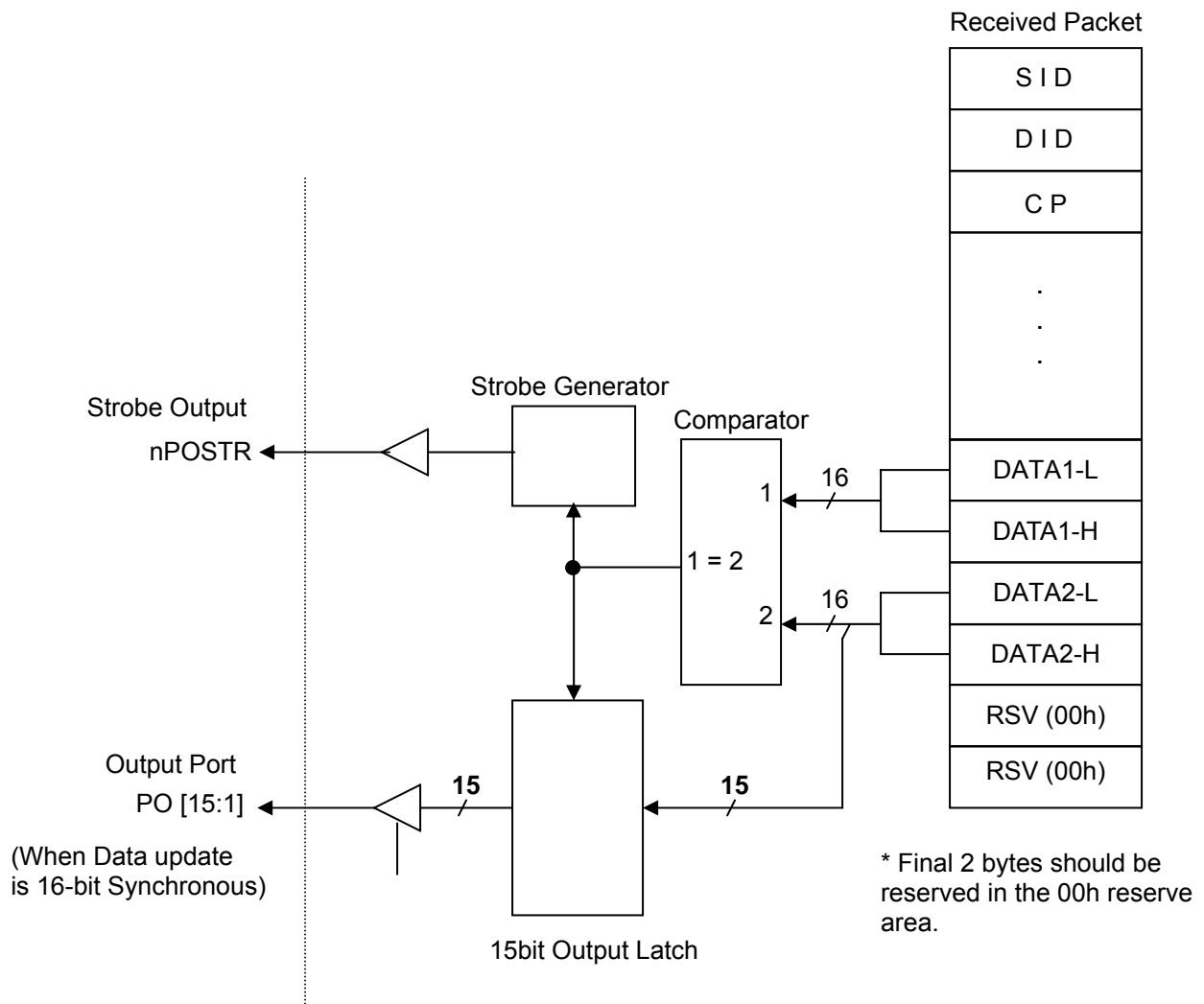


Figure 14 - Reception Packet Buffer Configuration (SPRE [2:0] = other than 111)

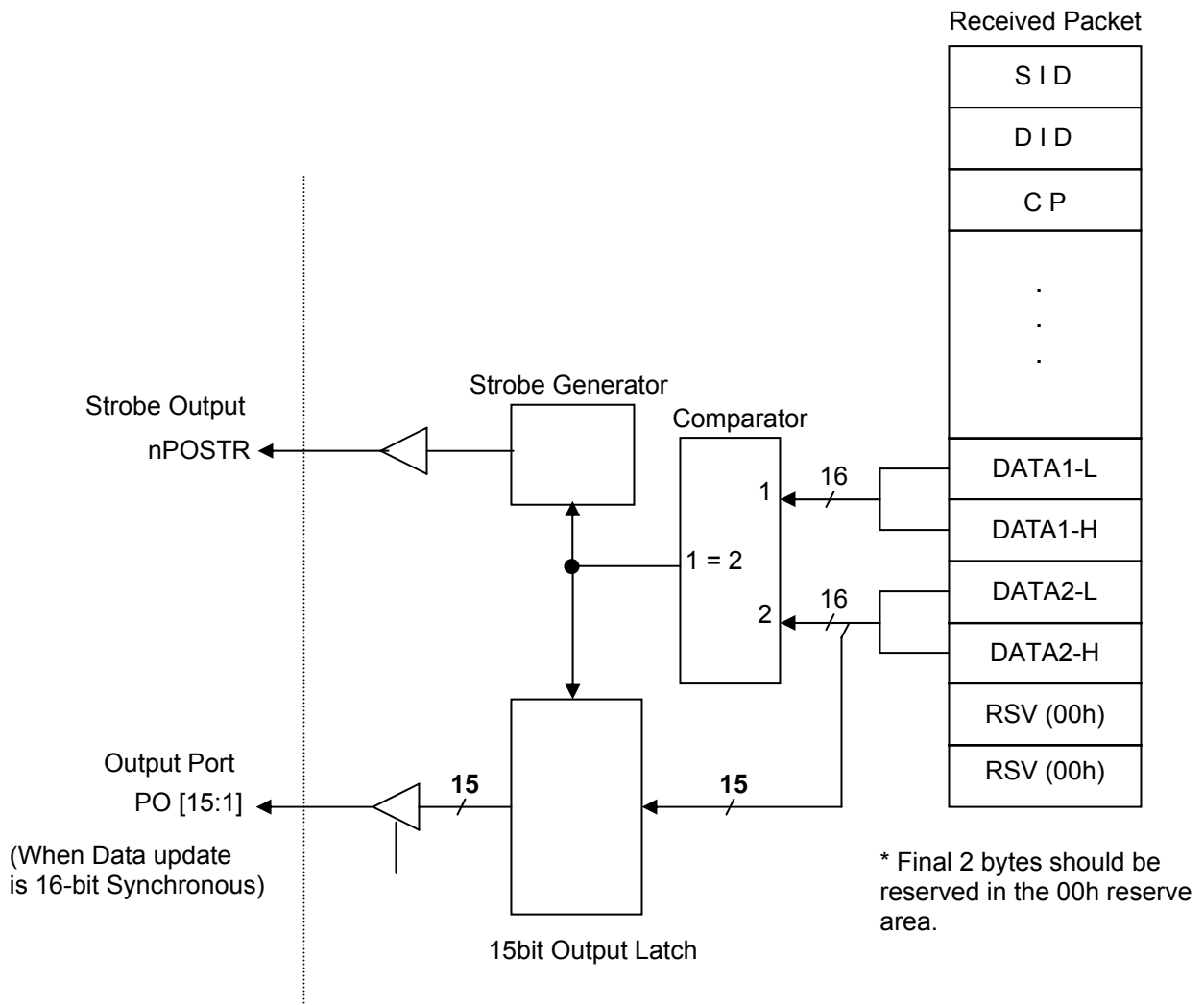


Figure 15- Reception Packet Buffer Configuration (SPRE [2:0]=111)

2.11 Diagnostic Mode

Diagnostic mode allows node number #31^(*) to temporarily join a network consisting of 30 or less nodes. The Diagnostic mode is set by setting the nDIAG pin to 0. The Diagnosis mode pin should be set only on the node with largest node number (#n) in the network; on the other nodes it should be tied to 1.

Diagnostic Mode = OFF , Node Number n=5

| Node Number | nDIAG Pin | Node that gave TOKEN | Designated MAXID |
|-------------|-----------|----------------------|------------------|
| #01 | "1" | #02 | #05 |
| #02 | "1" | #03 | #05 |
| #03 | "1" | #04 | #05 |
| #04 | "1" | #05 | #05 |
| #05 | "1" | #01 | #05 |

Diagnostic Mode = ON , Node Number n=5+1

| Node Number | nDIAG Pin | Node that gave TOKEN | Designated MAXID |
|-------------|-----------|----------------------|------------------|
| #01 | "1" | #02 | #05 |
| #02 | "1" | #03 | #05 |
| #03 | "1" | #04 | #05 |
| #04 | "1" | #05 | #05 |
| #05 | "0" | #06 * | #31(Compulsion) |
| #31 | "1" | #01 | #31 |

* Because the #06 Node does not exist increment to 31

When receiving a packet from node number #31, CirLink latches the last MSB (bit 7) of the last byte and outputs it to the external output, FLASHO. This function is effective regardless of the nDIAG pin status, and enables node #31^(*) to control the FLASHO outputs of other nodes. After hardware reset, the external output FLASHO stays in high-impedance until a packet is received.

^(*) Changes depending on the page size setting (PS[1:0]: See Below).

| Page Size | Node ID For Diagnosis |
|-------------------|-----------------------|
| 32B (PS[1:0]=11) | #31(1Fh) |
| 64B (PS[1:0]=10) | #15(Fh) |
| 128B (PS[1:0]=01) | #7(7h) |
| 256B (PS[1:0]=00) | #3(3h) |

2.12 Network Standard Time (NST)

Network standard time (NST) is a 16-bit free-running counter. Each node adjusts the time after receiving a packet from the clock master node (CM node), ensuring that all nodes share the common standard time on the network. This minimizes phase deviation among nodes within about 100 μ s.

The NST prescaler pin (NSTPRE2, 0) is used to set the count speed of the NST. The following table lists the relations among setting, resolution, and maximum time:

| NST Prescale NSTPRE[2:0] | Prescale | 40MHz Xtal | | 20MHz Xtal | |
|-----------------------------|----------|------------|------------|------------|------------|
| | | Resolution | MAX Period | Resolution | MAX Period |
| 000 | 1:32 | 0.8us | 52.4ms | 1.6us | 105ms |
| 001 | 1:64 | 1.6us | 105ms | 3.2us | 210ms |
| 010 | 1:128 | 3.2us | 210ms | 6.4us | 419ms |
| 011 | 1:256 | 6.4us | 419ms | 12.8us | 839ms |
| 100 | 1:512 | 12.8us | 839ms | 25.6us | 1.68s |
| 101 | 1:1024 | 25.6us | 1.68s | 51.2us | 3.36s |
| 110 | 1:2048 | 51.2us | 3.36s | 102.4us | 6.71s |
| 111 | 1:4096 | 102.4us | 6.71s | 204.8us | 13.42s |

| NST Prescale NSTPRE[2:0] | Prescale | 32MHz Xtal | | 16MHz Xtal | |
|-----------------------------|----------|------------|------------|------------|------------|
| | | Resolution | MAX Period | Resolution | MAX Period |
| 000 | 1:32 | 1.0us | 0.07s | 2.0us | 0.13s |
| 001 | 1:64 | 2.0us | 0.13s | 4.0us | 0.26s |
| 010 | 1:128 | 4.0us | 0.26s | 8.0us | 0.52s |
| 011 | 1:256 | 8.0us | 0.52s | 16.0us | 1.05s |
| 100 | 1:512 | 16.0us | 1.05s | 32.0us | 2.10s |
| 101 | 1:1024 | 32.0us | 2.10s | 64.0us | 4.19s |
| 110 | 1:2048 | 64.0us | 4.19s | 128.0us | 8.39s |
| 111 | 1:4096 | 128.0us | 8.39s | 256.0us | 16.78s |

2.12.1 Functions Provided by NST

Automatic generation of packet with time stamp

Setting one (1) to the NSTSEND bit in the MODE register allows the last 2 bytes in a packet to be reserved for the NST area, and the newest value of NST is automatically sent in these 2 bytes (nothing is written in the sending buffer RAM).

In the case of the clock master node (described in a later section), the same operation is carried out regardless of the NSTSEND value. The value is used as the time stamp of the packet and also used to maintain synchronization of time on the network.

NST carry output

The change of any digit in NST can be output as a periodic pulse to the nNSTCOUT pin. NSTC [3:0] in the CARRY register (external pin in the standalone mode) is used to select the digit. The pulse width of the carry output is the same length as one cycle of the NST resolution. As long as NST is synchronized properly, every node can output the pulse with the same phase.

Time readout

Accessing the NST register can dynamically provide the latest time data. Since NST is a 16 bit wide counter, it is necessary to read the even address side (10h) first when an 8-bit bus is used. When the even address is read out, the remaining 8 bits of the NST are latched internally

2.12.2 Time-synchronous Sequence

CM and CS nodes

To synchronize NST, one clock master (CM) should be designated on the network. The other nodes become clock slave nodes (CS node). The clock master ID (CMID) must be set in the CMID register on every node (external pins in the standalone mode). All nodes on the network use the same value as CMID.

CM node:

CMID equals to its node ID

Only one node on the network

Counts NST and notifies the CS nodes of the NST by sending packets.

CS node:

CMID not equal to its node ID

Receives a packet from the node specified by CMID and synchronizes NST with its own clock.

Preset at first receive

The NST counter of each node starts free running immediately after power-up. CS nodes preset the received NST as the NST of its own after receiving the first packet from the CM node. This preset operation is performed only once for the first receive.

The preset operation is performed after power-up and also immediately after resetting NSTSTOP in the MODE register from 1 to 0, after writing CMID register, and after software reset.

Phase tracking after second receive

The CS nodes that are preset by the first reception from the CM node switch into the time synchronization mode by PLL.

The CS nodes that switch into PLL operation keep comparing their NST to the received NST at every receive from the CM node. If the phase is different, the CS nodes dynamically control the speed of their counters to adjust phase to correspond to the phase of the NST in the CM node.

Supplement: When the difference count value between the receiver's NST and the received NST from CM node, is +2 and above, the receiver's counter is slowed to compensate. When the difference is -1 and

below, the receiver's counter is speeded up. When the difference is 0 or +1, the local counter makes no adjustment.

2.12.3 Phase Error

Sending frequency and phase error in CM

The NST once set in the CS node will gradually drift out of synchronization as time progresses. This is caused by differences between each XTAL. The less frequently the CM node sends packets, in other words, the longer the sending interval is, the greater the phase deviates.

The NST resolution for a 16-MHz XTAL is 32 μ s with the prescaler set to the intermediate (NSTPRE = 100). For the XTAL of precision 100 ppm, the phase error of maximum 200 μ s per second occurs between two nodes. The minimum period to cause the phase error of 32 μ s (equals to a LSB of NST) is 0.16 (32/200) seconds. That is to say, if the CM node keeps sending packets every 160 ms or shorter, the phase error of the CM and CS nodes can be kept within 32 μ s. The following table shows the sending intervals of the CM node that keeps the phase error within one LSB of NST:

| NSTPRE[2:0] | 16MHz(20MHz) XTAL | | 32MHz(40MHz) XTAL | |
|-------------|--------------------------------|----------------------------|--------------------------------|--------------------------|
| | NST Resolution | TX Cycle of CM Node | NST Resolution | TX Cycle of CM Node |
| 000 | 2.0 (1.6) μ s | =< 10 (8) ms | 1.0 (0.8) μ s | =< 5(4) ms |
| 001 | 4.0 (3.2) μ s | =< 20 (16) ms | 2.0 (1.6) μ s | =< 10 (8) ms |
| 010 | 8.0 (6.4) μ s | =< 40 (32) ms | 4.0 (3.2) μ s | =< 20 (16) ms |
| 011 | 16.0 (12.8) μ s | =< 80 (64) ms | 8.0 (6.4) μ s | =< 40 (32) ms |
| 100 | 32.0 (25.6) μ s | =< 160 (128) ms | 16.0 (12.8) μ s | =< 80 (64) ms |
| 101 | 64.0 (51.2) μ s | =< 320 (256) ms | 32.0 (25.6) μ s | =< 160 (128) ms |
| 110 | 128.0 (102.4) μ s | =< 640 (512) ms | 64.0 (51.2) μ s | =< 320 (256) ms |
| 111 | 256.0 (204.8) μ s | =< 1280 (1024) ms | 128.0 (102.4) μ s | =< 640 (512) ms |

The interval that the CM node can send packets (TX Cycle of CM Node) is less than the time required for all nodes to send full-size packets to the specific destination nodes at the same token rotation. The time can be calculated with the following formula.

[Calculation]

$$(352.5 \times br + 11 \times br \times B) \times N$$

br: Bit cycle (br=400ns @2.5 Mbps)

B: Number of Data Byte (Except header as SID, DID and C.P)

N: Node Number

That is, if the rate is 2 Mbps under the 32 page, 32 byte mode, the CM node has the opportunity of sending within 10.4 ms, which is calculated by $(352.5 \times 0.5 \mu\text{s} + 11 \times 0.5 \mu\text{s} \times 29B) \times 31$. That is frequent enough against 160 ms in the above table on this page.

Communication speed (Data rate) and phase error

The time difference becomes longer as communication speed becomes slower. The reason for this is because some data processing in CirLink such as CRC check is dependent upon the data rate. The relation between the transfer speed and time difference from CM to CS is listed as follows.

| CKP[2:0] | 16MHz(20MHz) XTAL | | 32MHz(40MHz) XTAL | |
|----------|---------------------|---------------------------|---------------------|---------------------------|
| | Communication Speed | CM --> CS Time Difference | Communication Speed | CM --> CS Time Difference |
| 000 | 2.0M (2.5M) bps | 27.5 (22) us | 4.0M (5.0M) bps | 13.8 (11) us |
| 001 | 1.0M (1.25M) bps | 55 (44) us | 2.0M (2.5M) bps | 27.5 (22) us |
| 010 | 500K (625K) bps | 110 (88) us | 1.0M (1.25M) bps | 55 (44) us |
| 011 | 250K (312.5K) bps | 220 (176) us | 500K (625K) bps | 110 (88) us |
| 100 | 125K (156.25K) bps | 440 (352) us | 250K (312.5K) bps | 220 (176) us |
| 101 | 62.5K (78.125K) bps | 880 (704) us | 125K (156.25K) bps | 440 (352) us |

Notes : "CM --> CS Time Difference" does NOT include cable Propagation Delay.

CirLink has an offset value built-in to absorb the phase error depending on communication speed. Moreover, the offset value can be manually set at the higher threshold of the CARRY register.

NOTE: Only automatic setup is available in the standalone mode and condition of NSTPRE2 = L(0).

OFSMOD (CARRY register: bit 15)

0: Automatic offset (default) 1: Manual offset

NSTOFS4 -0 (CARRY register: bit 12 to 8)

The offset value is selected among 0 to 31.

The actual offset time is "NST resolution x NSTOFS4-0".

Unlock flag

Synchronization between the NST unlock flag in the CM node and the NST in any other node is tracked by the NSTUNLOC signal in the INTSTA register. This flag can be used as an interrupt source. In the standalone mode, this flag is output to nINTR pin.

0: Synchronous lock state, 1: Synchronous unlock state (default)

*About approval condition for Synchronous lock /unlock state

- Unlock to lock state (NSTUNLOC=0)

The difference between own NST and NST from CM node is within +/-2. And NST from CM node must be received three times or more continuously, and all of those differences must be within +/-2.

- Lock to unlock state (NSTUNLOC=1)

The difference between own NST and NST from CM node is is not within +/-2. Or NST from CM node must be received three times or more continuously, and all of those differences are not within +/-2.

A possible cause of unlock status not being cancelled is that the CM node's NST pre-scalar setting is not synchronized. A possible cause of sometimes falling into unlock status is that the CM node's transmission frequency is low.

In the case of CM node, the flag becomes 0 in a steady state (synchronous lock status) for no apparent reason. As the initial settings in this case depends on the function modes, listed below:

In Peripheral mode, the CM node ID is set in a register after cancellation of Hardware Reset. After these values are imported, the output is 1 until the node becomes a CM node (it becomes 0 after that). During Software Reset, due to the CM Node ID being immediately imported, the CM Node ID is fixed at 1 and transitioning to 0 immediately after being set up in the register.

In standalone mode, the CM node ID is a pin setting; when it is the same setting as the CM node setting, output is 1 during Hardware Reset, and 0 when Hardware Reset is cancelled.

Unlock Phase difference register

The phase difference between the NST in the CM node and the NST in the subject node can be monitored through the NSTDIF register.

DIFDIR (NSTDIF register: bit 15)

Indicates the direction of phase difference

0: Ahead of CM node 1: Behind of CM node

NSTDIF 14-0 (NSTDIF register: bit 14-0)

Absolute difference from the CM node is indicated as a value from 0 to 32,768.

Accessing the NSTDIF register can dynamically provide the latest time data. Since NSTDIF is a 16 bit value, it is necessary to read the even address side (32h) first when 8-bit bus is used. When the even address is read out, the remaining 8 bits of the NST are latched internally.

2.12.4 nNSTCOUT Pulse Generation Cycle

20MHz - Xtal

| NST resolution setting | | Pulse Cycle of nNSTCOUT | | | |
|------------------------|-------------------------|-------------------------|---------|-----------|---------|
| NSTPRE[2:0] | Resolution / MAX Period | NSTC[3:0] | Cycle | NSTC[3:0] | Cycle |
| 000 | 1.6us/105ms | 0000 | 3.2us | 1000 | 819.2us |
| | | 0001 | 6.4us | 1001 | 1.6ms |
| | | 0010 | 12.8us | 1010 | 3.3ms |
| | | 0011 | 25.6us | 1011 | 6.6ms |
| | | 0100 | 51.2us | 1100 | 13.1ms |
| | | 0101 | 102.4us | 1101 | 26.2ms |
| | | 0110 | 204.8us | 1110 | 52.4ms |
| | | 0111 | 409.6us | 1111 | 104.9ms |
| 001 | 3.2us/210ms | 0000 | 6.4us | 1000 | 1.6ms |
| | | 0001 | 12.8us | 1001 | 3.3ms |
| | | 0010 | 25.6us | 1010 | 6.6ms |
| | | 0011 | 51.2us | 1011 | 13.1ms |
| | | 0100 | 102.4us | 1100 | 26.2ms |
| | | 0101 | 204.8us | 1101 | 52.4ms |
| | | 0110 | 409.6us | 1110 | 104.9ms |
| | | 0111 | 819.2us | 1111 | 209.7ms |
| 010 | 6.4us/419ms | 0000 | 12.8us | 1000 | 3.3ms |
| | | 0001 | 25.6us | 1001 | 6.6ms |
| | | 0010 | 51.2us | 1010 | 13.1ms |
| | | 0011 | 102.4us | 1011 | 26.2ms |
| | | 0100 | 204.8us | 1100 | 52.4ms |
| | | 0101 | 409.6us | 1101 | 104.9ms |
| | | 0110 | 819.2us | 1110 | 209.7ms |
| | | 0111 | 1.6ms | 1111 | 419.4ms |
| 011 | 12.8us/839ms | 0000 | 25.6us | 1000 | 6.6ms |
| | | 0001 | 51.2us | 1001 | 13.1ms |
| | | 0010 | 102.4us | 1010 | 26.2ms |
| | | 0011 | 204.8us | 1011 | 52.4ms |
| | | 0100 | 409.6us | 1100 | 104.9ms |
| | | 0101 | 819.2us | 1101 | 209.7ms |
| | | 0110 | 1.6ms | 1110 | 419.4ms |
| | | 0111 | 3.3ms | 1111 | 838.9ms |
| 100 | 25.6us/1.68s | 0000 | 51.2us | 1000 | 13.1ms |
| | | 0001 | 102.4us | 1001 | 26.2ms |
| | | 0010 | 204.8us | 1010 | 52.4ms |
| | | 0011 | 409.6us | 1011 | 104.9ms |
| | | 0100 | 819.2us | 1100 | 209.7ms |
| | | 0101 | 1.6ms | 1101 | 419.4ms |
| | | 0110 | 3.3ms | 1110 | 838.9ms |
| | | 0111 | 6.6ms | 1111 | 1.68s |
| 101 | 51.2us/3.35s | 0000 | 102.4us | 1000 | 26.2ms |
| | | 0001 | 204.8us | 1001 | 52.4ms |
| | | 0010 | 409.6us | 1010 | 104.9ms |
| | | 0011 | 819.2us | 1011 | 209.7ms |
| | | 0100 | 1.6ms | 1100 | 419.4ms |
| | | 0101 | 3.3ms | 1101 | 838.9ms |
| | | 0110 | 6.6ms | 1110 | 1.68s |
| | | 0111 | 13.1ms | 1111 | 3.35s |
| 110 | 102.4us/6.71s | 0000 | 204.8us | 1000 | 52.4ms |
| | | 0001 | 409.6us | 1001 | 104.9ms |
| | | 0010 | 819.2us | 1010 | 209.7ms |
| | | 0011 | 1.6ms | 1011 | 419.4ms |
| | | 0100 | 3.3ms | 1100 | 838.9ms |
| | | 0101 | 6.6ms | 1101 | 1.68s |
| | | 0110 | 13.1ms | 1110 | 3.35s |
| | | 0111 | 26.2ms | 1111 | 6.71s |
| 111 | 204.8us/13.42s | 0000 | 409.6us | 1000 | 104.9ms |
| | | 0001 | 819.2us | 1001 | 209.7ms |
| | | 0010 | 1.6ms | 1010 | 419.4ms |
| | | 0011 | 3.3ms | 1011 | 838.9ms |
| | | 0100 | 6.6ms | 1100 | 1.68s |
| | | 0101 | 13.1ms | 1101 | 3.35s |
| | | 0110 | 26.2ms | 1110 | 6.71s |
| | | 0111 | 52.4ms | 1111 | 13.42s |

Note: nNSTCOUT outputs Low pulse qual to the NST resolution

16MHz - Xtal

| NST resolution setting | | Pulse Cycle of nNSTCOUT | | | |
|------------------------|-------------------------|-------------------------|---------|-----------|---------|
| NSTPRE[2:0] | Resolution / MAX period | NSTC[3:0] | Cycle | NSTC[3:0] | Cycle |
| 000 | 2.0us/131ms | 0000 | 4.0us | 1000 | 1.0ms |
| | | 0001 | 8.0us | 1001 | 2.0ms |
| | | 0010 | 16.0us | 1010 | 4.1ms |
| | | 0011 | 32.0us | 1011 | 8.2ms |
| | | 0100 | 64.0us | 1100 | 16.4ms |
| | | 0101 | 128.0us | 1101 | 32.8ms |
| | | 0110 | 256.0us | 1110 | 65.5ms |
| | | 0111 | 512.0us | 1111 | 131.1ms |
| 001 | 4.0us/262ms | 0000 | 8.0us | 1000 | 2.0ms |
| | | 0001 | 16.0us | 1001 | 4.1ms |
| | | 0010 | 32.0us | 1010 | 8.2ms |
| | | 0011 | 64.0us | 1011 | 16.4ms |
| | | 0100 | 128.0us | 1100 | 32.8ms |
| | | 0101 | 256.0us | 1101 | 65.5ms |
| | | 0110 | 512.0us | 1110 | 131.1ms |
| | | 0111 | 1.0ms | 1111 | 262.1ms |
| 010 | 8.0us/524ms | 0000 | 16.0us | 1000 | 4.1ms |
| | | 0001 | 32.0us | 1001 | 8.2ms |
| | | 0010 | 64.0us | 1010 | 16.4ms |
| | | 0011 | 128.0us | 1011 | 32.8ms |
| | | 0100 | 256.0us | 1100 | 65.5ms |
| | | 0101 | 512.0us | 1101 | 131.1ms |
| | | 0110 | 1.0ms | 1110 | 262.1ms |
| | | 0111 | 2.0ms | 1111 | 524.3ms |
| 011 | 16.0us/1.05s | 0000 | 32.0us | 1000 | 8.2ms |
| | | 0001 | 64.0us | 1001 | 16.4ms |
| | | 0010 | 128.0us | 1010 | 32.8ms |
| | | 0011 | 256.0us | 1011 | 65.5ms |
| | | 0100 | 512.0us | 1100 | 131.1ms |
| | | 0101 | 1.0ms | 1101 | 262.1ms |
| | | 0110 | 2.0ms | 1110 | 524.3ms |
| | | 0111 | 4.1ms | 1111 | 1.05s |
| 100 | 32.0us/2.10s | 0000 | 64.0us | 1000 | 16.4ms |
| | | 0001 | 128.0us | 1001 | 32.8ms |
| | | 0010 | 256.0us | 1010 | 65.5ms |
| | | 0011 | 512.0us | 1011 | 131.1ms |
| | | 0100 | 1.0ms | 1100 | 262.1ms |
| | | 0101 | 2.0ms | 1101 | 524.3ms |
| | | 0110 | 4.1ms | 1110 | 1.05s |
| | | 0111 | 8.2ms | 1111 | 2.10s |
| 101 | 64.0us/4.19s | 0000 | 128.0us | 1000 | 32.8ms |
| | | 0001 | 256.0us | 1001 | 65.5ms |
| | | 0010 | 512.0us | 1010 | 131.1ms |
| | | 0011 | 1.0ms | 1011 | 262.1ms |
| | | 0100 | 2.0ms | 1100 | 524.3ms |
| | | 0101 | 4.1ms | 1101 | 1.05s |
| | | 0110 | 8.2ms | 1110 | 2.10s |
| | | 0111 | 16.4ms | 1111 | 4.19s |
| 110 | 128.0us/8.39s | 0000 | 256.0us | 1000 | 65.5ms |
| | | 0001 | 512.0us | 1001 | 131.1ms |
| | | 0010 | 1.0ms | 1010 | 262.1ms |
| | | 0011 | 2.0ms | 1011 | 524.3ms |
| | | 0100 | 4.1ms | 1100 | 1.05s |
| | | 0101 | 8.2ms | 1101 | 2.10s |
| | | 0110 | 16.4ms | 1110 | 4.19s |
| | | 0111 | 32.8ms | 1111 | 8.39s |
| 111 | 256.0us/16.78s | 0000 | 512.0us | 1000 | 131.1ms |
| | | 0001 | 1.0ms | 1001 | 262.1ms |
| | | 0010 | 2.0ms | 1010 | 524.3ms |
| | | 0011 | 4.1ms | 1011 | 1.05s |
| | | 0100 | 8.2ms | 1100 | 2.10s |
| | | 0101 | 16.4ms | 1101 | 4.19s |
| | | 0110 | 32.8ms | 1110 | 8.39s |
| | | 0111 | 65.5ms | 1111 | 16.78s |

Note: nNSTCOUT outputs Low pulses equal to the NST resolution

NST Supplements

Setting NST send mode nullifies the last two-byte areas in the sending buffer. That is, the NST value is not written in the last two-byte areas. The NST value is directly loaded to the parallel-to-serial conversion register for transmit without using the buffer area RAM (not stored in a buffer). Therefore, the CircLink always sends the newest NST value.

In addition, the clock master node (CM) sends NST, regardless of the NST send mode (CM node forcibly enters the NST sending mode).

The NST value to be sent is the value immediately before the last two bytes are sent to the parallel to serial conversion register. In the other words, the NST value shows the time immediately after sending the third data from the last.

From the viewpoint of the receiver, the NST value is stored at the last two bytes area in the buffer page corresponding to the SID value of the received packet. If the SID value in the receive packet is the ID of the clock master node, its NST value is automatically adjusted. The received NST becomes available for time adjustment at the time when ending "0" becomes OK after CRC error check completion.

2.13 CMI Modem

Refer to Appendix A - CMI Modem at the end of this document.

2.14 HUB Function

CircLink integrates a 3-port HUB function to expand the network. The HUB function enables conversion of different communication media among twist-pair cable, fiber optics, and the like. In addition, the HUB function expands the connection node number and cable length limitations caused by transceiver performance limitations.

The HUB function is enabled by nHUBON pin. Among three ports, one is used internally for the connection to CircLink main unit and the remaining two are used as external ports.

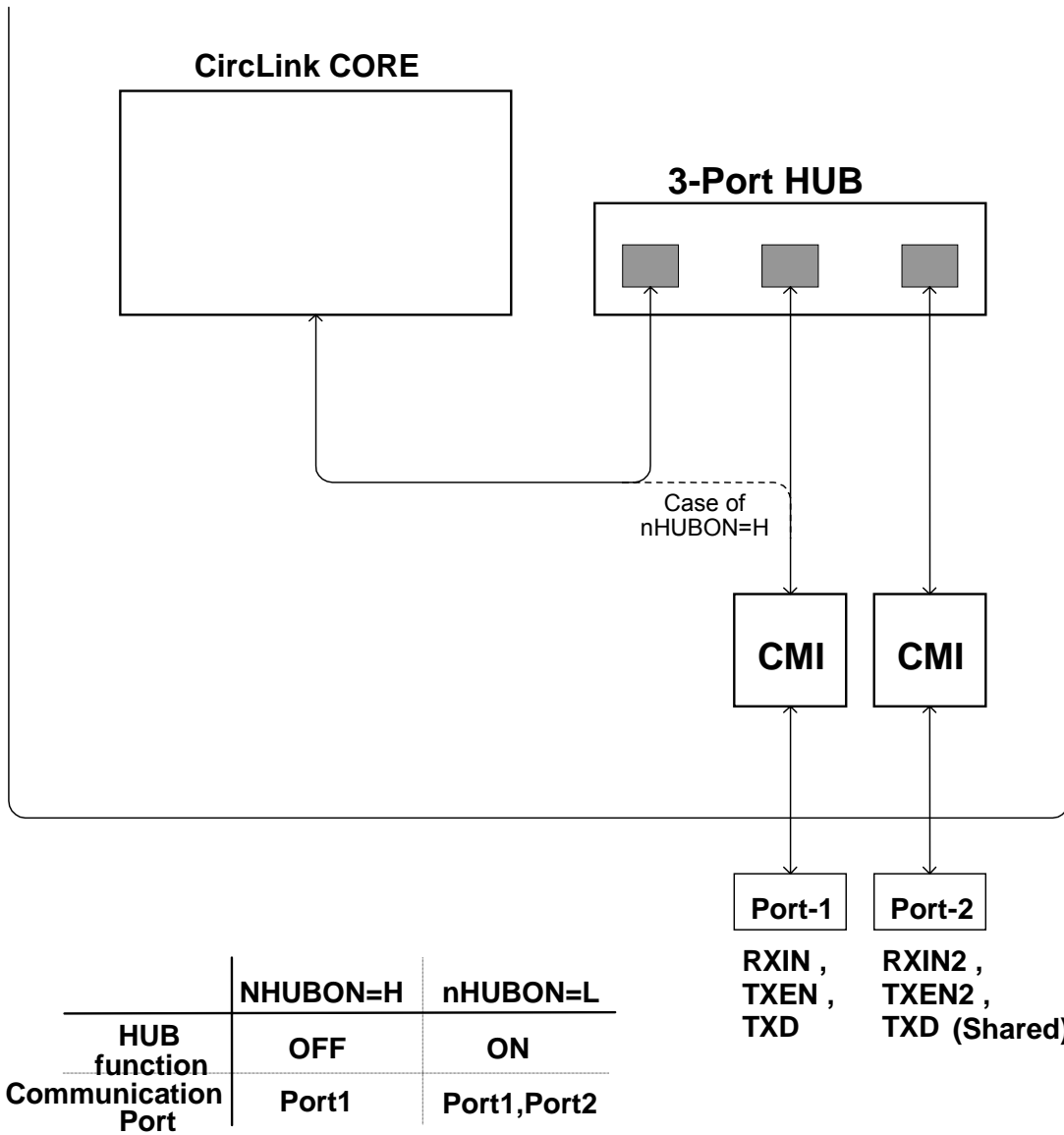
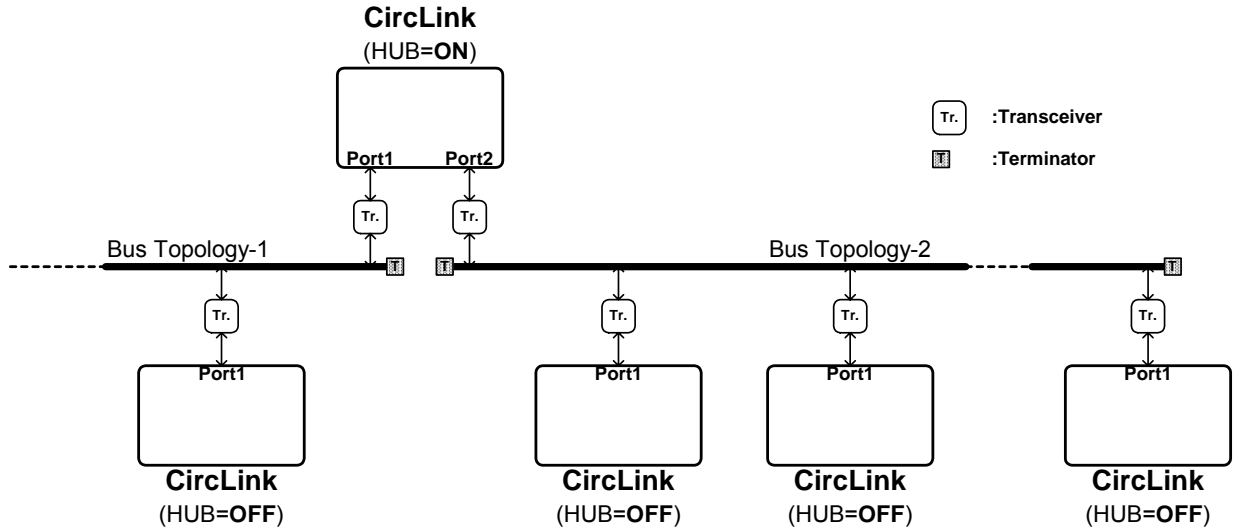


Figure 16 - Internal 3 Port HUB Block Diagram

2.14.1 Operation Example of HUB Function

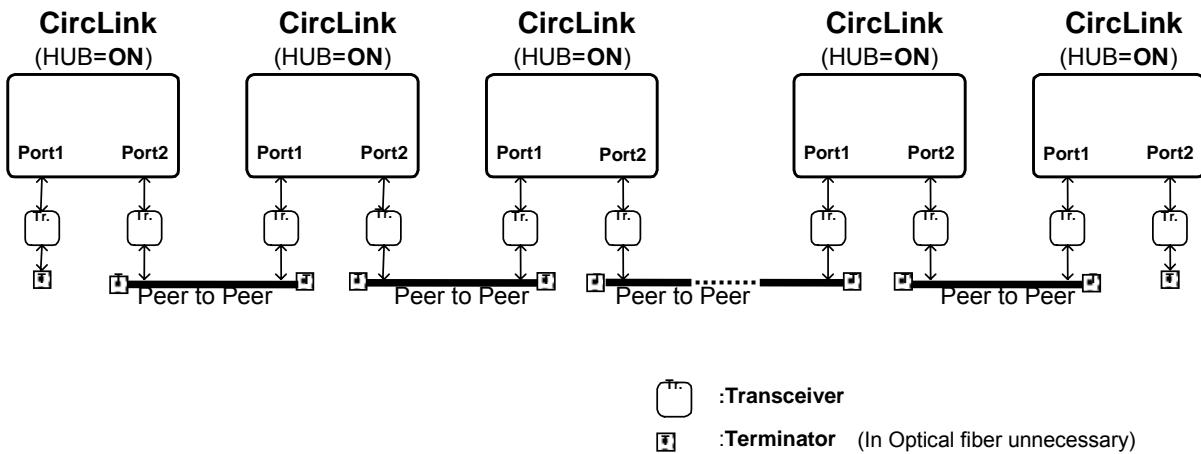
1. Dividing bus connection

The bus can be electrically divided by setting the HUB function ON.



2. Cascade connection

Fiber optics can be connected as cascade by using the HUB function.



2.14.2 Timer Expansion in Multi-stage Cascade Connection

An extra delay of 0.5 μs is added to the message when HUB is set to ON. A delay of 2.0 μs is also added in the CMI coding/decoding processing when CMI is set to ON. When configuring a cascade connection and setting both HUB and CMI to ON, a 2.5 μs (2.0 μs + 0.5 μs) delay is added to a message every time the message passes a node.

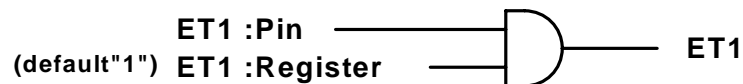
This delay may make the response timer timeout in the CirLink, causing communication failure. The response timer monitors responses from the nodes and is normally set to 74.6 μs . The one way propagation delay time permitted for cable, HUB circuit, and CMI decoding/coding circuit is 31 μs , which is calculated by $(74.6 \mu\text{s} - 12.6 \mu\text{s})/2$; where 12.6 μs is the CirLink response time. This is equivalent to the delay time of a 12-stage cascade connection HUB/CMI circuit.

$$(31 \mu\text{s} / 2.5 \mu\text{s} = 12.4 \rightarrow 12\text{-stage})$$

If the sum of cable delay and HUB/CMI delay is over 31 μs , set ET1 to 0 to extend the response timeout time to 298.4 μs , which is four times longer than the normal delay time. Taking this measure, the one way propagation delay time is extended to $(298.4 \mu\text{s} - 12.6 \mu\text{s}) / 2 = 142.9 \mu\text{s}$. ($142.9 \mu\text{s} / 2.5 \mu\text{s} = 57.2 \rightarrow 57\text{-stage}$).

| Response Timer | Idle Timer | Configuration Timer |
|---------------------|-------------------|---------------------|
| 74.6 μS | 82 μS | 52mS |
| 298.4 μS | 328 μS | 104mS |

The timer can be set by the ET1 pin or internal register and has a structure of AND logic in the CirLink as shown below.



Remarks:

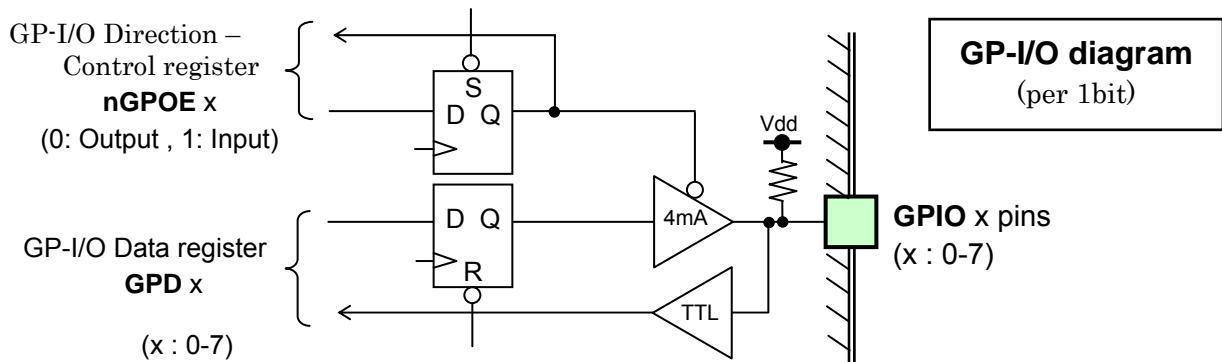
The typical time delay added in ON state HUB is 0.5 μs . However, it is extended to 1.0 μs if the optical mode is ON (nOPMD = L) and CMI is OFF (nCMI BYP = L).

NOTE: Values in text and table are based on a 2.5 Mbps network speed. When CirLink operates at 1.25 Mbps, the value should be doubled. When operating at 5 Mbps, the value should be half. To be precise, the propagation delay time of the cable and the transceiver should also be added.

2.15 8-Bit General-purpose I/O Port (New function)

When Circlink is used in the peripheral mode, 11* or more General-purpose I/O ports (GPIO) are utilized as the CPU interface with Circlink. (*for 8-bit data bus and Multiplex bus mode).

Eight GPIOs are added to the Circlink side as the substitution (GPIO7-0 pins).



Two registers named "Direction control register" and "Data register" are added for the GP-I/O control. Moreover, to allocate these registers in COMR7 (Address=0Eh), the subaddress is enhanced by one bit (SUBAD3).

- Sub address register -> Sub Address : SUBAD3-0 (Address=0Ah)

The subaddress is enhanced by SUBAD3 bit

- Direction Control register -> GP-I/O Direction : nGPOE7-0 (Address=0Eh, SUBAD=1011)

GP-I/O Direction Control register --- The direction can be set by every one bit.

nGPOEx = 0 : Output mode

nGPOEx = 1 : Input mode

- Data register -> GP-I/O Data : GPD7-0 (Address=0Eh, SUBAD=1010)

GP-I/O Data register

GPD7-0 : Write operation ---- Write data which outputs to GPI7-0 pin

: Read operation ---- Read the state of the GPIO7-0 pin

Chapter 3 Description of Registers

3.1 Register Map

Table 7 shows the CirLink register map. All registers are 16 bits wide and can be word-accessed and byte-accessed in 16-bit mode (W16 = H) and 8-bit mode (W16 = L) respectively. In the case of byte access, the lower byte (bits 7 to 0) is assigned to an even address and the upper byte (bits 15 to 8) to an odd address by default. This assignment can be reversed by setting the nSWAP pin to L.

Table 7 - CirLink Register Map

Adr. : CPU Address A[5:0] in Hex value. (Address 00h to 0Fh are registers specific to ARCNET)

- Word access (W16=High)

| Adr. | D15 - D0 | Adr. | D15 - D0 | Adr. | D15 - D0 | Adr. | D15 - D0 |
|------|----------|------|----------|------|----------|------|----------|
| 00 | COMR0 | 10 | NST | 20 | CMID | 30 | CKP |
| 02 | COMR1 | 12 | INTSTA | 22 | MODE | 32 | NSTDIF |
| 04 | COMR2 | 14 | INTMSK | 24 | CARRY | 34 | PININFO |
| 06 | COMR3 | 16 | ECCMD | 26 | RXMH | 36 | Not Used |
| 08 | COMR4 | 18 | RSID | 28 | RXML | 38 | Not Used |
| 0A | COMR5 | 1A | SSID | 2A | MAXID | 3A | ERRINFO |
| 0C | COMR6 | 1C | RXFH | 2C | NID | 3C | Reserved |
| 0E | COMR7 | 1E | RXFL | 2E | PS | 3E | Reserved |

- Byte access and No Swap (W16=Low, nSWAP=High)

| Adr. | D7 - D0 | Adr. | D7 - D0 | Adr. | D7 - D0 | Adr. | D7 - D0 |
|------|-------------|------|------------|------|------------|------|-------------|
| 00 | COMR0 | 10 | NST - L | 20 | CMID | 30 | CKP |
| 01 | (all zero) | 11 | NST - H | 21 | (all zero) | 31 | (all zero) |
| 02 | COMR1 | 12 | INTSTA - L | 22 | MODE - L | 32 | NSTDIF - L |
| 03 | (all zero) | 13 | INTSTA - H | 23 | MODE - H | 33 | NSTDIF - H |
| 04 | COMR2 | 14 | INTMSK - L | 24 | CARRY - L | 34 | PININFO - L |
| 05 | (all zero) | 15 | INTMSK - H | 25 | CARRY - H | 35 | PININFO - H |
| 06 | COMR3 | 16 | ECCMD | 26 | RXMH - L | 36 | Not Used |
| 07 | (all zero) | 17 | (all zero) | 27 | RXMH - H | 37 | Not Used |
| 08 | COMR4 | 18 | RSID | 28 | RXML - L | 38 | Not Used |
| 09 | (all zero)* | 19 | MRSID | 29 | RXML - H | 39 | Not Used |
| 0A | COMR5 | 1A | SSID | 2A | MAXID | 3A | ERRINFO- L |
| 0B | (all zero) | 1B | (all zero) | 2B | (all zero) | 3B | ERRINFO- H |
| 0C | COMR6 | 1C | RXFH - L | 2C | NID | 3C | Reserved |
| 0D | (all zero) | 1D | RXFH - H | 2D | (all zero) | 3D | Reserved |
| 0E | COMR7 | 1E | RXFL - L | 2E | PS | 3E | Reserved |
| 0F | (all zero) | 1F | RXFL - H | 2F | (all zero) | 3F | Reserved |

*: When the WORD-MODE is enabled (WDMD_bit=1), this address is mapped another COMR4.

- Byte access and Swap (W16=Low, nSWAP=Low)

| Adr. | D7 - D0 | Adr. | D7 - D0 | Adr. | D7 - D0 | Adr. | D7 - D0 |
|------|-------------|------|------------|------|------------|------|-------------|
| 00 | (all zero) | 10 | NST - H | 20 | (all zero) | 30 | (all zero) |
| 01 | COMR0 | 11 | NST - L | 21 | CMID | 31 | CKP |
| 02 | (all zero) | 12 | INTSTA - H | 22 | MODE - H | 32 | NSTDIF - H |
| 03 | COMR1 | 13 | INTSTA - L | 23 | MODE - L | 33 | NSTDIF - L |
| 04 | (all zero) | 14 | INTMSK - H | 24 | CARRY - H | 34 | PININFO - H |
| 05 | COMR2 | 15 | INTMSK - L | 25 | CARRY - L | 35 | PININFO - L |
| 06 | (all zero) | 16 | (all zero) | 26 | RXMH - H | 36 | Not Used |
| 07 | COMR3 | 17 | ECCMD | 27 | RXMH - L | 37 | Not Used |
| 08 | (all zero)* | 18 | MRSID | 28 | RXML - H | 38 | Not Used |
| 09 | COMR4 | 19 | RSID | 29 | RXML - L | 39 | Not Used |
| 0A | (all zero) | 1A | (all zero) | 2A | (all zero) | 3A | ERRINFO- H |
| 0B | COMR5 | 1B | SSID | 2B | MAXID | 3B | ERRINFO- L |
| 0C | (all zero) | 1C | RXFH - H | 2C | (all zero) | 3C | Reserved |
| 0D | COMR6 | 1D | RXFH - L | 2D | NID | 3D | Reserved |
| 0E | (all zero) | 1E | RXFL - H | 2E | (all zero) | 3E | Reserved |
| 0F | COMR7 | 1F | RXFL - L | 2F | PS | 3F | Reserved |

*: When the WORD-MODE is enabled (WDMD_bit=1), this address is mapped another COMR4.

Initial value of each register

The value under "init.value" in each register list indicates the initial value when **hardware reset** is applied to Circlink via the nRESET pin. With some exceptions, **software reset** does not initialize them.

Exceptions (software reset available)

Circlink internal communication protocol controller

COMR0 register (R) : All status information

COMR0 register (W) : All interrupt masks

COMR1 register (R) : All diagnostic information

COMR1 register (W) : All commands issued

ECCMD register : All commands issued

INTSTA register : ALL EC status information

INTMSK register : All EC interrupt masks

RXFH, RXFL registers : All receive flags

ERRINFO register : All error information

Hardware reset: Resets entire Circlink unit.

Performed by nRESET pin set to L.

Software reset: Resets only the units related to communication functions.

The reset method is described as below.

How to do software reset

1) Permanent software reset

Set the RESET bit of the COMR6 register to 1

(Retains until the bit is changed to 0)

Set the node ID set to 00h

(Retains until the setting is changed to other than 00h)

2) Temporary software reset

Software reset occurs for 100 ns (at 20 MHz CLK input) immediately after rewriting the object bits or writing the object registers. This reset is automatically released.

Rewriting INIMODE bit of the MODE register

Rewriting TXEN bit of COMR6 or MODE register from 0 to 1

Rewriting the following registers for INIMODE = 1

MAXID register

NID register

PS register

CKP register

NOTES:

- The communication function unit will start operation within 1.0 μ s (at 2.5 Mbps) after releasing software reset. It is therefore necessary to wait for at least 1.0 μ s (at 2.5 Mbps) after releasing software reset before writing data to a register reset by software (see previous page). The writing can be ignored.
After 10 μ s (at 2.5 Mbps) following the software reset, D1h is written to address = 0 in page #00 of the RAM and node ID value is written to the address = 1.
- Values in text are at 2.5 Mbps. When 1.25 Mbps, the value should be doubled accordingly. When 5 Mbps, the value should be half of the 2.5Mbps' respectively.

3.2 Details of Register

3.2.1 COMR0 Register: Status/interrupt Mask Register

| COMR0 (Status Register) | | address:00h | |
|-------------------------|-------|-------------|----------------------------------|
| [READ] | | | |
| bit | name | init. value | Description |
| 15-8 | ----- | 0 | reserved (all "0") |
| *1 7 | ----- | 1 | reserved |
| 6,5 | ----- | 1,1 | reserved |
| 4 | POR | 1 | Power On Reset |
| 3 | ----- | 0 | reserved |
| 2 | RECON | 0 | Reconfiguration |
| 1 | TMA | 0 | Transmitter Message Acknowledged |
| 0 | TA | 1 | Transmitter Available |

| COMR0 (Mask Register) | | address:00h | |
|-----------------------|----------|-------------|-----------------------|
| [WRITE] | | | |
| bit | name | init. value | description |
| 15-8 | ----- | 0 | reserved (all "0") |
| *1 7 | ----- | 0 | reserved ("0") |
| 6-4 | ----- | 0,0,0 | reserved (all "0") |
| 3 | EXCNAK | 0 | Excessive NAK |
| 2 | RECON | 0 | Reconfiguration |
| *1 1 | NXTIDERR | 0 | Next ID Error |
| 0 | TA | 0 | Transmitter Available |

*1 Not equivalent to the ARCNET original specifications.

- When reading: ARCNET status register

POR (bit 4)

When this bit is 1, it indicates that a hardware or software reset has occurred.. This bit can be cleared by writing the POR clear command (0Eh).

RECON (bit 2)

When this bit is 1 it indicates that a reconfiguration has occurred. This bit can be cleared by software reset or by writing the RECON clear command (16h).

TMA (bit 1)

When this bit is 1, it indicates that a transmission has been performed correctly (except broadcast messages). This bit is valid only after the TA bit has been set to 1 and can be cleared by a software reset or by writing the send command (03h).

TA (bit 0)

When this bit is 1, it indicates that sending is complete, and 0 indicates that sending is in progress. This bit becomes 0 when a write or send command (03h) is executed. In Free Buffer mode (TXM = 0) or a one-

packet send at remote buffer mode (TXM = 1 and RTO = 1), this bit becomes 1 by the completion of the one-packet send or written send-cancellation command (01h). This bit also becomes 0 after the first send command and remains 0 until the TX cancel command is issued. Under this condition the node will automatically continue to send. This bit becomes 1 when the mode exits from the consecutive automatic send with the writing of the send cancellation command (01h) or RTO bit = 1. The same TA bit also exists in bit 0 of the EC interrupt status register. This bit can also be set by a software reset.

- When writing: ARCNET mask register (cleared by software reset)

EXCNAK (bit 3)

This bit is set to 1 and the EXCNAK bit in the COMR1 (Diagnostic register) becomes 1 to generate the interrupt.

(The COM bit in the EC interrupt mask register = 1)

RECON (bit 2)

This bit is set to 1 and the RECON bit in the status register (COMR0) becomes 1 to generate the interrupt.

(The COM bit in the EC interrupt mask register = 1)

NXTIDERR (bit 1)

This bit is set to 1 and the NXTIDERR bit in the diagnostic register (COMR1) becomes 1 to generate the interrupt.

(The COM bit in the EC interrupt mask register = 1)

TA (bit 0)

This bit is set to 1 and the TA bit in the status register (COMR0) becomes 1 to generate the interrupt.

(The COM bit in the EC interrupt mask register = 1)

3.2.2 COMR1 Register: Diagnostic/Command Register

| COMR1 (Diagnostic Register) | | address:02h | | |
|-----------------------------|----------|-------------|--------------------|-------------|
| [READ] | | | | |
| bit | name | init. value | Description | |
| 15-8 | ----- | 0 | reserved (all "0") | |
| 7 | MY-RECON | 0 | My Reconfiguration | |
| 6 | DUPID | 0 | Duplicate ID | |
| 5 | RCVACT | 0 | Receive Activity | |
| 4 | TOKEN | 0 | Token Seen | |
| 3 | EXCNAK | 0 | Excessive NAK | |
| 2 | TENTID | 0 | Tentative ID | |
| *1 | 1 | NXTIDERR | 0 | New Next ID |
| | 0 | ----- | 0 | Reserved |

| COMR1 (Command Register) | | address:02h | |
|--------------------------|-------|-------------|--------------------|
| [WRITE] | | | |
| bit | name | init. value | Description |
| 15-8 | ----- | -- | Reserved (all "0") |
| 7-0 | D7-0 | -- | D7-0 |

*1 Not equivalent to the ARCNET original specifications.

- When reading: ARCNET diagnostic register

MY-RECON (bit 7)

When this bit is 1, it indicates that the local reconfiguration timer has timed out. This timeout sends a reconfiguration burst signal. It is read after an interrupt has been generated by setting RECON bit = 1. (RECON bit = 1 is set after MY-RECON bit is set to 1.) The bit is cleared when read or by software reset.

DUPID (bit 6)

When this bit is 1 in the offline state (TXEN = 0), it indicates that a duplicate node ID exists on the network. In this state, the network cannot be accessed (TXEN = 1). Check that all the node ID settings are correct. In the online state (TXEN = 1), DUPID is set to 1 every time a token addressed to it is received**. This bit is cleared when read or by software reset.

** Disregard this first setting of DUPID=0 -> 1. The second setting indicates a token addressed to its own Circlink.

RCVACT (bit 5)

When this bit is 1, it indicates that activity has been detected at the Circlink receive input. This bit is cleared when read or by software reset.

TOKEN (bit 4)

When this bit is 1, it indicates that a token signal on the network has been detected. Note that the token signal sent by this bit cannot be detected. This bit is cleared when read or by software reset.



EXCNAK (bit 3)

When this bit is 1, it indicates that a "NAK" was received 4 or 128 times from the receiving node (Four NAKS is determined by a bit setting) in response to "Free Buffer Enquiry" during the send. It is possibly caused by the blind state (ECRI = 1) of the destination node. This bit can not be cleared by a bit-read but can be cleared by software reset or by writing the EXCNAK clear command (0Eh).

TENTID (bit 2)

When this bit is 1, it indicates that the COMR7-000 (Tentative ID register) matches the ID value in a token signal in the network. Note that the ID value in a token signal sent by this bit itself cannot be compared. With the function in normal online state (TXEN = 1), a node ID map of the network can be created. This bit is cleared when read or by software reset.

NXTIDERR (bit 1)

This bit is set when receiving no response from the token passed to the node with the ID of node ID + 1^{*2} and the token is passed to another node. This bit can be cleared by a software reset or by the writing of NXTIDERR clear command (09h), but is not cleared when read.

*2: Node 01 when the node is MAXID node.

NOTE: To detect the DUPID and TENTID bits, wait for the maximum polling cycle time of token after the NID or TENTID value is changed.

- When writing: ARCNET command register

This command register is not used in Circlink: the EC command register in 3.2.12 must be used. The commands described there include all valid Circlink commands.

3.2.3 COMR2 Register: Page Register

COMR2 (Page Register) address:04h
[READ/WRITE]

| bit | name | init. value | description |
|--------|---------|-------------|--------------------|
| 15-8 | ----- | 0 | reserved (all "0") |
| 7 | RDDATA | X | Read Data |
| 6 | AUTOINC | X | Auto Increment |
| *1 5 | nWRAPAR | 0 | Wrap-around mode |
| *1 4-0 | PAGE4-0 | X | Page 4-0 |

*1: Not equivalent to the ARCNET original specifications. (Bit length variable)

- When reading/writing: ARCNET address pointer upper register (New)

RDDATA (bit 7)

This bit specifies the type of access to data register (COMR4) handled.

1: Read from data register

0: Write to data register

AUTOINC (bit 6)

This specifies an automatic increment mode of the RAMADR accessing data register (COMR4). The incremental value is +1 for 8-bit bus width and 0 word mode (W16 = L, WDMD = 0), and +2 for 8-bit bus width and 1 word mode (W16=L, WDMD=1) or 16-bit bus width (W16=1).

1: Automatically incremented

0: Not automatically incremented

nWRAPAR (bit 5)

This bit specifies internal operation mode when the most significant bit (MSB) of RAMADR is carried over.

1: Move to the top of the next page

0: Go back to the top of the current page

PAGE 4-0 (bits 4 to 0)

These bits specify the page numbers of the packet buffers. Rewriting these five bits is not valid before the address in the page (COMR3) is written. Note that the upper limit of the specifiable value is restricted by the page size, and unnecessary higher bits are deleted.

3.2.4 COMR3 Register: Page-internal Address Register

COMR3 (Address Register) address:06h
[READ/WRITE]

| bit | name | init. value | description |
|--------|-----------|-------------|--------------------|
| 15-8 | ----- | 0 | reserved (all "0") |
| *1 7-0 | RAMADR7-0 | X | RAM Address 7-0 |

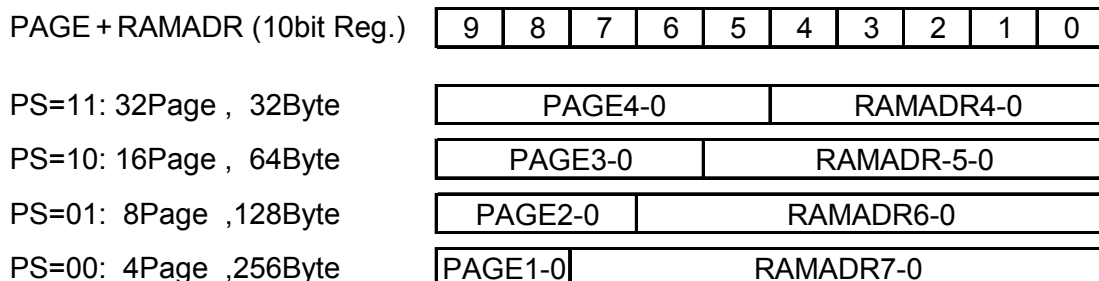
*1: Not equivalent to ARCNET original specifications. (The bit length variable)

- When reading/writing: ARCNET address pointer lower register (New)

RAMADR 7-0 (bits 7 to 0)

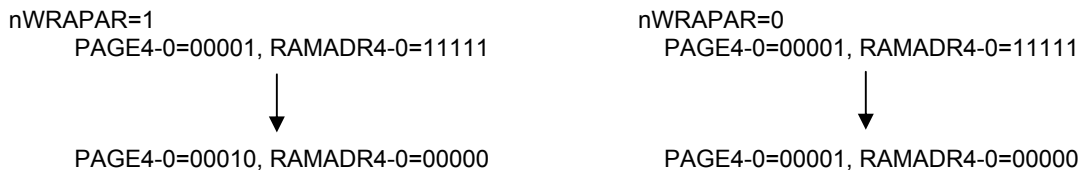
These bits specify addresses in the pages of the packet buffers. When the AUTOINC bit of COMR2 is 1, the value increments every time the data register (COM4) is accessed. The upper limit of the specifiable value is restricted by the size of the page.

The COMR2 page (PAGE) and COMR3 page-internal address (RAMADR) registers actually comprise one 10-bit register. The boundary differs depending on the specification of the page size, as shown below:



References of 2.5.1 chapter "RAM access" about the structure of a/the packet buffer

In continuously accessing data register with AUTOINC = 1 set, you can specify how to carry out overflowing RAMADR with nWRAPAR bit of COMR2. Zero (0) set-up carries it out to the top of the current page and one (1) set-up move it to the top of the next page (or to #00 if the current is the final page). An example of the operation at PS = 11 is shown below.



COMR4 Register: Data Register

(1) 16 Bit Mode (W16=H)

COMR4 (Data Register) address:08h
[READ/WRITE]

| | bit | Name | init. Value | description |
|----|------|-----------|-------------|---------------|
| *1 | 15-0 | RAMDT15-0 | X | RAM Data 15-0 |

(2) 8 Bit Mode and Word Mode=ON (W16=L, WDMD=1)

COMR4 (Data Register) address:08h/09h
[READ/WRITE]

| | bit | name | init. value | Description |
|----|------|-----------|-------------|---------------|
| *1 | 15-8 | RAMDT15-8 | X | RAM Data 15-8 |
| *1 | 7-0 | RAMDT7-0 | X | RAM Data 7-0 |

NOTE: To preserve the upper and lower bytes of word data in the same packet, COMR4 must be accessed in the order of 08h access → 09h access.

(access in the order of 09h → 08h, 08h → 08h, or 09h → 09h will not preserve this data). This restriction applies to both reading and writing.

The upper/lower relationship is selected by the nSWAP pin.

(3) 8 Bit Mode and Word Mode=Off (W16=L, WDMD=0)

COMR4 (Data Register) address:08h or 09h
[READ/WRITE]

| | bit | Name | init. Value | Description |
|----|------|----------|-------------|--------------------|
| | 15-8 | ----- | 0 | Reserved (all "0") |
| *1 | 7-0 | RAMDT7-0 | X | RAM Data 7-0 |

*1 Not equivalent to the ARCNET original specifications.

- When reading/writing: ARCNET Data register(New)

Writing/ reading out the address in the 1 kByte RAM is indicated by the page register and intra-page address register. Data access to packet buffer is performed via the data register.

Reading/writing is set by the RDDATA bit of COMR2.

NOTE: Data can be accessed using settings in the RDDATA register only. For example, data register writing with RDDATA = 1 setting, or data register reading with RDDATA = 0 setting will not normally be completed.

3.2.5 COMR5 Register: Sub-address Register

| COMR5 (Sub-address reg.) | | address:0Ah | |
|--------------------------|----------|-------------|--------------------|
| [READ/WRITE] | | | |
| bit | name | init. value | description |
| 15-4 | ----- | 0 | reserved (all "0") |
| 3-0 | SUBAD3-0 | 0,0,0,0 | Sub Address 3-0 |

NOTE: Do not set the value "5-9h, C-Fh" to SUBAD3-0.

- When reading/writing: ARCNET sub-address register

SUBAD [2:0] (bits 2 to 0)

Specifying sub-addresses for selecting seven registers assigned to COMR7. Be sure to set the sub-address first, and then access to COMR7.

SUBAD3-0 = 0000 (0h) : Selection of TENTATIVE ID Register

SUBAD3-0 = 0001 (1h) : Selection of NODE ID Register

SUBAD3-0 = 0010 (2h) : Selection of SETUP1 Register

SUBAD3-0 = 0011 (3h) : Selection of NEXT ID Register (Only Read)

SUBAD3-0 = 0100 (4h) : Selection of SETUP2 Register

SUBAD3-0 = 1010 (Ah) : Selection of GPIO Data Register

SUBAD3-0 = 1011 (Bh) : Selection of GPIO Direction Control Register

3.2.6 COMR6 Register: Configuration Register

COMR6 (Configuration reg.) address:0Ch
[READ/WRITE]

| bit | name | init. value | description |
|--------|----------|-------------|--------------------|
| 15-8 | ----- | 0 | reserved (all "0") |
| 7 | RESET | 0 | Reset |
| *1 6 | ----- | 0 | reserved ("0") |
| *3 5 | TXEN | 0/1 *4 | Transmit Enable |
| 4 | ET1 | 1 | Extended Timeout 1 |
| 3 | ET2 | 1 | Extended Timeout 2 |
| *2 2 | BACKPLAN | 1 | Back Plane |
| *5 1-0 | ----- | 0,0 | reserved (all "0") |

*1 Not equivalent to the ARCNET original specifications.

(Function elimination)

*2 Not equivalent to the ARCNET original specifications.

(Change Initial Value)

*3 Not equivalent to the ARCNET original specifications.

(Additional Function)

*4 The Initial value changes by operation mode.

0 (Off Line) at the time of peripheral mode

1 (On Line) at the time of standalone mode.

*5 These specification are not equal with ARCNET specification.

(SUBAD1-0 be integration to the COMR5 register)

- When reading/writing: ARCNET configuration register

RESET (bit 7)

This bit sets a software reset. Setting this bit to 1 causes software reset and setting 0 releases it.

TXEN (bit 5)

This bit sets access to the network (online and offline respectively); Setting 1 to this bit is on-line and setting 0 is off-line. A temporary software reset is applied when the bit is changed from 0 to 1. (The software reset is released automatically.) The software reset is not applied when the bit is changed from 1 to 0.

This bit is the same as the TXEN bit in the mode register described in 3.2.18, which is the bit usually used.

Datasheet**ET1, ET2 (bits 4 and 3)**

These bits set the timeout time of the response and idle timers. The following timeout times are the values applicable when the transfer rate is 2.5 Mbps (the values become half at 5 Mbps).

ET2,ET1 = 0,0 Response Timer = 1193.6 uS Idle Timer = 1312 uS MAX Distances = 118.4 km

ET2,ET1 = 0,1 Response Timer = 596.8 uS Idle Timer = 656 uS MAX Distances = 57.6 km

ET2,ET1 = 1,0 Response Timer = 298.4 uS Idle Timer = 328 uS MAX Distances = 28.8 km

ET2,ET1 = 1,1 Response Timer = 74.7 uS Idle Timer = 82 uS MAX Distances = 6.4 km

These timeout times must be identical in every node on the network. Refer to the description of the RCNTM1, 0 bits in the SETUP2 register.

BACKPLAN (bit 2)

This bit selects back plane mode and normal (dipulse) mode; setting 1 to the bit selects back plane mode and setting 0 selects normal (dipulse) mode. Back plane mode is usually used (default).

3.2.7 COMR7 Register

Seven registers are defined for COMR7, selected by the selection of the SUBAD [3:0] bits of COMR5.

| COMR7-0000 (Tent. ID Register) | | | | address:0Eh |
|--------------------------------|--------|-------------|--------------------|-------------|
| [READ/WRITE] | | | | SUBAD=0000 |
| bit | Name | init. value | Description | |
| 15-5 | ----- | 0 | reserved (all "0") | |
| *1 4-0 | TID4-0 | all "0" | Tentative Node ID | |

*1 Not equivalent to the ARCNET original specifications.

(Reduction in a the number of bits)

- When reading/writing: ARCNET Tentative ID register

TID [4:0] (bits 4 to 0)

The ID value specified by this register is compared with the ID value in a token signal in the network and the results indicated by the TENTID bit of the diagnostic register. TENTID becomes 1 if the comparison result matches.

| COMR7-0001 (Node ID Register) | | | | address:0Eh |
|-------------------------------|--------|-------------|--------------------|-------------|
| [READ/WRITE] | | | | SUBAD=0001 |
| bit | name | init. value | Description | |
| 15-5 | ----- | 0 | reserved (all "0") | |
| *1 4-0 | NID4-0 | all "0" | My Node ID | |

*1 Not equivalent to the ARCNET original specifications.

(Reduction the number of bits)

- When reading/writing: ARCNET Node ID register

NID [4:0] (bits 4 to 0)

When INIMODE = 1, this bit specifies the node ID. This function is the same as that of the NID register described in 3.2.23, which is usually used instead of this register.

| COMR7-0010 (Setup1 Register) | | | | address:0Eh |
|------------------------------|----------|-------------|----------------------------|-------------|
| [READ/WRITE] | | | | SUBAD=0010 |
| bit | name | init. value | description | |
| 15-8 | ----- | 0 | reserved (all "0") | |
| *1 7 | ----- | 1 | reserved ("1") | |
| 6 | FOURNAKS | 0 | Four NACKS | |
| 5 | ----- | 0 | reserved ("0") | |
| 4 | ----- | 0 | reserved ("0") | |
| 3-1 | CKP2-0 | 0,0,0 | Clock Prescaler Bits 2,1,0 | |
| 0 | ----- | 0 | reserved ("0") | |

*1: Not equivalent to the ARCNET original specifications. (Function elimination)

- When reading/writing: ARCNET SETUP1 register

FOURNAKS (bit 6)

This bit specifies the number of NAK responses to the "Free Buffer Enquiry", function of the EXCNAK bit of the diagnostic register. Setting 1 to this bit specifies 4 times, and to 0 specifies 128 times.

CKP [2:0] (bits 3 to 1)

INIMODE = 1 specifies the communication speed (transfer rate). This function is the same as that of the CKP register described in 3.2.25, which is usually used instead of this register.

| COMR7-0011 (Next ID Register) | | | | address:0Eh |
|-------------------------------|-----------|-------------|--------------------|-------------|
| [READ ONLY] | | | | SUBAD=0011 |
| bit | name | init. value | description | |
| 15-5 | ----- | 0 | reserved (all "0") | |
| *1 4-0 | NEXTID4-0 | all "0" | Next Node ID | |

*1: Not equivalent to the ARCNET original specifications.

(Reduction the number of bits and function modifications)

NOTE: Do not write to this register.

- When reading: ARCNET NEXT ID register

NEXTID [4:0] (bit 4 to 0)

It is possible for the node to read out value of the node ID from a sending node. In CirLink, the following ID value is fixed to the ID value of the node + 1. In case of no response after sending the token to the node of ID value equaling to the node ID + 1 (absent receiver) and the token is passed to another node, the NEXTIDERR bit of the diagnostic register will be set to 1.

COMR7-0100 (Setup2 Register) address:0Eh
 [READ/WRITE] SUBAD=0100

| | bit | Name | init. value | description |
|----|------|----------|-------------|-----------------------------------|
| | 15-8 | ----- | 0 | reserved (all "0") |
| *1 | 7 | ----- | 0 | reserved ("0") |
| *3 | 6 | FARB | 0 | reserved ("0") |
| *1 | 5,4 | ----- | 0,0 | reserved (all "0") |
| *1 | 3 | ----- | 1 | reserved ("0") |
| *1 | 2 | ----- | 1 | reserved ("0") |
| *2 | 1-0 | RCNTM1-0 | 1,1 | Reconfiguration (RECON) Timer 1,0 |

*1 Not equivalent to the ARCNET original specifications. (Reduction function)

*2 Not equivalent to the ARCNET original specifications. (Change initial value)

*3 Not equivalent to the ARCNET original specifications. (Addition of new function)

- When reading/writing: ARCNET Setup2 Register

FARB (bit 6)

Increases the speed of the RAM Access controller. In default setting, it sets the yes/no setting of temporary relay reception of 128 byte/page during CKP=000 setting. For further details, please refer to section 2.9.1 - Temporary Receive and Direct Receive.

0: 128-byte/page temporary relay reception **denied** (Default),

RAM Access controller input clock has a single-sided function.

1: 128-byte/page temporary relay reception **allowed**

RAM Access controller input clock has a double-sided function. Accordingly, the input clock must be **below 20 MHz**.

NOTE: The FARB bit switch must be operated during Software Reset.

RCNTM1, RCNTM0 (bits 1 and 0)

These bits set the timeout time of the reconfiguration timer. The following timeout times are applicable when the transfer rate is 2.5 Mbps. (The values become half at 5 Mbps)

RCNTM1-0

00 : Timeout = 840 mS

01 : Timeout = 210 mS

10 : Timeout = 105 mS

11 : Timeout = 52 mS (Default)

The timeout times above are values for COMR6: Reconfiguration register's ET1 and ET2 = 1,1 respectively. If ET1 and ET2 are other than the above value, the timeout time is doubled. (This includes the case of ET1 pin=Low.) Refer to section 2.14.2 ET1 pin and 3.2.7 ET1, ET2 bit for details.



COMR7-1010 (GPIO Data Register) address:0Eh
 [READ/WRITE] SUBAD=1010

| bit | Name | init. value | description |
|--------|--------|-------------|--------------------|
| 15-8 | ----- | 0 | reserved (all "0") |
| *1 7-0 | GPD7-0 | all "0" | GP-I/O Data |

*1 Not exist in the ARCNET original specifications.

- When reading/writing: GPIO Data Register

GPD[7:0] (bit 7-0)

Write : write data which outputs to GPI7-0 pin

Read : read the state of the GPIO7-0 pin

GPD7 corresponds to the GPIO7 pin. (Refer to section 2.15.)

COMR7-1011 (GPIO Direction Register) address:0Eh
 [READ/WRITE] SUBAD=1011

| bit | Name | init. value | description |
|--------|----------|-------------|----------------------|
| 15-8 | ----- | 0 | reserved (all "0") |
| *1 7-0 | nGPOE7-0 | all "1" | GP-I/O Output Enable |

*1 Not exist in the ARCNET original specifications.

- When reading/writing: GPIO Direction Register

nGPOE[7:0] (bit 7-0)

Set the direction of GPIO7-0 pin. The direction can be set by every one bit.

nGPOE7 corresponds to the GPIO7 pin. (Refer to section 2.15.)

0 : Output mode

1 : Input mode

Supplement: Refer to the ARCNET Controller COM20020 Rev.D Data Sheet for further details on each bit of COMR0 to COMR7.

3.2.8 NST Register: Network Standard Time

NST address:10h
(Read Only)

| Bit | name | init. value | description |
|------|---------|-------------|-----------------------|
| 15-0 | NST15-0 | 0000h | Network Standard Time |

NST15-0 (bits 15 to 0)

These bits indicate the standard time in the network. Refer to section 2.12 for details.

Accessing the NST register can dynamically provide the latest time data. Since NST is a 16 bit counter, it is necessary to read the even address side (10h) first when an 8-bit bus is used. When the even address side (11h) is read out, the remaining 8 bits of the NST are latched internally.

3.2.9 INTSTA Register: EC Interrupt Status

INTSTA address:12h
(Read Only, Read/Write)

| bit | name | dir. | init. value | Description |
|-----|----------|------|-------------|----------------------------------|
| 15 | RXERR | R/W | 0 | Receiver Error |
| 14 | CMIECC | R/W | 0 | CMI RX Error Correction occurred |
| 13 | NSTUNLOC | R | 1 or 0 | NST Unlock |
| 12 | WARTERR | R | 0 | Warning Timer Error |
| 11 | FRCV | R/W | 0 | Free-format mode Received |
| 10 | RRCV | R/W | 0 | Remote-buffer mode Received |
| 9 | MRCV | R/W | 0 | My Received |
| 8 | SIDF | R/W | 0 | SID Found |
| 7 | TKNRETF | R/W | 0 | Token Retry occurred |
| 6 | ACKNAKF | R/W | 0 | Corrupt ACK/NAK Recovered |
| 5 | HUBWDTO | R/W | 0 | HUB Watch Dog Timer time-out |
| 4 | CPERR | R/W | 0 | Tx CP Error |
| 3 | COM | R | 0 | ARCNET CORE Interrupt |
| 2 | FBENR | R/W | 0 | FBE No Reply |
| 1 | TXERR | R/W | 0 | Transmitter Error |
| 0 | TA | R | 1 | Transmitter Available |

The upper 8 bits indicate the receive status, and the lower 8 bits indicate the send status. Every bit in this register can be used to generate an interrupt.

RXERR (bit 15)

This bit indicates that receive has stopped due to an error during packet receive. As soon as this bit is set, the details of the error are indicated by the RXEC 2-0 (bits 7 to 5) in the ERRINFO register, and the ID of the sending node is stored to RESID 4-0 (bits 4 to 0) in the same register. Note that this bit is not set by any message other than a packet (Token, FBE, ACK, or NAK).

This bit is cleared by writing 1 or by a software reset.

**CMIECC (bit 14)**

This bit indicates that error correction of received data has been performed in the CMI decoding circuit. As soon as this bit is set, the details of the error are stored in CMIEI3-0 (bits 11 to 8) of the ERRINFO register.

This bit is cleared by writing a 1 or by software reset.

NSTUNLOC (bit 13)

Indicates synchronizing with the CM node's NST. This bit is set by Software Reset. For further details, please refer to section 2.12.

0: Synchronous Lock status 1: Synchronous Unlock Status (Initial Value)

In the CM node, this flag goes into steady state 0 (Synchronous Lock status). Accordingly, the initial settings are as detailed below:

In Peripheral mode, the CM node ID is set in a register after cancellation of Hardware Reset. After these values are imported, the output is 1 until it assumes itself as a CM node (it becomes 0 after that). During Software Reset, due to the CM Node ID being immediately imported, the CM Node ID is fixed at 1→0 immediately after set-up in the register.

In standalone mode, the CM node ID is the pin setting when it is the same setting as the CM node setting. The output is 1 during Hardware Reset, and 0 when Hardware Reset is cancelled.

WARTERR (bit 12)

This bit is set if data is not received by any page set in remote buffer receive mode within a fixed period. This bit is cleared by the WARTERR clear command or by a software reset.

1: No receive within a fixed period, 0: Receive within a fixed period

FRCV (bit 11)

This bit is set if the reception by any page set in free format receive mode is completed normally. This bit is cleared by writing a 1 or by a software reset.

1: Receive complete, 0: Receive in progress

RRCV (bit 10)

This bit is set if the reception of any page set in remote buffer receive mode is completed normally. This bit is cleared by writing a 1 or by a software reset.

1: Receive complete, 0: Receive in progress

MRCV (bit 9)

This bit is set if the reception of a packet sent to this node (DID = NID) is completed normally. This bit is cleared by writing a 1 or by a software reset.

1: Receive complete, 0: Receive in progress

SIDF (bit 8)

This bit is set if a packet sent from the SID specified by the SSID register is received. This bit is cleared by writing a 1 or by a software reset.

TKNRETF (bit 7)

This bit indicates that a token retry is performed. Refer to section 2.4.1 - Reducing Token Loss for details. This bit is cleared by writing a 1 or by a software reset.

ACKNAKF (bit 6)

This bit indicates that counter measures to handle corrupted ACK/NAK data have been implemented. Refer to section 2.4.1 for details. This bit is cleared by writing a 1 or by a software reset.

HUBWDTO (bit 5)

This bit indicates that the HUB unit has been reset which was caused by timeout of watchdog timer. This is done to prevent the direction control circuit of the HUB unit from hanging-up. A timeout occurs if the transmit signal from HUB is continuously active for 3.27 ms or more. (when using 2.5 Mbps. At 5 Mbps, the value is half -> 1.64 ms)

This timeout causes the HUB unit and two CMI units to be automatically reset. (If the HUB unit is OFF, the CMI units are not reset.) This bit is cleared by writing a 1 or by a software reset.

CPERR (bit 4)

This bit is set if the CP field of the preceding packet is of a value that exceeded the page boundary, or is between 00h and 02h, both of which are invalid CP settings.

Refer to section 2.5.3, Packet Data Structure for details. This bit is cleared by writing a 1 or by a software reset.

1: Packet including invalid CP field is sent, 0: Normal packet is sent

COM (bit 3)

This bit is set to 1 if there is an interrupt from the ARCNET core. Be sure to set the COMR0 mask register bits when required.

This bit is set to 1 when the interrupt is generated by EXCNAK, RECON, NXTIDERR and TA bit in the mask register of COMR0.

FBENR (bit 2)

Both FBENR and TXERR bits are set if there is no response to FBE . If FBENR is set, it is possible to determine that data is transmitted to a node that is not receiving properly, thus identifying failures based on deformed packet data. This bit is cleared by writing a 1, issuing a send command, or by a software reset.

TXERR (bit 1)

This bit is set if sending fails. Be aware that this function is the opposite of that of the ARCNET-original TMA bit. This bit is cleared by writing a 1 , issuing the send command, or by a software reset.

TA (bit 0)

This bit is the same as the TA bit of the COMR0: ARCNET status register. (Refer to that register for details.) This bit becomes 0 only while the send command is being issued.

Combination and meaning of transmission status

| TA | TXERR | FBENR | Meaning |
|----|-------|-------|---------|
|----|-------|-------|---------|

Datasheet

| | | | |
|---|---|---|--------------------------------|
| 0 | X | X | Transmitting |
| 1 | 0 | 0 | Transmit complete |
| 1 | 1 | 0 | Transmit Error by data error |
| 1 | 1 | 1 | Transmit Error by FBE unanswer |

3.2.10 INTMSK Register: EC Interrupt Mask

| INTMSK | | | | address:14h (Read/Write) |
|--------|----------|-------------|----------------------------------|-----------------------------|
| bit | name | init. value | description | |
| 15 | RXERR | 0 | Receiver Error | |
| 14 | CMIECC | 0 | CMI RX Error Correction occurred | |
| 13 | NSTUNLOC | 0 | NST Unlock | |
| 12 | WARTERR | 0 | Warning Timer Error | |
| 11 | FRCV | 0 | Free-format mode Received | |
| 10 | RRCV | 0 | Remote-buffer mode Received | |
| 9 | MRCV | 0 | My Received | |
| 8 | SIDF | 0 | SID Found | |
| 7 | TKNRETF | 0 | Token Retry occurred | |
| 6 | ACKNAKF | 0 | Corrupt ACK/NAK Recovered | |
| 5 | HUBWDTO | 0 | HUB Watch Dog Timer time-out | |
| 4 | CPERR | 0 | TX CP Error | |
| 3 | COM | 0 | ARCNET CORE Interrupt | |
| 2 | FBENR | 0 | FBE No Reply | |
| 1 | TXERR | 0 | Transmitter Error | |
| 0 | TA | 0 | Transmitter Available | |

This register corresponds to interrupt status, and being set to 1, the interrupt signal becomes active when the corresponding status becomes 1.

3.2.11 ECCMD Register: EC Command Register

| ECCMD | | address:16h (Read/Write) | |
|-------|----------|-----------------------------|--------------------|
| bit | name | init. value | description |
| 15-8 | ----- | 0 | reserved (all "0") |
| 7-0 | ECCMD7-0 | 00h | EC Command |

ECCMD 7-0 (bits 7 to 0)

This command is unique to Circlink. When the bus width is 8 bits ($W16 = 0$), access to higher bytes is invalid; the command accesses the lower bytes. When the bus width is 16 bits ($W16 = 1$), "00h" should be specified for the higher bytes. The readable value from this register is the prior write command.

03h: Send command

This command instructs the Circlink to start sending. After issuing the send command, sending is started upon receipt of token to the node. In continuous send mode ($TXM = 1$, $RTO = 0$) or in remote buffer sending mode, an automatic send operation repeats whenever a node receives the token after the first send command has been issued.

In Free Format send mode ($TXM = 0$) or the remote buffer send mode, a send command must be issued each time in single send mode ($TXM = 1$, $RTO = 1$).

01h: Sending cancellation command

This command cancels the prior send command. After cancellation, the TA bit is set to 1. If this command is issued before the node receives the token, cancellation of the send is possible.

It is necessary to confirm tTA bit =1 because the cancellation is actually executed when the token arrives.

In continuous send mode ($TXM = 1$, $RTO = 0$) in the remote buffer send mode, continuous send operation can be stopped. (To restart, a send command is necessary.)

09h: NXTIDERR clear command

This command clears the NXTIDERR bit in COMR1 (Diagnostic register).

0Ah: WARTERR clear command

This command instructs initialization and start of the warning timer function. In addition, this command clears the WARTERR bit and the INTSTA register as well as the receive flag in the page that is set to the remote buffer mode.

0Eh: POR, EXCNAK clear command

This command clears the POR bit in COMR0 (status register) and the EXCNAK bit in COMR1 (diagnostic register). These bits cannot be cleared individually.

16h: RECON clear command

This command clears the RECON bit in COMR0 (status register).

1Eh: Concurrent operation of POR, EXCNAK clear and RECON clear command

These commands clear all POR, EXCNAK, and RECON bits.

3.2.12 RSID Register: Receive SID

RSID address:18h
(Read Only)

| bit | name | init. value | description |
|-------|----------|-------------|--------------------|
| 15-13 | ----- | -- | reserved (all "0") |
| 12-8 | MRSID4-0 | all "0" | My Received SID |
| 7-5 | ----- | -- | reserved (all "0") |
| 4-0 | RSID4-0 | all "0" | Received SID |

MRSID 4-0 (bits 12 to 8)

SID of the packet to the node received last.

RSID 4-0 (bits 4 to 0)

SID of packet received last.

3.2.13 SSID Register: SID

SSID address:1Ah
(Read/Write)

| bit | name | init. value | description |
|------|---------|-------------|--------------------|
| 15-5 | ----- | -- | reserved (all "0") |
| 4-0 | SSID4-0 | all "0" | Search SID |

SSID 4-0 (bits 4 to 0)

When a packet having SID as defined in section 3.2.13, is received, the SIDF bit of the interrupt status register is set.

3.2.14 RXFH Register: Receive Flag (higher side)

| RXFH | | | | address:1Ch (Read/Write) |
|------|-------|-------------|-------------------------|-----------------------------|
| bit | Name | Init. value | description | |
| 15 | RXF31 | 1 | Receive Flag (Page #31) | |
| 14 | RXF30 | 1 | Receive Flag (Page #30) | |
| 13 | RXF29 | 1 | Receive Flag (Page #29) | |
| 12 | RXF28 | 1 | Receive Flag (Page #28) | |
| 11 | RXF27 | 1 | Receive Flag (Page #27) | |
| 10 | RXF26 | 1 | Receive Flag (Page #26) | |
| 9 | RXF25 | 1 | Receive Flag (Page #25) | |
| 8 | RXF24 | 1 | Receive Flag (Page #24) | |
| 7 | RXF23 | 1 | Receive Flag (Page #23) | |
| 6 | RXF22 | 1 | Receive Flag (Page #22) | |
| 5 | RXF21 | 1 | Receive Flag (Page #21) | |
| 4 | RXF20 | 1 | Receive Flag (Page #20) | |
| 3 | RXF19 | 1 | Receive Flag (Page #19) | |
| 2 | RXF18 | 1 | Receive Flag (Page #18) | |
| 1 | RXF17 | 1 | Receive Flag (Page #17) | |
| 0 | RXF16 | 1 | Receive Flag (Page #16) | |

RXF31-16 (bits 15 to 0)

This is a flag that indicates the receive status of pages from 16 to 31. The definition is different depending on the receive mode of the corresponding page. In the free format receive mode, the register becomes a writable register. This register is effective only when page size is set to the 32-byte mode due to RAM size; in other sizes, the readout is always "1".

Free format receive mode

[Flag definition] 1: Receive completed/Unauthorized state

0: Receive authorized

[Clear condition] Writing "1", or last data readout of corresponding page only in nACLR = 0

Remote buffer receive mode

[Flag definition] 1: Receive within a fixed time period

0: No receive within a fixed time period.

[Clear condition] Writing 0Ah (WARTERR clear command) in the ECCMD register, or OK in the warning monitoring result

If the all-receive-inhibit bit, ECRI, in the mode register is returned from 1 to 0, all the receive flags return to 1 regardless of their receive mode.

3.2.15 RXFL Register: Receive Flag (lower side)

| RXFL | | | | address:1Eh (Read/Write) |
|------|-------|-------------|-------------------------|-----------------------------|
| bit | name | Init. value | description | |
| 15 | RXF15 | 1 | Receive Flag (Page #15) | |
| 14 | RXF14 | 1 | Receive Flag (Page #14) | |
| 13 | RXF13 | 1 | Receive Flag (Page #13) | |
| 12 | RXF12 | 1 | Receive Flag (Page #12) | |
| 11 | RXF11 | 1 | Receive Flag (Page #11) | |
| 10 | RXF10 | 1 | Receive Flag (Page #10) | |
| 9 | RXF09 | 1 | Receive Flag (Page #09) | |
| 8 | RXF08 | 1 | Receive Flag (Page #08) | |
| 7 | RXF07 | 1 | Receive Flag (Page #07) | |
| 6 | RXF06 | 1 | Receive Flag (Page #06) | |
| 5 | RXF05 | 1 | Receive Flag (Page #05) | |
| 4 | RXF04 | 1 | Receive Flag (Page #04) | |
| 3 | RXF03 | 1 | Receive Flag (Page #03) | |
| 2 | RXF02 | 1 | Receive Flag (Page #02) | |
| 1 | RXF01 | 1 | Receive Flag (Page #01) | |
| 0 | ----- | 0 | reserved ("0") | |

RXF15-01 (bits 15 to 1)

This is flag indicates the receive status of pages 01 to 15. The definition is different depending on the receive mode of the corresponding page. In the free format receive mode, the register becomes a writable register. Bits from 15 to 4 are not effective when the page size is 128/256 and bits 15 to 4 are not effective when the page size is 256 bytes (the readout is always "1").

Free format receive mode

[Flag definition] 1: Receive completed/Unauthorized

0: Receive authorized

[Clear condition] Writing "1", or last data readout of corresponding page only in nACLR = 0

Remote buffer receive mode

[Flag definition] 1: Receive within a fixed time period

0: No receive within a fixed time period.

[Clear condition] Writing 0Ah (WARTERR clear command) in the ECCMD register, or OK in the warning monitoring result

If the all-receive-inhibit bit, ECRI, in the mode register is returned from 1 to 0, all the receive flags return to 1 regardless of their receive mode.

Supplement: Clearing the Receive Flag by writing 1

In Free Format receive mode receive flags RXF31 to RXF1 become 1 after receive completion and must be cleared (0) after being read. The clearance is executed by writing "1" in object bits to clear only the receive flag bits.

For example, if the readout data of the RXFH register (higher receive flag) is 01h; in this case, the data means receive completion of page #16. If this readout data (01h) is written back to the RXFH register, only the RXF 16 bit is cleared. Therefore, the bit in the RXFH register that is set after the RXFH register readout is not cleared by mistake. The important point is that the bits subject to be cleared are the bits of which the CPU recognizes as "1."

This description is also applicable to clearing flags in the Interrupt Status register.

3.2.16 CMID Register: Clock Master Node ID

| CMID | | | | address:20h (Read/Write) |
|------|---------|-------------|----------------------|-----------------------------|
| bit | name | init. value | description | |
| 15-5 | ----- | -- | reserved (all "0") | |
| 4-0 | CMID4-0 | all "0" | Clock Master Node ID | |

CMID 4-0 (bits 4 to 0)

These bits specify IDs of the clock master node and the standard node of the network standard time (NST). If a packet is received from the node set, the NST is loaded. If 0 is set, loading is not executed.

3.2.17 MODE Register: Operation Mode Setup Register

address:22h
(Read/Write)

| bit | Name | init. value | description |
|-------|----------|-------------|--------------------------------------|
| 15-13 | ----- | -- | reserved (all "0") -> Must write 000 |
| 12 | CMIERRMD | 0 | CMI RX Error Mode |
| 11 | NSTSEND | 0 | Network Standard Time SEND |
| 10 | NSTSTOP | 0 | Network Standard Timer STOP |
| 9 | INIMODE | 0 | Initialize Mode |
| 8 | TXEN | 0 or 1 | Tx Enable |
| 7 | ECRI | 0 | Circlink Receive Inhibit |
| 6 | BRE | 0 | Broadcast Receive Enable |
| 5 | TXM | 0 | Transmitter Mode |
| 4 | RTO | 0 | Remote buffer Tx Once mode |
| 3 | WDMD | 0 | Packet Data Word Mode |
| 2 | nTKNRTY | 0 | TOKEN Retry |
| 1 | nACKNAK | 0 | ACKNACK Mode |
| 0 | nACLR | 0 | Receive Flag Auto Clear |

CMIERRMD (bit12)

This bit sets the operation mode in the event of error correction during data packet receive in the CMI decoding circuit. When error correction (CMIECC = 1) is performed during a receive, if the receive is terminated this bit is set to 1. The receive termination process should follow 2.9.1 "Temporary receive and direct receive."

1: Terminates packet receive , 0: Does not terminate packet receive

NSTSEND (bit11)

This bit has a function that allows the nodes to alternate clock master to add the NST value to the last two bytes of packet similar to the function in clock master node. When this bit is set to 1, NST is sent instead of the last two bytes that are written in packet RAM.

1: Adds NST , 0: Dose not add NST

NSTSTOP (bit10)

This bit stops NST at the current count value.

1: Stops NST count , 0: Dose not stop NST count

INIMODE (bit 9)

This bit selects whether the Circlink initialization, which includes the MAXID number setup, page size setup, the node number setup, and communication rate prescaler setup, are set via an external input pin or by register specification. Since this bit is important in network settings, this bit must be rewritten in the condition of TXEN = 0 (offline). When this bit is rewritten, software reset is automatically executed. (The software reset is released automatically.)

1: Sets via register, 0: Sets via external input pin

TXEN (bit 8)

Setting this bit to 1 in CirLink enables network participation. The initial value differs depending on the operation mode; the starting status is 0 = offline and 1 = online in the peripheral mode and the standalone mode, respectively. This bit is the same as the TXEN bit in the COMR6 register. If this bit is rewritten from 0 to 1, software reset is automatically executed. (The software reset is released automatically.) The software reset is not applied when the bit is changed from 1 to 0.

1: Online state, 0: Offline state

ECRI (bit 7)

This bit stops automatic issuing of receive commands to the ARCNET core. The CirLink always receives; to stop receiving, set this bit to 1. Moreover, this bit returns NAK to the free buffer enquiry (FBE) to the bit. Returning this bit from 1 to 0 sets the receive flag registers RXF01 to RXF31 to the (initial) value of 1. When CirLink receives a token issued by itself, ECRI is set. This causes a delay because setting/clearing ECRI affects reception flags RXF0-RXF3. The delay is 52 ms; when the network data rate is 2.5 Mbps, and scales accordingly for other rates.

1: Normal stop, 0: Normal operation

NOTE: The delay will be caused by the time the result of changing ECRI reflected internally. ECRI is reflected when the token to oneself is received, and do the following processing, please after inserting the weight of maximum value (52mS @2.5Mbps) at the time of token surroundings cycle when you change ECRI. 52mS or less is delayed to the initialization operation of reception flag register RXF01-RXF31 when ECRI is returned to 1→0.

52mS is a value for 2.5Mbps. This time depends on transfer rate. If it is 5Mbps, this time is half (26mS). If it's 1.25Mbps, it is two time (104mS).

BRE (bit 6)

1: Receives broadcast packet, 0: Not receive

TXM (bit 5)

1: Remote buffer sending mode, 0: Free format sending mode

RTO (bit 4)

This bit specifies the sending count in the remote buffer sending mode

1: Only one packet sending, 0: Continuous auto-sending

WDMD (bit 3)

This bit specifies the data structure mode to access data register (COMR4) through 8-bit bus. When this bit is set to 1, to protect the higher and lower bytes of word data as one packet, it is necessary to perform an access to COMR4 in the order of 08h to 09h. (Protection is unavailable in the order of 09h to 08h, 08h to 08h, and 09h to 09h) The rule is applicable for both write and read.

1: 16-bit data batch, 0: 8-bit data batch

nTKNRTY (bit 2)

Setting this bit to 1 disables token re-send. (original operation of ARCNET)

nACKNAK (bit 1)

Setting this bit to 1 generates reconfiguration in ACK/NAK deformation. (original operation of ARCNET)

nACLR (bit 0)

Setting this bit to 1 disables automatic clearance of receive flag in the readout of the last data in the free format receive mode.

3.2.18 CARRY Register: Carry Selection for External Output

CARRY

address:24h

(Read/Write)

| bit | name | init. value | description |
|-------|-----------|-------------|--------------------|
| 15 | OFSMOD | 0 | OFFSET Mode |
| 14,13 | ----- | -- | reserved (all "0") |
| 12-8 | NSTOFS4-0 | all "0" | NST OFFSET |
| 7-4 | NSTC3-0 | 8h | NST Carry Select |
| 3-0 | WARTC3-0 | 8h | WART Carry Select |

OFSMOD (CARRY register: bit 15)

0: Automatic offset (default)

1: Manual offset

NOTE: Do not set OFSMOD bit = 1, when NSTPRE2 pin = Low

NSTOFS4-0 (CARRY register: bits 12 to 8)

These bit selects an offset from 0 to 31. The offset is "NST resolution * NSTOFS4-0".

NSTC3-0 (bits 7 to 4)

These bits specify the generation timing of external pulse output, nNSTCOUT, by means of the digit position of NST.

| NSTC3-0 | CARRY Digit | Check Output Cycle |
|---------|-------------|---------------------------------|
| 0000 | NST[0] | NST Resolution * 2 ¹ |
| 0001 | NST[1] | NST Resolution * 2 ² |
| 0010 | NST[2] | NST Resolution * 2 ³ |
| : | : | : |
| 1111 | NST[15] | NST Resolution* 2 ¹⁶ |

Refer to section 2.12 for the NST resolution.

WARTC3-0 (bits 3 to 0)

These bits specify the warning monitoring time at remote buffer receive by means of the digit position of timer (WT). Refer to section 2.9.4 for details of WT.

| WARTC3-0 | CARRY Digit | Check Period |
|----------|-------------|---------------------------------|
| 0000 | ----- | ILLEGAL Setting |
| 0001 | WT[1] | WT Resolution * 2 ¹ |
| 0010 | WT[2] | WT Resolution * 2 ² |
| : | : | : |
| 1111 | WT[15] | WT Resolution * 2 ¹⁵ |

3.2.19 RXMH register: Receive mode (higher side)

RXMH

 address:26h
(Read/Write)

| bit | name | init. value | description |
|-----|-------|-------------|-------------------------|
| 15 | RXM31 | 0 | Receive Mode (Page #31) |
| 14 | RXM30 | 0 | Receive Mode (Page #30) |
| 13 | RXM29 | 0 | Receive Mode (Page #29) |
| 12 | RXM28 | 0 | Receive Mode (Page #28) |
| 11 | RXM27 | 0 | Receive Mode (Page #27) |
| 10 | RXM26 | 0 | Receive Mode (Page #26) |
| 9 | RXM25 | 0 | Receive Mode (Page #25) |
| 8 | RXM24 | 0 | Receive Mode (Page #24) |
| 7 | RXM23 | 0 | Receive Mode (Page #23) |
| 6 | RXM22 | 0 | Receive Mode (Page #22) |
| 5 | RXM21 | 0 | Receive Mode (Page #21) |
| 4 | RXM20 | 0 | Receive Mode (Page #20) |
| 3 | RXM19 | 0 | Receive Mode (Page #19) |
| 2 | RXM18 | 0 | Receive Mode (Page #18) |
| 1 | RXM17 | 0 | Receive Mode (Page #17) |
| 0 | RXM16 | 0 | Receive Mode (Page #16) |

RXM31-16 (bits 15 to 0)

These bits specify the receive mode of page 16 to 31. The specification is effective only in the 32-byte mode of page size. If the page size is set to 64, 128, or 256 bytes, the mode is tied to the free format receive mode (0).

1: Remote buffer receive mode

0: Free format receive mode

NOTE: If the number of nodes in the network is small, the receive mode of unused nodes (pages) should be set to the free format receive mode (0). If the mode is set to the remote buffer mode (1) by mistake, the unused pages undergo warning timer response monitoring (except for the self node).

3.2.20 RXML Register: Receive Mode (lower side)

| RXML | | | | address:28h (Read/Write) |
|------|-------|-------------|-------------------------|-----------------------------|
| bit | name | init. value | Description | |
| 15 | RXM15 | 0 | Receive Mode (Page #15) | |
| 14 | RXM14 | 0 | Receive Mode (Page #14) | |
| 13 | RXM13 | 0 | Receive Mode (Page #13) | |
| 12 | RXM12 | 0 | Receive Mode (Page #12) | |
| 11 | RXM11 | 0 | Receive Mode (Page #11) | |
| 10 | RXM10 | 0 | Receive Mode (Page #10) | |
| 9 | RXM09 | 0 | Receive Mode (Page #09) | |
| 8 | RXM08 | 0 | Receive Mode (Page #08) | |
| 7 | RXM07 | 0 | Receive Mode (Page #07) | |
| 6 | RXM06 | 0 | Receive Mode (Page #06) | |
| 5 | RXM05 | 0 | Receive Mode (Page #05) | |
| 4 | RXM04 | 0 | Receive Mode (Page #04) | |
| 3 | RXM03 | 0 | Receive Mode (Page #03) | |
| 2 | RXM02 | 0 | Receive Mode (Page #02) | |
| 1 | RXM01 | 0 | Receive Mode (Page #01) | |
| 0 | ----- | -- | reserved ("0") | |

RXM15-08 (bits 15 to 8)

These bits specify the receive mode of pages 08 to 15. The specification is effective only in the 32- or 64-byte mode of page size. If the page size is set to 128, or 256 bytes, the mode is tied to the free format receive mode (0).

1: Remote buffer receive mode

0: Free format receive mode

RXM07-04 (bits 7 to 4)

These bits specify the receive mode of pages 04 to 07. The specification is effective only in the 32-, 64-, or 128-byte mode of page size. If the page size is set to 256-bytes, the mode is tied to the free format receive mode (0).

1: Remote buffer receive mode

0: Free format receive mode

RXM03-01 (bit 3-1)

These bits specify the receive mode of pages 01 to 03. The specification is effective in any page sizes.

1: Remote buffer receive mode

0: Free format receive mode

NOTE: If the number of nodes in the network is small, the receive mode of unused nodes (pages) should be set to the free format receive mode (0). If the mode is set to the remote buffer receive mode (1) by mistake, the unused pages undergo warning timer response monitoring (except for the self node).

3.2.21 MAXID Register: Selection of Max. ID

MAXID address:2Ah
(Read/Write)

| bit | name | init. value | Description |
|------|----------|-------------|--------------------|
| 15-5 | ----- | -- | Reserved (all "0") |
| 4-0 | MAXID4-0 | all "1" | MAXID |

MAXID 4-0 (bits 4 to 0)

These bits specify the max. node ID.

When INIMODE in the mode register and nDIAG pin are set to 1, the value set in this register is selected as the max. node ID. When INIMODE is set to 0, values in MAXID 4-0 of the external input pin become readable. Refer to section 1.6.9.

NOTE: To change these bits, be sure to set TXEN to 0 (off-line) before hand. If these bits change during the on-line state, it executes a software reset automatically (the software reset is released automatically).

3.2.22 NID Register: Selection of the Node ID

NID address:2Ch
(Read/Write)

| bit | Name | init. value | Description |
|------|--------|-------------|--------------------|
| 15-5 | ----- | -- | Reserved (all "0") |
| 4-0 | NID4-0 | all "0" | My Node ID |

NID4-0 (bits 4 to 0)

These bits specify the node ID.

When INIMODE of the mode register is set to 1, the value set in this register is selected as the node ID. When INIMODE is set to 0, values in NID 4-0 of the external input pin become readable. Refer to section 1.6.10.

NOTE: To change these bits, be sure to set TXEN to 0 (off-line) before hand. If these bits change during the on-line state, it executes a software reset automatically. (The software reset is released automatically.)

3.2.23 PS Register: Page Size Selection

| PS | | | | address:2Eh (Read/Write) |
|------|-------|-------------|--------------------|-----------------------------|
| bit | Name | init. value | Description | |
| 15-2 | ----- | -- | Reserved (all "0") | |
| 1-0 | PS1-0 | 0,0 | Page Size | |

PS1-0 (bits 1 to 0)

These bits specify the page size.

When INIMODE of the mode register is set to 1, the value set in this register is selected as the page size. When INIMODE is set to 0, values in PS1-0 of the external input pin become readable. Refer to section 1.6.8.

NOTE: To change these bits, be sure to set TXEN to 0 (off-line) beforehand. If these bits change during the on-line state, a software reset will be executed automatically (the software reset is released automatically).

3.2.24 CKP Register: Communication Rate Selection

| CKP | | | | address:30h (Read/Write) |
|------|--------|-------------|----------------------------|-----------------------------|
| bit | Name | init. value | Description | |
| 15-5 | ----- | -- | reserved (all "0") | |
| 2-0 | CKP2-0 | 0,0,0 | Clock Prescaler Bits 2,1,0 | |

CKP (bits 2 to 0)

These bits specify the communication rate of the CirLink. When INIMODE of the mode register is set to 1, the value set in this register is selected as the communication rate. When INIMODE is set to 0, values in CKP2-0 of the external input pin become readable. Refer to section 1.6.15.

NOTE: To change these bits, be sure to set TXEN to 0 (off-line) beforehand. If these bits change during the on-line state a software reset will be executed automatically (the software reset is released automatically).

3.2.25 NSTDIF Register: NST Phase Difference

| NSTDIF | | | | address:32h (Read Only) |
|--------|------------|-------------|------------------------|----------------------------|
| Bit | name | init. value | description | |
| 15 | DIFDIR | 1 | Differential Direction | |
| 14-0 | NSTDIF14-0 | all"0" | NST Differential | |

DIFDIR (NSTDIF register: bit 15)

This bit indicates a direction of NST phase difference. This bit is not applicable for the clock master node.

0: Ahead of CM node

1: Behind CM node

NSTDIF14-0 (NSTDIF register: bit 14-0)

These bits are used to express the absolute value of the phase difference between a CM node and NST in 0 to 32, 768. These bits are not applicable if the node is a clock master node.

Supplement: If the node is a clock master node, the NSTDIF register is tied to 0000h.

Accessing the NST register can dynamically provide the latest time data. Since NST is a 16 bit value, it is necessary to read the even address side (32h) first when 8-bit bus is used. When the even address side (13h) is read out, the remaining 8 bits of the NST are latched internally.

3.2.26 PININFO Register: Pin Setup Information

| PININFO | | | | address:34h (Read Only) |
|---------|-----|---------|-------------|-------------------------------|
| | bit | name | init. value | description |
| *1 | 15 | nSWAP | -- | status of nSWAP pin |
| *1 | 14 | W16 | -- | status of W16 pin |
| | 13 | nOPMD | -- | status of nOPMD pin |
| | 12 | nHUBON | -- | status of nHUBON pin |
| | 11 | nEHWR | -- | status of nEHWR pin |
| | 10 | nEHRD | -- | status of nEHRD pin |
| | 9 | nCMIBYP | -- | status of nCMIBYP pin |
| | 8 | CHKTSTP | -- | status of CHKTSTP (Test pins) |
| *1 | 7 | nSWAP | -- | status of nSWAP pin |
| *1 | 6 | W16 | -- | status of W16 pin |
| | 5 | nDIAG | -- | status of nDIAG pin |
| | 4 | TXENPOL | -- | status of TXENPOL pin |
| | 3 | NSTPRE1 | -- | status of NSTPRE1 pin |
| | 2 | NSTPRE0 | -- | status of NSTPRE0 pin |
| | 1 | WPRE1 | -- | status of WPRE1 pin |
| | 0 | WPRE0 | -- | status of WPRE0 pin |

Current status of several CirLink setup pins except for nMUX, nRWM, nSTALONE, nDSINV, ALEPOL, NSTPRE2, and WPRE2 can be read. It is useful to find pin setup errors by reading the current status.

CHKTSTP (bit 8) becomes 1 when one of the test pins (nTEST[3:0], nTMODE) becomes Low, thereby notifying the CirLink being in some test mode.

*1: The nSWAP and W16 pins used to set the CPU bus can read out bit 7 and 6 in either

accesses of 16 bit, 8 bit without swap or 8 bit with swap.

3.2.27 ERRINFO Register: Error Information

ERRINFO address:3Ah
(Read Only)

| bit | name | init. value | description |
|-------|----------|-------------|--|
| 15 | ----- | 0 | reserved ("0") |
| 14-12 | RCNCD2-0 | 0 | Reconfiguration Error Code |
| 11-8 | CMIEI3-0 | 0 | CMI RX Error Correction Information Code |
| 7-5 | RXEC2-0 | 0 | RX Error Code |
| 4-0 | RESID | 0 | RX Error SID |

RCNCD2-0 (bits 14 to 12)

These bits represent the reconfiguration-generation-cause code, which is the cause of the RECON bit (bit 2) of COMR0, in three bits. Issuing CLEAR FLAGS command to COMR1 or software reset clears these bits.

RCNCD2-0

- 000 : Received garbage data (noise) during the wait period after token sending (other than 000 to 101)
- 001 : Received a signal other than ACK during the wait period after packet sending
- 010 : Generated trailing 0 error after ACK receive during the wait period after packet sending
- 011 : Received a signal other than NAK/ACK during the wait period after F.B.E sending
- 100 : Generated trailing 0 error after ACK receive during the wait period after F.B.E sending
- 101 : Generated trailing 0 error after NAK receive during the wait period after F.B.E sending
- 11x : Undefined

001 to 101 do not generate reconfiguration since they are saved by NAK/ACK counter-deformation function (nACKNAK = 0: default). The reconfiguration generation cause at nACKNAK = 0 is only 000.

CMIEI3-0 (bits 11 to 8)

These bits represent the CMI receive error correction code, which is the cause of CMIECC bit (bit 14) = 1 in the INTSTA register in bits CMIE2-0-0. In CMIEI3, it indicates which port is the generation port. However, if HUB is turned off, the status is retained to 0. (0: Port 1 side, 1: Port 2 side)

Writing 1 to the CMIECC bit or software reset clears these bits.

CMIEI3

0: Port 1

1: Port 2

CMIEI2-0

- 000 : Corrected error data 10 to 00 in State#11 (S11)
- 001 : Corrected error data 11 to 01 in State#11 (S11)
- 010 : Corrected error data 10 to 11 in State#00 (S00)
- 011 : Corrected error data 00 to 01 in State#00 (S00)
- 100 : Corrected error data 10 to 00 in State#01a (S01a)
- 101 : Corrected error data 11 to 01 in State#01a (S01a)
- 110 : Corrected error data 10 to 10 in State#01b (S01b)
- 111 : Corrected error data 00 to 01 in State#01b (S01b)

For state numbers, refer to the State Transition of the State Machine in [A-5 CMIRX Block](#) in Appendix A CMI Modem.

RXEC2-0 (bits 7 to 5)

These bits represent the packet receive error code, which is the cause of RXERR bit (bit 15) = 1 in the INTSTA register in three bits. Writing 1 to the RXERR bit or software reset clears the setting. (Default is 000.)

RXEC2-0

- 000 : Frame error or Broadcast receiving when broadcast receiving prohibition is set. (BRE=0)
- 001 : CP error (Other than CP=0: 0 is long packet and it is not sent)
- 010 : CRC error
- 011 : Length error (Trailing 0 error)
- 100 : Mismatch of two DID (Other than in broadcast and addressed to the other node)
- 101 : Receive stop caused by CMIECC generation
- 110 : Receive in receive-unauthorized page (only in free format mode)
- 111 : Two or more simultaneously occur among 011, 101, and 110

RESID4-0 (bits 4 to 0)

These bits represent the SID value in receive packet, which causes RXERR bit (bit 15) = 1 in the INTSTA register, in five bits. Writing 1 to RXERR bit or software reset clears these bits.

Appendix A CMI Modem

A-1 Outline

Isolation by pulse transformers is widely used in this network. However, because in standard ARCNET transmission the presence or absence of a pulse is indicated by 0 or 1, in data consisting of a sequence of zeros such as 0x00 a prolonged succession of no pulses results in magnetic saturation of the transformer. As a countermeasure, an external circuit on the standard ARCNET is designed to prevent magnetic saturation (e.g. HYC4000). Because such an external component is not available in the CirLink external circuit, where only a normal RS485 transceiver and pulse transformer are installed, a CMI modem circuit is built in and converts the ARCNET into CMI coding.

A-2 CMI Code

In the CMI code the same value cannot continue for more than 2 bits.

The state it can take is decided, so it has a self-restoring function.

In CMI coding, input data is transitioned in 1-bit portions. Bits are indicated either as 11, 00, or 01. CMI coding is carried out by making these into CMI coding symbols. At decoding, the process is the exact opposite.

The CMI coding state transition diagram is shown below.

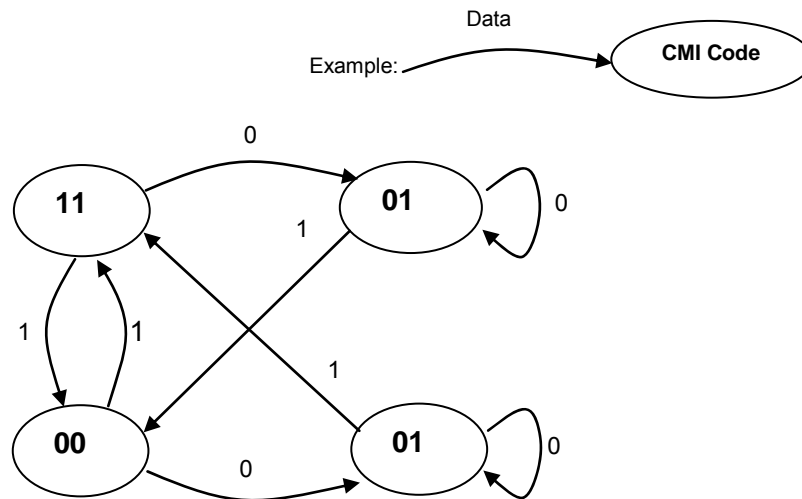


Figure 17 - CMI Coding State transition diagram

A-3 CMI Modem Configuration

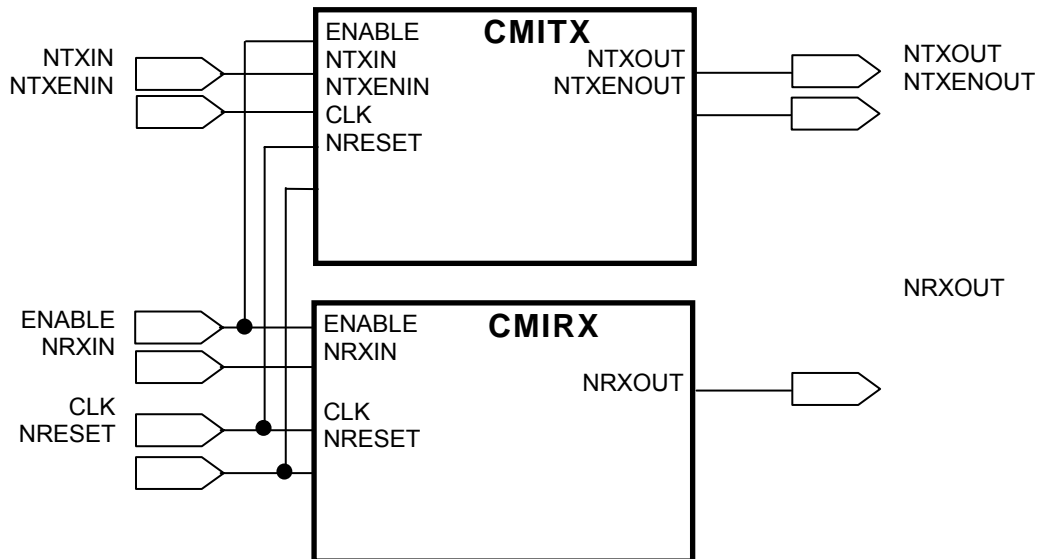


Figure 18 - CMI Modem Block Diagram

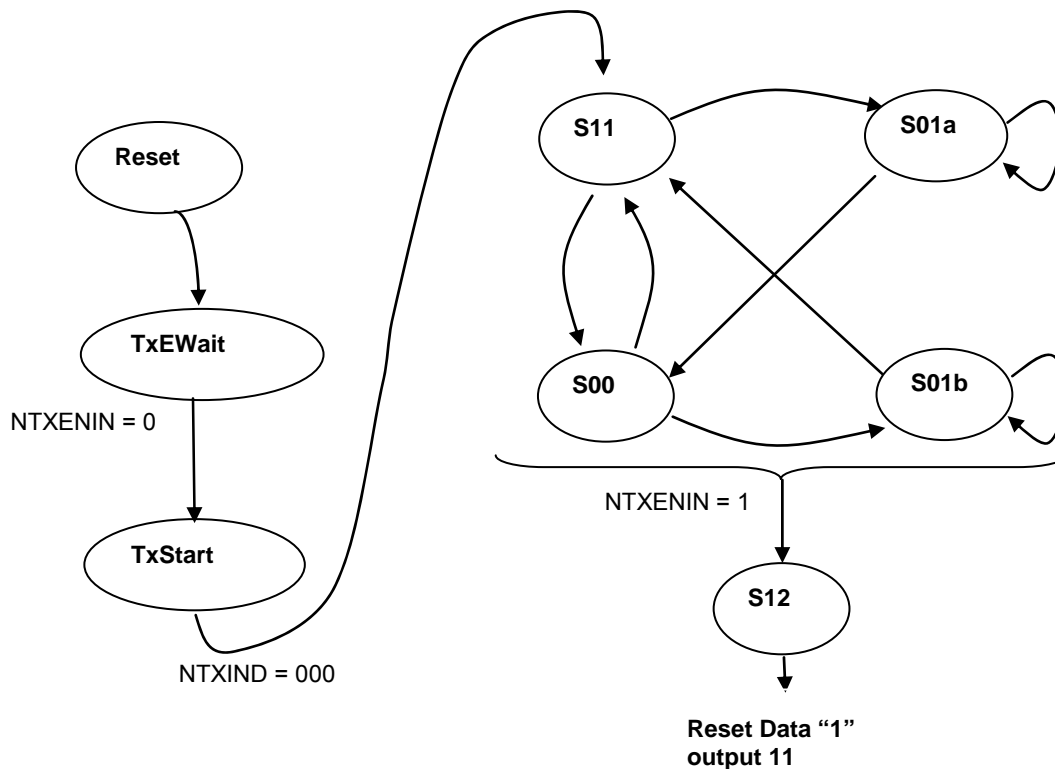
| | |
|----------|---|
| NTXIN | Input, Negative-Logic, ARCNET Controller PULSE1 output |
| NTXENIN | Input, Negative-Logic, ARCNET Controller TXEN output |
| NRXIN | Input, Negative-Logic, Line Receiver Reception output |
| CLK | Input, Start up detection, Same clock as ARCNET controller |
| NRESET | Input, Negative-Logic, Reset Signal |
| ENABLE | Input, Positive-Logic, clock division signal in synchronizer |
| NTXOUT | Output, Negative-Logic*, Input to Line Driver Data pin |
| NTXENOUT | Output, Negative-Logic, Input to Line Driver TxEnable pin |
| NRXOUT | Output, Negative-Logic, Input to the ARCNET Controller RXIN pin |

*: CMI Code in Appendix A is stated as Positive Logic (Active High).

A-4 CMITX Block

State Machine

| | |
|----------------|--|
| State_Reset: | Reset Status |
| State_TxEWait: | Wait for TxEnable |
| State_TxStart: | Wait for start of Data Output |
| State_S11: | Data "1" Output |
| State_S00: | Data "1" Output |
| State_S01a: | Data "0" Output |
| State_S01b: | Data "0" Output |
| State_S12: | 10 bit output with "0" ending after TxEnable termination |



Function Outline

- After Reset, stand by with TxEWait, enter TxStart by NTXENIN = 0 and start output of NTXENOUT = 0. Then, enter S11 by NTXIND = 000 and start output of data from CMI code symbol 11. (The ARCNET Message header is NTXIND = 00001111).
- When NTXENIN = 1 is detected, supplementary output of 10 bit "0" data (symbol 01) is carried out, and then terminated.

A-5 CMIRX Block

State Machine

State_Reset: Reset Status

State_Wait10: Detect line status 1 → 0

State_Wait01: Detect line status 0 → 1

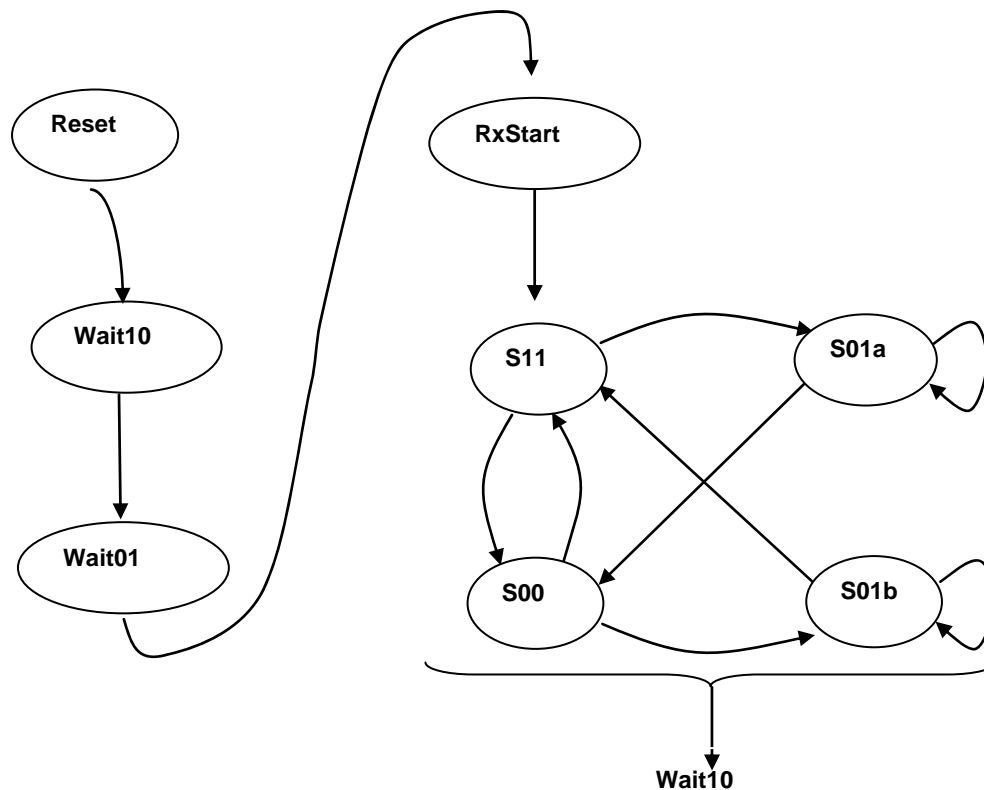
State_RxStart: Detect symbol 01100110, start Data reception

State_S11: Received Data “1” symbol 11

State_S00: Received Data “1” symbol 00

State_S01a: Received Data “0” symbol 01

State_S01b: Received Data “0” symbol 01



Function Outline

- After waiting for symbol transition 11→00 in Wait10, wait for symbol transition 00→11 in wait 01. Then finish without receiving instable action from the network after dataflow termination. Then in RxStart, start reception after detecting an Alert pattern from the message header.
- After receiving “0” data in S01 in 10 consecutive bits, then terminate reception and return to Wait 10.

A-6 Details Regarding Reception

Reception Data Analysis

Reception data is sampled one bit at a time by an 8 CLK analysis function, and is entered into the SHIFTD 32-bit Shift register. Normally, this is a data bit 1 process in Shift register bit 8. Because jitter is contained in the actual reception data, synchronization is achieved.

Starting Reception

Reception data is set in accordance with the ARCNET Controller: Various messages start with a bit “1” sequence (ALERT), and no data exists on the line prior to the first bit “1”. Because the output of the reception comparator in non-dataflow (Non-Driving period) within a message is unstable, those changes are warded off in Wait 10 and Wait 01. Afterwards, reception is started when the Alert starting pattern is detected. Because the first bit “1” in Alert Reception is set, the start symbol is 01100110 and 1 → 0 is the RxStart point.

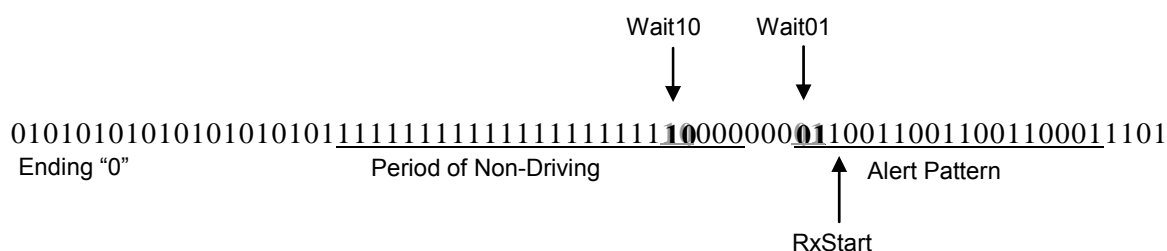


Figure 19 - Example of Unstable Comparator Output

Recovery

If the Symbol is 11 or 00, data is “1”, and if the Symbol is 01, data is “0”. This output is sequencer output, and reflects the sequencer state. Data length is set to a standard of 8 CLK, but this can be expanded or contracted by ± 2 CLK for synchronization purposes.

Error Correction

If symbols not occurring in the CMI transition diagram are received, they will be read as the nearest matching symbol. For example, if symbol 10 not present in the CMI is received, it is read as either symbol 11 or symbol 00, which will trigger an error. If Symbol 11 were received immediately before, it will be corrected to 00, because 11 cannot be repeated in the sequence. Conversely, if 00 is received immediately before, it is corrected to 11. However, if a repeated sequence of 11 is received immediately after receiving symbol 11, or if a repeated sequence of 00 is received immediately after symbol 00, it is corrected to 01.

Ending

In ACRNET, a “0” ending is attached in final bit 9 of message transmissions. The ARCNET “0” is non-dataflow 0 and has no function. However, in the CMI, this “0” is active data, flowed as “0” in symbol 01. Due to this, the “0” ending expected by the ARCNET controller is transmitted as CMI code. However, because the CMI code bit “0” is displayed in symbol 01, what follows the final bit “0” retains the same state and the symbol becomes “0111111....”. It is then read at the receiving end as bit “010*0*...” (0* is the result of misreading 11 as a 01). This is to say that the noise immediately after the bit 9 ending “0” becomes bit 1 reception. Since the ARCNET Controller is immediately after reception termination, this noise has no effect. There are two countermeasures available:

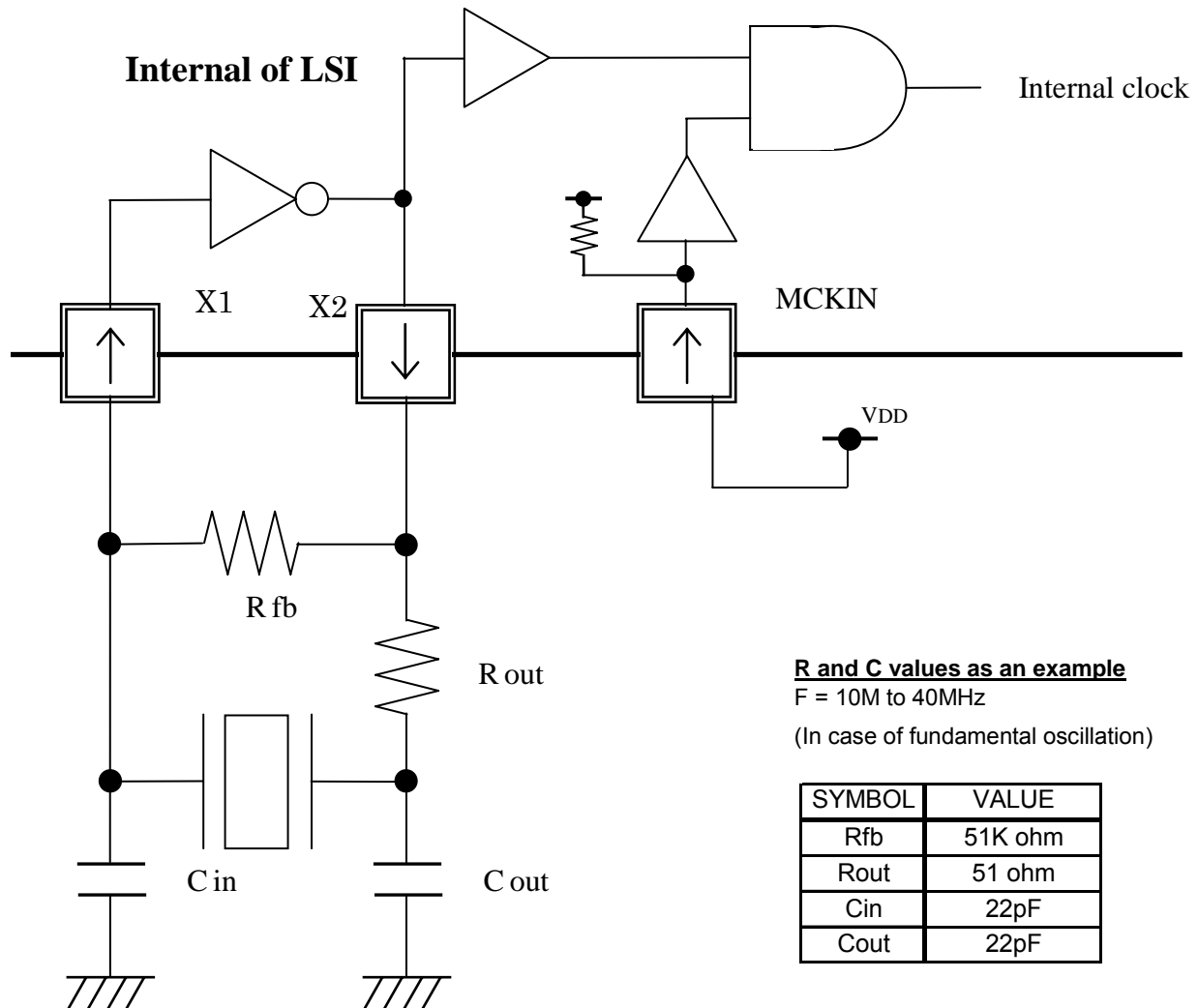
**Measure 1**

The transmitting end transmits "0" as a bit 10 ending. If the receiving end receives a 10-bit "0" sequence, it ends reception and enters an Alert pattern.

Measure 2

A restriction is set to read Symbol 01111111 not as bit "0100" but as "0000". This works by automatically transitioning to S11 subsequent symbols that are 0 when symbol 11 is detected in S01b state. However, if they remain as 1, they stay in the S01b and are read as bit "0". On the other hand, as a countermeasure against silent nodes like the ARCNET not actively data flowing symbol "01" during "0" ending, when reception data is fixed at either 0 or 1, they are not read as bit "1" but as bit "0". Due to this, measures are taken even if there is a node with temporary non-dataflow "0" ending output. Due to the highest consecutive value after a single symbol in the CMI being 3 symbols, fixed symbol 0 or 1 sequence is separated from normal CMI code and can be read as non-dataflow bit "0".

Appendix B Crystal Oscillator Circuit



NOTE: Above R, C values may not be correct for a crystal you select. You may have to determine the correct values. If you use an overtone type crystal, follow the manufacturer's recommendations for connection details.

Appendix C Diagram of Package External Measurement

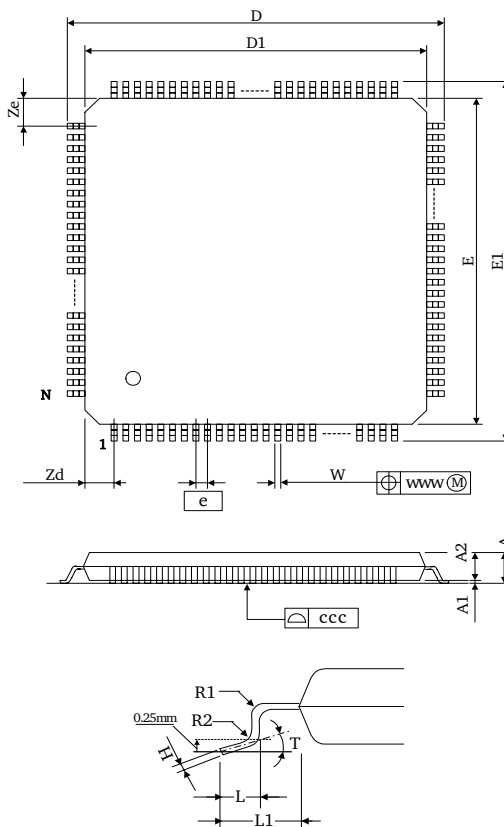


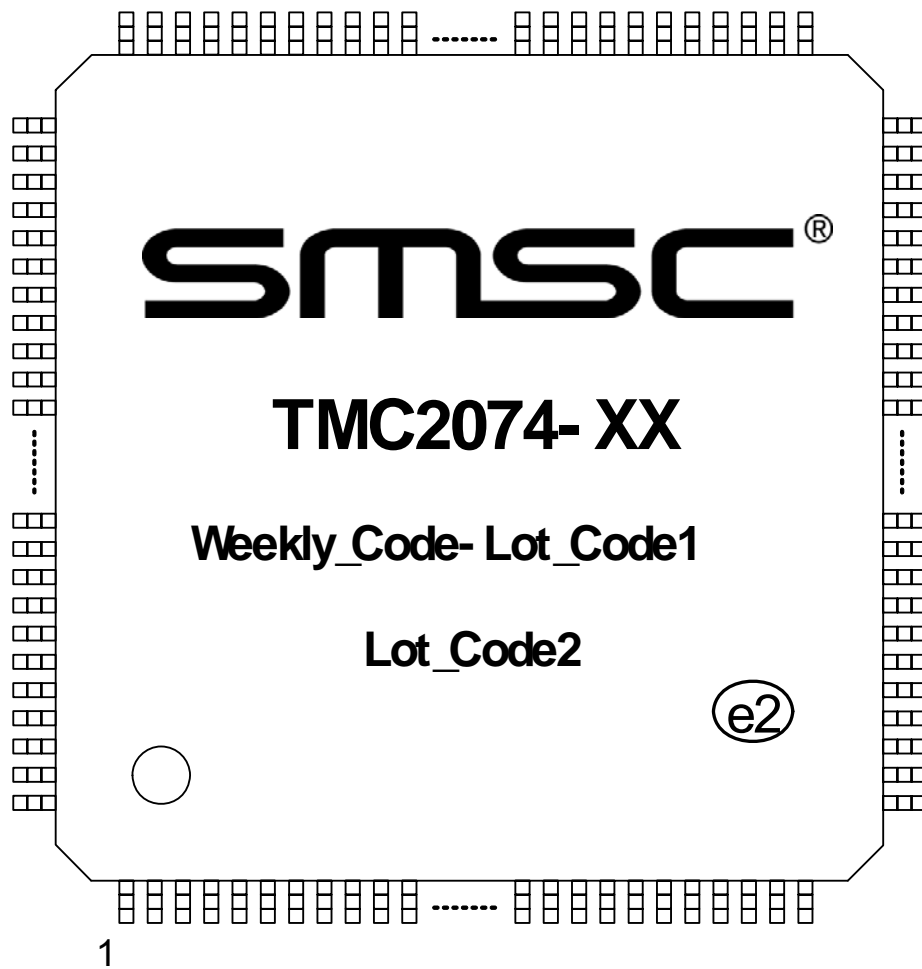
Figure 20 - TMC2074 128 Pin Package Outline
Table 8 - TMC2074 128 Pin Package Parameters

| SYMBOL | ITEMS | MIN | TYP | MAX |
|--------|-------------------------|-----------|------|-------|
| A | Overall Package Height | - | - | 1.2 |
| A1 | Standoff | 0.05 | - | 0.15 |
| A2 | Body Thickness | 0.95 | - | 1.05 |
| D | X Span | 15.8 | - | 16.2 |
| D1 | X body Size | 13.8 | - | 14.2 |
| E | Y Span | 15.8 | - | 16.2 |
| E1 | Y body Size | 13.8 | - | 14.2 |
| H | Lead Frame Thickness | 0.09 | - | 0.2 |
| L | Lead Foot Length | 0.45 | 0.6 | 0.75 |
| L1 | Lead Length | - | 1.0 | - |
| e | Lead Pitch | 0.4 Basic | | |
| T | Lead Foot Angle | 0° | - | 7° |
| W | Lead Width | 0.13 | 0.18 | 0.23 |
| www | Lead position Tolerance | -0.035 | - | 0.035 |
| R1 | Lead Shoulder Radius | 0.08 | - | - |
| R2 | Lead Foot Radius | 0.08 | - | 0.2 |
| ccc | Coplanarity | - | - | 0.08 |
| N | Pin count | 128 | | |

NOTES:

- 1) Controlling Unit: millimeter.
- 2) Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm.

Appendix D Marking Specifications



Appendix E Electrical Characteristics

Maximum Rated Values(V_{ss}=0V)

| ITEM | SYMBOL | VALUES | UNIT |
|-------------------------------|------------------|------------------------------|------|
| Power Supply Voltage | V _{dd} | -0.3 to +5.0 | V |
| Input Voltage (X1 pin) | V _{in} | -0.3 to V _{dd} +0.3 | V |
| Input Voltage (Except X1 pin) | | -0.3 to +7.0 | V |
| Output Voltage | V _{out} | -0.3 to V _{dd} +0.3 | V |
| Input Current | I _{in} | ±10 | mA |
| Storage Temperature | T _{stg} | -55 to +125 | °C |

Conditions of Standard Function (V_{ss}=0V)

| ITEM | SYMBOL | VALUE | UNIT |
|----------------------------------|------------------|--------------|------|
| Power Supply Voltage | V _{dd} | 3.0 to 3.6 | V |
| Operating Temperature | T _a | 0 to +70 | °C |
| Input Voltage (Except X1 pin) *1 | V _{in} | -0.3 to +5.5 | V |
| Input rising/falling time *2 | dt/dV | 0 to 5 | nS/V |
| Input Clock Frequency | f _{x1} | 10 to 40 | MHz |
| Input Clock Frequency Tolerance | df _{x1} | ±100 | ppm |

*1: Apply to 3-state output pins when hi-impedance(Hi-Z) state.

*2: Apply to nCS,nWR,nRD,ALE,nPISTR,RXIN,RXIN2,MCKIN pins.

DC Characteristics

| SYMBOL | ITEM | | CONDITION | MIN | TYP | MAX | UNIT |
|-------------------|--------------------------------------|-------------|--|----------------------|------|-----|------|
| V _{IH} * | High Level Input Voltage | | | 2.0 | | | V |
| V _{IL} * | Low Level Input Voltage | | | | | 0.8 | V |
| I _{IH} | High Level Input Current | | V _{in} = V _{dd} | -10 | | 10 | μA |
| I _{IL} | Low Level Input Current | | V _{in} = V _{ss} | -10 | | 10 | μA |
| | Pull-up Attached | | | -200 | | 10 | |
| I _{OZ} | Output Off Leak Current | | V _{out} = V _{dd} or V _{ss} | -10 | | 10 | μA |
| | Pull-up Attached | | | -200 | | 10 | |
| V _H | Schmitt Trigger Hysteresis Voltage | | | | 0.5 | | V |
| V _{OH} * | High Level Output Voltage | 4 mA Buffer | I _{OH} = -4mA | 2.4 | | | V |
| | | | I _{OH} = -1mA | V _{dd} -0.5 | | | |
| V _{OL} * | Low Level Output Voltage | 4 mA Buffer | I _{OL} = 4mA | | | 0.4 | V |
| | | | | | | | |
| I _{DD} | Operating Current (All outputs open) | | f _{X1} = 20MHz | | 25mA | | mA |
| | | | f _{X1} = 40MHz | | 40mA | | |

* Except X1 and X2 pins

AC Characteristics

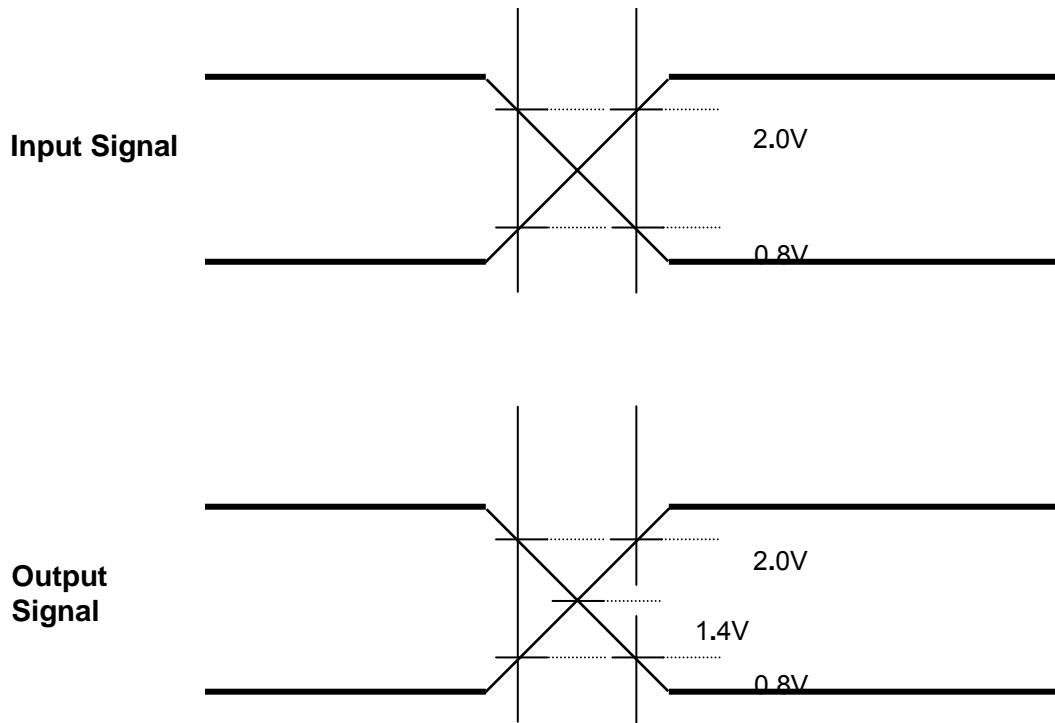


Figure 21 - Timing Measurement Points

NOTE: Detailed AC-Timing Specifications are provided in another document.

Appendix F Appendix F: CircLink Controller Product Comparative Table

| ITEMS | CircLink | | |
|--|---|--|--|
| | TMC2072 | TMC2074 | TMC2084 |
| * Common | | | |
| Power supply voltage | 3.3V +/-0.3V 5V tolerant I/O | 3.3V +/-0.3V 5V tolerant I/O | 3.3V +/-0.3V 5V tolerant I/O |
| Temperature range | 0 to +70C | 0 to +70C | 0 to +70C |
| Package | TQFP-100pin 14x14x1.4mm Body 0.5mm Pitch | VTQFP-128pin 14x14x1.0mm Body 0.4mm Pitch | TQFP-48pin 7x7x1.4mm Body 0.5mm Pitch |
| Max. Data Rate | 5Mbps | 5Mbps | 5Mbps |
| HUB function | External 2 ports | External 2 ports | none |
| Transmission code | CMI / RZ code | CMI / RZ code | CMI / RZ code |
| TXEN polarity setting | Pin setting | Pin setting | Active-High Only |
| NodeID, MaxID, PageSize setting | Pin / Bit setting | Pin / Bit setting | Shared Pins |
| Data Rate Prescaler setting | Pin / Bit setting | Pin / Bit setting | none |
| Page-Size | 32/64/128/256 bytes | 32/64/128/256 bytes | 64/128 bytes |
| Max. Node count | 31/15/ 7/ 3 nodes | 31/15/ 7/ 3 nodes | 15/ 7 nodes |
| Operation Mode | Peripheral mode Only | Peripheral/Standalone mode | Standalone mode Only |
| * Peripheral Mode (With CPU mode) | | | |
| Internal RAM size | 1K bytes | 1K bytes | - |
| Data Bus width | 8/16bit | 8/16bit | - |
| Support CPU | CPU Type: nRD&nWR/DIR&nDS Bus Type: MUX/Non-MUX | CPU Type: nRD&nWR/DIR&nDS Bus Type: MUX/Non-MUX | - |
| New Flag for Warning Timer | none | none | - |
| General Poupose-I/O | 8bit | 8bit | - |
| * Standalone Mode (CPU Less mode) | | | |
| Number of I/O Port | - | IN : 16 OUT : 16 | IN : 0/ 8/16 OUT : 32/24/16 |
| Verious Setting by | - | Pins | Shared Pins and a Packet |
| Tx Trigger | - | 7 kinds | 10 kinds |
| Receive Broadcast | - | No | Yes |
| Send Status | - | No | Yes |
| Anti-Chatter Sampling Freq. | - | 2.44KHz | 1.22KHz/19.1Hz |



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