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FAIRCHILD SEMICONDUCTOR®

October 2008

# FDS4897AC

## Dual N & P-Channel PowerTrench® MOSFET

**N-Channel: 40 V, 6.1 A, 26 mΩ  P-Channel: -40 V, -5.2 A, 39 mΩ**

### Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 26 mΩ at $V_{GS}$ = 10 V, $I_D$ = 6.1 A
- Max $r_{DS(on)}$ = 31 mΩ at $V_{GS}$ = 4.5 V, $I_D$ = 5.6 A

Q2: P-Channel

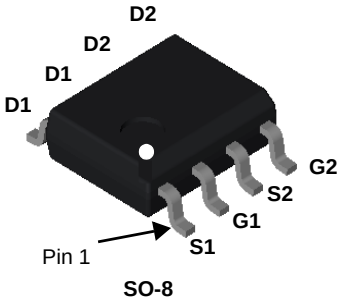
- Max $r_{DS(on)}$ = 39 mΩ at $V_{GS}$ = -10 V, $I_D$ = -5.2 A
- Max $r_{DS(on)}$ = 65 mΩ at $V_{GS}$ = -4.5 V, $I_D$ = -4.1 A
- 100% UIL Tested
- RoHS Compliant

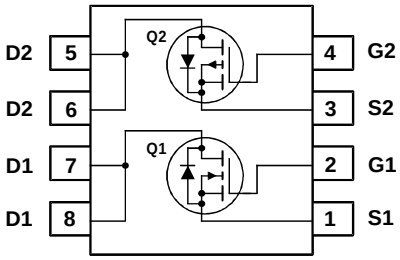
### General Description

These dual N- and P-Channel MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

### Applications

- Inverter
- Power Supplies




## MOSFET Maximum Ratings $T_A$ = 25 °C unless otherwise noted

| Symbol | Parameter | | Q1 | Q2 | Units |
|---|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | 40 | -40 | V |
| $V_{GS}$ | Gate to Source Voltage | | ±20 | ±20 | V |
| $I_D$ | Drain Current - Continuous | | 6.1 | -5.2 | A |
| | - Pulsed | | 24 | -24 | |
| $P_D$ | Power Dissipation for Dual Operation | | 2.0 | | W |
| | Power Dissipation for Single Operation | $T_A$ = 25 °C (Note 1a) | 1.6 | | |
| | | $T_A$ = 25 °C (Note 1b) | 0.9 | | |
| $E_{AS}$ | Single Pulse Avalanche Energy | (Note 3) | 37 | 73 | mJ |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | -55 to +150 | | °C |

### Thermal Characteristics

| | | | |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case, (Note 1) | 40 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction to Ambient, (Note 1a) | 78 | |

### Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| FDS4897AC | FDS4897AC | SO-8 | 13 ” | 12 mm | 2500 units |

## Electrical Characteristics $T_J$ = 25 °C unless otherwise noted

| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V<br>$I_D$ = -250 μA, $V_{GS}$ = 0 V | Q1<br>Q2 | 40<br>-40 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C<br>$I_D$ = -250 μA, referenced to 25 °C | Q1<br>Q2 | | 37<br>-32 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 32 V, $V_{GS}$ = 0 V<br>$V_{DS}$ = -32 V, $V_{GS}$ = 0 V | Q1<br>Q2 | | | 1<br>-1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | Q1<br>Q2 | | | ±100<br>±100 | nA<br>nA |
| **On Characteristics** | | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA<br>$V_{GS}$ = $V_{DS}$, $I_D$ = -250 μA | Q1<br>Q2 | 1.5<br>-1.5 | 2.0<br>-2.0 | 3.0<br>-3.0 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C<br>$I_D$ = -250 μA, referenced to 25 °C | Q1<br>Q2 | | -6<br>6 | | mV/°C |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 6.1 A<br>$V_{GS}$ = 4.5 V, $I_D$ = 5.6 A<br>$V_{GS}$ = 10 V, $I_D$ = 6.1 A, $T_J$ = 125 °C | Q1 | | 20<br>24<br>30 | 26<br>31<br>39 | mΩ |
| | | $V_{GS}$ = -10 V, $I_D$ = -5.2 A<br>$V_{GS}$ = -4.5 V, $I_D$ = -4.1 A<br>$V_{GS}$ = -10 V, $I_D$ = -5.2 A, $T_J$ = 125 °C | Q2 | | 28<br>45<br>41 | 39<br>65<br>57 | |
| $g_{FS}$ | Forward Transconductance | $V_{DD}$ = 5 V, $I_D$ = 6.1 A<br>$V_{DD}$ = -5 V, $I_D$ = -5.2 A | Q1<br>Q2 | | 24<br>14 | | S |
| **Dynamic Characteristics** | | | | | | | |
| $C_{iss}$ | Input Capacitance | Q1<br>$V_{DS}$ = 20 V, $V_{GS}$ = 0 V, f = 1 MHZ | Q1<br>Q2 | | 795<br>765 | 1055<br>1015 | pF |
| $C_{oss}$ | Output Capacitance | Q2<br>$V_{DS}$ = -20 V, $V_{GS}$ = 0 V, f = 1 MHZ | Q1<br>Q2 | | 95<br>135 | 130<br>180 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | Q1<br>Q2 | | 65<br>80 | 100<br>120 | pF |
| $R_g$ | Gate Resistance | | Q1<br>Q2 | | 1.7<br>3.6 | | Ω |
| **Switching Characteristics** | | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | Q1<br>$V_{DD}$ = 20 V, $I_D$ = 6.1 A,<br>$V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | Q1<br>Q2 | | 6<br>8 | 12<br>15 | ns |
| $t_r$ | Rise Time | | Q1<br>Q2 | | 2<br>3 | 10<br>10 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | Q2<br>$V_{DD}$ = -20 V, $I_D$ = -5.2 A,<br>$V_{GS}$ = -10 V, $R_{GEN}$ = 6 Ω | Q1<br>Q2 | | 17<br>17 | 30<br>30 | ns |
| $t_f$ | Fall Time | | Q1<br>Q2 | | 2<br>3 | 10<br>10 | ns |
| $Q_{g(TOT)}$ | Total Gate Charge | Q1<br>$V_{GS}$ = 10 V, $V_{DD}$ = 20 V, $I_D$ = 6.1 A | Q1<br>Q2 | | 15<br>15 | 21<br>20 | nC |
| $Q_{gs}$ | Gate to Source Charge | | Q1<br>Q2 | | 2.5<br>2.6 | | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | Q2<br>$V_{GS}$ = -10 V, $V_{DD}$ = -20 V, $I_D$ = -5.2 A | Q1<br>Q2 | | 2.9<br>3.2 | | nC |

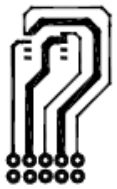
## Electrical Characteristics $T_J$ = 25 °C unless otherwise noted

| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **Drain-Source Diode Characteristics** | | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 1.3 A (Note 2)<br>$V_{GS}$ = 0 V, $I_S$ = -1.3 A (Note 2) | Q1<br>Q2 | | 0.75<br>-0.76 | 1.2<br>-1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | Q1<br>$I_F$ = 6.1 A, di/dt = 100 A/s | Q1<br>Q2 | | 17<br>20 | 31<br>36 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | Q2<br>$I_F$ = -5.2 A, di/dt = 100 A/s | Q1<br>Q2 | | 7<br>10 | 15<br>20 | nC |

**Notes:**

**1:** $R_{\theta JA}$ is determined with the device mounted on a 1in$^2$ pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 78 °C/W when mounted on a 1 in$^2$ pad of 2 oz copper



b) 135 °C/W when mounted on a minimun pad

**2:** Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

**3:** Starting $T_J$ = 25 °C, N-ch: L = 3 mH, $I_{AS}$ = 5 A, $V_{DD}$ = 40 V, $V_{GS}$ = 10 V; P-ch: L = 3 mH, $I_{AS}$ = -7 A, $V_{DD}$ = -40 V, $V_{GS}$ = -10 V.

## Typical Characteristics (Q1 N-Channel) $T_J$ = 25 °C unless otherwise noted

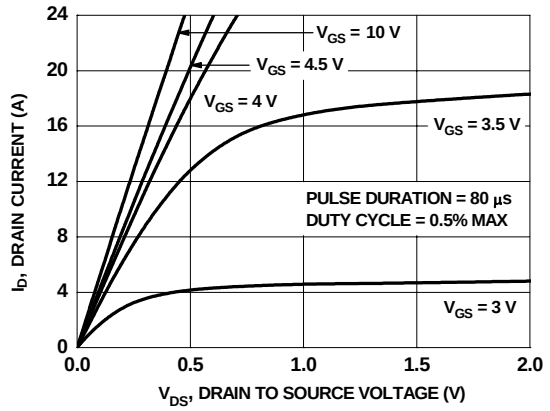



**Figure 1. On Region Characteristics**

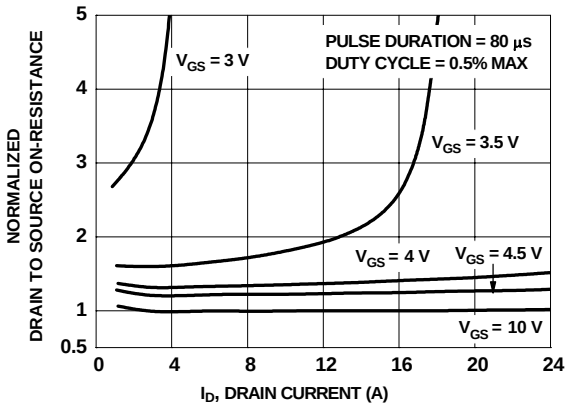



**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**

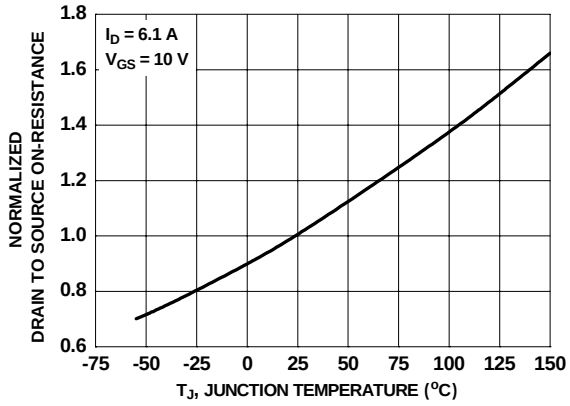



**Figure 3. Normalized On Resistance vs Junction Temperature**

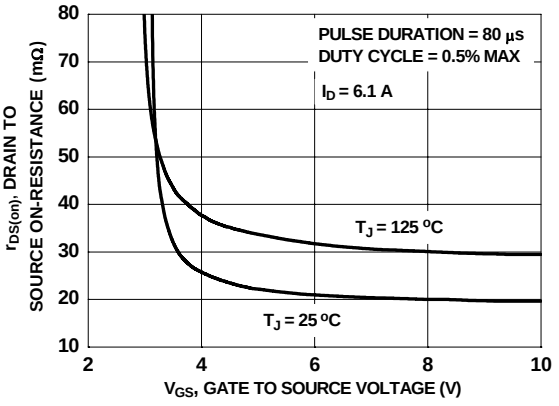



**Figure 4. On-Resistance vs Gate to Source Voltage**

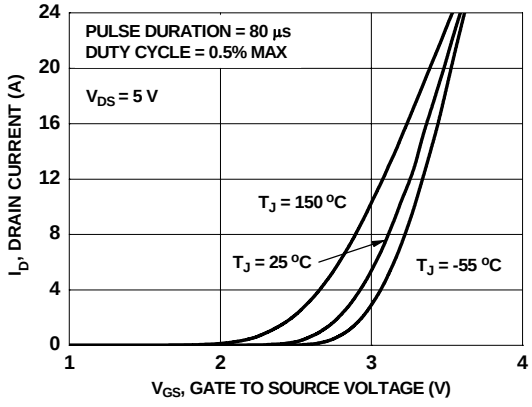



**Figure 5. Transfer Characteristics**

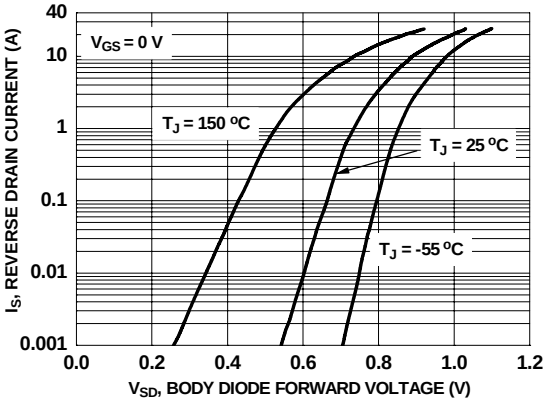



**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

## Typical Characteristics (Q1 N-Channel) $T_J$ = 25 °C unless otherwise noted

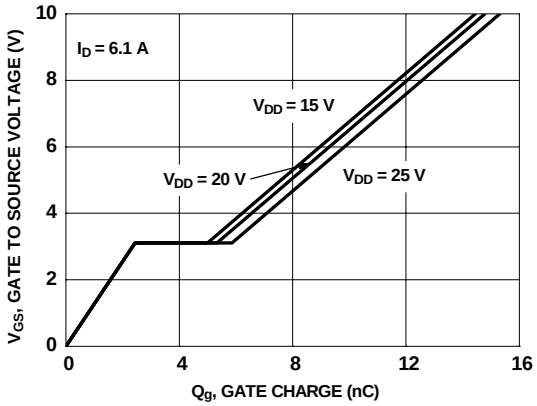



**Figure 7. Gate Charge Characteristics**

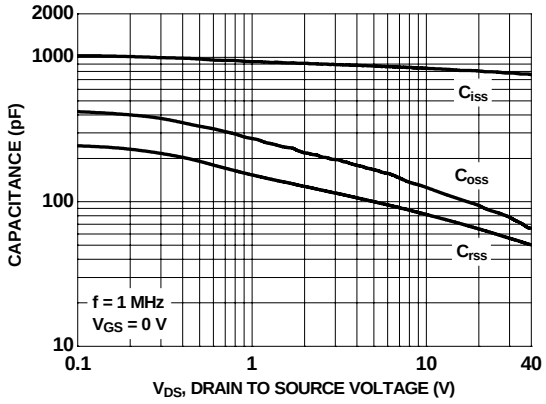



**Figure 8. Capacitance vs Drain to Source Voltage**

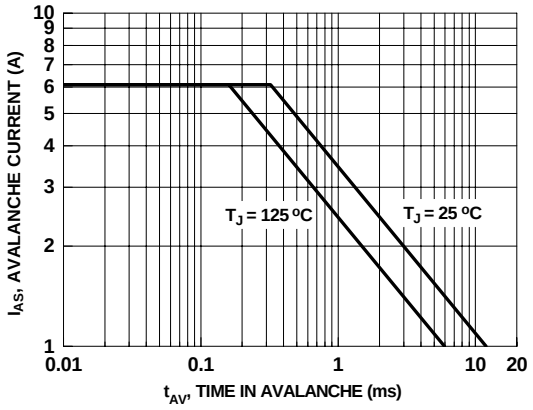



**Figure 9. Unclamped Inductive Switching Capability**

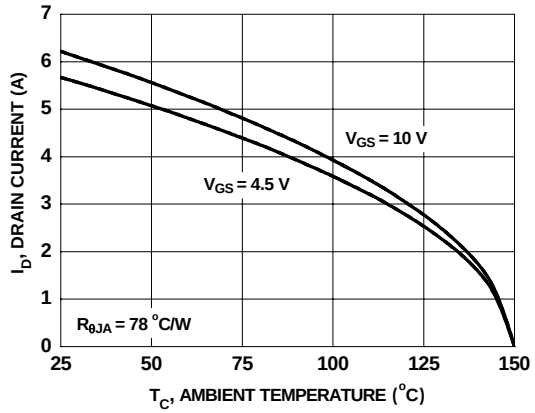



**Figure 10. Maximum Continuous Drain Current vs Ambient Temperature**

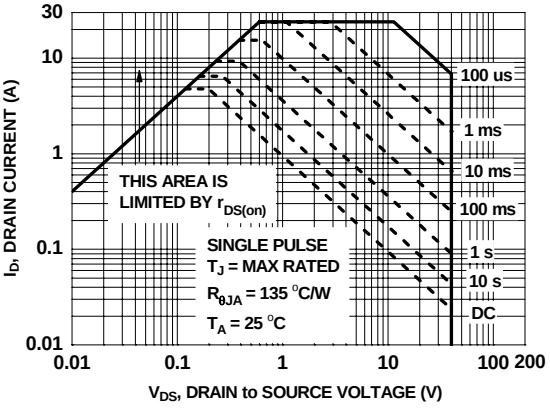



**Figure 11. Forward Bias Safe Operating Area**

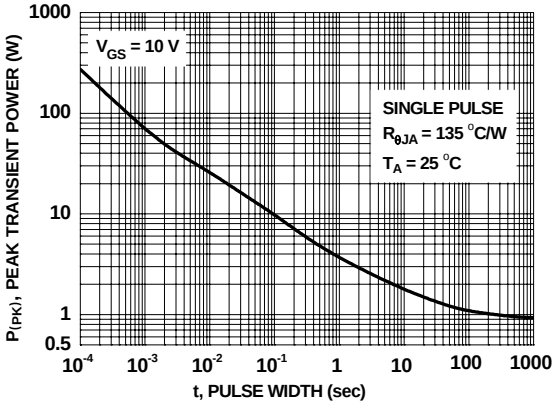



**Figure 12. Single Pulse Maximum Power Dissipation**

## Typical Characteristics (Q1 N-Channel) $T_J$ = 25 °C unless otherwise noted

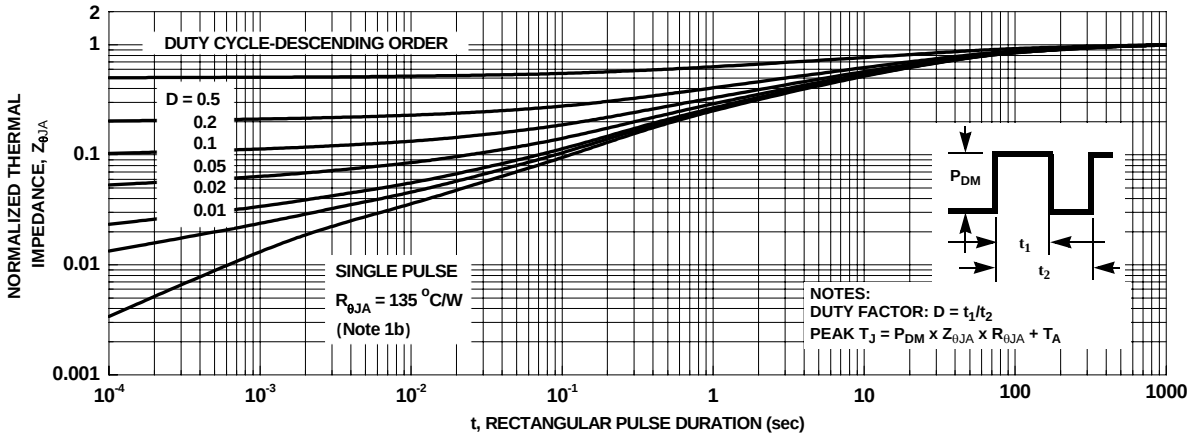



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

## Typical Characteristics (Q2 P-Channel) $T_J$ = 25 °C unless otherwise noted

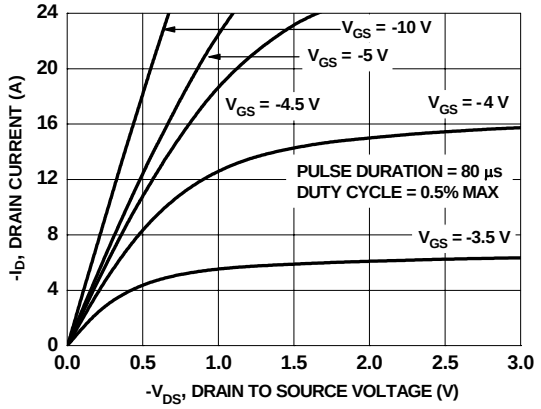



**Figure 15. On- Region Characteristics**

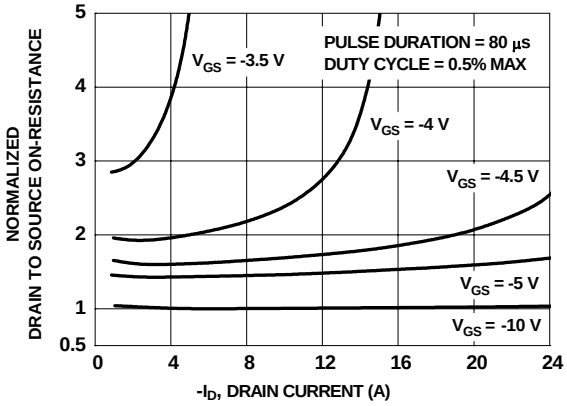



**Figure 16. Normalized on-Resistance vs Drain Current and Gate Voltage**

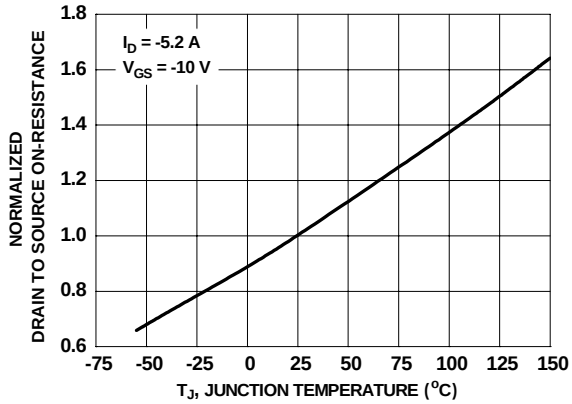



**Figure 17. Normalized On-Resistance vs Junction Temperature**

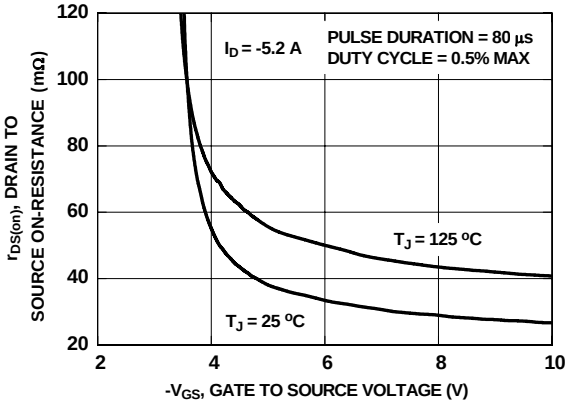



**Figure 18. On-Resistance vs Gate to Source Voltage**

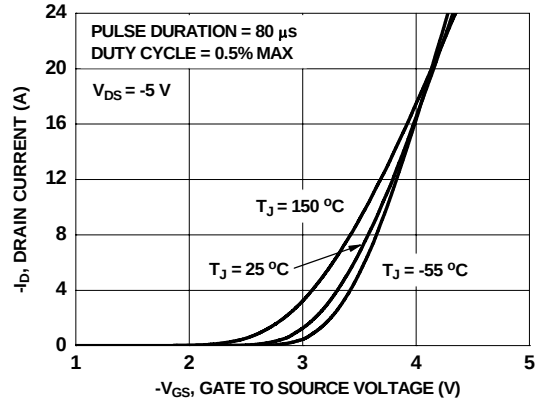



**Figure 19. Transfer Characteristics**

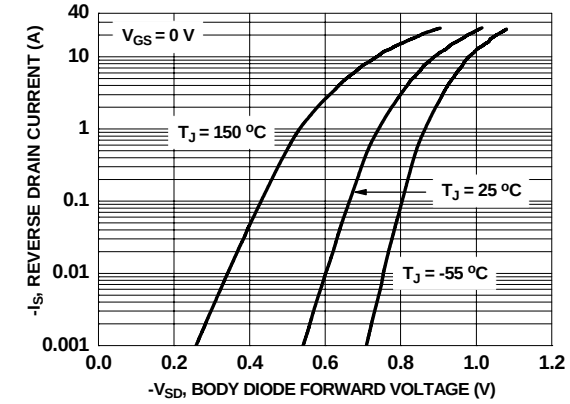



**Figure 20. Source to Drain Diode Forward Voltage vs Source Current**

## Typical Characteristics (Q2 P-Channel) $T_J$ = 25 °C unless otherwise noted

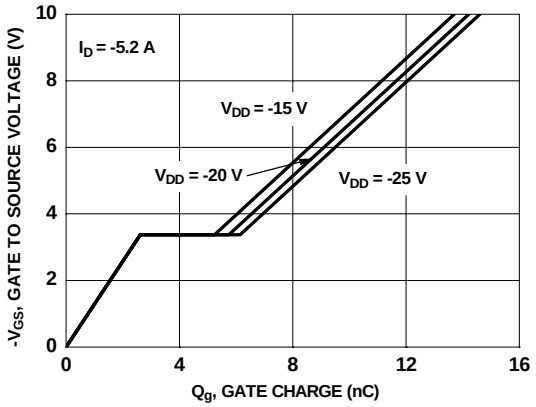



**Figure 21. Gate Charge Characteristics**

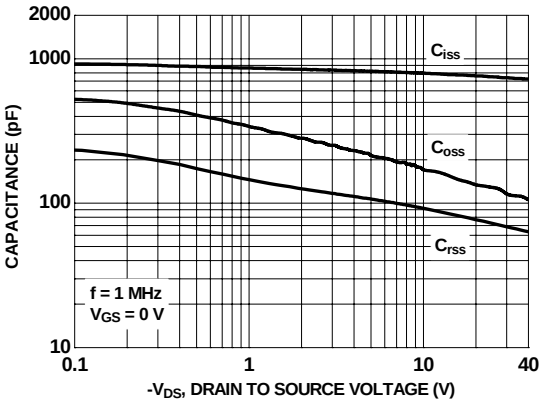



**Figure 22. Capacitance vs Drain to Source Voltage**

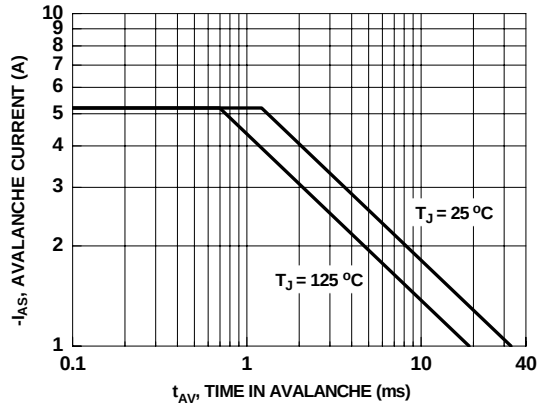



**Figure 23. Unclamped Inductive Switching Capability**

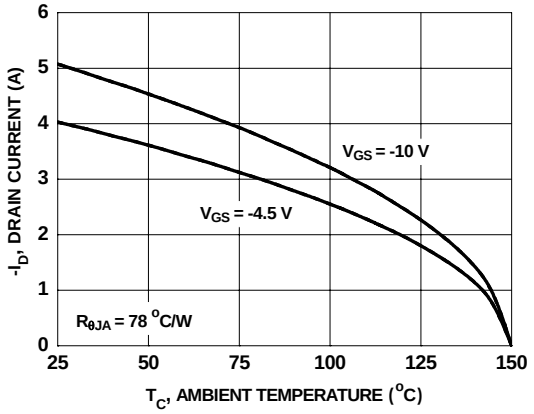



**Figure 24. Maximum Continuous Drain Current vs Ambient Temperature**

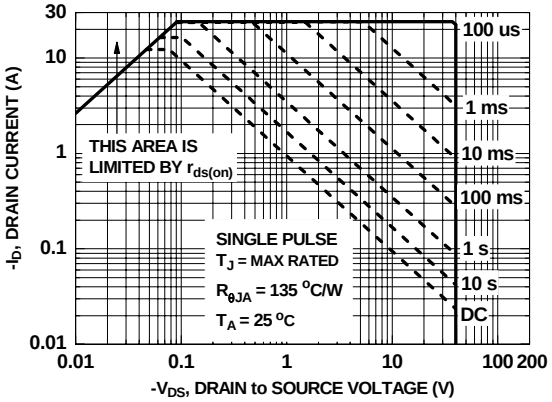



**Figure 25. Forward Bias Safe Operating Area**

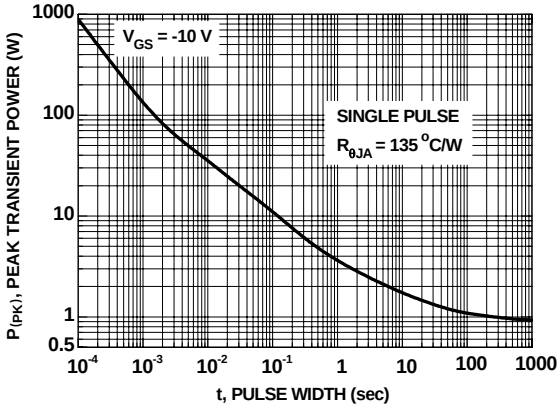



**Figure 26. Single Pulse Maximum Power Dissipation**

## Typical Characteristics (Q2 P-Channel) $T_J$ = 25 °C unless otherwise noted

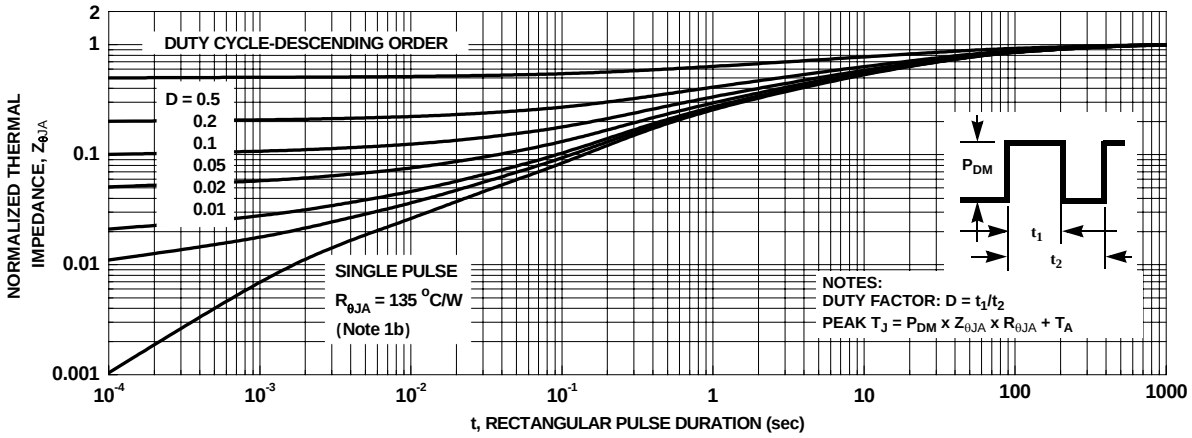



**Figure 27. Junction-to-Ambient Transient Thermal Response Curve**

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**ANTI-COUNTERFEITING POLICY**

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Farichild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufactures of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed application, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Farichild strongly encourages customers to purchase Farichild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handing and storage and provide access to Farichild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address and warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Farichild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

| Datasheet Identification | Product Status | Definition |
|---|---|---|
| Advance Information | Formative / In Design | Datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
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