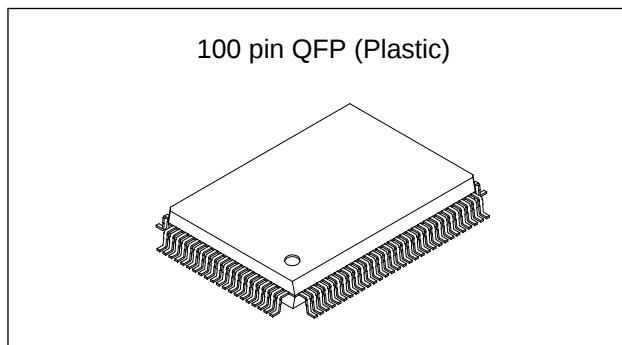


CMOS 8-bit Single Chip Microcomputer

Description

The CXP88132/88140 is a CMOS 8-bit microcomputer which consists of A/D converter, serial interface, timer/counter, time base timer, vector interruption, high precision timing pattern generation circuits, PWM generator, PWM for tuner, VISS/VASS circuit, 32kHz timer/event counter, remote control receiving circuit, FDP controller/driver, VCR vertical sync separation circuit and the measuring circuit which measure signals of capstan FG and drum FG/PG and other servo systems, as well as basic configurations like 8-bit CPU, ROM, RAM and I/O port. They are integrated into a single chip.

Also, CXP88132/88140 provides sleep/ stop function which enables to lower power consumption and ultra-low speed instruction mode in 32kHz operation.



Structure

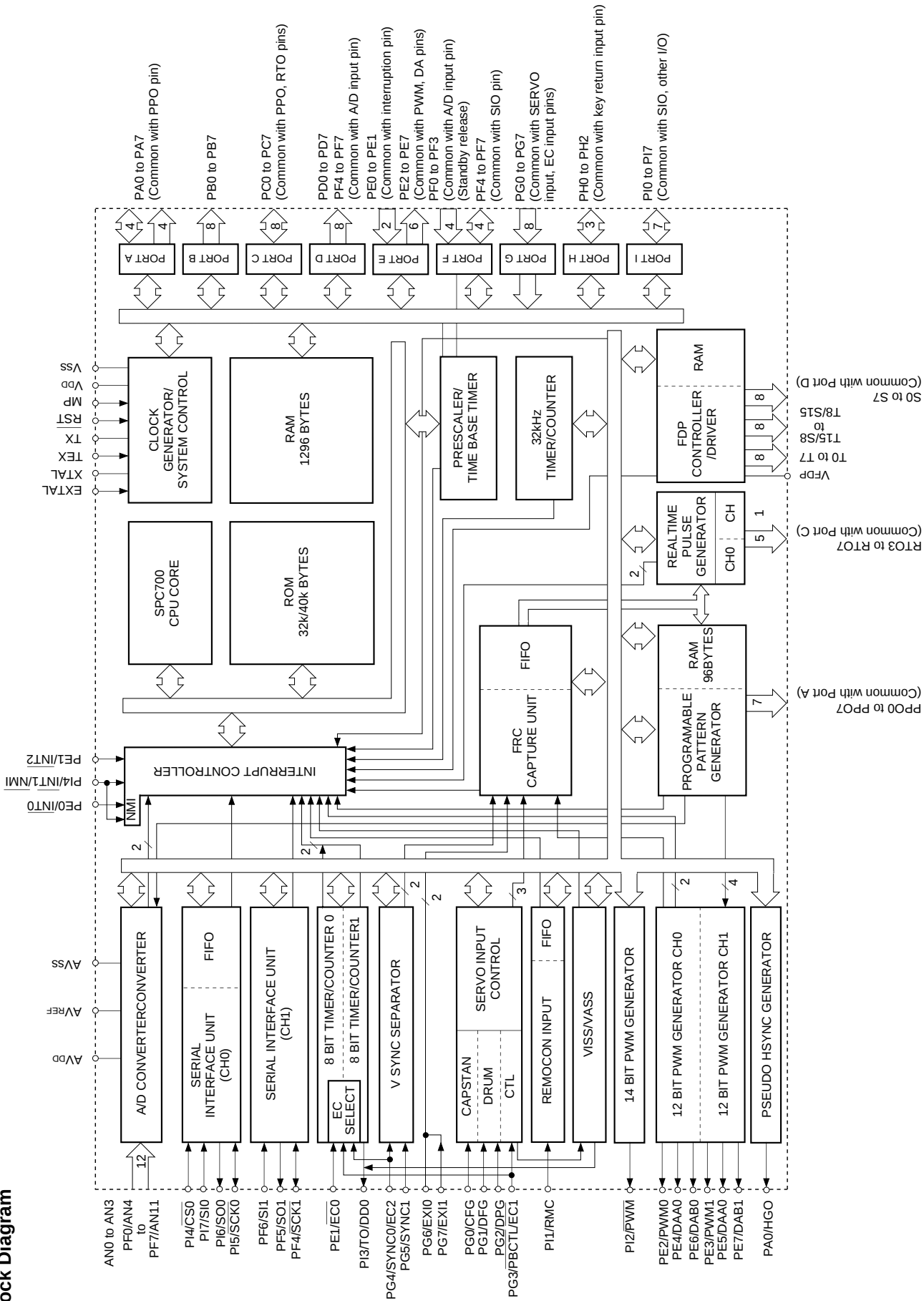
Silicon gate CMOS IC

Features

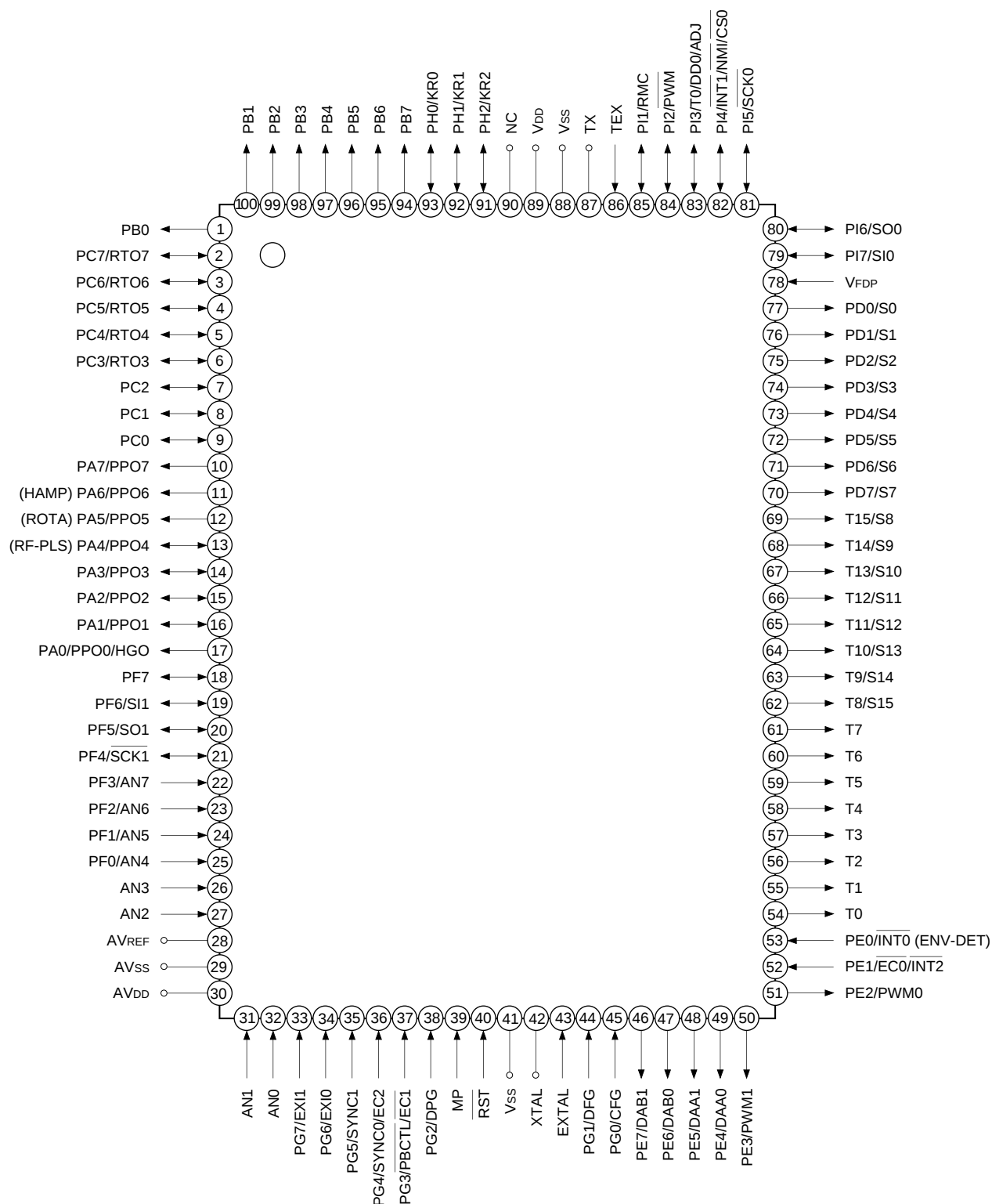
- A wide instruction set (213 instructions) which cover various types of data
 - 16-bit arithmetic instruction/multiplication and division instructions/boolean bit operation instruction
- Minimum instruction cycle During operation 250ns/16MHz, During operation 122μs/32kHz
- Incorporated ROM capacity 32Kbytes (CXP88132), 40Kbytes (CXP88140)
- Incorporated RAM capacity 1296bytes
- Peripheral function
 - A/D converter 8-bit, 8-channel, successive approximation system (Conversion time: 20.0μs/16MHz)
 - Serial I/O with auto transfer mode Incorporated 8-stage FIFO for data (1 to 8 bytes auto transfer)
 - Timer 8-bit timer/counter, 2-channel, 19-bit time base timer
 - High precision timing pattern generation PPG 8 pins 32-stage programmable circuit RTG 5 pins 2-channel
 - PWM/DA gate output 12-bit, 2-channel (Repetitive frequency 62.5kHz/16MHz)
 - Servo input control Capstan FG, Drum FG/PG, CTL input
 - VSYNC separator Incorporated 26-bit and 8-stage FIFO
 - FRC capture unit 14-bit
 - PWM output for tuner Pulse duty auto detection circuit
 - VISS/VASS circuit 32kHz oscillation circuit, ultra-low speed instruction mode
 - 32kHz timer/event counter 8-bit pulse measuring counter, 6-stage FIFO
 - Remote control receiving circuit Max.148 segments can be displayed
 - FDP controller/driver Hardware key scanning function (Max.16 × 3 key matrix available)
 - Tri-state output PPG 1 pin, RTG 1 pin, output 8 pins
 - Pseudo HSYNC output function
 - High speed head switching circuit
- Interruption 22 factors, 15 vectors, multi-interruption possible
- Standby mode SLEEP/STOP
- Package 100-pin plastic QFP
- Piggyback/evaluation chip CXP88100

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Block Diagram



Pin Configuration (Top View)



- Note)**
1. NC (Pin 90) is always connected to V_{DD}.
 2. Vss (Pins 41 and 88) are both connected to GND.

Pin Description

Symbol	I/O	Description		
PA0/PPO0/ HGO	Output/Real time output/output	(Port A) 8-bit I/O port. Enable to specify I/O by bit unit. Data is gated with RTO content by OR-gate and they are output. (8 pins)	Pseudo HSYNC output pin.	Real-time pulse generator (RTG) output. Functions as high precision real-time pulse output port. (5 pins) Head switching output pins.
PA1/PPO1	I/O/ Real time output			
PA2/PPO2				
PA3/PPO3				
PA4/PPO4	Output/ Real time output			
PA5/PPO5				
PA6/PPO6				
PA7/PPO7				
PB0 to PB7	Output	8-bit output port. Tri-state can be controlled. (8 pins)		
PC0/PPO8 to PC7/PPO15	Output/ Real time output	(Port C) 8-bit I/O port. Enable to specify I/O by bit unit. Data is gated with RTO content by OR-gate and they are output. (8 pins)	Real-time pulse generator (RTG) output. Functions as high precision real-time pulse output port. (5 pins)	
T0 to T7	Output	FDP timing signal output pin.		
T8/S15 to T15/S8	Output/Output	Output pins for FDP timing signal and segment signal.		
PD0 to PD7	Output	(Port D) 8-bit output port. (8 pins)	FDP segment signal output pin.	
PE0/ $\overline{\text{INT0}}$	Input/Input	(Port E) 8-bit port. Lower 2 bits are input pins and upper 6 bits are output pins. (8 pins)	Trigger pulse input pin for head switching output.	Input pin to request external interruption. Active when falling edge.
PE1/ $\overline{\text{EC0}}$ / INT2	Input/Input/Input		External event input pin for timer/counter.	Input pin to request external interruption. Active when falling edge.
PE2/PWM0	Output/Output		PWM output pins. (2 pins)	
PE3/PWM1	Output/Output			
PE4/DAA0	Output/Output			
PE5/DAA1	Output/Output			
PE6/DAB0	Output/Output		DA gate pulse output pins. (2 pins)	
PE7/DAB1	Output/Output			
AN0 to AN3	Input	Analog input pins to A/D converter. (8 pins)		
PF0/AN0 to PF3/AN3	Input/Input	(Port F) 8-bit I/O port. Enable to specify I/O by bit unit. (8 pins)		
PF4/SCK1	I/O/I/O		Serial clock (CH1) I/O pin.	
PF5/SO1	I/O/Output		Serial data (CH1) output pin.	
PF6/SI1	I/O/Input		Serial data (CH1) input pin.	
PF7	I/O			

Symbol	I/O	Description	
PG0/CFG	Input/Input	(Port G) 8-bit input port. (8 pins)	Capstan FG input pin.
PG1/DFG	Input/Input		Drum FG input pin.
PG2/DPG	Input/Input		Drum PG input pin.
PG3/ PBCTL/EC1	Input/Input/Input		Playback CTL input pin. External event input pin for timer/counter.
PG4/ SYNC0/EC2	Input/Input/Input		Composite sync signal input pin. External event input pin for timer/counter.
PG5/SYNC1	Input/Input		
PG6/EXI0	Input/Input		External input pin for FRC capture unit.
PG7/EXI1	Input/Input		
PH0/KR0 to PH7/KR2	I/O/Input	(Port H) 3-bit I/O port. (3 pins)	Key return input signal for key scanning at FDP segment signal.
PI1/RMC	I/O/Input	(Port I) 8-bit I/O port. Enable to specify I/O by bit unit. (8 pins)	Remote control receiving circuit input pin.
PI2/PWM	I/O/Input		14-bit PWM output pin.
PI3/TO/ DDO/ADJ	I/O/Input		Timer/counter, CTL duty detection, 32kHz oscillation adjustment output pin.
PI4/INT1/ NMI/CS0	I/O/Input/ Input/Input		Input pin to request external interruption, non-maskable interruption and for serial chip select (CH0). Active when falling edge.
PI5/SCK0	I/O/Input		Serial clock (CH1) I/O pin.
PI6/SO0	I/O/Output		Serial data (CH1) output pin.
PI7/SI0	I/O/Input		Serial data (CH1) input pin.
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.	
XTAL	Output		
TEX	Input	Connecting pin of crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open. (Feedback resistor is not removed.)	
TX	Output		
RST	Input	System reset pin of active "L" level.	
MP	Input	Microprocessor mode input pin. Always connect to GND.	
V _{FDP}		FPD voltage supply pin when specifying internal resistor by mask option.	
AV _{DD}		Positive power supply pin of A/D converter.	
AV _{REF}	Input	Reference voltage input pin of A/D converter.	
AV _{SS}		GND pin of A/D converter.	
V _{DD}		Positive power supply pin.	
V _{SS}		GND pin. Connect both V _{SS} pins to GND.	

Pin	Circuit format	When reset
PA0/PPO0/ HGO 1 pin		Hi-Z
PA1/PPO1 1 pin		Hi-Z
PA2/PPO2 to PA4/PPO4 3 pins		Hi-Z
PA5/PPO5 to PA7/PPO7 3 pins		Hi-Z

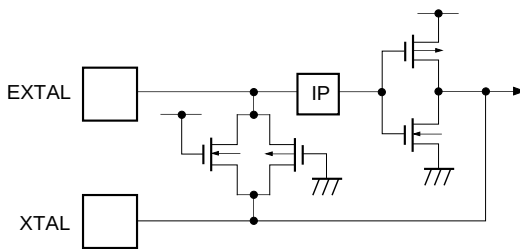
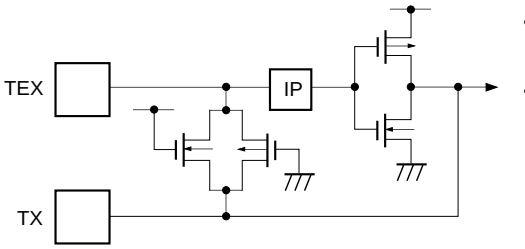
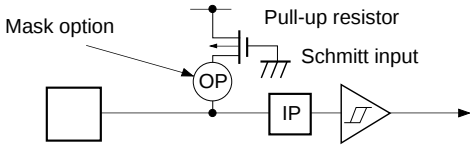
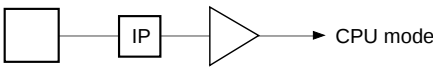
- 7 -

Pin	Circuit format	When reset
PC5/RTO5 to PC7/RTO7 3 pins	Port C RTO data Port C data Port C direction (Every bit) Data bus RD (Port C) Input protection circuit IP	Hi-Z
PD0/S0 to PD7/S7 8 pins	Port D Segment output data Output selection control signal ("0" when reset) Port D data Data bus RD (Port D) High voltage drive transistor Mask option OP Pull-down resistor V_{FDP}	Hi-Z
T0 to T7 8 pins	Timing output data Output selection control signal ("0" when reset) High voltage drive transistor Mask option OP Pull-down resistor V_{FDP}	Hi-Z
T8/S15 to T15/S8 8 pins	Timing output data Output selection control signal ("0" when reset) Segment output data High voltage drive transistor Mask option OP Pull-down resistor V_{FDP}	Hi-Z

Pin	Circuit format	When reset
PE0/ $\overline{\text{INT0}}$ PE1/ $\overline{\text{EC0/INT2}}$ 2 pins	Port E	Hi-Z
PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1 4 pins	Port E	Hi-Z
PE6/DAB0 PE7/DAB1 2 pins	Port E	High level
PF0/AN4 to PF3/AN7 4 pins	Port F	Hi-Z
PF4/ $\overline{\text{SCK1}}$ 2 pins	Port F	Hi-Z

Pin	Circuit format	When reset
PF5/SO1 1 pin	Port F	Hi-Z
PF6/SI1 1 pin	Port F	Hi-Z
PF7 1 pin	Port F	Hi-Z
PG0/CFG PG1/DFG PG2/DPG PG3/PBCTL/ EC1 PG4/SYNC0/ EC2 PG5/SYNC1 PG6/EXI0 PG7/EXI1 8 pins	Port G Note) For PG4/SYNC and PG5/SYNC1, CMOS schmitt input or TTL schmitt input can be selected with the mask option.	Hi-Z

Pin	Circuit format	When reset
PI2/PWM PI3/TO/ DDO/ADJ 2 pins	Port I Port I function select (PI2: From 14-bit PWM, timer/counter PI3: From CTL duty detection circuit, 32kHz timer) Port I data Port I direction Data bus RD (Port I) MPX IP	Hi-Z
PI1/RMC PI4/INT1/ NMI/CS0 PI7/SI0 1 pin	Port I Port I data Port I direction Data bus RD (Port I) MPX IP (PI1: To remote control circuit PI4: To interruption circuit PI3: To serial CH0)	Hi-Z
PI5/SCK0 PI6/SO0 2 pins	Port I Port I function select From serial CH0 Port I data Port I direction Data bus RD (Port I) MPX MPX To SI0 Schmitt input Note) P15 is schmitt input IP	Hi-Z
PH0/KR0 to PH2/KR2 3 pins	Port H Port H data Port H direction Data bus RD (Port H) MPX IP Key input signal	Hi-Z

Pin	Circuit format	When reset
EXTAL XTAL 2 pins	 • Shows the circuit composition during oscillation. • Feedback resistor is removed during stop.	Hi-Z
TEX TX 2 pins	 • Shows the circuit composition during oscillation. • Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time TEX pin outputs "L" level and TX pin outputs "H" level.	Oscillation
$\overline{\text{RST}}$ 1 pin	 Mask option Pull-up resistor Schmitt input	Low level
MP 1 pin	 CPU mode	Hi-Z

Absolute Maximum Ratings

(V_{SS} = 0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	−0.3 to +7.0	V	
	AV _{DD}	AV _{SS} to +7.0* ¹	V	
	AV _{SS}	−0.3 to +0.3	V	
Input voltage	V _{IN}	−0.3 to +7.0* ²	V	
Output voltage	V _{OUT}	−0.3 to +7.0* ³	V	
Display output voltage	V _{OD}	V _{DD} − 4.0 to V _{DD} + 0.3	V	As P-channel transistor is open drain, V _{DD} is reference.
High level output current	I _{OH}	−5	mA	All pins excluding display outputs (value per pin)* ³
	I _{ODH1}	−15	mA	Display outputs S0 to S7 (value per pin)
	I _{ODH2}	−35	mA	Display outputs T0 to T7, and T8/S15 to T15/S8 (value per pin)
High level total output current	ΣI _{OH}	−50	mA	Total for all pins excluding display outputs
	ΣI _{ODH}	−100	mA	Total for all display outputs
Low level output current	I _{OL}	15	mA	
Low level total output current	ΣI _{OL}	130	mA	Total for all outputs
Operating temperature	T _{opr}	−20 to +75	°C	
Storage temperature	T _{stg}	−55 to +150	°C	
Allowable power dissipation	P _D	600	mW	

*¹ AV_{DD} and V_{DD} should be set to a same voltage.

*² V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*³ It specifies output current of general-purpose I/O port.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	Guaranteed range during high speed mode (1/2 dividing clock) operation
		3.5	5.5		Guaranteed range during low speed mode (1/16 dividing clock) operation
		2.7	5.5		Guaranteed operation range by TEX clock
		2.5	5.5		Guaranteed data hold operation range during STOP
Analog power supply	AV _{DD}	4.5	5.5	V	*1
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	*2
	V _{IHS}	0.8V _{DD}	V _{DD}	V	CMOS schmitt input*3
	V _{IHTS}	2.2	V _{DD}	V	TTL schmitt input*4
	V _{IHEX}	V _{DD} - 0.4	V _{DD} + 0.3	V	EXTAL pin*5 TEX pin*6
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	*2
	V _{ILS}	0	0.2V _{DD}	V	CMOS schmitt input*3
	V _{ILTS}	0	0.8	V	TTL schmitt input*4
	V _{ILEX}	-0.3	0.4	V	EXTAL pin*5 TEX pin*6
Operating temperature	Topr	-20	+75	°C	

*1 AV_{DD} and V_{DD} should be set to a same voltage.

*2 Normal input port (each pin of PA1 to PA4, PC, PF0 to PF3, PF5, PF7, PH, PI2, PI3 and PI6), MP pin

*3 Each pin of $\overline{\text{RST}}$, PE0/ $\overline{\text{INT0}}$, PE1/ $\overline{\text{EC0/INT2}}$, PF4/ $\overline{\text{SCK1}}$, PF6/SI1, PI1/RMC, PI4/ $\overline{\text{CS0/NMI/INT1}}$, PI5/ $\overline{\text{SCK0}}$, PI7/SI1 and PG (For PG4 and PG5, when CMOS schmitt input is selected with mask option)

*4 Each pin of PG4 and PG5 (When TTL schmitt input is selected with mask option)

*5 It specifies only when the external clock is input.

*6 It specifies only when the external event is input.

DC Characteristics

(Ta = -20 to +75°C, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	VOH	PA to PC, PE PF4 to PF7, PH, PI1 to PI7, <u>RST</u> *1 (VOL only)	VDD = 4.5V, IOH = -0.5mA	4.0			V
			VDD = 4.5V, IOH = -1.2mA	3.5			V
Low level output voltage	VOL		VDD = 4.5V, IOL = 1.8mA			0.4	V
			VDD = 4.5V, IOL = 3.6mA			0.6	V
Display output current	IOH	S0 to S7		-8			mA
		S8/T15 to S15/T8, T0 to T7	VDD = 4.5V, VOH = VDD - 2.5V	-20			mA
Open drain output leakage current (P-CH Tr OFF in state)	ILOL	S0 to S7, S8/T15 to S15/T8, T0 to T7	VDD = 5.5V, VOL = VDD - 35V VFDP = VDD - 35V			-20	μA
Pull-down resistor*3	RL	S0 to S7, S8/T15 to S15/T8, T0 to T7	VDD = 5V, VFDP - VDD = 30V	60	100	270	kΩ
Input current	IIHE	EXTAL	VDD = 5.5V, VIH = 5.5V	0.5		40	μA
			VDD = 5.5V, VIL = 0.4V	-0.5		-40	μA
	IIIE	TEX	VDD = 5.5V, VIH = 5.5V	0.1		10	μA
			VDD = 5.5V, VIL = 0.4V	-0.1		-10	μA
	IILR	<u>RST</u> *2		-1.5		-400	μA
I/O leakage current	IIZ	PA to PC, PE to PI, AN1 to AN3, MP, <u>RST</u> *2	VDD = 5.5V, VI = 0, 5.5V			±10	μA
Supply current*4	IDD1	VDD, VSS	16MHz crystal oscillation (C1 = C2 = 15pF), VDD = 5V ± 10%*5		25	45	mA
	IDDS1		16MHz crystal oscillation (C1 = C2 = 15pF), VDD = 5V ± 10%, SLEEP mode		1.2	8	mA
	IDD2		32kHz crystal oscillation (C1 = C2 = 47pF), VDD = 3V ± 10%		40	100	μA
	IDDS2		32kHz crystal oscillation (C1 = C2 = 47pF), VDD = 3V ± 10%, SLEEP mode		7	30	μA
	IDDS3		VDD = 5.5V, STOP mode (32kHz, 16MHz oscillation stop)			10	μA
Input capacity	CIN	Other than S0 to S15, T0 to T7, PA0, PA5 to PA7 PE2 to PE7 PB, VDD, VSS AVDD, AVSS	Clock 1MHz 0V other than the measured pins		10	20	pF

- *1 $\overline{\text{RST}}$ pin is specified when evaluation mode is in use.
- *2 $\overline{\text{RST}}$ pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when non-resistor is selected.
- *3 When built-in pull-down resistor is selected with mask option.
- *4 When entire output pins are open.
- *5 When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 0002FEH) to "00" and operating in high speed mode (1/2 dividing clock).

AC Characteristics

(1) Clock timing

($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
System clock frequency	f_c	XTAL EXTAL	Fig. 1, Fig. 2	1		16	MHz
System clock input pulse width	t_{XL} , t_{XH}	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive	28			ns
System clock input rise and fall times	t_{CR} , t_{CF}	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count clock input pulse width	t_{EH} , t_{EL}	$\overline{\text{EC0}}$, $\overline{\text{EC1}}$, $\overline{\text{EC2}}$	Fig. 3	$t_{\text{sys}} + 200^*$			ns
Event count clock input rise and fall times	t_{ER} , t_{EF}	$\overline{\text{EC0}}$, $\overline{\text{EC1}}$, $\overline{\text{EC2}}$	Fig. 3			20	ms
System clock frequency	f_c	TEX TX	$V_{DD} = 2.7$ to 5.5V Fig. 2 (32kHz clock applying condition)		32.768		kHz
Event count clock input pulse width	t_{TL} , t_{TH}	TEX	Fig. 3	10			μs
Event count clock input rise and fall times	t_{TR} , t_{TF}	TEX	Fig. 3			20	ms

* t_{sys} indicates three values according to the contents of the clock control register (address; 00FEH) upper 2 bits (CPU clock selection).

$t_{\text{sys}} [\text{ns}] = 2000/f_c$ (Upper 2 bits = "00"), $4000/f_c$ (Upper 2 bits = "01"), $16000/f_c$ (Upper 2 bits = "11")

Fig. 1. Clock timing

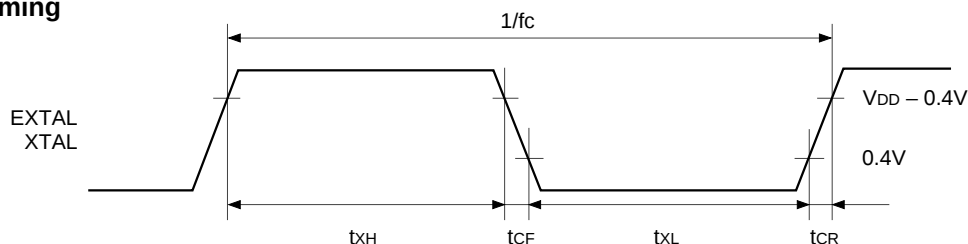


Fig. 2. Clock applying condition

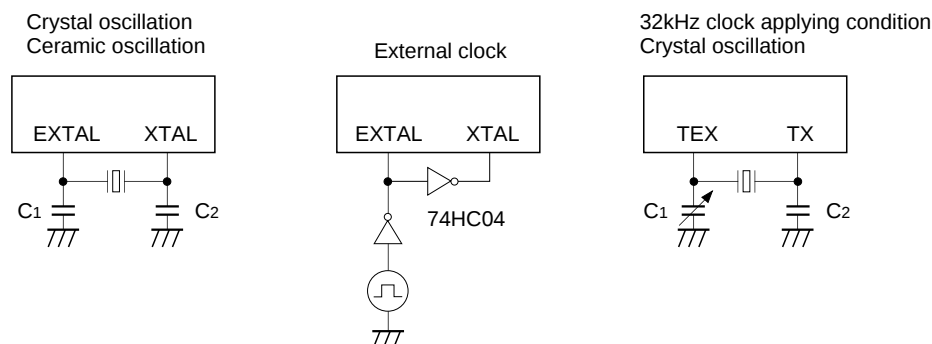
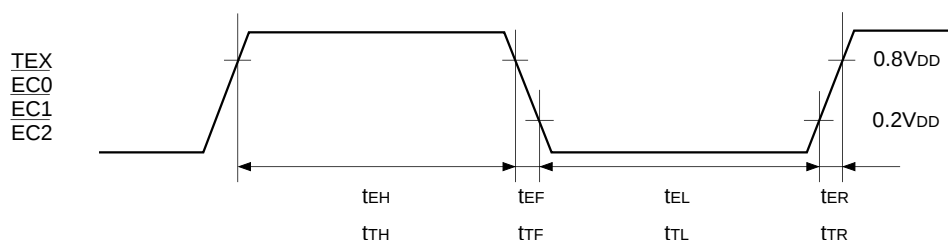


Fig. 3. Event count clock timing

**(2) Serial transfer (CH0)**(Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V)

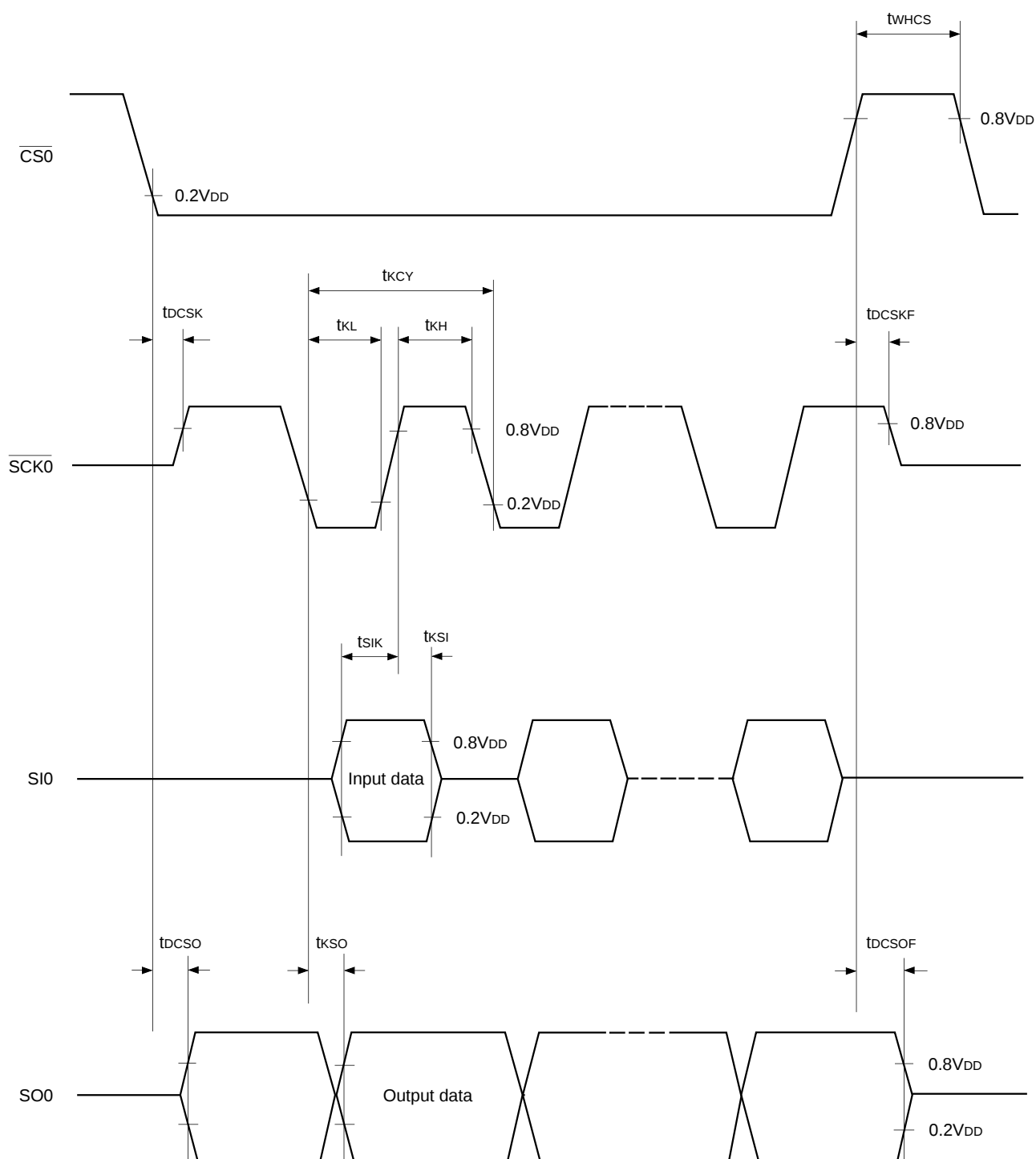
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{CS0}} \downarrow \rightarrow \overline{\text{SCK0}}$ delay time	t_{DCSK}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK0}}$ = output mode)		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}} \uparrow \rightarrow \overline{\text{SCK0}}$ floating delay time	t_{DCSKF}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK0}}$ = output mode)		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}} \downarrow \rightarrow \text{SO0}$ delay time	t_{DCSO}	SO0	Chip select transfer mode		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}} \uparrow \rightarrow \text{SO0}$ floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}}$ high level width	t_{WHCS}	$\overline{\text{CS0}}$	Chip select transfer mode	$t_{\text{sys}} + 200$		ns
$\overline{\text{SCK0}}$ cycle time	t_{KCY}	$\overline{\text{SCK0}}$	Input mode	$2t_{\text{sys}} + 200$		ns
			Output mode	$16000/\text{fc}$		ns
$\overline{\text{SCK0}}$ high and low level widths	t_{KH} t_{KL}	$\overline{\text{SCK0}}$	Input mode	$t_{\text{sys}} + 100$		ns
			Output mode	$8000/\text{fc} - 50$		ns
SI0 input set-up time (against $\overline{\text{SCK0}} \uparrow$)	t_{SIK}	SI0	$\overline{\text{SCK0}}$ input mode	100		ns
			$\overline{\text{SCK0}}$ output mode	200		ns
SI0 input hold time (against $\overline{\text{SCK0}} \uparrow$)	t_{KSI}	SI0	$\overline{\text{SCK0}}$ input mode	$t_{\text{sys}} + 200$		ns
			$\overline{\text{SCK0}}$ output mode	100		ns
$\overline{\text{SCK0}} \downarrow \rightarrow \text{SO0}$ delay time	t_{KSO}	SO0	$\overline{\text{SCK0}}$ input mode		$t_{\text{sys}} + 200$	ns
			$\overline{\text{SCK0}}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FE_H) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The load of $\overline{\text{SCK0}}$ output mode and SO0 output delay time is 50pF + 1TTL.

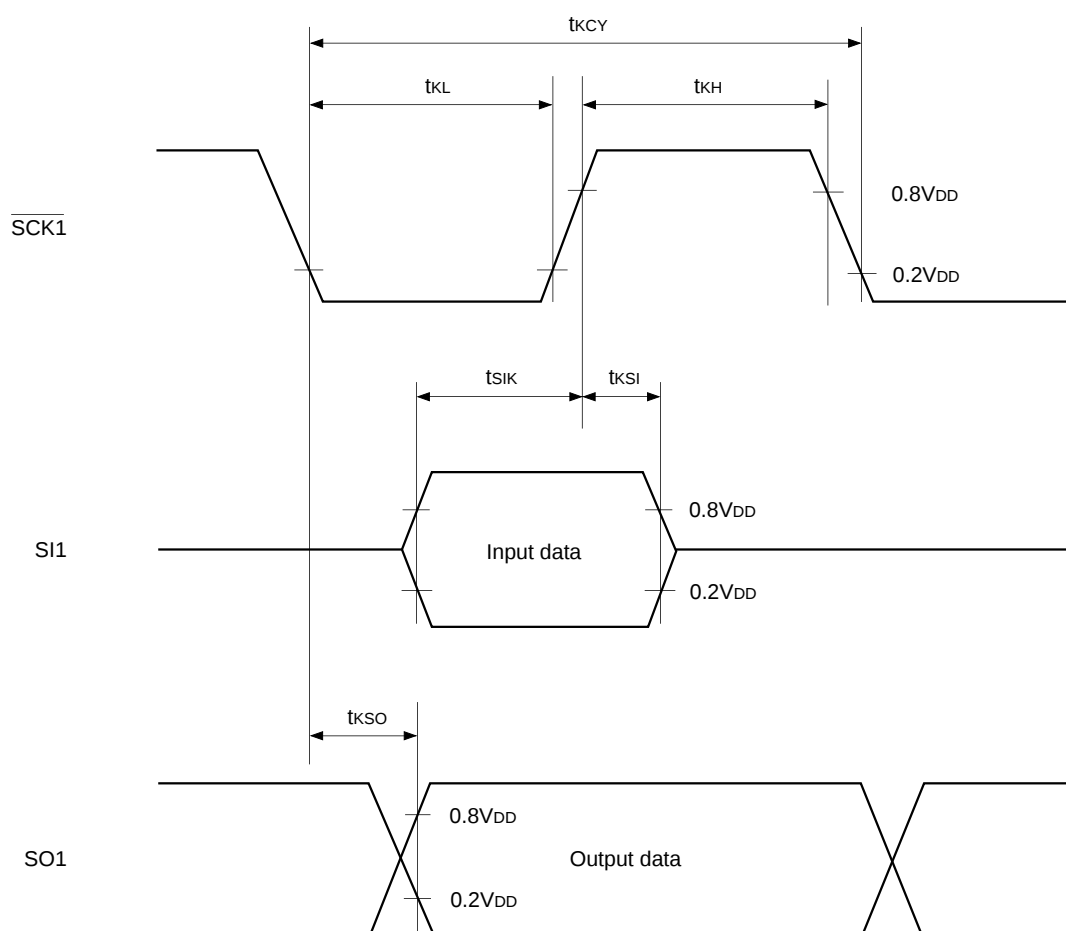
Fig. 4. Serial transfer CH0 timing



Serial transfer (CH1)

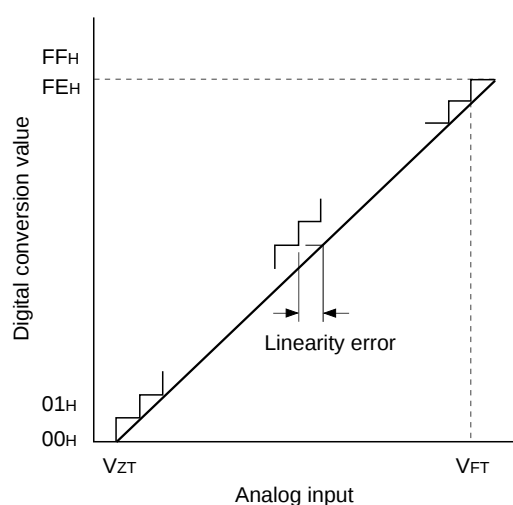
(Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY}	$\overline{\text{SCK1}}$	Input mode	1000		ns
			Output mode	16000/fc		ns
$\overline{\text{SCK1}}$ high and low level widths	t_{KH} t_{KL}	$\overline{\text{SCK1}}$	Input mode	400		ns
			Output mode	8000/fc - 50		ns
SI1 input set-up time (against $\overline{\text{SCK1}}$ ↑)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (against $\overline{\text{SCK1}}$ ↑)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		200	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

Note) The load of $\overline{\text{SCK1}}$ output mode and SO1 output delay time is 50pF + 1TTL.**Fig. 5. Serial transfer CH1 timing**

(3) A/D converter characteristics ($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = AV_{DD} = 4.5$ to 5.5V , $AV_{REF} = 4.0$ to AV_{DD} , $V_{SS} = AV_{SS} = 0\text{V}$)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Only for A/D converter operation $T_a = 25^\circ\text{C}$			± 1	LSB
Absolute error			$V_{DD} = AV_{DD} = AV_{REF} = 5.0\text{V}$ $V_{DD} = AV_{SS} = 0\text{V}$			± 2	LSB
Conversion time	t_{CONV}			$160/f_{\text{ADC}}$			μs
Sampling time	t_{SAMP}			$12/f_{\text{ADC}}$			μs
Reference input voltage	V_{REF}	AV_{REF}	$V_{DD} = AV_{DD} = 4.5$ to 5.5V	$AV_{DD} - 0.5$		AV_{DD}	V
Analog input voltage	V_{IAN}	$AN0$ to $AN7$		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operation mode $AV_{\text{REF}} = 4.0$ to 5.5V		0.6	1.0	mA
			SLEEP mode STOP mode 32kHz operation mode			10	μA

Fig. 6. Definitions of A/D converter terms

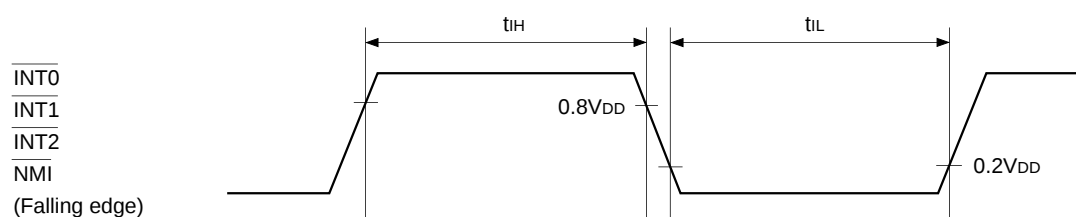
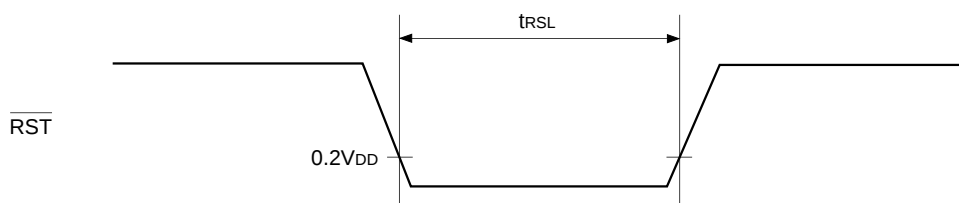
* The value of f_{ADC} is as follows by selecting ADC operation clock (MSC: Address $01FFH$ bit 0).

When PS2 is selected, $f_{\text{ADC}} = f_c/2$

When PS1 is selected, $f_{\text{ADC}} = f_c$

(4) Interruption, reset input(Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t _{IH} t _{IL}	$\overline{\text{INT0}}$ $\overline{\text{INT1}}$ $\overline{\text{INT2}}$ $\overline{\text{NMI}}$		1		μs
Reset input low level width	t _{RSL}	$\overline{\text{RST}}$		32/fc		μs

Fig. 7. Interruption input timing**Fig. 8. Reset input timing****(5) Others**(Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V)

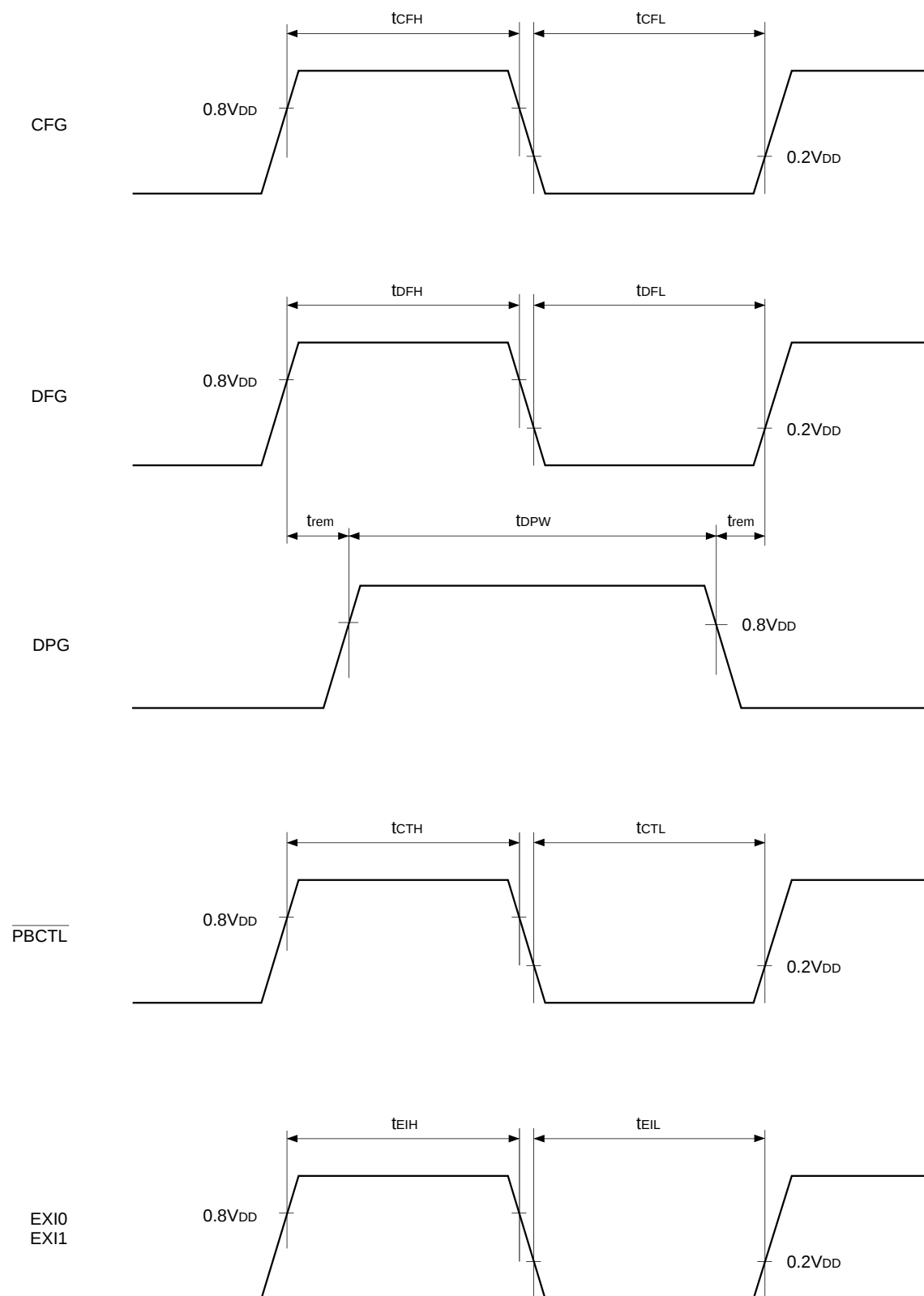
Item	Symbol	Pin	Condition	Min.	Max.	Unit
CFG input high and low level widths	t _{CFH} t _{CFL}	CFG		$t_{FRC} \times 24 + 200$		ns
DFG input high and low level widths	t _{DFH} t _{DFL}	DFG		$t_{FRC} \times 16 + 200$		ns
DPG minimum pulse width	t _{DPW}	DPG		$t_{FRC} \times 8 + 200$		ns
DPG minimum removal time	t _{rem}	DPG		$t_{FRC} \times 16 + 200$		ns
$\overline{\text{PBCTL}}$ input high and low level widths	t _{CTH} t _{CTL}	$\overline{\text{PBCTL}}$	$t_{sys} = 2000/fc$	$t_{FRC} \times 8 + t_{sys} + 200$		ns
EXI input high and low level widths	t _{EIH} t _{EIL}	EXI0 EXI1	$t_{sys} = 2000/fc$	$t_{FRC} \times 8 + t_{sys} + 200$		ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address; 00FE_H) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) $t_{FRC} = 1000/fc$ (ns)

Fig. 9. Other timings



Supplement

Fig. 10. Recommended oscillation circuit



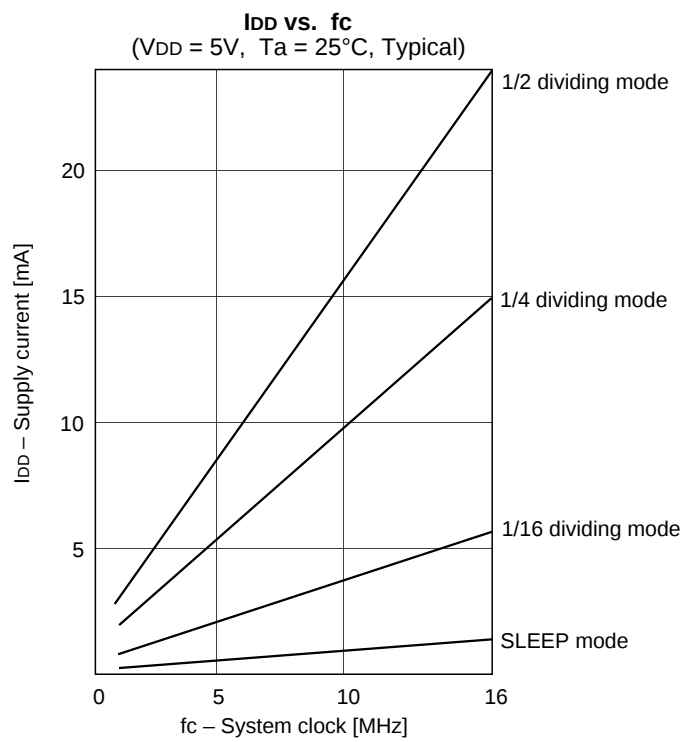
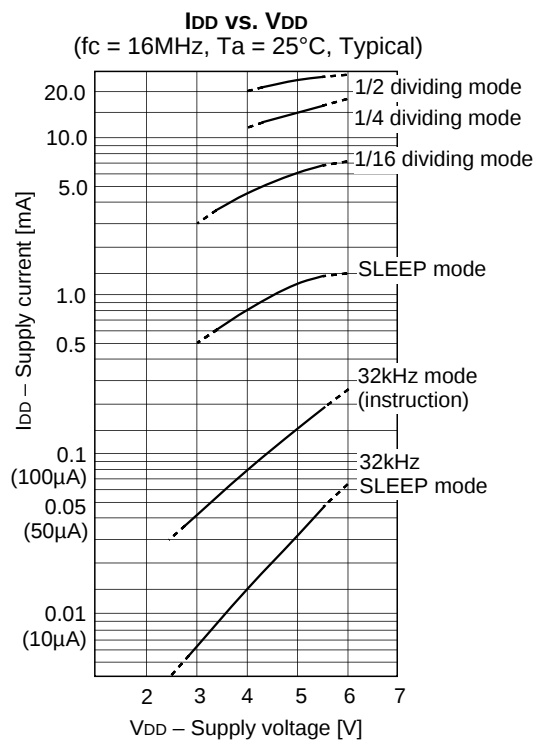
Manufacturer	Model	fc (MHz)	C ₁ (pF)	C ₂ (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	22 (15)	22 (15)	0	(i)
		10.00				
		12.00	15	15		
		16.00	12	12		
	P3	32.768kHz	30	18	470K	(ii)

Mask option table

Item	Content	
Reset pin pull-up resistor	Non-existent	Existent
Power-on reset circuit	Non-existent	
High voltage drive output port pull-down resistor	Non-existent	Existent
Input circuit format*	CMOS schmitt	TTL schmitt

* In PG4/SYNC0/ $\overline{EC}2$ pin and PG5/SYNC1 pin, the input circuit format can be selected every pin.

Characteristics Curve



Unit: mm

Technical drawing of a rectangular component with dimensions and a detail view.

Top View Dimensions:

- Overall width: 23.9 ± 0.4
- Inner width: $20.0 - 0.1$ to $+0.4$
- Overall height: 17.9 ± 0.4
- Inner height: $14.0 - 0.01$ to $+0.4$
- Distance from left edge to first hole: 0.65

Feature Callouts:

- Feature M: ± 0.12 M
- Feature A: 0.15

Side View Dimensions:

- Overall height: 15.8 ± 0.4
- Distance from top edge to bottom edge: $2.75 - 0.15$ to $+0.35$

Detail A:

- Angle: 0° to 15°
- Dimension: 0.8 ± 0.2
- Dimension: (16.3)

SONY CODE	QFP-100P-L01
EIAJ CODE	*QFP100-P-1420-A
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g



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Электрон
Связь**

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