HIGH GRADE Specification HIGH RELIABILITY series

Microwire BUS Serial EEPROMs

Supply voltage 1.8V~5.5V
Operating temperature –40°C~+85°C type

BR93L46-W, BR93L56-W, BR93L66-W, BR93L76-W, BR93L86-W

● Description

BR93L□□-W series is a serial EEPROM of serial 3-line interface method.

● Features

- 3-line communications of chip select, serial clock, serial data input / output (the case where input and output are shared)
- Actions available at high speed 2MHz clock (2.5 ~ 5.5V)
- Speed write available (write time 5 ms max.)
- Same package and pin layout from 1Kbit to 16Kbit
- 1.8 ~ 5.5V single power source action
- Highly reliable connection by Au pad and Au wire
- Address auto increment function at read action
- Write mistake prevention function
  - Write prohibition at power on
  - Write prohibition by command code
  - Write mistake prevention function at low voltage
- Program cycle auto delete and auto end function
- Program condition display by READY / $\overline{\text{BUSY}}$
- Low current consumption
  - At write action (at 5V) : 1.2mA (Typ.)
  - At read action (at 5V) : 0.3mA (Typ.)
  - At standby action (at 5V) : 0.1µA (Typ.) (CMOS input)
- TTL compatible input / output
- Compact package SOP8, SOP-J8, SSOP-B8, TSSOP-B8, MSOP8, TSSOP-B8J
- Data retention for 40 years
- Data rewrite up to 1,000,000 times
- Data at shipment all addresses FFFFh

●BR93L Series

Capacity	Bit format	Type	Power source voltage	SOP8		SOP-J8		SSOP-B8		TSSOP-B8		MSOP8	TSSOP-B8J
Package type				F	RF	FJ	RFJ	FV	RFV	FVT	RFVT	RFVM	RFVJ
1Kbit	64 × 16	BR93L46-W	1.8 ~ 5.5V	●	●	●	●	●	●	●	●	●	●
2Kbit	128 × 16	BR93L56-W	1.8 ~ 5.5V	●	●	●	●	●	●	●	●	●	●
4Kbit	256 × 16	BR93L66-W	1.8 ~ 5.5V	●	●	●	●	●	●	●	●	●	●
8Kbit	512 × 16	BR93L76-W	1.8 ~ 5.5V	●	●	●	●		●		●	●	●
16Kbit	1K × 16	BR93L86-W	1.8 ~ 5.5V	●	●	●	●		●		●	●	●

Ver.B Oct.2005

● Absolute Maximum Ratings (Ta=25˚C)

Parameter	Symbol	Limits		Unit
Impressed voltage	V_{CC}	-0.3 ~ +6.5		V
Permissible dissipation	Pd	SOP8 (F, RF)	450 (*1)	mW
		SOP-J8 (FJ, RFJ)	450 (*2)	
		SSOP-B8 (FV, RFV)	300 (*3)	
		TSSOP-B8 (FVT, RFVT)	330 (*4)	
		MSOP8 (RFVM)	310 (*5)	
		TSSOP-B8J (RFVJ)	310 (*6)	
Storage temperature range	Tstg	-65 ~ +125		˚C
Action temperature range	Topr	-40 ~ +85		˚C
Terminal voltage	-	-0.3 ~ V_{CC}+0.3		V

* When using at Ta = 25˚C or higher, 4.5mW (*1, *2), 3.0mW (*3), 3.3mW (*4),3.1mW (*5, *6) to be reduced per 1˚C.

● Recommended action conditions

Parameter	Symbol	Limits	Unit
Power source voltage	V_{CC}	1.8 ~ 5.5	V
Input voltage	V_{IN}	0 ~ V_{CC}	V

● Electrical characteristics (Unless otherwise specified, Ta=-40 ~ +85˚C, Vcc=2.5 ~ 5.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
"L" input voltage 1	V_{IL1}	-0.3	-	+0.8	V	4.0V≤V_{CC}≤5.5V
"L" input voltage 2	V_{IL2}	-0.3	-	0.2xV_{CC}	V	V_{CC}≤4.0V
"H" input voltage 1	V_{IH1}	2.0	-	V_{CC}+0.3	V	4.0V≤V_{CC}≤5.5V
"H" input voltage 2	V_{IH2}	0.7xV_{CC}	-	V_{CC}+0.3	V	V_{CC}≤4.0V
"L" output voltage 1	V_{OL1}	0	-	0.4	V	I_{OL}=2.1mA, 4.0V≤V_{CC}≤5.5V
"L" output voltage 2	V_{OL2}	0	-	0.2	V	I_{OL}=100μA
"H" output voltage 1	V_{OH1}	2.4	-	V_{CC}	V	I_{OH}=-0.4mA, 4.0V≤V_{CC}≤5.5V
"H" output voltage 2	V_{OH2}	V_{CC}-0.2	-	V_{CC}	V	I_{OH}=-100μA
Input leak current	I_{LI}	-1	-	+1	μA	V_{IN}=0~V_{CC}
Output leak current	I_{LO}	-1	-	+1	μA	V_{OUT}=0~V_{CC}, CS=0V
Current consumption at action	I_{CC1}	-	-	3.0	mA	f_{SK}=2MHz, $t_{E/W}$=5ms (WRITE)
	I_{CC2}	-	-	1.5	mA	f_{SK}=2MHz (READ)
	I_{CC3}	-	-	4.5	mA	f_{SK}=2MHz, $t_{E/W}$=5ms (WRAL,ERAL)
Standby current	I_{SB}	-	-	2	μA	CS=0V, DO=OPEN

◎Radiation resistance design is not made.

(Unless otherwise specified, Ta=-40 ~ +85˚C, Vcc=1.8 ~ 2.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
"L" input voltage	V_{IL}	-0.3	-	0.2xV_{CC}	V	
"H" input voltage	V_{IH}	0.7xV_{CC}	-	V_{CC}+0.3	V	
"L" output voltage	V_{OL}	0	-	0.2	V	I_{OL}=100μA
"H" output voltage	V_{OH}	V_{CC}-0.2	-	V_{CC}	V	I_{OH}=-100μA
Input leak current	I_{LI}	-1	-	+1	μA	V_{IN}=0~V_{CC}
Output leak current	I_{LO}	-1	-	+1	μA	V_{OUT}=0~V_{CC}, CS=0V
Current consumption at action	I_{CC1}	-	-	1.5	mA	f_{SK}=500kHz, $t_{E/W}$=5ms (WRITE)
	I_{CC2}	-	-	0.5	mA	f_{SK}=500kHz (READ)
	I_{CC3}	-	-	2	mA	f_{SK}=500kHz (WRAL,ERAL)
Standby current	I_{SB}	-	-	2	μA	CS=0V, DO=OPEN

◎Radiation resistance design is not made.

● Memory cell characteristics (Ta=25˚C, Vcc=1.8 ~ 5.5V)

Parameter	Min.	Typ.	Max.	Unit
Number of data rewrite times *1	1,000,000	-	-	Times
Data hold years *1	40	-	-	Years

*1 Not 100% TESTED

● Action timing characteristics (Ta=-40 ~ +85˚C, Vcc=2.5 ~ 5.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SK frequency	f_{SK}	-	-	2	MHz
SK "H" time	t_{SKH}	230	-	-	ns
SK "L" time	t_{SKL}	230	-	-	ns
CS "L" time	t_{CS}	200	-	-	ns
CS setup time	t_{CSS}	50	-	-	ns
DI setup time	t_{DIS}	100	-	-	ns
CS hold time	t_{CSH}	0	-	-	ns
DI hold time	t_{DIH}	100	-	-	ns
Data "1" output delay time	t_{PD1}	-	-	200	ns
Data "0" output delay time	t_{PD0}	-	-	200	ns
Time from CS to output establishment	t_{SV}	-	-	150	ns
Time from CS to High-Z	t_{DF}	-	-	150	ns
Write cycle time	$t_{E/W}$	-	-	5	ms

(Ta=-40 ~ +85˚C, Vcc=1.8 ~ 2.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SK frequency	f_{SK}	-	-	500	kHz
SK "H" time	t_{SKH}	0.8	-	-	μs
SK "L" time	t_{SKL}	0.8	-	-	μs
CS "L" time	t_{CS}	1	-	-	μs
CS setup time	t_{CSS}	200	-	-	ns
DI setup time	t_{DIS}	100	-	-	ns
CS hold time	t_{CSH}	0	-	-	ns
DI hold time	t_{DIH}	100	-	-	ns
Data "1" output delay time	t_{PD1}	-	-	0.7	μs
Data "0" output delay time	t_{PD0}	-	-	0.7	μs
Time from CS to output establishment	t_{SV}	-	-	0.7	μs
Time from CS to High-Z	t_{DF}	-	-	200	ns
Write cycle time	$t_{E/W}$	-	-	5	ms

● Sync data input / output timing

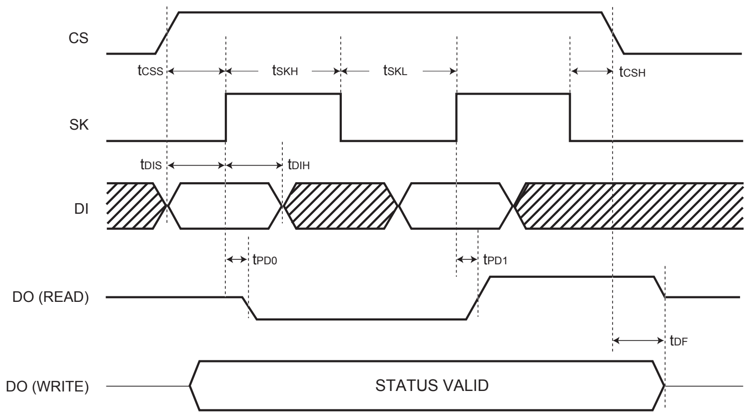


Fig.1 Sync data input / output timing

○ Data is taken by DI in sync with the rise of SK.

○ At read action, data is output from DO in sync with the rise of SK.

○ The status signal at write (READY / $\overline{\text{BUSY}}$) is output after tCS from the fall of CS after write command input, at the area DO where CS is "H", and valid until the next command start bit is input. And, while CS is "L", DO becomes High-Z.

○ After completion of each mode execution, set CS "L" once for internal circuit reset, and execute the following action mode.

● Characteristic data

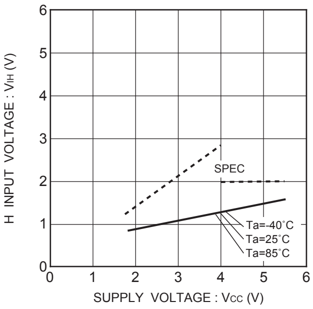


Fig. 2 H input voltage V_{IH} (CS,SK,DI)

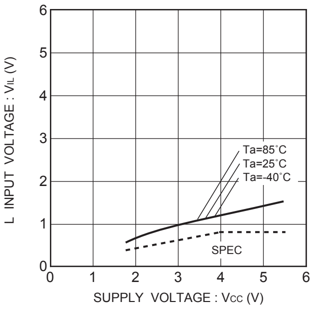


Fig. 3 H input voltage V_{IL}(CS,SK,DI)

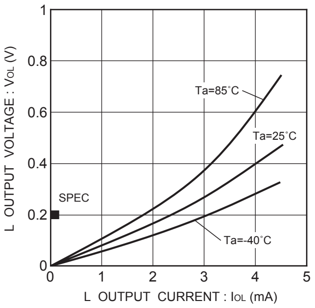


Fig. 4 L output voltage V_{OL}-I_{OL}(V_{CC}=1.8V)

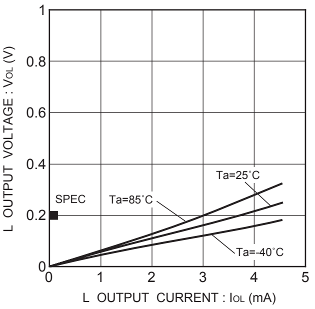


Fig. 5 L output voltage V_{OL}-I_{OL}(V_{CC}=2.5V)

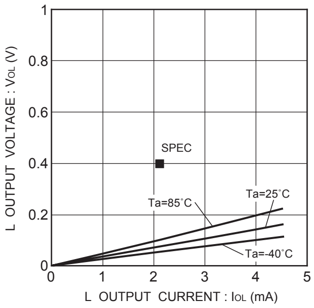


Fig. 6 L output voltage V_{OL}-I_{OL}(V_{CC}=4.0V)

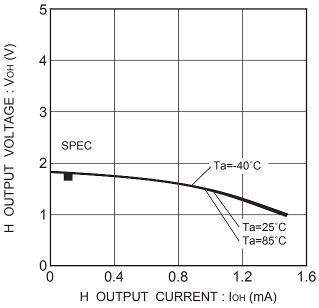


Fig. 7 H output voltage V_{OH}-I_{OH}(V_{CC}=1.8V)

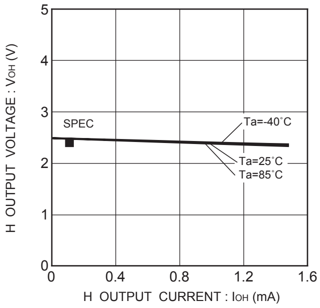


Fig. 8 H output voltage V_{OH}-I_{OH}(V_{CC}=2.5V)

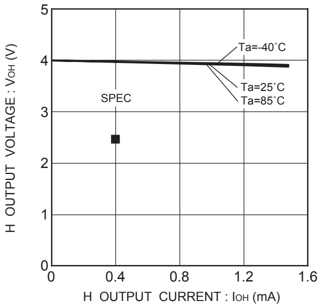


Fig. 9 H output voltage V_{OH}-I_{OH}(V_{CC}=4.0V)

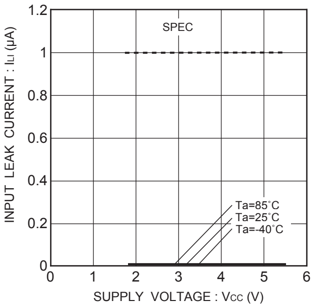


Fig. 10 Input leak current I_{LI} (CS,SK,DI)

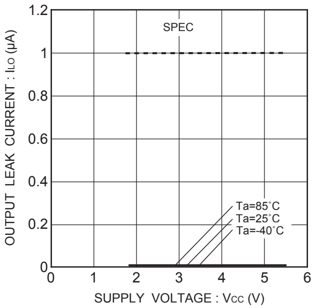


Fig. 11 Output leak current I_{LO} (DO)

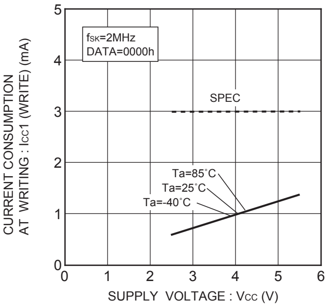


Fig. 12 Current consumption at WRITE action
$I_{CC}1$(WRITE,f_{SK}=2MHz)

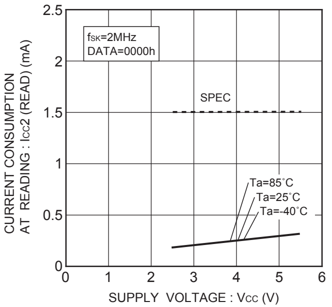


Fig. 13 Consumption current at READ action
$I_{CC}2$(READ,f_{SK}=2MHz)

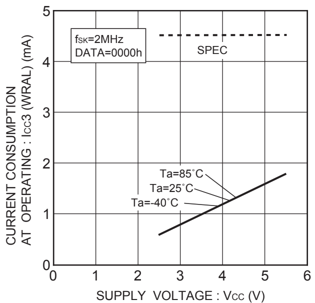


Fig. 14 Consumption current at WRAL action
$I_{CC}3$(WRAL,f_{SK}=2MHz)

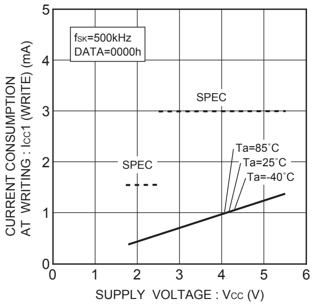


Fig. 15 Current consumption at WRITE action
$I_{CC}1$(WRITE,f_{SK}=500kHz)

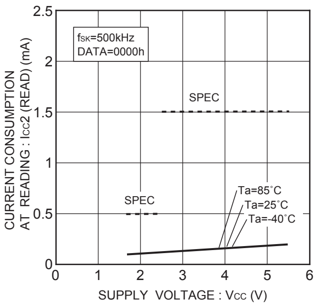


Fig. 16 Consumption current at READ action
$I_{CC}2$(READ,f_{SK}=500kHz)

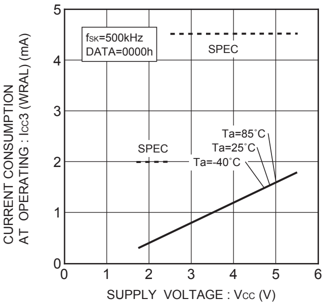


Fig. 17 Consumption current at WRAL action I_{CC}3(WRAL,f_{SK}=500kHz)

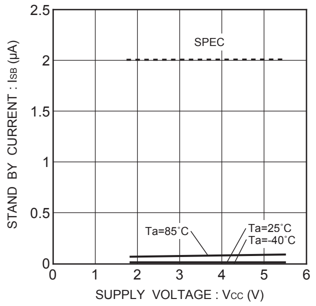


Fig. 18 Consumption current at standby action I_{SB}

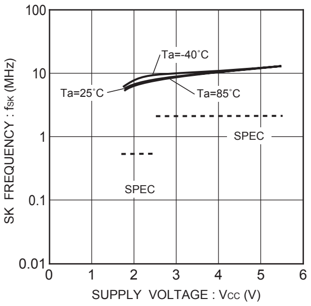


Fig. 19 SK frequency f_{SK}

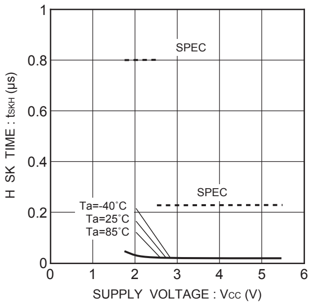


Fig. 20 SK high time t_{SKH}

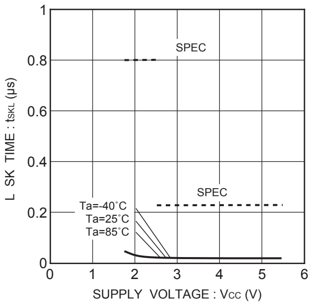


Fig. 21 SK low time t_{SKL}

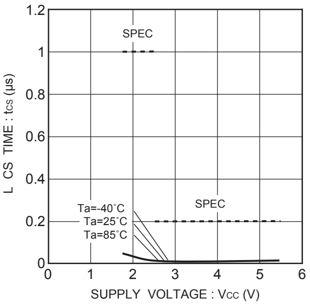


Fig. 22 CS low time t_{CS}

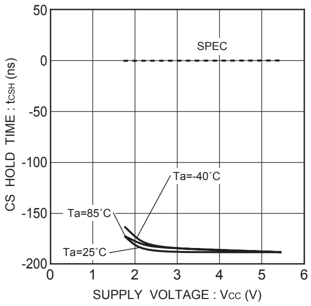


Fig. 23 CS hold time t_{CSH}

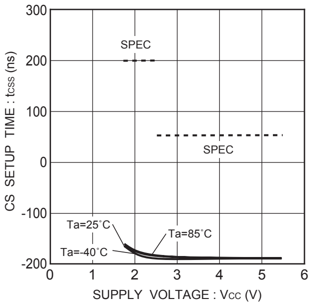


Fig. 24 CS setup time t_{CSS}

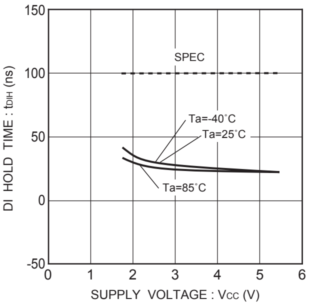


Fig. 25 DI hold time t_{DIH}

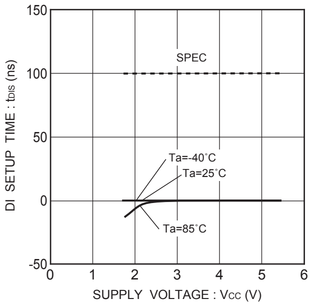


Fig. 26 DI setup time t_{DIS}

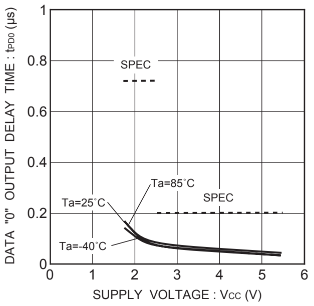


Fig. 27 Data "0" output delay time t_{PD0}

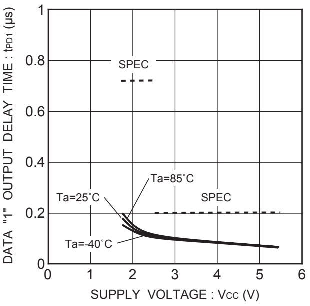


Fig. 28 Output data "1" delay time t_{PD1}

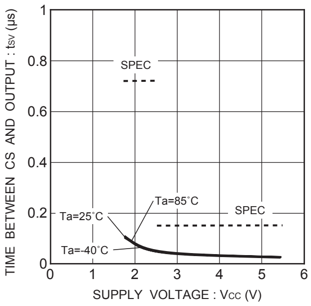


Fig. 29 Time from CS to output establishment t_{SV}

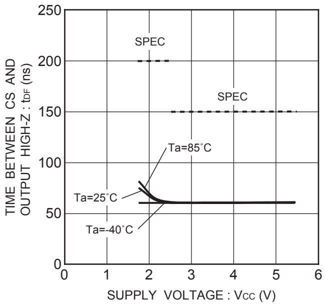


Fig. 30 Time from CS to High-Z t_{DF}

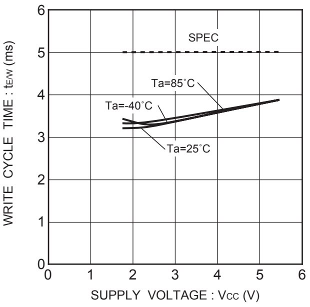


Fig. 31 Write cycle time $t_{E/W}$

● Block diagram

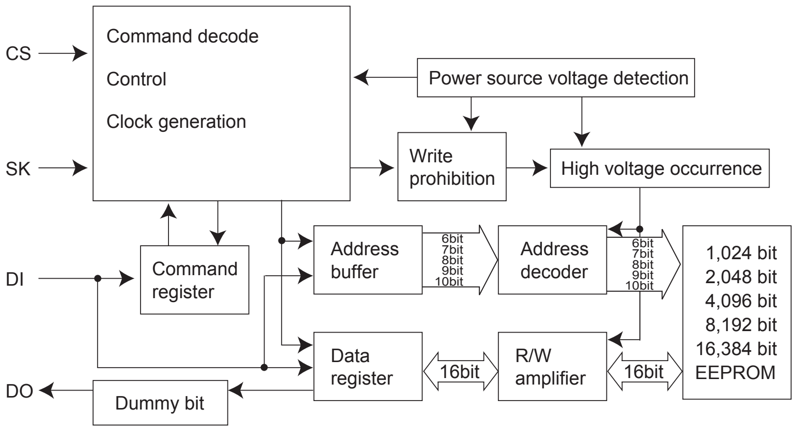


Fig. 32 Block diagram

● Pin assignment and function

* BR93L46/56/66-W

Fig. 33 Pin assignment diagram

Pin name	I / O	Function
Vcc	-	Power source
GND	-	All input / output reference voltage, 0V
CS	Input	Chip select input
SK	Input	Serial clock input
DI	Input	Start bit, ope code, address, and serial data input
DO	Output	Serial data output, READY / $\overline{\text{BUSY}}$ internal condition display output
NC	-	Non connected terminal, Vcc, GND or OPEN

●Description of operations

Communications of the Microwire Bus are carried out by SK (serial clock), DI (serial data input), DO (serial data output), and CS (chip select) for device selection.

When to connect one EEPROM to a microcontroller, connect it as shown in Fig. 34 (a) or Fig. 34 (b). When to use the input and output common I/O port of the microcontroller, connect DI and DO via a resistor as shown in Fig. 34 (b) (Refer to pages 13/16.), and connection by 3 lines is available.

In the case of plural connections, refer to Fig. 34 (c).

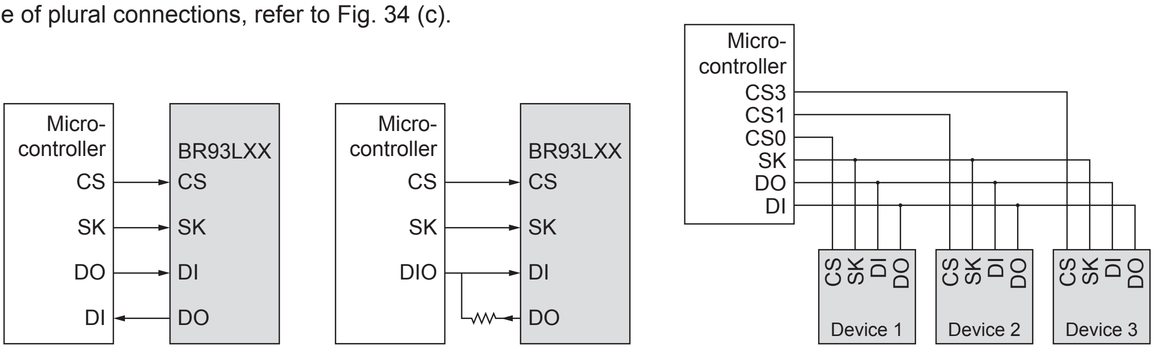


Fig. 34-(a) Connection by 4 lines Fig. 34-(b) Connection by 3 lines Fig. 34-(c) Connection example of plural devices

Fig. 34 Connection method with microcontroller

Communications of the Microwire Bus are started by the first "1" input after the rise of CS. This input is called a start bit. After input of the start bit, input ope code, address and data. Address and data are input all in MSB first manners.

"0" input after the rise of CS to the start bit input is all ignored. Therefore, when there is limitation in the bit width of PIO of the microcontroller, input "0" before the start bit input, to control the bit width.

● Command mode

Command	Start bit	Ope code	Address			Data
			BR93L46-W	BR93L56/66-W	BR93L76/86-W	
Read (READ) *1	1	10	A5,A4,A3,A2,A1,A0	A7,A6,A5,A4,A3,A2,A1,A0	A9,A8,A7,A6,A5,A4,A3,A2,A1,A0	D15 ~ D0 (READ DATA)
Write enable (WEN)	1	00	1 1 * * * *	1 1 * * * * * *	1 1 * * * * * * * *	
Write (WRITE) *2	1	01	A5,A4,A3,A2,A1,A0	A7,A6,A5,A4,A3,A2,A1,A0	A9,A8,A7,A6,A5,A4,A3,A2,A1,A0	D15 ~ D0 (WRITE DATA)
Write all (WRAL) *2	1	00	0 1 * * * *	0 1 * * * * * *	0 1 * * * * * * * *	D15 ~ D0 (WRITE DATA)
Write disable (WDS)	1	00	0 0 * * * *	0 0 * * * * * *	0 0 * * * * * * * *	
Erase (ERASE)	1	11	A5,A4,A3,A2,A1,A0	A7,A6,A5,A4,A3,A2,A1,A0	A9,A8,A7,A6,A5,A4,A3,A2,A1,A0	
Chip erase (ERAL)	1	00	1 0 * * * *	1 0 * * * * * *	1 0 * * * * * * * *	

- Input the address and the data in MSB first manners.
- As for *, input either VIH or VIL.

A7 of BR93L56-W becomes Don't Care.
A9 of BR93L76-W becomes Don't Care.

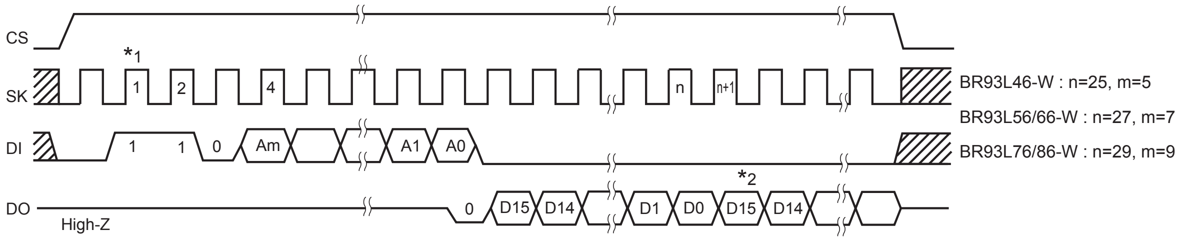
* Start bit
Acceptance of all the commands of this IC starts at recognition of the start bit.
The start bit means the first "1" input after the rise of CS.

*1 As for read, by continuous SK clock input after setting the read command, data output of the set address starts, and address data in significant order are sequentially output continuously. (Auto increment function)

*2 When the read, and the write all commands are executed, data written in the selected memory cell is automatically deleted, and input data is written.

● Timing chart

1) Read cycle (READ)



*1 Start bit
When data "1" is input for the first time after the rise of CS, this is recognized as a start bit. And when "1" is input after plural "0" are input, it is recognized as a start bit, and the following operation is started. This is common to all the commands to described hereafter.

Fig. 35 Read cycle

○ When the read command is recognized, input address data (16bit) is output to serial. And at that moment, at taking A0, in sync with the rise of SK, "0" (dummy bit) is output. And, the following data is output in sync with the rise of SK.
This IC has address auto increment function valid only at read command. This is the function where after the above read execution, by continuously inputting SK clock, the above address data is read sequentially. And, during the auto increment, keep CS at "H".

2) Write cycle (WRITE)

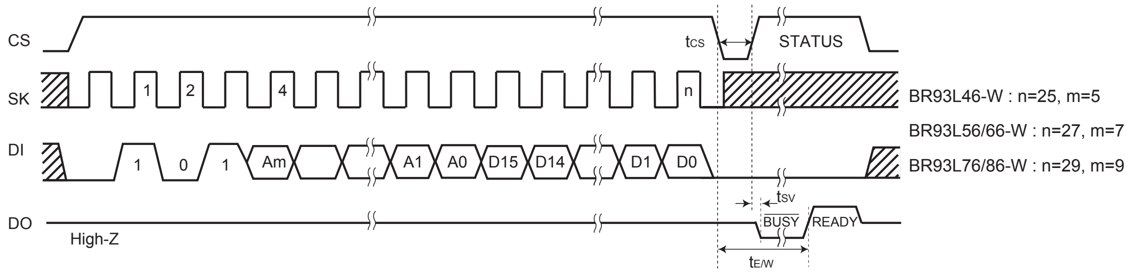


Fig. 36 Write cycle

○ In this command, input 16bit data (D15 ~ D0) are written to designated addresses (Am ~ A0). The actual write starts by the fall of CS of D0 taken SK clock.
When STATUS is not detected, (CS = "L" fixed) Max. 5ms in conformity with tE/W, and when STATUS is detected (CS = "H"), all commands are not accepted for areas where "L" ($\overline{\text{BUSY}}$) is output from D0, therefore, do not input any command.

3) Write all cycle (WRAL)

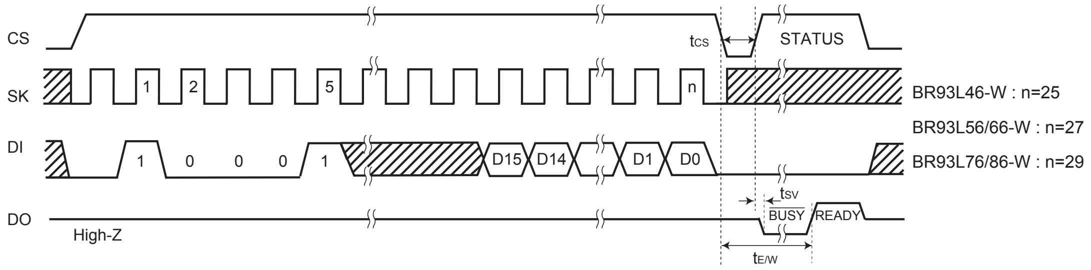


Fig. 37 Write all cycle

○ In this command, input 16bit data is written simultaneously to all addresses. Data is not written continuously per one word but is written in bulk, the write time is only Max. 5ms in conformity with tE/W.

4) Write enable (WEN) / disable (WDS) cycle

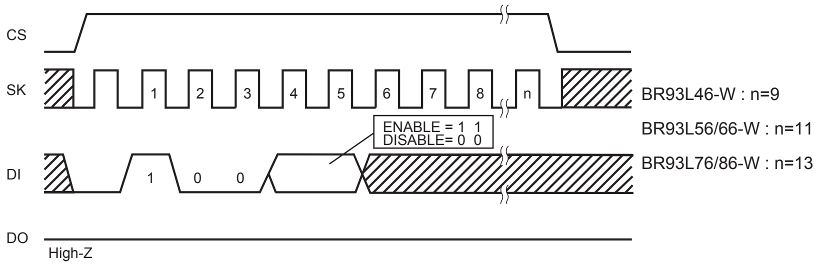


Fig. 38 Write enable (WEN) / disable (WDS) cycle

○ At power on, this IC is in write disable status by the internal RESET circuit. Before executing the write command, it is necessary to execute the write enable command. And, once this command is executed, it is valid until the write disable command is executed or the power is turned off. However, the read command is valid irrespective of write enable / disable command. Input to SK after 6 clocks of this command is available by either "H" or "L", but be sure to input it.

○ When the write enable command is executed after power on, write enable status gets in. When the write disable command is executed then, the IC gets in write disable status as same as at power on, and then the write command is canceled thereafter in software manner. However, the read command is executable. In write enable status, even when the write command is input by mistake, write is started. To prevent such a mistake, it is recommended to execute the write disable command after completion of write.

5) Erase cycle timing (ERASE)

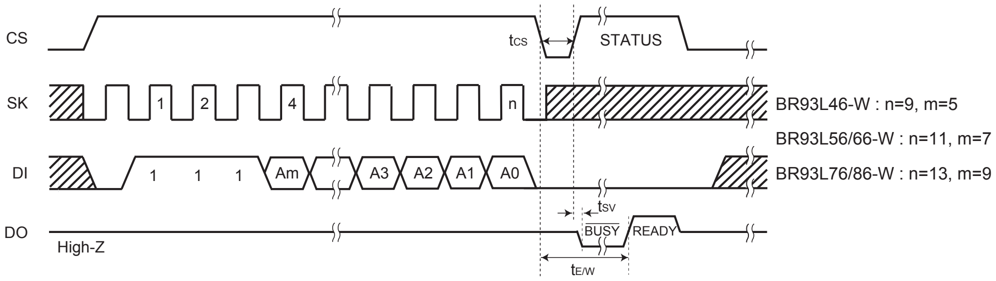


Fig. 39 Erase cycle timing

○ In this command, data of the designated address is made into "1". The data of the designated address becomes "FFFFh". Actual ERASE starts at the fall of CS after the fall of A0 taken SK clock.
In ERASE, status can be detected in the same manner as in WRITE command.

6) Chip erase cycle timing (ERAL)

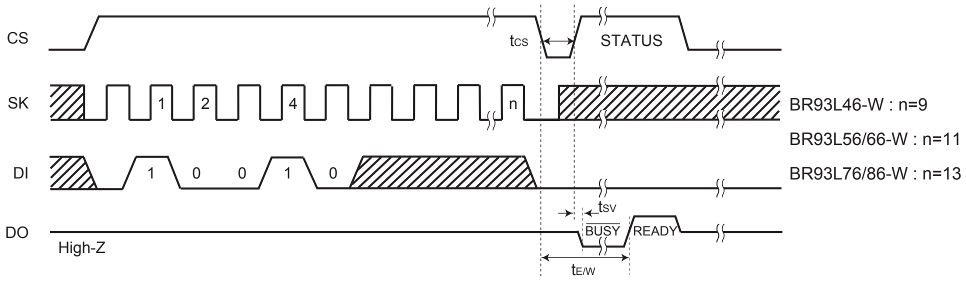


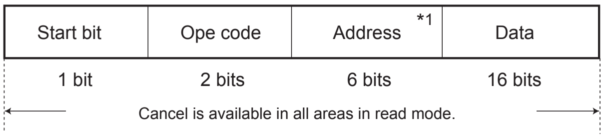
Fig. 40 Chip erase cycle timing

○ In this command, data of all addresses is erased. Data of all addresses becomes "FFFFh". Actual ERASE starts at the fall of CS after the fall of the n-th clock from the start bit input.
In ERAL, status can be detected in the same manner as in WRITE command.

● Application

1) Method to cancel each command

○READ



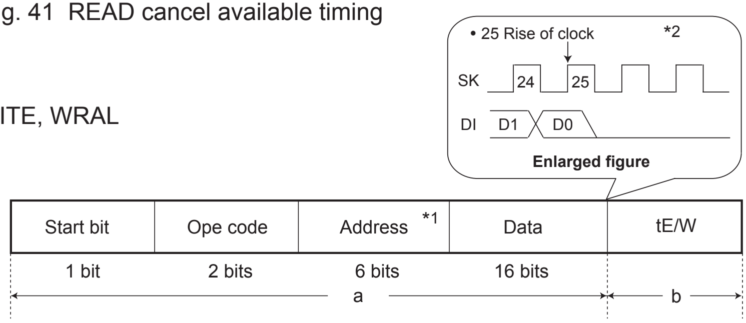
(In the case of BR93L46-W)

- Method to cancel : cancel by CS = "L"

*1 Address is 8 bits in BR93L56-W, and BR93L66-W.
Address is 10 bits in BR93L76-W, and BR93L86-W.

Fig. 41 READ cancel available timing

○WRITE, WRAL



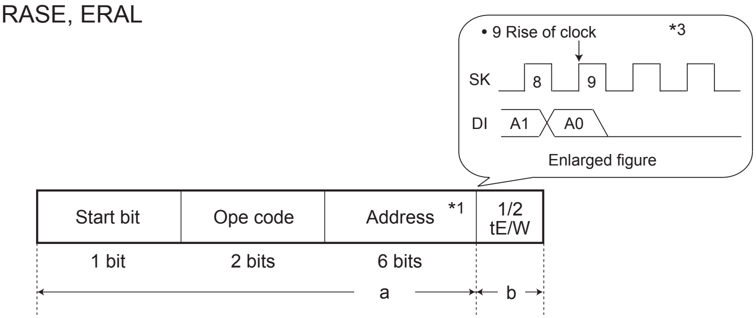
(In the case of BR93L46-W)

a : From start bit to 25 clock rise *2
Cancel by CS = "L"
b : 25 clock rise and after *2
Cancellation is not available by any means. If Vcc is made OFF in this area, designated address data is not guaranteed, therefore write once again.
And when SK clock is input continuously, cancellation is not available.

*1 Address is 8 bits in BR93L56-W, and BR93L66-W.
Address is 10 bits in BR93L76-W, and BR93L86-W.
*2 27 clocks in BR93L56-W, and BR93L66-W
29 clocks in BR93L76-W, and BR93L86-W

Fig. 42 WRITE, WRAL cancel available timing

○ERASE, ERAL



a : From start bit to 9 clock rise *3
Cancel by CS = "L"
b : 9 clock rise and after *3
Cancellation is not available by any means. If Vcc is made OFF in this area, designated address data is not guaranteed, therefore write once again.
And when SK clock is input continuously, cancellation is not available.

*1 Address is 8 bits in BR93L56-W, and BR93L66-W.
Address is 10 bits in BR93L76-W, and BR93L86-W.
*2 11 clocks in BR93L56-W, and BR93L66-W
13 clocks in BR93L76-W, and BR93L86-W

Fig. 43 ERASE, ERAL cancel available timing

2) At standby

○ Standby current

When CS is "L", SK input is "L", DI input is "H", and even with middle electric potential, current does not increase.

○ Timing

As shown in Fig. 44, when SK at standby is "H", if CS is started, DI status may be read at the rise edge.
At standby and at power ON/OFF, when to start CS, set SK input or DI input to "L" status. (Refer to Fig. 45.)

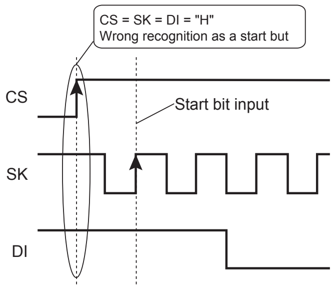


Fig. 44 Wrong action timing

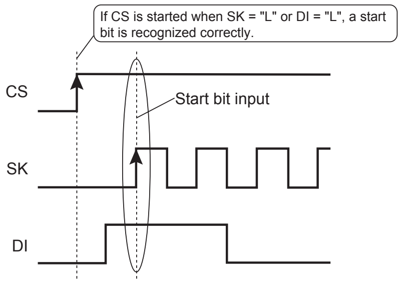


Fig. 45 Normal action timing

3) Equivalent circuit

Output circuit

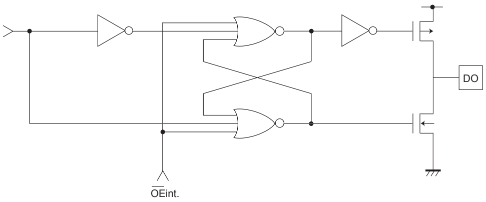


Fig. 46 Output circuit (DO)

Input circuit

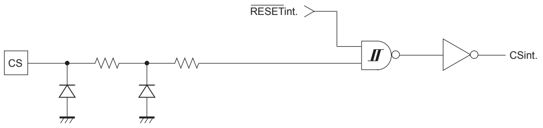


Fig. 47 Input circuit (CS)

Input circuit

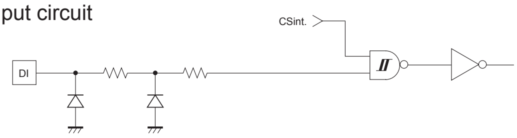


Fig. 48 Input circuit (DI)

Input circuit

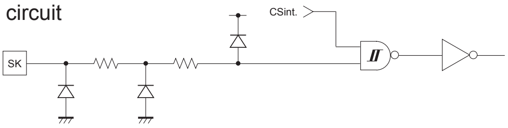


Fig. 49 Input circuit (SK)

4) I/O peripheral circuit

4-1) Pull down CS.

By making CS = "L" at power ON/OFF, mistake in operation and mistake write are prevented.

○ Pull down resistance Rpd of CS pin

To prevent mistake in operation and mistake write at power ON/OFF, CS pull down resistance is necessary. Select an appropriate value to this resistance value from microcontroller VOH, IOH, and VIL characteristics of this IC.

$$\text{Rpd} \geq \frac{\text{VOHM}}{\text{IOHM}} \quad \cdots ①$$

$$\text{VOHM} \geq \text{VIHE} \quad \cdots ②$$

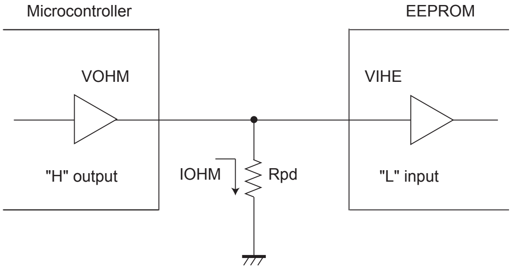


Fig. 50 CS pull down resistance

Example) When Vcc = 5V, VIHE = 2V, VOHM = 2.4V, IOHM = 2mA, from the equation ①,

$$\text{Rpd} \geq \frac{2.4}{2\times10^{-3}}$$

$$\therefore \quad \text{Rpd} \geq 1.2\ (\text{K}\Omega)$$

With the value of Rpd to satisfy the above equation, VOHM becomes 2.4V or higher, and with VIHE (= 2.0V), the equation ② is also satisfied.

- VIHE : EEPROM VIH specifications
- VOHM : Microcontroller VOH specifications
- IOHM : Microcontroller IOH specifications

4-2) DO is available in both pull up and pull down.

DO output become "High-Z" in other READY / $\overline{\text{BUSY}}$ output timing than after data output at read command and write command.

When malfunction occurs at "High-Z" input of the microcontroller port connected to DO, it is necessary to pull down and pull up DO.

When there is no influence upon the microcontroller actions, DO may be OPEN.

If DO is OPEN, and at timing to output status READY, at timing of CS = "H", SK = "H", DI = "H", EEPROM recognizes this as a start bit, resets READY output, and DO = "High-Z", therefore, READY signal cannot be detected. To avoid such output, pull up DO pin for improvement.

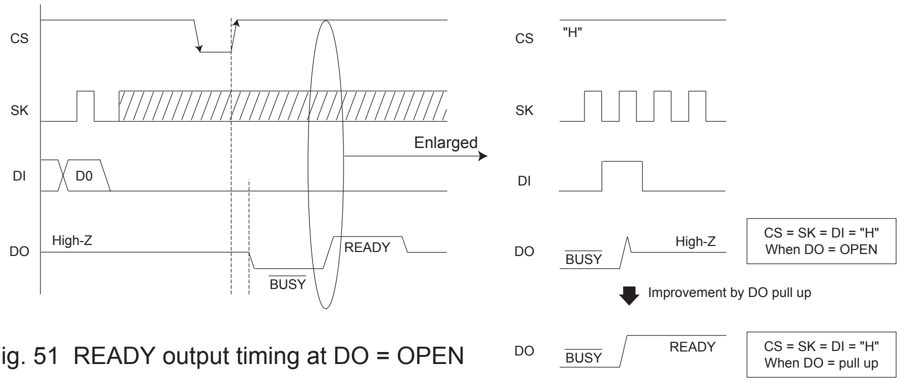


Fig. 51 READY output timing at DO = OPEN

○ Pull up resistance Rpu and pull down resistance Rpd of DO pin

As for pull up and pull down resistance value, select an appropriate value to this resistance value from microcontroller VIH, VIL, and VOH, IOH, VOL, IOL characteristics of this IC.

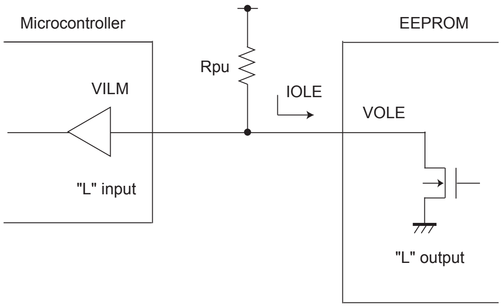


Fig. 52 DO pull up resistance

$$\mathrm{Rpu} \geq \frac{\mathrm{V_{CC}\text{-}VOLE}}{\mathrm{IOLE}} \quad \cdots ③$$

$$\mathrm{VOLE} \leq \mathrm{VILM} \quad \cdots ④$$

Example) When Vcc = 5V, VOLE = 0.4V, IOLE = 2.1mA, VILM = 0.8V, from the equation ③,

$$\mathrm{Rpu} \geq \frac{5\text{-}0.4}{2.1\times10^{-3}}$$

$$\therefore \quad \mathrm{Rpu} \geq 2.2\ (\mathrm{K}\Omega)$$

With the value of Rpu to satisfy the above equation, VOLE becomes 0.4V or below, and with VILM (= 0.8V), the equation ④ is also satisfied.

- VOLE : EEPROM VOL specifications
- IOLE : EEPROM IOL specifications
- VILM : Microcontroller VIL specifications

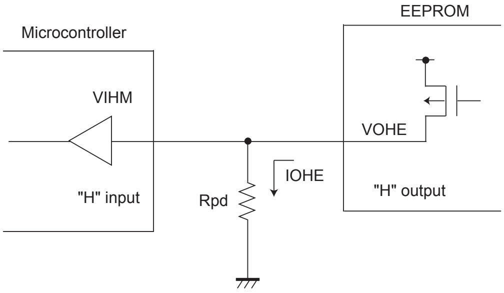


Fig. 53 DO pull down resistance

$$\mathrm{Rpd} \geq \frac{\mathrm{VOHE}}{\mathrm{IOHE}} \quad \cdots ⑤$$

$$\mathrm{VOHE} \geq \mathrm{VIHM} \quad \cdots ⑥$$

Example) When Vcc = 5V, VOHE = Vcc - 0.2V, IOHE = 0.1mA, VIHM = Vcc × 0.7V from the equation⑤ ,

$$\mathrm{Rpd} \geq \frac{5\text{-}0.2}{0.1\times10^{-3}}$$

$$\therefore \quad \mathrm{Rpd} \geq 48\ (\mathrm{K}\Omega)$$

With the value of Rpd to satisfy the above equation, VOHE becomes 2.4V or below, and with VIHM (= 3.5V), the equation ⑥ is also satisfied.

- VOHE : EEPROM VOH specifications
- IOHE : EEPROM IOH specifications
- VIHM : Microcontroller VIH specifications

5) READY / $\overline{\text{BUSY}}$ status display (DO terminal) (common to BR93L46-W, BR93L56-W, BR93L66-W, BR93L76-W, BR93L86-W)

This display outputs the internal status signal. When CS is started after tCS (Min. 200ns) from CS fall after write command input, "H" or "L" is output.

R/$\overline{\text{B}}$ display = "L" ($\overline{\text{BUSY}}$) = write under execution
(D0 status)

After the timer circuit in the IC works and creates the period of tE/W, this time circuit completes automatically. And write to the memory cell is made in the period of tE/W, and during this period, other command is not accepted.

R/$\overline{\text{B}}$ display = "H" (READY) = command wait status
(D0 status)

Even after tE/W (Max. 5ms) from write of the memory cell, the following command is accepted. Therefore, CS = "H" in the period of tE/W, and when input is in SK, DI, malfunction may occur, therefore, DI = "L" in the area CS = "H". (Especially, in the case of shared input port, attention is required.)

* Do not input any command while status signal is output. Command input in $\overline{\text{BUSY}}$ area is cancelled, but command input in READY area is accepted. Therefore, status READY output is cancelled, and malfunction and mistake write may be made.

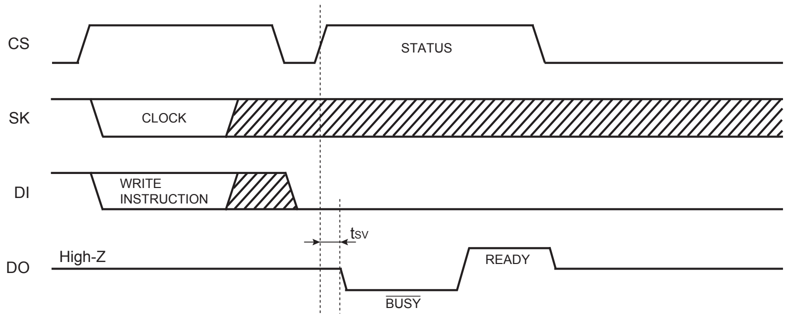


Fig. 54 R/$\overline{\text{B}}$ status output timing chart

6) When to directly connect DI and DO

This IC has independent input terminal DI and output terminal DO, and separate signals are handled on timing chart, meanwhile, by inserting a resistance R between these DI and DO terminals, it is possible to carry out control by 1 control line.

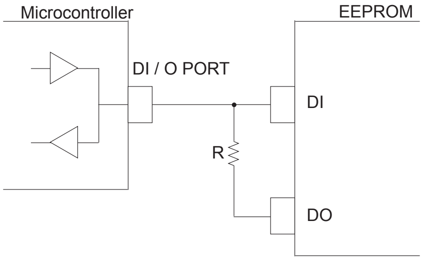


Fig. 55 DI, DO control line common connection

○ Data collision of microcontroller DI/O output and DO output and feedback of DO output to DI input

Drive from the microcontroller DI/O output to DI input on I/O timing, and signal output from DO output occur at the same time in the following points.

(1) 1 clock cycle to take in A0 address data at read command
Dummy bit "0" is output to DO terminal.
→When address data A0 = "1" input, through current route occurs.

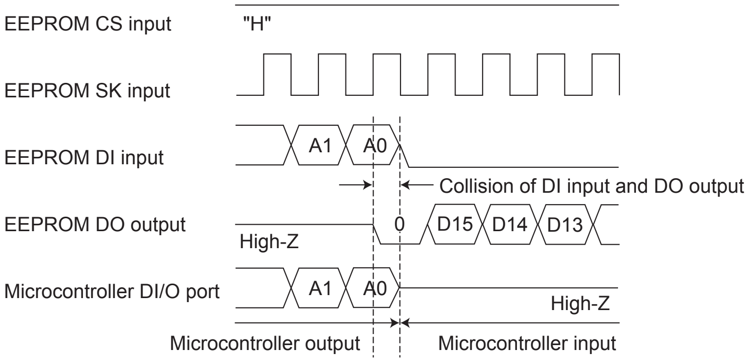


Fig. 56 Collision timing at read data output at DI, DO direct connection

(1) Timing of CS = "H" after write command. DO terminal in READY / BUSY function output.
When the next start bit input is recognized, "HIGH-Z" gets in.
→Especially, at command input after write, when CS input is started with microcontroller DI/O output "L",
READY output "H" is output from DO terminal, and through current route occurs.

Feedback input at timing of these (1) and (2) does not cause disorder in basic operations, if resistance R is inserted.

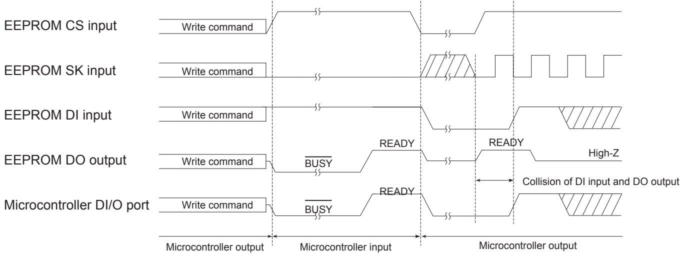


Fig. 57 Collision timing at DI, DO direct connection

Note) As for the case (2), attention must be paid to the following.
When status READY is output, DO and DO are shared, DI = "H" and the microcontroller DI/O = "High-Z" or the microcontroller DI/O = "H", if SK clock is input, DO output is input to DI and is recognized as a start bit, and malfunction may occur. As a method to avoid malfunction, at status READY output, set SK = "L", or start CS within 4 clocks after "H" of READY signal is output.

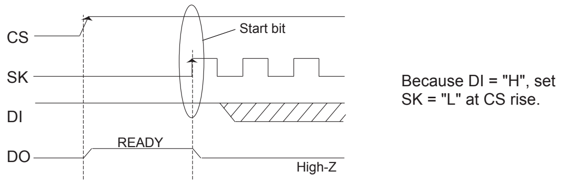


Fig. 58 Start bit input timing at DI, DO direct connection

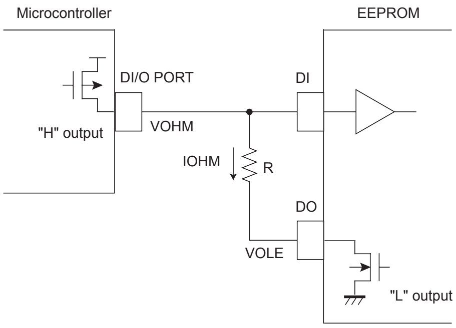
○Selection of resistance value R

The resistance R becomes through current limit resistance at data collision. When through current flows, noises of power source line and instantaneous stop of power source may occur. When allowable through current is defined as I, the following relation should be satisfied. Determine allowable current amount in consideration of impedance and so forth of power source line in set. And insert resistance R, and set the value R to satisfy EEPROM input level VIH/VIL even under influence of voltage decline owing to leak current and so forth. Insertion of R will not cause any influence upon basic operations.

(1) Address data A0 = "1" input, dummy bit "0" output timing

(When microcontroller DI/O output is "H", EEPROM DO outputs "L", and "H" is input to DI)

- Make the through current to EEPROM 10mA or below.
- See to it that the input level VIH of EEPROM should satisfy the following.



Conditions

$$VOHM \leq VIHE$$

$$VOHM \leq IOHM \times R + VOLE$$

At this moment, if VOLE = 0V,

$$VOHM \leq IOHM \times R$$

$$\therefore \quad R \geq \frac{VOHM}{IOHM} \quad \cdots ⑦$$

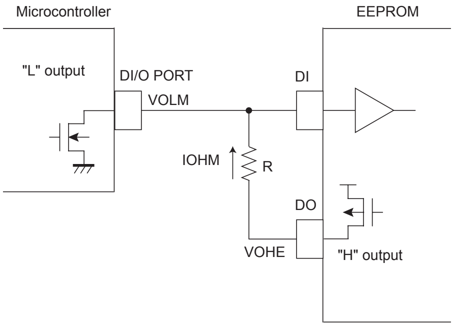
- VIHE : EEPROM VIH specifications
- VOLE : EEPROM VOL specifications
- VOHM : Microcontroller VOH specifications
- IOHM : Microcontroller IOH specifications

Fig. 59 Circuit at DI, DO direct connection (Microcontroller DI/O "H" output, EEPROM "L" output)

(2) DO status READY output timing

(When the microcontroller DI/O is "L", EEPROM DO outputs "H", and "L" is input to DI)

- Set the EEPROM input level VIL so as to satisfy the following.



Conditions

$$VOLM \geq VILE$$

$$VOLM \geq VOHE - IOLM \times R$$

At this moment, VOHE=V_{CC},

$$VOLM \geq V_{CC} - IOLM \times R$$

$$\therefore \quad R \geq \frac{V_{CC} - VOLM}{IOLM} \quad \cdots ⑧$$

- VILE : EEPROM VIL specifications
- VOHE : EEPROM VOH specifications
- VOLM : Microcontroller VOL specifications
- IOLM : Microcontroller IOL specifications

Fig. 60 Circuit at DI, DO direct connection (Microcontroller DI/O "L" output, EEPROM "H" output)

Example) When Vcc = 5V, VOHM = 5V, IOHM = 0.4mA, VOLM = 5V, IOLM = 0.4mA,

From the equation ⑦,

$$R \geq \frac{VOHM}{IOHM}$$

$$R \geq \frac{5}{0.4\times10^{-3}}$$

$$\therefore \quad R \geq 12.5\ [k□] \quad \cdots ⑨$$

From the equation ⑧,

$$R \geq \frac{V_{CC} - VOLM}{IOLM}$$

$$R \geq \frac{5 - 0.4}{2.1\times10^{-3}}$$

$$\therefore \quad R \geq 2.2\ [k□] \quad \cdots ⑩$$

Therefore, from the equations ⑨ and ⑩,

$$\therefore \quad R \geq 12.5\ [k□]$$

7) Notes on power ON/OFF

- At power ON/OFF, set CS "L".

When CS is "H", this IC gets in input accept status (active). If power is turned on in this status, noises and the likes may cause malfunction, mistake write or so. To prevent these, at power ON, set CS "L". (When CS is in "L" status, all inputs are cancelled.) And at power decline, owing to power line capacity and so forth, low power status may continue long. At this case too, owing to the same reason, malfunction, mistake write may occur, therefore, at power OFF too, set CS "L".

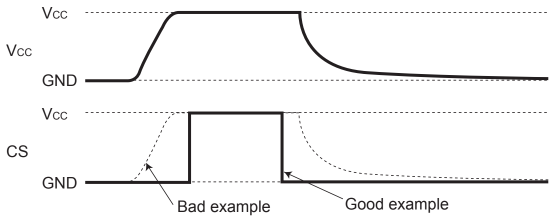


Fig. 61 Timing at power ON/OFF

(Bad example) CS pin is pulled up to Vcc.

In this case, CS becomes "H" (active status), and EEPROM may have malfunction, mistake write owing to noises and the likes.
Even when CS input is High-Z, the status becomes like this case, which please note.

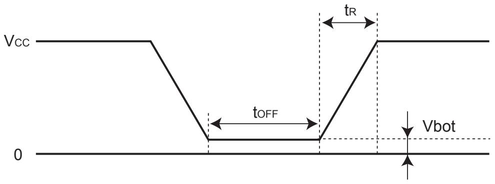
(Good example) It is "L" at power ON/OFF.

Set 10ms or higher to recharge at power OFF.
When power is turned on without observing this condition, IC internal circuit may not be reset, which please note.

○POR circuit

This IC has a POR (Power On Reset) circuit as mistake write countermeasure.
After POR action, it gets in write disable status. The POR circuit is valid only when power is ON, and does not work when power is OFF. However, if CS is "H" at power ON/OFF, it may become write enable status owing to noises and the likes.
For secure actions, observe the following conditions.

1 Set CS = "L".
2 Turn on power so as to satisfy the recommended conditions of tR, tOFF, Vbot for POR circuit action.



Recommended conditions of t_R, t_{OFF}, Vbot

t_R	t_{OFF}	Vbot
10ms or below	10ms or higher	0.3V or below
100ms or below	10ms or higher	0.2V or below

Fig. 62 Rise waveform diagram

○LVCC circuit

LVCC (Vcc - Lockout) circuit prevents data rewrite action at low power, and prevents wrong write.
At LVCC voltage (Typ. = 1.2V) or below, it prevent data rewrite.

8) Noise countermeasures

○Vcc noise (bypass capacitor)

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a by pass capacitor (0.1μF) between IC Vcc and GND, At that moment, attach it as close to IC as possible.
And, it is also recommended to attach a bypass capacitor between board Vcc and GND.

○SK noise

When the rise time (tR) of SK is long, and a certain degree or more of noise exists, malfunction may occur owing to clock bit displacement. To avoid this, a Schmitt trigger circuit is built in SK input. the hysteresis width of this circuit is set about 0.2V, if noises exist at SK input, set the noise amplitude 0.2Vp-p or below.
And it is recommended to set the rise time (tR) of SK 100ns or below. In the case when the rise time is 100ns or higher, take sufficient noise countermeasures. Make the clock rise, fall time as small as possible.

●Cautions on use

(1) Described numeric values and data are design representative values, and the values are not guaranteed.

(2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.

(3) Absolute Maximum Ratings
If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(4) GND electric potential
Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is not lower than that of GND terminal in consideration of transition status.

(5) Heat design
In consideration of allowable loss in actual use condition, carry out heat design with sufficient margin.

(6) Terminal to terminal shortcircuit and wrong packaging
When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

(7) Use in a strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently.

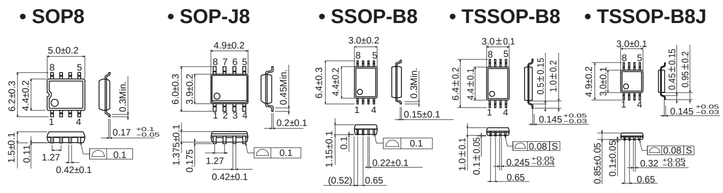
● Selection of order type

BR	93	L	46	F	-	W	E2
ROHM type name	BUS type 93 : Microwire	Operating temperature L : −40℃～＋85℃ A : −40℃～＋105℃ H : −40℃～＋125℃	Capacity Microwire BUS 46=1K 56=2K 66=4K 76=8K 86=16K	Package type F : SOP8 FJ : SOP-J8 RF : SOP8 RFJ : SOP-J8 FV : SSOP-B8 RFV : SSOP-B8 FVT : TSSOP-B8 RFVT : TSSOP-B8 RFVM : MSOP8 RFVJ : TSSOP-B8J		Double cell	Taping type name E2 : reel shape emboss taping TR : reel shape emboss taping (MSOP8 package only)

● Package specifications

SOP8/SOP-J8/SSOP-B8/TSSOP-B8/TSSOP-B8J

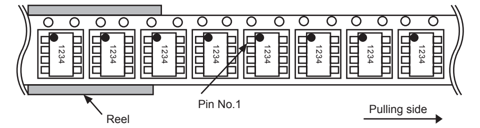
<External appearance>



(Unit : mm)

<Package specifications>

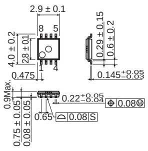
Package type	Emboss taping
Package quantity	2500pcs
Package direction	E2 (When the reel is gripped by the left hand, and the tape is pulled out by the right hand, No.1 pin of the product is at the left top.)



* For ordering, specify a number of multiples of the package quantity.

MSOP8

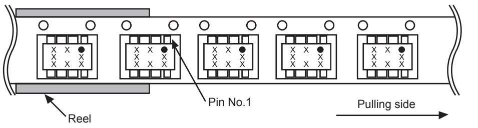
<External appearance>



(Unit : mm)

<Package specifications>

Package type	Emboss taping
Package quantity	3000pcs
Package direction	TR (When the reel is gripped by the left hand, and the tape is pulled out by the right hand, No.1 pin of the product is at the right top.)



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