

AS1106, AS1107

8-Digit LED Display Drivers

Data Sheet

1 General Description

The AS1106 and the AS1107 are compact display drivers for 7-segment numeric displays of up to 8 digits. The devices can be programmed via SPI, QSPI, and Microwire as well as a conventional 4-wire serial interface.

The devices include an integrated BCD code-B/HEX decoder, multiplex scan circuitry, segment and display drivers, and a 64-bit memory. Internal memory stores the LED settings, eliminating the need for continuous device reprogramming.

Every segment can be individually addressed and updated separately. Only one external resistor (R_{SET}) is required to set the current through the LED display. LED brightness can be controlled by analog or digital means. The devices can be programmed to use the internal code-B/HEX decoder to display numeric digits or to directly address each segment.

The AS1106 and the AS1107 feature an extremely low shutdown current of typically $3\mu A$, and an operational current of less than $500\mu A$. The number of digits can be programmed, the devices can be reset by software, and an external clock is also supported. Additionally, segment blinking can be synchronized across multiple drivers.

Several test modes are available for easy application debugging.

The devices are available in 24-pin DIP and 24-pin SOIC packages.

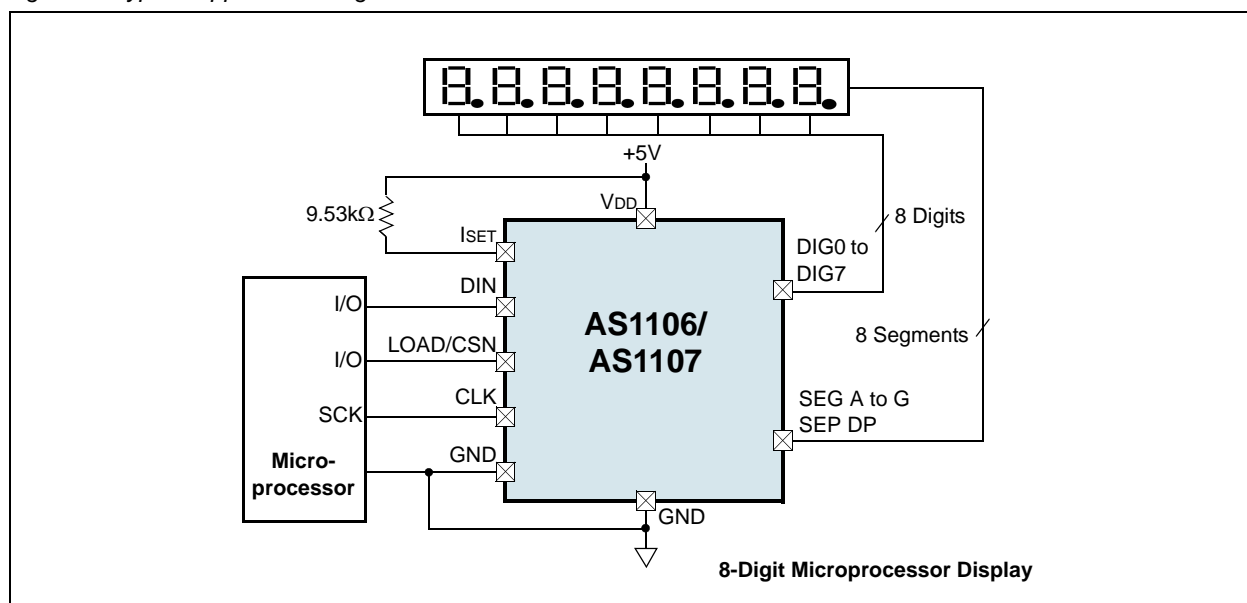
2 Key Features

- 10MHz SPI-, QSPI-, Microwire-Compatible Serial I/O
- Individual LED Segment Control
- Segment Blinking Control (can be synchronized across multiple drivers)
- Hexadecimal- or BCD-Code/No-Decode Digit Selection
- $3\mu A$ Low-Power Shutdown Current (typ; data retained)
- Extremely Low Operating Current 0.5mA in Open-Loop
- Digital and Analog Brightness Control
- Display Blanked on Power-Up
- Drive Common-Cathode LED Displays
- Low-EMI Low Slew-Rate Limited Segment Drivers (AS1107)
- Supply Voltage Range: 2.7 to 5.5V
- Software Reset
- Optional External Clock
- Packages:
 - 24-pin DIP
 - 24-pin SOIC

3 Applications

The AS1106 and AS1107 are ideal for bar-graph displays, instrument-panel meters, LED matrix displays, dot matrix displays, set-top boxes, white goods, professional audio equipment, medical equipment, industrial controllers and panel meters.

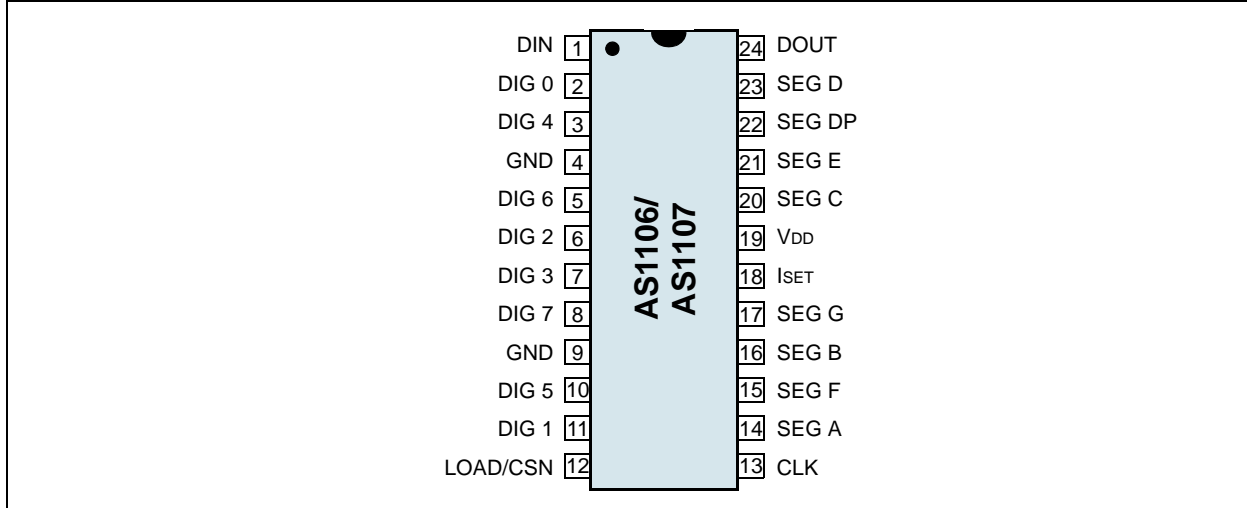
Figure 1. Typical Application Diagram



4 Pinout

Pin Assignments

Figure 2. DIP and SO Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Number	Description
DIN	1	Serial-Data Input. Data is loaded into the internal 16-bit shift register on the rising edge of pin CLK.
DIG 0: DIG 7	2, 3, 5, 6, 7, 8, 10, 11	Digit Drive Lines. 8 Eight-digit drive lines that sink current from the display common cathode. The AS1106 pulls the digit outputs to VDD when turned off. The AS1107 digit drivers are high-impedance when turned off.
GND	4, 9	Ground. Both GND pins must be connected.
LOAD/CSN	12	Load-Data Input (AS1106 only). The last 16 bits of serial data are latched on the rising edge of this pin. Chip-Select Input (AS1107 or AS1106 SPI-enabled only). Serial data is loaded into the shift register while this pin is low. The last 16 bits of serial data are latched on the rising edge of this pin.
CLK	13	Serial-Clock Input. 10MHz maximum rate. Data is shifted into the internal shift register on the rising edge of this pin. Data is clocked out of pin DOUT on the falling edge of this pin. On the AS1107 or AS1106 SPI-enabled, the CLK input is active only while LOAD/CSN is low.
SEG A: SEG G, SEG DP	14, 15, 16, 17, 20, 21, 22, 23	Seven Segment and Decimal Point Drive Lines. 8 seven-segment drives and decimal point drive that source current to the display. On the AS1106, when a segment driver is turned off it is pulled to GND. The AS1107 segment drivers are high-impedance when turned off.
ISET	18	Set Segment Current. Connect to VDD through RSET to set the peak segment current (see Selecting RSET Resistor Value and Using External Drivers on page 14).
VDD	19	Positive Supply Voltage. Connect to +2.7 to +5.5V supply.
DOUT	24	Serial-Data Output. The data into pin DIN is valid at pin DOUT 16.5 clock cycles later. This pin is used to daisy-chain several AS1106/AS1107 devices and is never high-impedance.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter		Min	Max	Units	Notes
Voltage (with respect to GND)	V _{DD}	-0.3	7	V	
	All other pins	-0.3	7 or V _{DD} + 0.3	V	
Current	DIG 0:DIG 7 Sink Current		500	mA	
	SEG A:SEG G, SEG DP		100	mA	
Continuous Power Dissipation (T _{AMB} = +85°C)	Narrow plastic DIP		1066	mW	Derate 13.3mW/°C above +70°C
	Wide SOIC		941	mW	Derate 11.8mW/°C above +70°C
Operating Temperature Ranges (T _{MIN} to T _{MAX})	AS1106PL, AS1106WL	0	+70	°C	
	AS1106PE, AS1106WE	-40	+85	°C	
	AS1107PL, AS1107WL	-40	+85	°C	
Storage Temperature Range		-65	+150	°C	
Package Body Temperature (Wide SOIC) ¹			+260	°C	
Soldering Temperature (Narrow DIP) ²			+260	°C	
Humidity		5	85	%	Non-condensing
Electrostatic Discharge ³	Digital outputs		1000	V	
	All other pins		1000	V	
Latch-Up Immunity ⁴			±200	mA	All pins except AS1106 pin 14: ±180 mA

1. The reflow peak soldering temperature (body temperature) is specified according to *IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for non-hermetic Solid State Surface Mount Devices"*.

2. Specified according *JESD22-B106 "Resistance to Soldering Temperature for Through-Hole Mounted Devices"*.

3. Norm: *MIL 883 E method 3015*.

4. Norm: *JEDEC 17*.

6 Electrical Characteristics

Conditions: $V_{DD} = 2.7$ to $5.5V$, $R_{SET} = 9.53k\Omega \pm 1\%$, $T_{AMB} = T_{MIN}$ to T_{MAX} (unless otherwise specified).

Table 3. Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Supply Voltage	V_{DD}		2.7	5.0	5.5	V
Shutdown Supply Current	I_{DDSD}	All digital inputs at V_{DD} or GND, $T_{AMB} = +25^{\circ}C$			10	μA
Operating Supply Current	I_{DD}	$R_{SET} =$ open circuit.			1	mA
		All segments and decimal point on; $I_{SEG} = -40mA$.		330		
Display Scan Rate	fosc	8 digits scanned	500	800	1300	Hz
Digit Drive Sink Current	I_{DIGIT}	$V_{OUT} = 0.65V$	320			mA
Segment Drive Source Current	I_{SEG}	$V_{DD} = 5.0V$, $V_{OUT} = (V_{DD} - 1V)$	-30	-40	-45	mA
Segment Current Slew Rate (AS1107 only)	$\Delta I_{SEG}/\Delta t$	$T_{AMB} = +25^{\circ}C$, $V_{DD} = 5.0V$, $V_{OUT} = (V_{DD} - 1V)$	10	20	50	mA/ μs
Segment Drive Current Matching	ΔI_{SEG}			3.0		%
Digit Drive Leakage (AS1107 only)	I_{DIGIT}	Digit off, $V_{DIGIT} = V_{DD}$			-10	μA
Segment Drive Leakage (AS1107 only)	I_{SEG}	Segment off, $V_{SEG} = 0V$			1	μA
Digit Drive Source Current (AS1106 only)	I_{DIGIT}	Digit off, $V_{DIGIT} = (V_{DD} - 0.3V)$	-2			mA
Segment Drive Sink Current (AS1106 only)	I_{SEG}	Segment off, $V_{SEG} = 0.3V$	5			mA
Slow Segment Blink Period (ON phase, Internal Oscillator)	$t_{SLOWBLINK}$		0.64	1	1.65	s
Fast Segment Blink Period (ON phase, Internal Oscillator)	$t_{FASTBLINK}$		0.32	0.5	0.83	s
Fast or Slow Segment Blink Duty Cycle (Guaranteed by design)			49.9	50	50.1	%

Table 4. Logic Inputs/Outputs Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Current DIN, CLK, LOAD/CSN	I_{IH} , I_{IL}	$V_{IN} = 0V$ or V_{DD}	-1		1	μA
Logic High Input Voltage	V_{IH}		$0.7 \times V_{DD}$			V
Logic Low Input Voltage	V_{IL}	$V_{DD} = 5.0V \pm 10\%$			0.8	V
		$V_{DD} = 3.0V \pm 10\%$			0.6	V
Output High Voltage	V_{OH}	D_{OUT} , $I_{SOURCE} = -1mA$, $V_{DD} = 5.0V \pm 10\%$	$V_{DD} - 1$			V
		D_{OUT} , $I_{SOURCE} = -1mA$, $V_{DD} = 3.0V \pm 10\%$	$V_{DD} - 0.5$			V
Output Low Voltage	V_{OL}	D_{OUT} , $I_{SINK} = 1.6mA$			0.4	V
Hysteresis Voltage	ΔV_I	DIN, CLK, LOAD/CSN		1		V

Table 5. Timing Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CLK Clock Period	tCP		100			ns
CLK Pulse Width High	tCH		50			ns
CLK Pulse Width Low	tCL		50			ns
CSM Fall to CLK Rise Setup Time (AS1107 or AS1106 SPI-programmed)	tcSS		25			ns
CLK Rise to LOAD/CSN Rise Hold Time	tCSH		0			ns
DIN Setup Time	tDS		25			ns
DIN Hold Time	tDH		0			ns
Output Data Propagation Delay	tDO	C _{LOAD} = 50pF			25	ns
LOAD Rising Edge to Next Clock Rising Edge (AS1106 only)	tLDCK		50			ns
Minimum LOAD/CSN Pulse High	tCSW		50			ns
Data-to-Segment Delay	tDSPD				2.25	ms

Note: See Figure 12 on page 8 for more information.

7 Typical Operating Characteristics

$V_{DD} = 5V$, $R_{SET} = 9.53k\Omega$, $T_{AMB} = 25^{\circ}C$ (unless otherwise specified).

Figure 3. Scan Frequency vs. Temperature

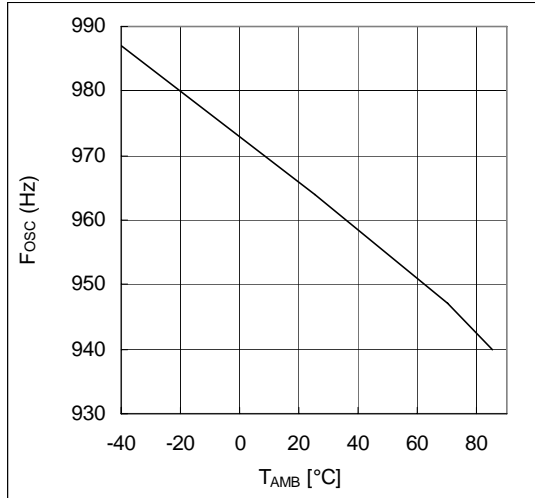


Figure 4. Scan Frequency vs. V_{DD}

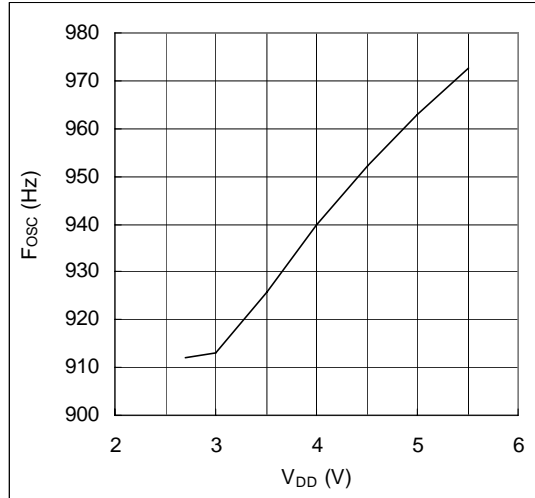


Figure 5. I_{SEG} vs. Temperature

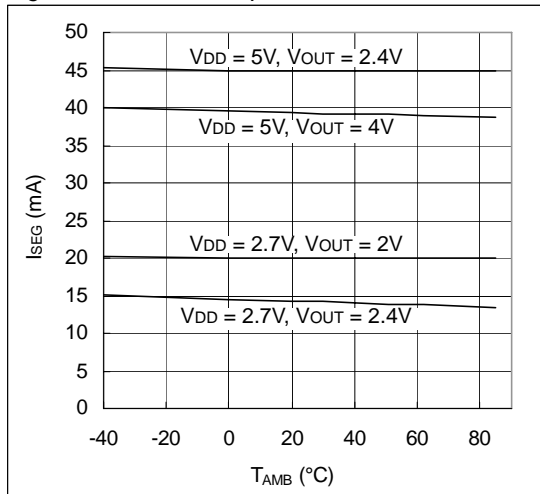


Figure 6. I_{SEG} vs. V_{DD}

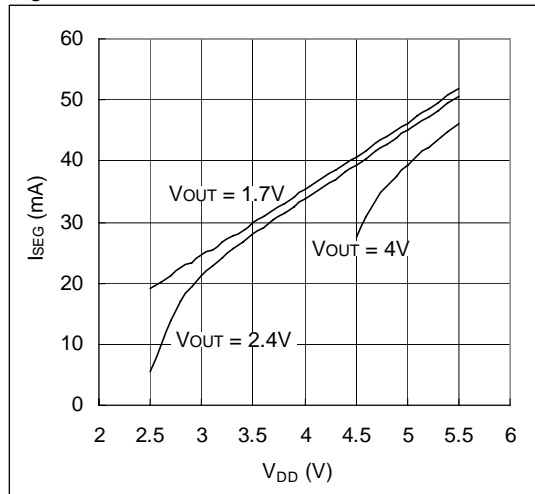


Figure 7. AS1106 Segment Output Current

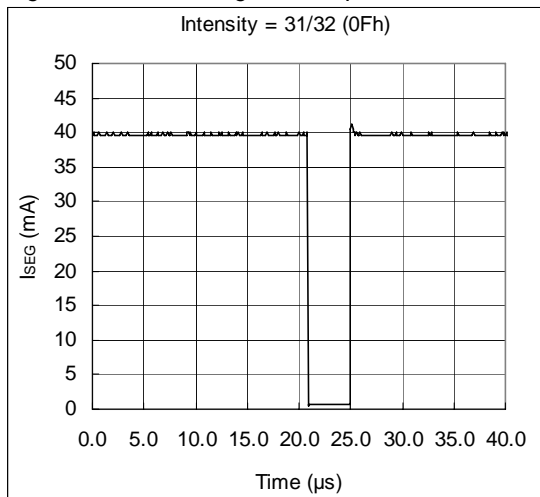


Figure 8. AS1107 Segment Output Current

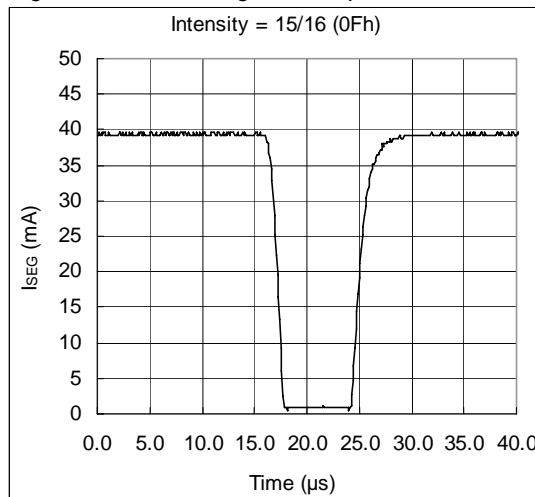


Figure 9. I_{SEG} vs. V_{OUT}

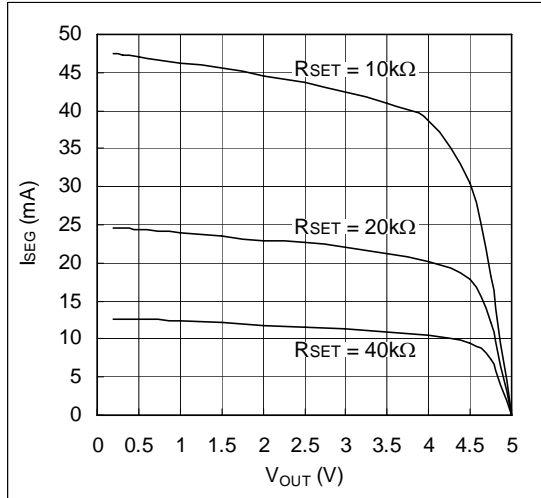


Figure 10. I_{SEG} vs. V_{OUT}

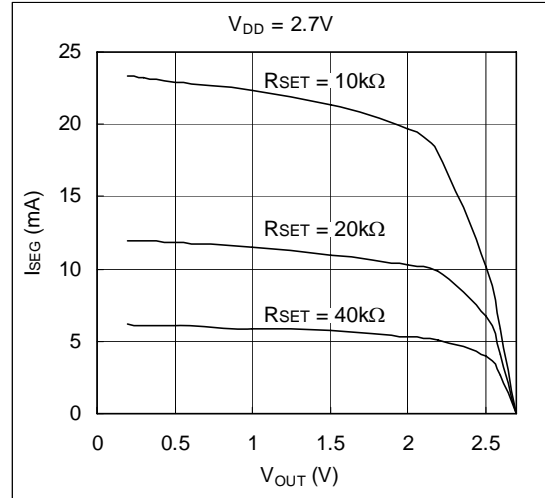
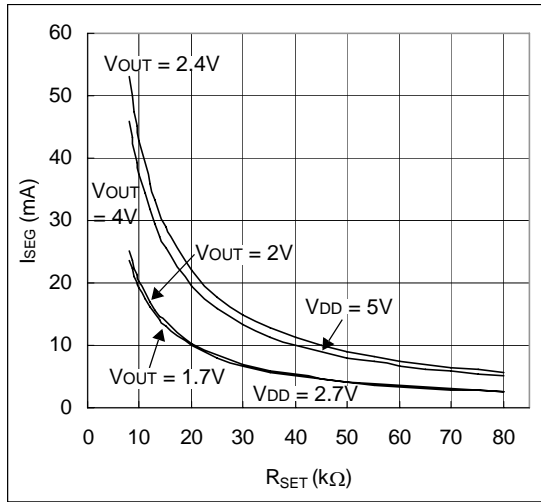


Figure 11. I_{SEG} vs. R_{SET}



8 Detailed Description

AS1106 vs. AS1107

The AS1106 and AS1107 are identical except for two features:

- The AS1107 segment drivers are slew-rate limited to reduce electromagnetic interference (EMI).
- The AS1107 serial interface is fully SPI compatible (programmable for AS1106).

Serial-Addressing Format

Programming the AS1106/AS1107 is done by writing to the device's internal registers (see Digit- and Control-Registers on page 9) via the 4-wire serial interface. A programming sequence consists of 16-bit packages as listed in Table 6.

The data is shifted into the internal 16-bit register with the rising edge of the CLK signal. With the rising edge of the LOAD/CSN signal the data is latched into a digit- or control-register. The LOAD/CSN signal must go high after the 16th rising clock edge.

The LOAD/CSN signal can also come later but this must happen just before the next rising edge of CLK, otherwise the data will be lost. The contents of the internal shift register are applied 16.5 clock cycles later to pin DOUT. The data is clocked out at the falling edge of CLK.

The first 4 bits (D15:D12) are "don't care", bits D11:D8 contain the register address, and bits D7:D0 contain the data. The first bit is D15, the most significant bit (MSB). The exact timing is shown in Figure 12.

Table 6. 16-Bit Serial Data Format

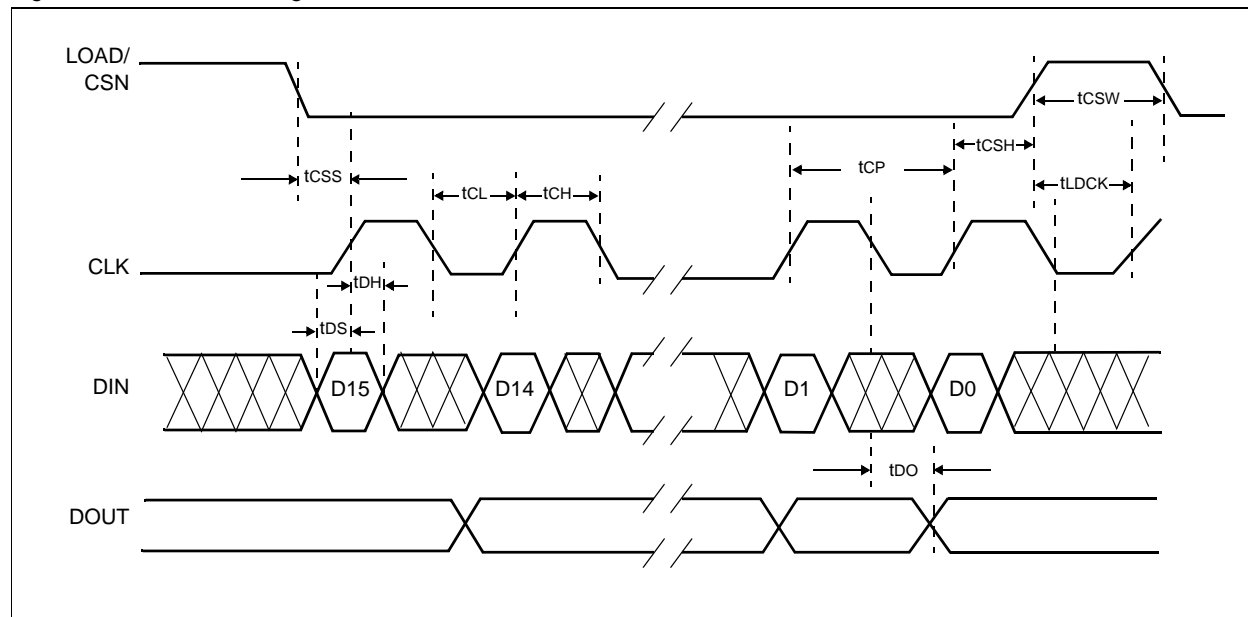
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	X	Register Address (see Table 7)				MSB				Data				LSB

Initial Power-Up

On initial power-up, the AS1106/AS1107 registers are reset to their default values, the display is blanked, and the device goes into shutdown mode. At this time, all registers should be programmed for normal operation.

Note: The default settings enable only scanning of one digit; the internal decoder is disabled and the Intensity Control Register (see page 12) is set to the minimum values.

Figure 12. Interface Timing



Shutdown Mode

The AS1106/AS1107 devices feature a shutdown mode, where they consume only 10µA (max) current. Shutdown mode is entered via a write to the Shutdown Register (see Table 8). For the AS1106, at that point, all segment current sources are pulled to ground and all digit drivers are connected to V_{DD}, so that all segments are blanked. The AS1107 behavior is identical except the drivers are high impedance.

Note: During shutdown mode the Digit-Registers maintain their data.

Shutdown mode can either be used as a means to reduce power consumption or for generating a flashing display (repeatedly entering and leaving shutdown mode). For minimum supply current in shutdown mode, logic input should be at GND or V_{DD} (CMOS logic level).

The devices need typically 250µs to exit shutdown mode, and during shutdown mode the AS1106/AS1107 is fully programmable. Only the display test mode (see page 11) overrides shutdown mode.

When entering or leaving shutdown mode, the Feature Register is reset to its default values (all 0s) when Shutdown Register bit D7 (page 10) = 0.¹

Note: If the AS1106/AS1107 is used with an external clock, Shutdown Register bit D7 should be set to 1 when writing to the Shutdown Register.

Digit- and Control-Registers

The AS1106/AS1107 devices contain 8 Digit-Registers and 6 control-registers, which are listed in Table 7. All registers are selected using a 4-bit address word, and communication is done via the serial interface.

- Digit Registers – These registers are realized with an on-chip 64-bit memory. Each digit can be controlled directly without rewriting the whole register contents.
- Control Registers – These registers consist of decode mode, display intensity, number of scanned digits, shutdown, display test and features selection registers.

Table 7. Register Address Map

Register	HEX Code	Address					Page
		D15:D12	D11	D10	D9	D8	
No-Op	0xX0	X	0	0	0	0	13
Digit 0	0xX1	X	0	0	0	1	N/A
Digit 1	0xX2	X	0	0	1	0	N/A
Digit 2	0xX3	X	0	0	1	1	N/A
Digit 3	0xX4	X	0	1	0	0	N/A
Digit 4	0xX5	X	0	1	0	1	N/A
Digit 5	0xX6	X	0	1	1	0	N/A
Digit 6	0xX7	X	0	1	1	1	N/A
Digit 7	0xX8	X	1	0	0	0	N/A
Decode-Mode	0xX9	X	1	0	0	1	10
Intensity Control	0xXA	X	1	0	1	0	12
Scan Limit	0xXB	X	1	0	1	1	12
Shutdown	0xXC	X	1	1	0	0	10
N/A	0xXD	X	1	1	0	1	N/A
Feature	0xXE	X	1	1	1	0	13
Display Test	0xFF	X	1	1	1	1	11

1. When Shutdown Register bit D7 = 1, the Feature Register is left unchanged when entering or leaving shutdown mode.

Shutdown Register (0xXC)

The Shutdown Register controls AS1106/AS1107 shutdown mode (see Shutdown Mode on page 9).

Table 8. Shutdown Register Format (Address (HEX) = 0xXC))

Mode	HEX Code	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Shutdown Mode, Reset Feature Register to Default Settings	0x00	0	X	X	X	X	X	X	0
Shutdown Mode, Feature Register Unchanged	0x80	1	X	X	X	X	X	X	0
Normal Operation, Reset Feature Register to Default Settings	0x01	0	X	X	X	X	X	X	1
Normal Operation, Feature Register Unchanged	0x81	1	X	X	X	X	X	X	1

Decode Enable Register (0xX9)

The Decode Enable Register sets the decode mode. BCD/HEX decoding (either BCD code – characters 0:9, E, H, L, P, and -, or HEX code – characters 0:9 and A:F) is selected by bit D2 (page 13) of the Feature Register. The Decode Enable Register is used to select the decode mode or no-decode for each digit. Each bit in the Decode Enable Register corresponds to its respective display digit (i.e., bit D0 corresponds to digit 0, bit D1 corresponds to digit 1 and so on). Table 10 lists some examples of the possible settings for the Decode Enable Register bits.

Note: A logic high enables decoding and a logic low bypasses the decoder altogether.

When decode mode is used, the decoder looks only at the lower-nibble (bits D3:D0) of the data in the Digit-Registers, disregarding bits D6:D4. Bit D7 sets the decimal point (SEG DP) independent of the decoder and is positive logic (bit D7 = 1 turns the decimal point on). Table 10 lists the code-B font; Table 11 lists the HEX font.

When no-decode mode is selected, data bits D7:D0 of the Digit-Registers correspond to the segment lines of the AS1106/AS1107. Table 12 shows the 1:1 pairing of each data bit to the appropriate segment line.

Table 9. Decode Enable Register Format (Address (HEX) = 0xX9))

Decode Mode	HEX Code	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
No decode for digits 7:0	0x00	0	0	0	0	0	0	0	0
Code-B/HEX decode for digit 0. No decode for digits 7:1	0x01	0	0	0	0	0	0	0	1
Code-B/HEX decode for digits 3:0. No decode for digits 7:4	0x0F	0	0	0	0	1	1	1	1
Code-B/HEX decode for digits 7:0	0xFF	1	1	1	1	1	1	1	1

Figure 13. Standard 7-Segment LED Intensity Control and Inter-Digit Blanking

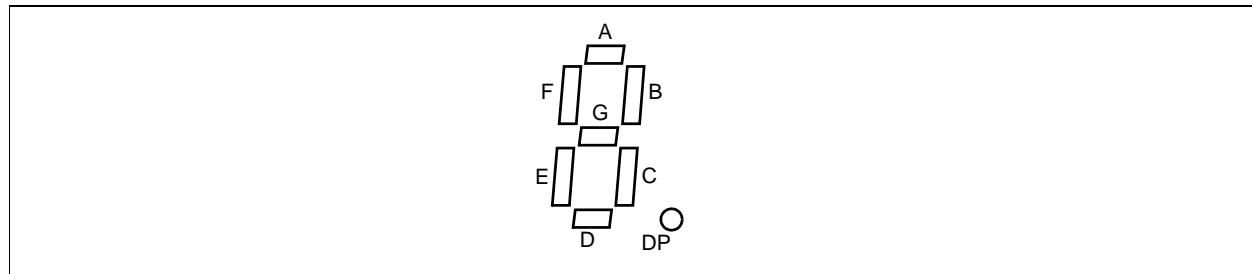


Table 10. Code-B Font

7-Segment Character	Register Data							On Segments = 1						
	D7 [†]	D6:D4	D3	D2	D1	D0	DP [†]	A	B	C	D	E	F	G
0		X	0	0	0	0		1	1	1	1	1	1	0
1		X	0	0	0	1		0	1	1	0	0	0	0
2		X	0	0	1	0		1	1	0	1	1	0	1
3		X	0	0	1	1		1	1	1	1	0	0	1
4		X	0	1	0	0		0	1	1	0	0	1	1

Table 10. Code-B Font (Continued)

7-Segment Character	Register Data							On Segments = 1						
	D7 [†]	D6:D4	D3	D2	D1	D0	DP [†]	A	B	C	D	E	F	G
5		X	0	1	0	1		1	0	1	1	0	1	1
6		X	0	1	1	0		1	0	1	1	1	1	1
7		X	0	1	1	1		1	1	1	0	0	0	0
8		X	1	0	0	0		1	1	1	1	1	1	1
9		X	1	0	0	1		1	1	1	1	0	1	1
-		X	1	0	1	0		0	0	0	0	0	0	1
E		X	1	0	1	1		1	0	0	1	1	1	1
H		X	1	1	0	0		0	1	1	0	1	1	1
L		X	1	1	0	1		0	0	0	1	1	1	0
P		X	1	1	1	0		1	1	0	0	1	1	1
Blank		X	1	1	1	1		0	0	0	0	0	0	0

[†] The decimal point is enabled by setting bit D7 = 1.

Table 11. HEX Font

7-Segment Character	Register Data							On Segments = 1						
	D7 [†]	D6:D4	D3	D2	D1	D0	DP [†]	A	B	C	D	E	F	G
0		X	0	0	0	0		1	1	1	1	1	1	0
1		X	0	0	0	1		0	1	1	0	0	0	0
2		X	0	0	1	0		1	1	0	1	1	0	1
3		X	0	0	1	1		1	1	1	1	0	0	1
4		X	0	1	0	0		0	1	1	0	0	1	1
5		X	0	1	0	1		1	0	1	1	0	1	1
6		X	0	1	1	0		1	0	1	1	1	1	1
7		X	0	1	1	1		1	1	1	0	0	0	0
8		X	1	0	0	0		1	1	1	1	1	1	1
9		X	1	0	0	1		1	1	1	1	0	1	1
A		X	1	0	1	0		1	1	1	0	1	1	1
b		X	1	0	1	1		0	0	1	1	1	1	1
C		X	1	1	0	0		1	0	0	1	1	1	0
d		X	1	1	0	1		0	1	1	1	1	0	1
E		X	1	1	1	0		1	0	0	1	1	1	1
F		X	1	1	1	1		1	0	0	0	1	1	1

[†] The decimal point is enabled by setting bit D7 = 1.

Table 12. No-Decode Mode Data Bits and Corresponding Segment Lines

	D7	D6	D5	D4	D3	D2	D1	D0
Corresponding Segment Line	DP	A	B	C	D	E	F	G

Display-Test Register (0xXF)

The AS1106/AS1107 devices can operate in two modes: normal mode and display test mode. In display test mode all LEDs are switched on at maximum brightness (duty cycle is 15/16 (AS1106) or 31/32 (AS1107)). The devices remain in display-test mode until the Display-Test Register is set for normal operation.

Note: All settings of the digit- and control-registers are maintained.

Table 13. Display-Test Register Format (Address (HEX) = 0xXF)

Mode	Register Data							
	D7	D6	D5	D4	D3	D2	D1	D0
Normal Operation	X	X	X	X	X	X	X	0
Display Test Mode	X	X	X	X	X	X	X	1

Intensity Control Register (0xA)

The brightness of the display can be controlled by digital means using the Intensity Control Register and by analog means using RSET (see Selecting RSET Resistor Value and Using External Drivers on page 14).

Display brightness is controlled by an integrated pulse-width modulator which is controlled by the lower-nibble of the Intensity Control Register. The modulator scales the average segment-current in 16 steps from a maximum of 31/32 down to 1/32 (15/16 to 1/16 for the AS1107) of the peak current set by RSET.

Table 14. Intensity Register Format (Address (HEX) = 0xA)

Duty Cycle		HEX Code	Register Data							
AS1106	AS1107		D7	D6	D5	D4	D3	D2	D1	D0
1/32 (min on)	1/16 (min on)	0xX0	X	X	X	X	0	0	0	0
3/32	2/16	0xX1	X	X	X	X	0	0	0	1
5/32	3/16	0xX2	X	X	X	X	0	0	1	0
7/32	4/16	0xX3	X	X	X	X	0	0	1	1
9/32	5/16	0xX4	X	X	X	X	0	1	0	0
11/32	6/16	0xX5	X	X	X	X	0	1	0	1
13/32	7/16	0xX6	X	X	X	X	0	1	1	0
15/32	8/16	0xX7	X	X	X	X	0	1	1	1
17/32	9/16	0xX8	X	X	X	X	1	0	0	0
19/32	10/16	0xX9	X	X	X	X	1	0	0	1
21/32	11/16	0xA	X	X	X	X	1	0	1	0
23/32	12/16	0xB	X	X	X	X	1	0	1	1
25/32	13/16	0xC	X	X	X	X	1	1	0	0
27/32	14/16	0xD	X	X	X	X	1	1	0	1
29/32	15/16	0xE	X	X	X	X	1	1	1	0
31/32 (max on)	15/16 (max on)	0xF	X	X	X	X	1	1	1	1

Scan-Limit Register (0xB)

The Scan-Limit Register controls which of the digits are to be displayed. When all 8 digits are to be displayed, the update frequency is typically 800Hz. If the number of digits displayed is reduced, the update frequency is increased. The frequency can be calculated using $8f_{OSC}/N$, where N is the number of digits. Since the number of displayed digits influences the brightness, RSET should be adjusted accordingly. Table 16 lists the maximum allowed current when fewer than 4 digits are used.

Note: To avoid differences in brightness this register should not be used to blank parts of the display (leading zeros).

Table 15. Scan-Limit Register Format (Address (HEX) = 0xB)

Scan Limit	HEX Code	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Display digit 0 only (see Table 16)	0xX0	X	X	X	X	X	0	0	0
Display digits 0:1 (see Table 16)	0xX1	X	X	X	X	X	0	0	1
Display digits 0:2 (see Table 16)	0xX2	X	X	X	X	X	0	1	0
Display digits 0:3	0xX3	X	X	X	X	X	0	1	1
Display digits 0:4	0xX4	X	X	X	X	X	1	0	0
Display digits 0:5	0xX5	X	X	X	X	X	1	0	1
Display digits 0:6	0xX6	X	X	X	X	X	1	1	0
Display digits 0:7	0xX7	X	X	X	X	X	1	1	1

Table 16. Maximum Segment Current for 1-, 2-, or 3-Digit Displays

Number of Digits Displayed	Maximum Segment Current (mA)
1	10
2	20
3	30

Feature Register (0xXE)

The Feature Register is used for enabling various features including switching the device into external clock mode, applying an external reset, selecting code-B or HEX decoding, enabling or disabling blinking, enabling or disabling the SPI-compatible interface (AS1106 only), setting the blinking rate, and resetting the blink timing.

Note: At power-up the Feature Register is initialized to 0.

Table 17. Feature Register Summary

D7	D6	D5	D4	D3	D2	D1	D0
blink_start	sync	blink_freq_sel	blink_en	spi_en	decode_sel	reg_res	clk_en

Table 18. Feature Register Bit Descriptions (Address (HEX) = 0xXE)

Addr: 0xXE		Feature Register		Bit Description
		Enables and disables various device features.		
Bit	Bit Name	Default	Access	
D0	clk_en	0	R/W	External clock active. 0 = Internal oscillator is used for system clock. 1 = Pin CLK of the serial interface operates as system clock input.
D1	reg_res	0	R/W	Resets all control registers except the Feature Register. 0 = Reset Disabled. Normal operation. 1 = All control registers are reset to default state (except the Feature Register) identically after power-up. Note: The Digit Registers maintain their data.
D2	decode_sel	0	R/W	Selects display decoding. 0 = Enable Code-B decoding (see Table 10 on page 10). 1 = Enable HEX decoding (see Table 11 on page 11).
D3	spi_en	0	R/W	Enables the SPI-compatible interface. 0 = Disable SPI-compatible interface (AS1106 only). 1 = Enable the SPI-compatible interface (AS1106 only). Note: The SPI-compatible interface is always enabled in the AS1107.
D4	blink_en	0	R/W	Enables blinking. 0 = Disable blinking. 1 = Enable blinking.
D5	blink_freq_sel	0	R/W	Sets blink with low frequency (with the internal oscillator enabled): 0 = Blink period typically is 1 second (0.5s on, 0.5s off). 1 = Blink period is 2 seconds (1s on, 1s off).
D6	sync	0	R/W	Synchronizes blinking on the rising edge of pin LOAD/CSN. The multiplex and blink timing counter is cleared on the rising edge of pin LOAD/CSN. By setting this bit in multiple AS1106/AS1107 devices, the blink timing can be synchronized across all the devices.
D7	blink_start	0	R/W	Start Blinking with display enabled phase. When bit D4 (blink_en) is set, bit D7 determines how blinking starts. 0 = Blinking starts with the display turned off. 1 = Blinking starts with the display turned on.

No-Op Register (0xX0)

The No-Op Register is used when multiple AS1106 or AS1107 devices are cascaded in order to support displays with more than 8 digits. The cascading must be done in such a way that all DOUT pins are connected to DIN of the next AS1106/AS1107 (see Figure 14 on page 16). The LOAD/CSN and CLK signals are connected to all devices.

For example, if five devices are cascaded, in order to perform a write operation to the fifth device, the write-command must be followed by four no-operation commands. When the LOAD/CSN signal goes high, all shift registers are latched. The first four devices will receive no-operation commands and only the fifth device will receive the intended operation command, and subsequently update its register.

9 Typical Application

Supply Bypassing and Wiring

In order to achieve optimal performance the AS1106/AS1107 should be placed very close to the LED display to minimize effects of electromagnetic interference and wiring inductance.

Furthermore, it is recommended to connect a 10 μ F electrolytic and a 0.1 μ F ceramic capacitor between pins VDD and GND to avoid power supply ripple (see Figure 14 on page 16).

Note: Both GND pins must be connected to ground.

Selecting R_{SET} Resistor Value and Using External Drivers

Brightness of the display segments is controlled via R_{SET}. The current that flows between VDD and ISET defines the current that flows through the LEDs.

Segment current is about 200 times the current in ISET. Typical values for R_{SET} for different segment currents, operating voltages, and LED voltage drop (V_{LED}) are given in Tables 19 - 23. The maximum current the AS1106/AS1107 devices can drive is 40mA. If higher currents are needed, external drivers must be used, in which case it is no longer necessary that the devices drive high currents.

In cases where the devices only drive a few digits, Table 16 specifies the maximum currents, and R_{SET} must be set accordingly.

Note: The display brightness can also be logically controlled (see Intensity Control Register (0xXA) on page 12).

Table 19. R_{SET} vs. Segment Current and LED Forward Voltage, V_{DD} = 2.7V

I _{SEG} (mA)	V _{LED} (V)	
	1.5	2.0
40	5k Ω	4.4k Ω
30	6.9k Ω	5.9k Ω
20	10.7k Ω	9.6k Ω
10	22.2k Ω	20.7k Ω

Table 20. R_{SET} vs. Segment Current and LED Forward Voltage, V_{DD} = 3.3V

I _{SEG} (mA)	V _{LED} (V)		
	1.5	2.0	2.5
40	6.7k Ω	6.4k Ω	5.7k Ω
30	9.1k Ω	8.8k Ω	8.1k Ω
20	13.9k Ω	13.3k Ω	12.6k Ω
10	28.8k Ω	27.7k Ω	26k Ω

Table 21. R_{SET} vs. Segment Current and LED Forward Voltage, V_{DD} = 3.6V

I _{SEG} (mA)	V _{LED} (V)			
	1.5	2.0	2.5	3.0
40	7.5k Ω	7.2k Ω	6.6k Ω	5.5k Ω
30	10.18k Ω	9.8k Ω	9.2k Ω	7.5k Ω
20	15.6k Ω	15k Ω	14.3k Ω	13k Ω
10	31.9k Ω	31k Ω	29.5k Ω	27.3k Ω

Table 22. R_{SET} vs. Segment Current and LED Forward Voltage, V_{DD} = 4.0V

I _{SEG} (mA)	V _{LED} (V)				
	1.5	2.0	2.5	3.0	3.5
40	8.6k Ω	8.3k Ω	7.9k Ω	7.6k Ω	5.2k Ω
30	11.6k Ω	11.2k Ω	10.8k Ω	9.9k Ω	7.8k Ω

Table 22. RSET vs. Segment Current and LED Forward Voltage, VDD = 4.0V (Continued)

ISEG (mA)	VLED(V)				
	1.5	2.0	2.5	3.0	3.5
20	17.7kΩ	17.3kΩ	16.6kΩ	15.6kΩ	13.6kΩ
10	36.89kΩ	35.7kΩ	34.5kΩ	32.5kΩ	29.1kΩ

Table 23. RSET vs. Segment Current and LED Forward Voltage, VDD = 5.0V

ISEG (mA)	VLED (V)					
	1.5	2.0	2.5	3.0	3.5	4.0
40	11.35kΩ	11.12kΩ	10.84kΩ	10.49kΩ	10.2kΩ	9.9kΩ
30	15.4kΩ	15.1kΩ	14.7kΩ	14.4kΩ	13.6kΩ	13.1kΩ
20	23.6kΩ	23.1kΩ	22.6kΩ	22kΩ	21.1kΩ	20.2kΩ
10	48.9kΩ	47.8kΩ	46.9kΩ	45.4kΩ	43.8kΩ	42kΩ

Table 24. Package Thermal Data

Package	Thermal Resistance (ΘJA)
24 Narrow DIP	+75°C/W
24 Wide SOIC	+85°C/W

Calculating Power Dissipation

The upper limit for power dissipation (PD) for the AS1106/AS1107 is determined from the following equation:

$$PD = (V_{DD} \times 1mA) + (V_{DD} - V_{LED})(DUTY \times I_{SEG} \times N) \quad (EQ 1)$$

Where:

VDD is the supply voltage.

DUTY is the duty cycle set by intensity register (page 12).

N is the number of segments driven (worst case is 8)

VLED is the LED forward voltage

ISEG = segment current set by RSET

Dissipation Example:

$$I_{SEG} = 40mA, N = 8, DUTY = 31/32, V_{LED} = 1.8V \text{ at } 40mA, V_{DD} = 5.25V \quad (EQ 2)$$

$$PD = 5.25V(1mA) + (5.25V - 1.8V)(31/32 \times 40mA \times 8) = 1.075W \quad (EQ 3)$$

Thus, for a PDIP package ΘJA = +75°C/W (from Table 24), the maximum allowed TAMB is given by:

$$T_{J,MAX} = T_{AMB} + PD \times \Theta_{JA} = 150^\circ C = T_{AMB} + 1.07W \times 75^\circ C/W \quad (EQ 4)$$

Where:

TAMB = +69.4°C.

The TAMB limit for SO Packages in the dissipation example above is +58.6°C.

8x8 LED Dot Matrix Driver

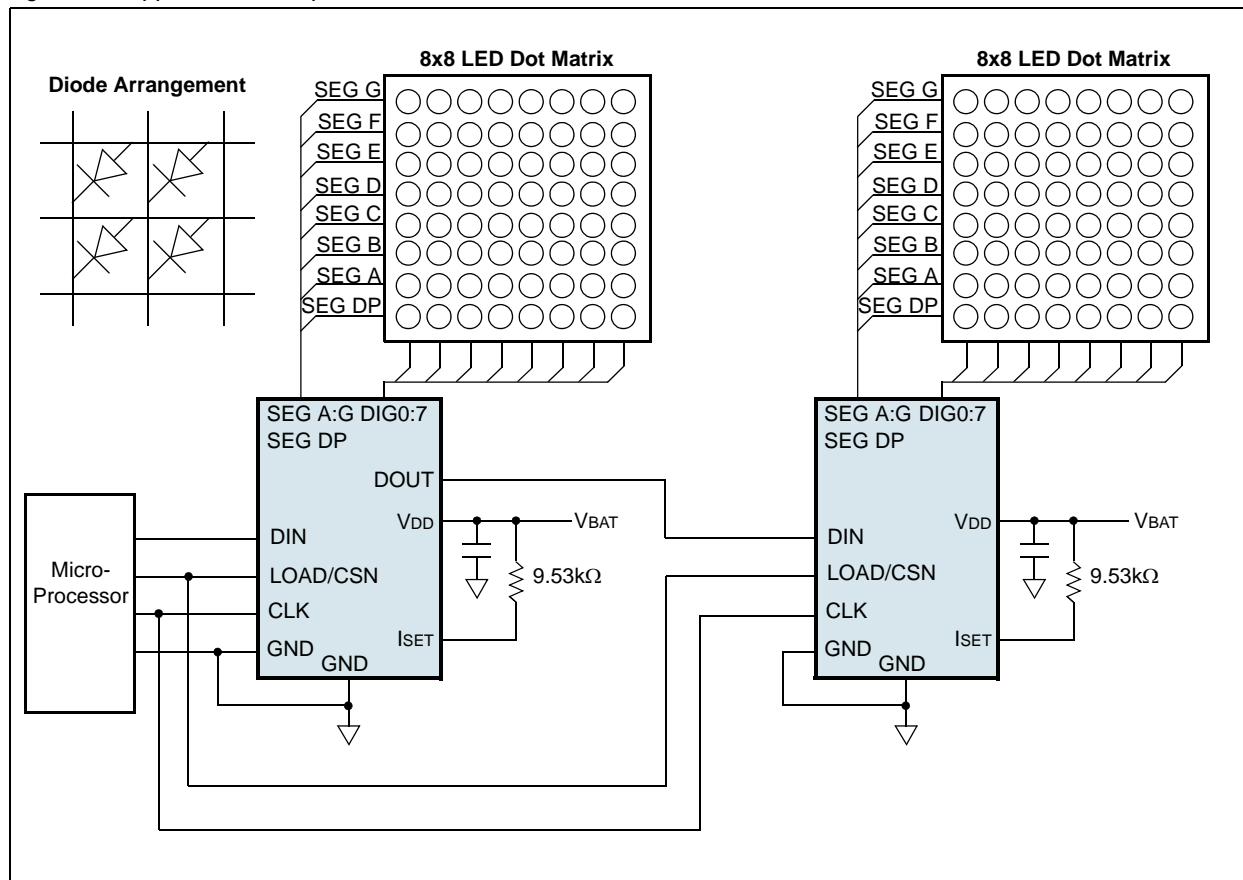
The application example in Figure 14 shows the AS1106 as an 8x8 LED dot matrix driver.

The LED columns have common cathodes and are connected to the DIG0:7 outputs. The rows are connected to the segment drivers. Each of the 64 LEDs can be addressed separately. The columns are selected via the digits as listed in Table 7 on page 9.

The Decode Enable Register (see page 10) must be set to '00000000' as described in Table 9 on page 10. Single LEDs in a column can be addressed as described in Table 12 on page 11, where bit D0 corresponds to segment G and bit D7 corresponds to segment DP.

Note: For a multiple-digit dot matrix, multiple AS1106 devices must be cascaded.

Figure 14. Application Example as LED Dot Matrix Driver



Cascading Drivers

The example in Figure 4 drives 2 dot matrix digits using a 4-wire microprocessor interface. All Scan-Limit Registers should be set to the same value so that one display will not appear brighter than the other.

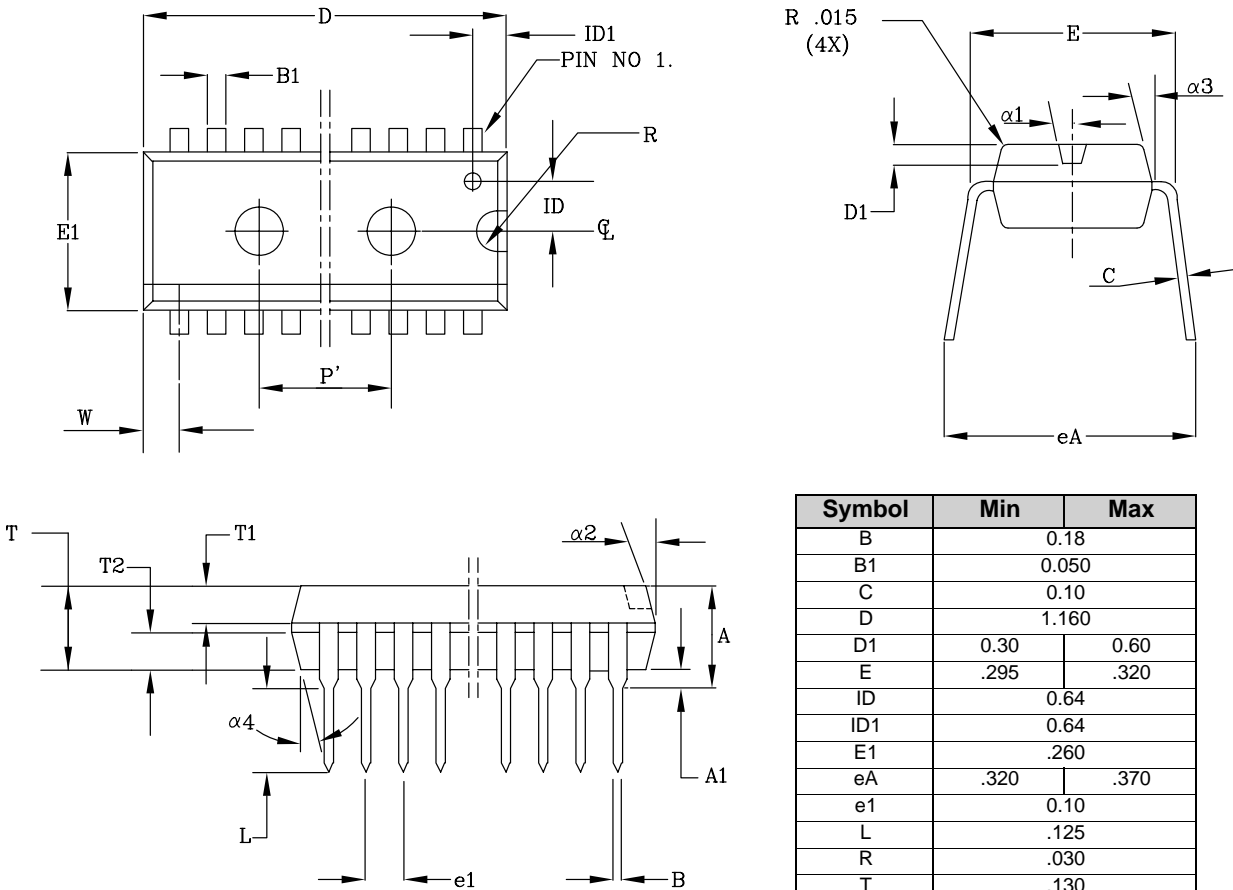
For example, to display 12 digits, set both Scan-Limit Registers to display 6 digits so that both displays have a 1/6 duty cycle per digit. If 11 digits are needed, set both Scan-Limit Registers to display 6 digits and leave one digit unconnected. Otherwise, if one driver is set to display 6 digits and the other to display 5 digits one display will appear brighter because its duty cycle per digit will be 1/5 and the other display's duty cycle will be 1/6.

Note: Refer to No-Op Register (0xX0) on page 13 for additional information.

10 Package Drawings and Markings

The AS1106 and AS1107 are available in 24-pin DIP and 24-pin SOIC packages.

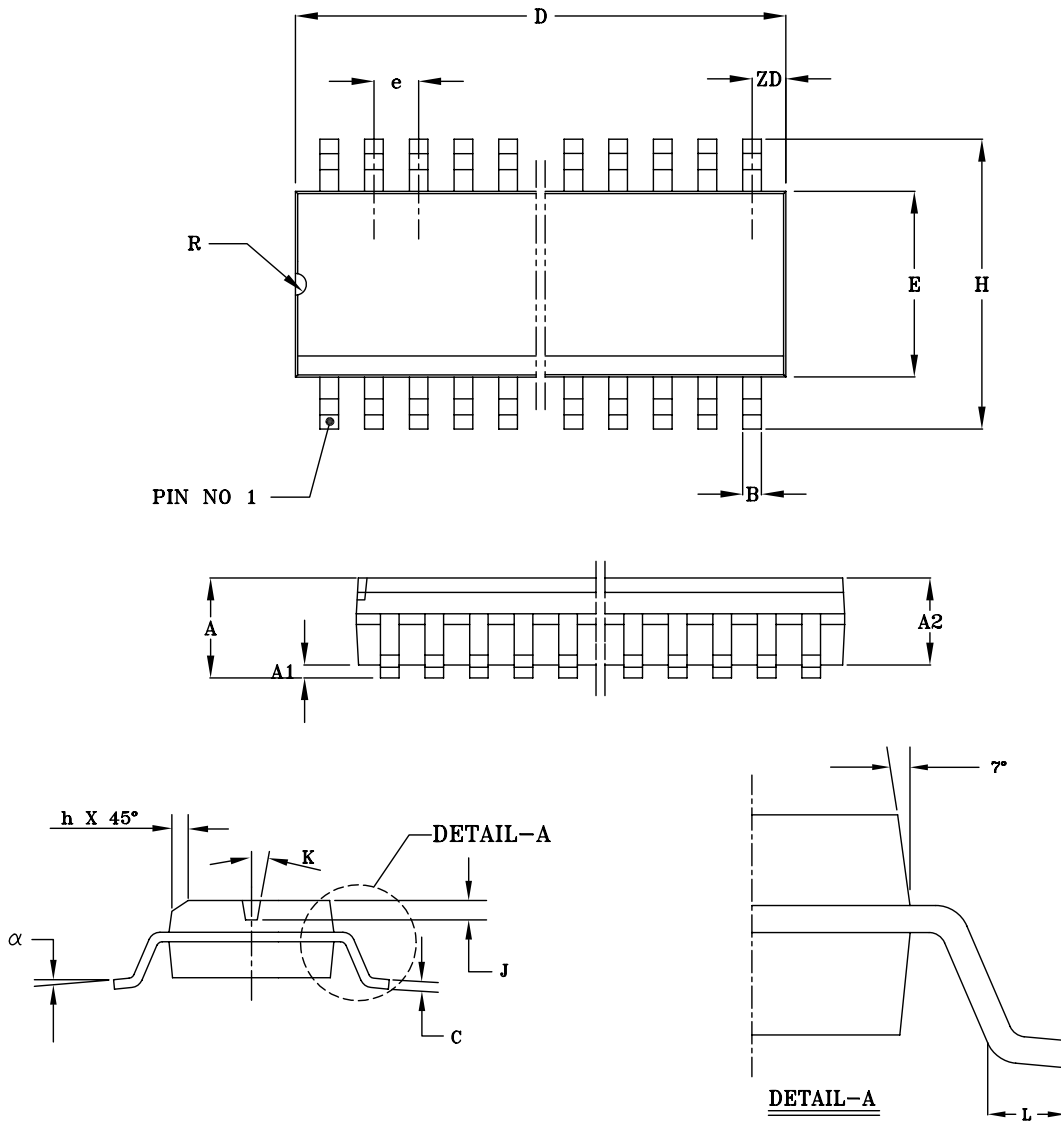
Figure 15. 24-pin DIP Package



Symbol	Min	Max
B		0.18
B1		0.050
C		0.10
D		1.160
D1	0.30	0.60
E	.295	.320
ID		0.64
ID1		0.64
E1		.260
eA	.320	.370
e1		0.10
L		.125
R		.030
T		.130
T1		.060
T2		.060
W		.030 REF
α1		7°
α2		7°
α3		7°
α4		7°
P'		.760
A	.145	.170
A1	.015	.040

Note: All dimensions in inches.

Figure 16. 24-pin SOIC Package



Symbol	Min	Max	Symbol	Min	Max
A	2.44	2.64	H	10.11	10.51
A1	0.10	0.30	h	0.31	0.71
A2	2.24	2.44	J	0.53	0.73
B	0.36	0.46	K	7° BSC	
C	0.23	0.32	L	0.51	1.01
D	15.20	15.40	R	0.63	0.89
E	7.40	7.50	ZD	0.66 REF	
e	1.27 BSC		α	0°	8°

Note: All dimensions in millimeters.

11 Ordering Information

The AS1106 and AS1107 are available in 24-pin DIP and 24-pin SOIC packages.

Table 25. Ordering Information

Part	Temperature Range	Delivery Form	Package
AS1106PL	0 to +70°C	Tubes	24-pin Narrow Plastic DIP, Pb-free
AS1106WL	0 to +70°C	Tubes	24-pin Wide SO, Pb-free
AS1106WL-T	0 to +70°C	Tape and Reel	24-pin Wide SO, Pb-free
AS1106PE	-40 to +85°C	Tubes	24-pin Narrow Plastic DIP, Pb-free
AS1106WE	-40 to +85°C	Tubes	24-pin Wide SO, Pb-free
AS1106WE-T	-40 to +85°C	Tape and Reel	24-pin Wide SO, Pb-free
AS1107PL	-40 to +85°C	Tubes	24-pin Narrow Plastic DIP, Pb-free
AS1107WL	-40 to +85°C	Tubes	24-pin Wide SO, Pb-free
AS1107WL-T	-40 to +85°C	Tape and Reel	24-pin Wide SO, Pb-free

All devices are RoHS compliant and free of halogene substances.

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