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Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

CY62146E MoBL

4-Mbit (256K × 16) Static RAM

Features

- Very high speed: 45 ns
- Wide voltage range: 4.5 V to 5.5 V
- Ultra low standby power
  - Typical standby current: 2.5 µA
  - Maximum standby current: 7 µA
- Ultra low active power
  - Typical active current: 3.5 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 44-pin thin small outline package (TSOP) Type II package

Functional Description

The CY62146E is a high performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL®) in portable applications. The device also has an automatic power down feature that reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected ($\overline{CE}$ HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH) or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

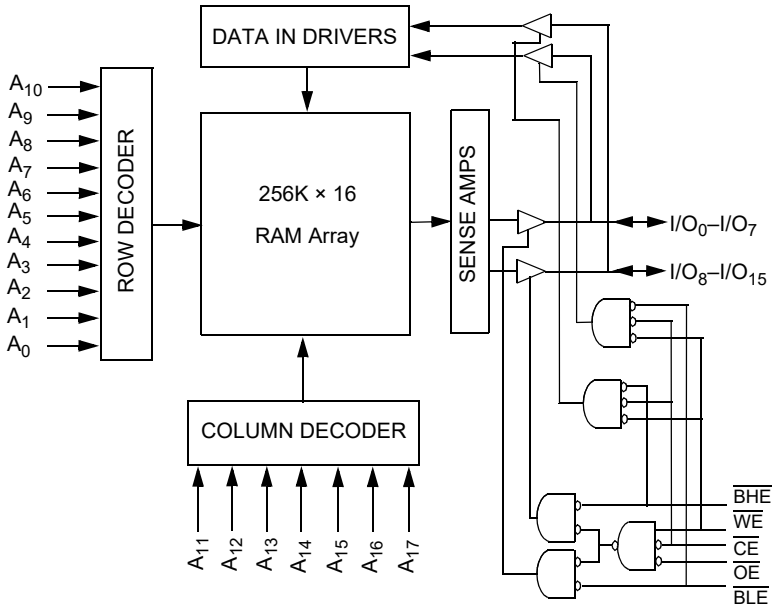
To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See Truth Table on page 11 for a complete description of read and write modes.

The CY62146E device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please Electrical Characteristics on page 4 for more details and suggested alternatives.

For a complete list of related documentation, click here.

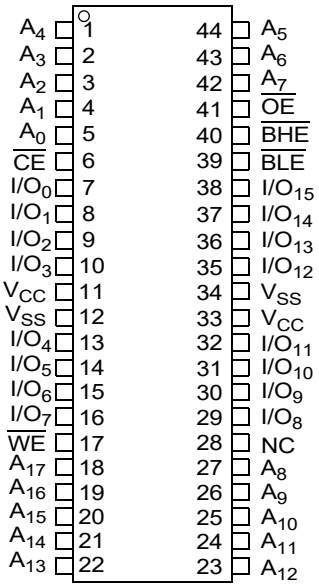
Logic Block Diagram



Contents

Pin Configurations

Figure 1. 44-pin TSOP II pinout (Top View) [1]



Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC}, (mA)				Standby, I_{SB2} (µA)	
						f = 1 MHz		f = f_{max}			
		Min	Typ [2]	Max		Typ [2]	Max	Typ [2]	Max	Typ [2]	Max
CY62146ELL	Industrial/ Automotive-A	4.5	5.0	5.5	45	3.5	6	15	20	2.5	7

Notes
1. NC pins are not connected on the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential .....–0.5 V to 6.0 V

DC voltage applied to outputs in high Z state [3, 4] .....–0.5 V to 6.0 V

DC input voltage [3, 4] .....–0.5 V to 6.0 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) .....>2001 V

Latch-up current .....>200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[5]
CY62146ELL	Industrial/ Automotive-A	–40 °C to +85 °C	4.5 V–5.5 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns (Industrial/Automotive-A)			Unit
				Min	Typ[6]	Max	
V_{OH}	Output high voltage	V_{CC} = 4.5 V	I_{OH} = –1.0 mA	2.4	–	–	V
		V_{CC} = 5.5 V	I_{OH} = –0.1 mA	–	–	3.4 [7]	
V_{OL}	Output low voltage	I_{OL} = 2.1 mA		–	–	0.4	V
V_{IH}	Input high voltage	4.5 ≤ V_{CC} ≤ 5.5		2.2	–	V_{CC} + 0.5	V
V_{IL}	Input low voltage	4.5 ≤ V_{CC} ≤ 5.5		–0.5	–	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = 1/t_{RC}	V_{CC} = V_{CCmax} I_{OUT} = 0 mA, CMOS levels	–	15	20	mA
		f = 1 MHz		–	3.5	6	
I_{SB2} [8]	Automatic CE power down current – CMOS inputs	$\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0, V_{CC} = $V_{CC(max)}$		–	2.5	7	µA

Notes

3. V_{IL}(min) = –2.0 V for pulse durations less than 20 ns for I < 30 mA.
4. V_{IH}(max) = V_{CC} + 0.75 V for pulse durations less than 20 ns.
5. Full Device AC operation assumes a minimum of 100 µs ramp time from 0 to V_{CC} (min) and 200 µs wait time after V_{CC} stabilization.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
7. Please note that the maximum V_{OH} limit does not exceed minimum CMOS V_{IH} of 3.5 V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum V_{IH} of 3.5 V, please refer to Application Note AN6081 for technical details and options you may consider.
8. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB2}/I_{CCDR} spec. Other inputs are left floating.

Capacitance

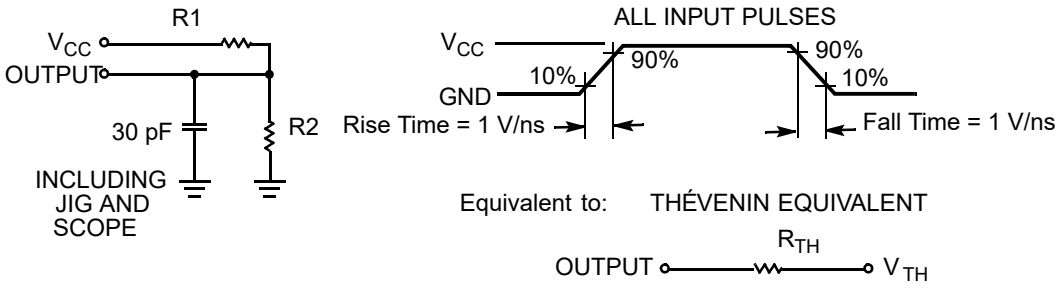
Parameter [9]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [9]	Description	Test Conditions	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	55.52	°C/W
Θ_{JC}	Thermal resistance (junction to case)		16.03	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	5.0 V	Unit
R1	1800	Ω
R2	990	Ω
R_{TH}	639	Ω
V_{TH}	1.77	V

Note
9. Tested initially after any design or process changes that may affect these parameters.

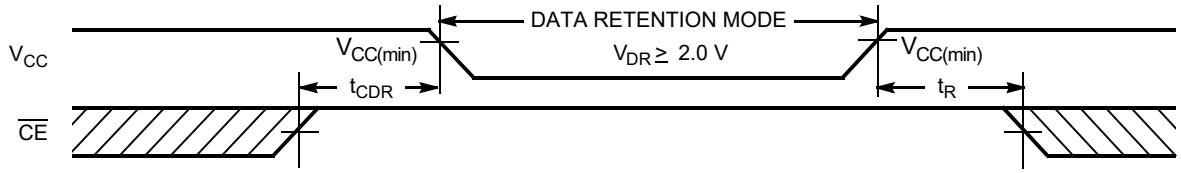
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [10]	Max	Unit
V_{DR}	V_{CC} for data retention		2	–	–	V
I_{CCDR} [11]	Data retention current	V_{CC} = 2 V, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	3	8.8	µA
t_{CDR} [12]	Chip deselect to data retention time		0	–	–	ns
t_R [13]	Operation recovery time		45	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
11. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB2}/I_{CCDR} spec. Other inputs are left floating.
12. Tested initially and after any design or process changes that may affect these parameters.
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

Switching Characteristics

Over the Operating Range

Parameter [14, 15]	Description	45 ns (Industrial/Automotive-A)		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[16]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[16, 17]	–	18	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[16]	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[16, 17]	–	18	ns
t_{PU}	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down	–	45	ns
t_{DBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to data valid	–	22	ns
t_{LZBE}	$\overline{BLE}$/$\overline{BHE}$ LOW to Low Z[16]	5	–	ns
t_{HZBE}	$\overline{BLE}$/$\overline{BHE}$ HIGH to High Z[16, 17]	–	18	ns
Write Cycle[18, 19]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{BW}	$\overline{BLE}$/$\overline{BHE}$ LOW to write end	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [16, 17]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [16]	10	–	ns

Notes

14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1 V/ns) or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3 V, and output loading of the specified I_{OL}/I_{OH} as shown in Figure 2 on page 5.
15. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes AN13842 and AN66311. However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
16. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
17. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
18. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
19. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [20, 21]

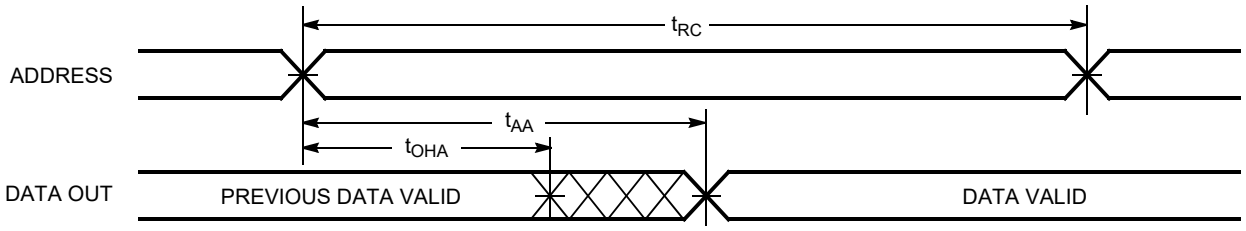
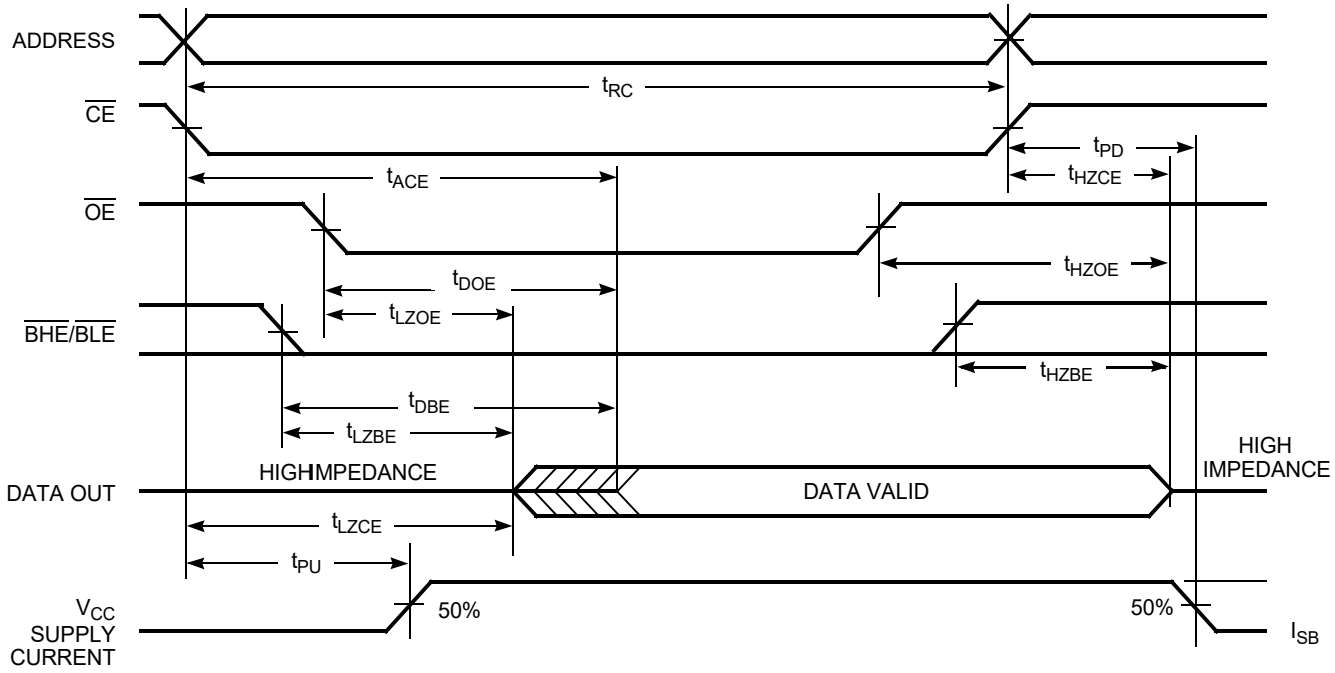


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [21, 22]



Notes
20. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$, or both = V_{IL}.
21. $\overline{WE}$ is HIGH for read cycle.
22. Address valid before or similar to $\overline{CE}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{WE}$ Controlled) [23, 24, 25]

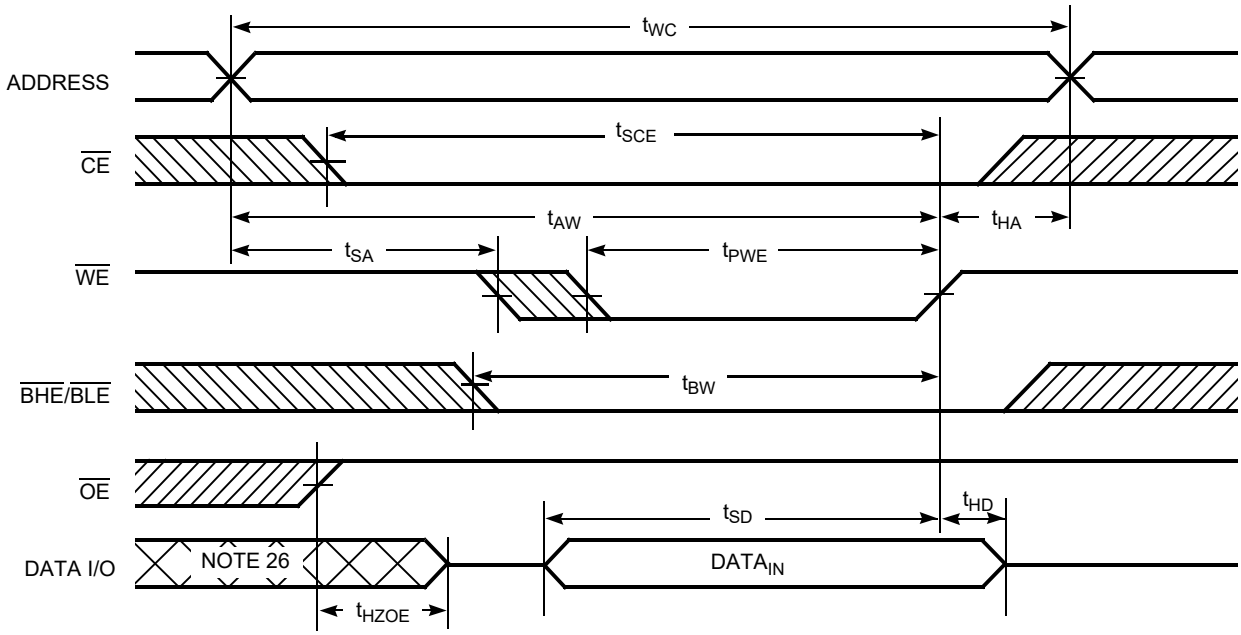
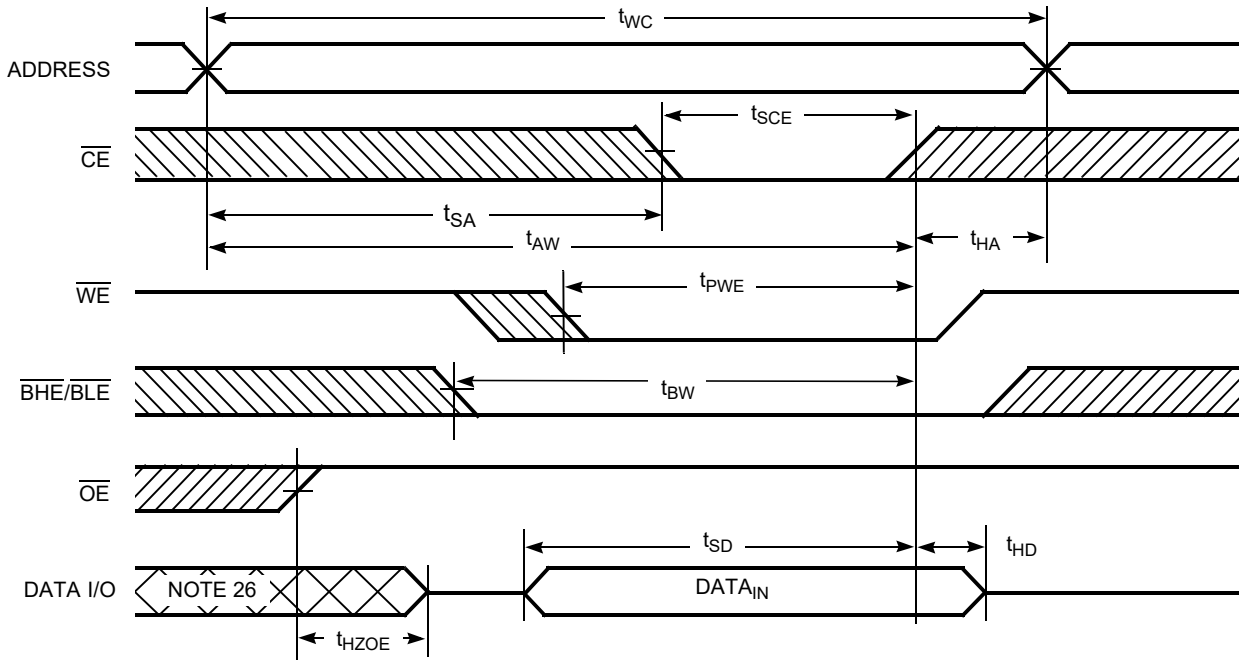


Figure 7. Write Cycle No. 2 ($\overline{CE}$ Controlled) [23, 24, 25]



Notes

23. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
24. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
25. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate the write by going inactive. The input setup and hold timing must be referenced to the edge of the signal that terminate the write.
26. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 (WE Controlled, OE LOW) [27, 28, 30]

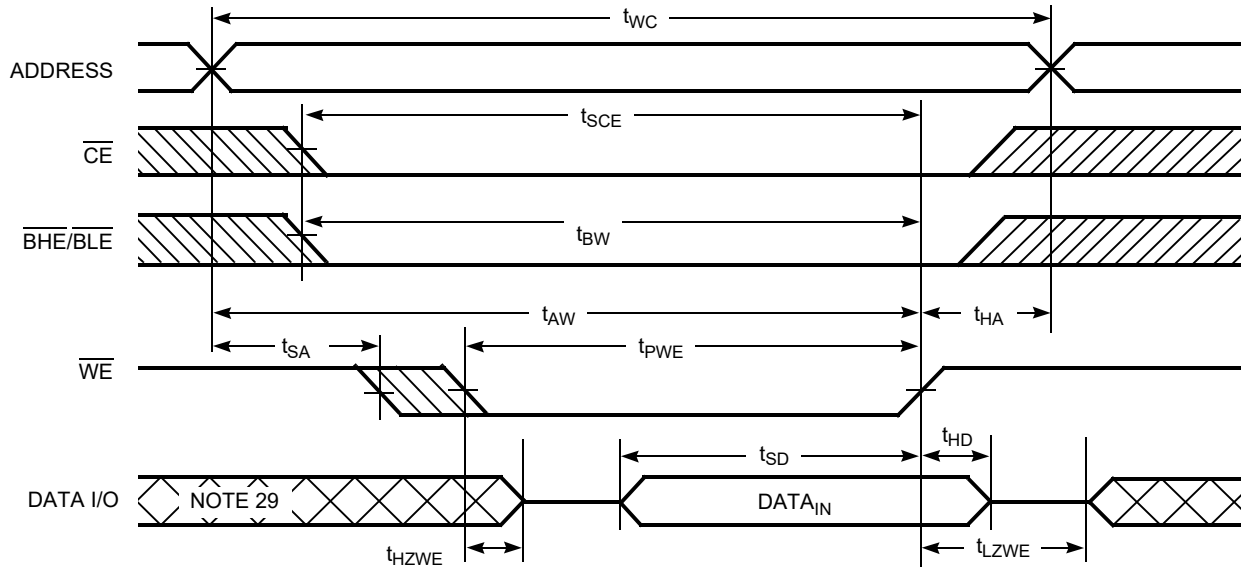
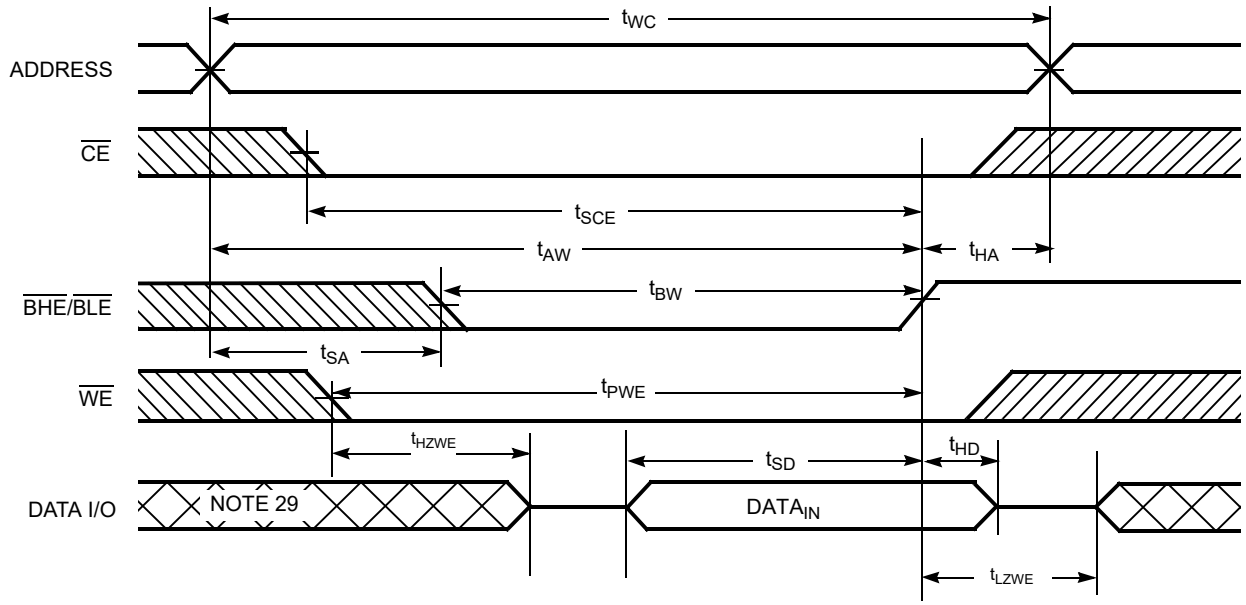


Figure 9. Write Cycle No. 4 (BHE/BLE Controlled, OE LOW) [27, 28]



Notes

27. If CE goes HIGH simultaneously with WE = V_{IH}, the output remains in a high impedance state.
28. The internal write time of the memory is defined by the overlap of WE, CE = V_{IL}, BHE, BLE or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate the write by going inactive. The input setup and hold timing must be referenced to the edge of the signal that terminate the write.
29. During this period, the I/Os are in output state. Do not apply input signals.
30. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE}.

Truth Table

$\overline{CE}$[31]	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X[31]	X[31]	High Z	Deselect/power down	Standby (I_{SB})
L	X	X	H	H	High Z	Output disabled	Active (I_{CC})
L	H	L	L	L	Data out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data out (I/O_0–I/O_7); I/O_8–I/O_{15} in High-Z	Read	Active (I_{CC})
L	H	L	L	H	Data out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High-Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data in (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data in (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data in (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Write	Active (I_{CC})

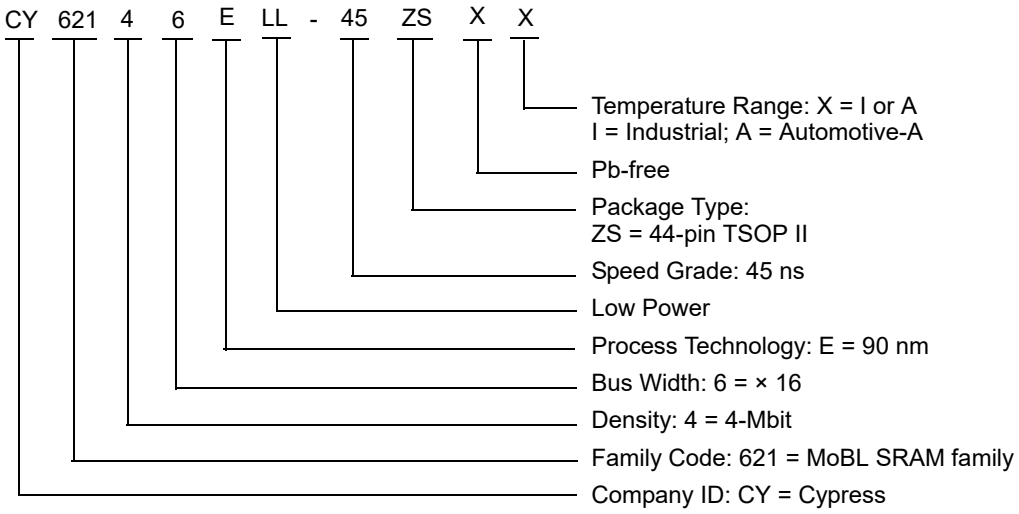
Note
31. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) must be at CMOS levels (not floating) to meet the I_{SB2} / I_{CCDR} spec. Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62146ELL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	Industrial

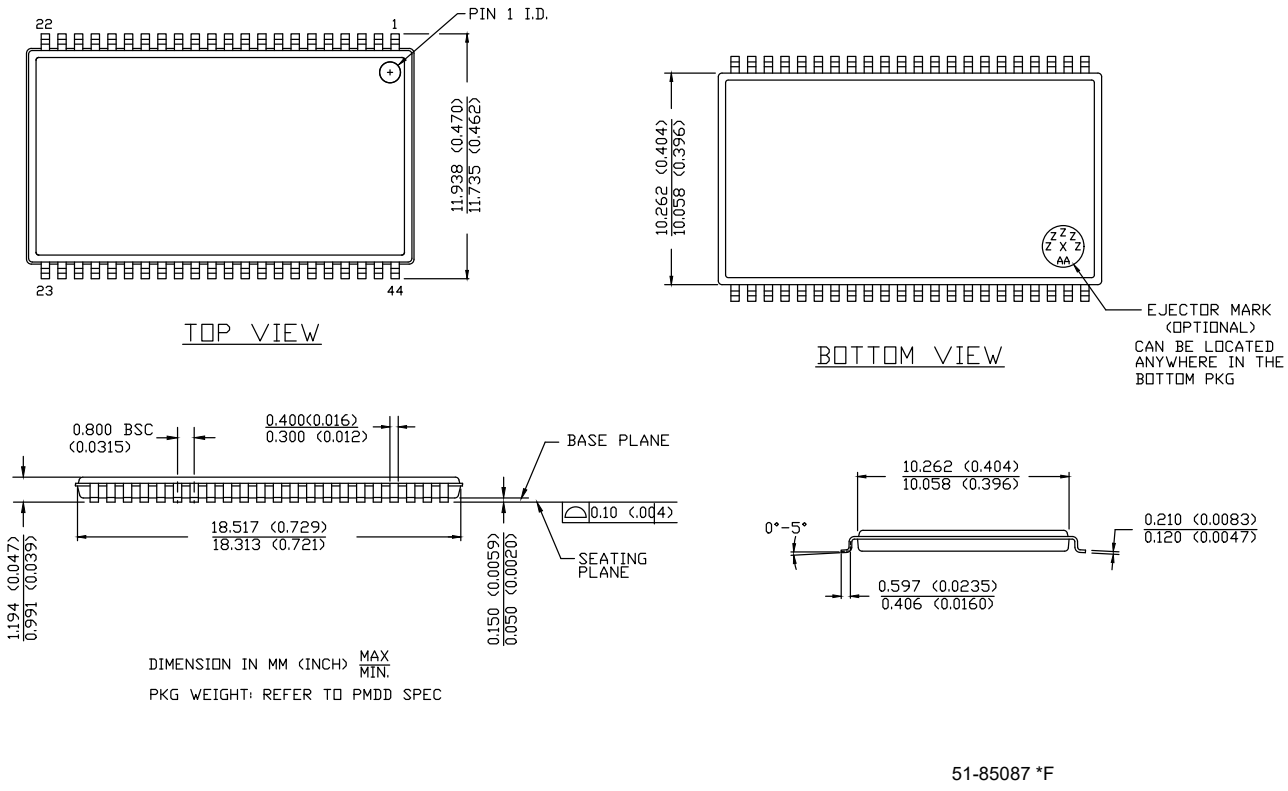
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagram

Figure 10. 44-pin TSOP II (18.4 × 10.2 × 1.194 mm) Package Outline, 51-85087



Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Gird Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62146E MoBL, 4-Mbit (256K × 16) Static RAM Document Number: 001-07970			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
**	463213	05/19/2006	New data sheet.
*A	684343	01/17/2007	Added Automotive-A Temperature Range related information in all instances across the document and made the information Preliminary (by shading in required places). Updated Ordering Information: Updated part numbers.
*B	925501	04/09/2007	Updated Electrical Characteristics: Added Note 8 and referred the same note in I_{SB2} parameter. Updated Data Retention Characteristics: Added Note 11 and referred the same note in I_{CCDR} parameter. Updated Switching Characteristics: Added Note 15 and referred the same note in “Parameter” column.
*C	1045260	05/07/2007	Changed status of Automotive-A Temperature Range related information from Preliminary to Final (by unshading in required places). Updated Ordering Information: No change in part numbers. Unshaded the Automotive-A MPNs (Changed status from Preliminary to Final).
*D	2073548	02/06/2008	Updated Data Retention Waveform: Updated Figure 3 (Corrected typo). Removed Note “$\overline{BHE}$. $\overline{BLE}$ is the AND of $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling the chip enable signals or by disabling $\overline{BHE}$ and $\overline{BLE}$.” and its reference. Updated to new template.
*E	2943752	06/03/2010	Updated Truth Table: Added Note 31 and referred the same note in “$\overline{CE}$” column. Updated Package Diagram: spec 51-85087 – Changed revision from *A to *C. Updated to new template.
*F	3109050	12/13/2010	Changed Table Footnotes to Notes in all instances across the document. Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions.
*G	3149059	01/20/2011	Updated Ordering Information: No change in part numbers. Updated Ordering Code Definitions (Corrected Errors). Added Acronyms and Units of Measure. Updated to new template. Completing Sunset Review.
*H	3296704	06/29/2011	Updated Functional Description: Updated description (Removed “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.”).
*I	3921993	03/05/2013	Updated Switching Waveforms: Added Note 25 and referred the same note in Figure 6, Figure 7. Removed Note “$\overline{WE}$ is HIGH for read cycle.” and its references in Figure 6, Figure 7. Added Note 28 and referred the same note in Figure 8, Figure 9. Updated Package Diagram: spec 51-85087 – Changed revision from *C to *E. Completing Sunset Review.

Document History Page (continued)

Document Title: CY62146E MoBL, 4-Mbit (256K × 16) Static RAM Document Number: 001-07970			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
*J	4013949	06/04/2013	Updated Functional Description: Updated description. Updated Electrical Characteristics: Added one more Test Condition "V_{CC} = 5.5 V, I_{OH} = –0.1 mA" for V_{OH} parameter and added maximum value corresponding to that Test Condition. Added Note 7 and referred the same note in maximum value for V_{OH} parameter corresponding to Test Condition "V_{CC} = 5.5 V, I_{OH} = –0.1 mA".
*K	4102022	08/14/2013	Updated Switching Characteristics: Updated Note 15. Updated to new template.
*L	4576478	11/21/2014	Updated Functional Description: Added "For a complete list of related documentation, click here." at the end. Updated Switching Characteristics: Added Note 19 and referred the same note in "Write Cycle". Updated Switching Waveforms: Added Note 30 and referred the same note in Figure 8.
*M	5196888	04/14/2016	Updated Thermal Resistance: Updated values of Θ_{JA} and Θ_{JC} parameters in "44-pin TSOP II" column. Updated to new template. Completing Sunset Review.
*N	6049346	01/29/2018	Updated Ordering Information: Updated part numbers. Updated to new template. Completing Sunset Review.
*O	6560791	04/29/2019	Updated to new template.
*P	6906316	06/26/2020	Updated Features: Changed value of Typical standby current from 1 µA to 2.5 µA. Changed value of Typical active current from 2 mA to 3.5 mA. Updated Product Portfolio: Changed typical value of Operating I_{CC} from 2 mA to 3.5 mA corresponding to "f = 1 MHz". Changed maximum value of Operating I_{CC} from 2.5 mA to 6 mA corresponding to "f = 1 MHz". Changed typical value of Standby, I_{SB2} from 1 µA to 2.5 µA. Updated Electrical Characteristics: Changed typical value of I_{CC} parameter from 2 mA to 3.5 mA corresponding to Test Condition "f = 1 MHz". Changed maximum value of I_{CC} parameter from 2.5 mA to 6 mA corresponding to Test Condition "f = 1 MHz". Changed typical value of I_{SB2} parameter from 1 µA to 2.5 µA. Updated Data Retention Characteristics: Changed typical value of I_{CCDR} parameter from 1 µA to 3 µA. Changed maximum value of I_{CCDR} parameter from 7 µA to 8.8 µA. Updated Package Diagram: spec 51-85087 – Changed revision from *E to *F. Updated to new template.

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