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Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

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4-Mbit (256K × 16) Static RAM

Features

■ Very high speed: 45 ns

■ Wide voltage range: 4.5 V to 5.5 V

■ Ultra low standby power

Typical standby current: 2.5 μA

Maximum standby current: 7 μA

■ Ultra low active power

□ Typical active current: 3.5 mA at f = 1 MHz

■ Easy memory expansion with CE and OE features

■ Automatic power down when deselected

 Complementary metal oxide semiconductor (CMOS) for optimum speed and power

Available in Pb-free 44-pin thin small outline package (TSOP) Type II package

Functional Description

The CY62146E is a high performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life $^{\rm TM}$ (MoBL $^{\rm (B)}$) in portable applications. The device also has an automatic power down feature that reduces power consumption when addresses are

not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected (\overline{CE} HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), both Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , \overline{BLE} HIGH) or during a write operation (\overline{CE} LOW and \overline{WE} LOW).

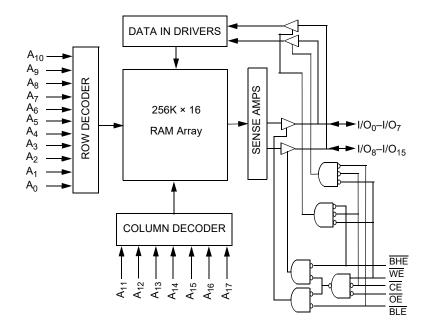
To write to the device, take Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins $(I/O_0$ through I/O₇) is written into the location specified on the address pins $(A_0$ through A_{17}). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins $(I/O_8$ through I/O₁₅) is written into the location specified on the address pins $(A_0$ through A_{17}).

To read <u>fro</u>m the device, take Chip Enable (CE) <u>and</u> Output Enable (\overline{OE}) LOW <u>while</u> forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by <u>the address pins appears on I/O₀ to I/O₇. If Byte High Enable (BHE) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See <u>Truth Table on page 11</u> for a complete description of read and write modes.</u>

The CY62146E device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please Electrical Characteristics on page 4 for more details and suggested alternatives.

For a complete list of related documentation, click here.

Logic Block Diagram





Contents

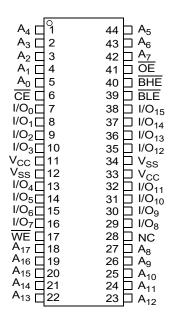
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Pin Configurations

Figure 1. 44-pin TSOP II pinout (Top View) [1]



Product Portfolio

							Power Dissipation					
Produ	ıct	Range	V _{CC} Range (V)		Speed	Operating I _{CC} , (mA)			Standby, I _{SB2}			
Floud	ıcı	Kange				(ns)	f = 1 MHz		f = f _{max}		(μ Ă)	
			Min	Typ ^[2]	Max		Typ [2] Max		Typ [2]	Max	Typ [2]	Max
CY62146	6ELL	Industrial/ Automotive-A	4.5	5.0	5.5	45	3.5	6	15	20	2.5	7

Notes

^{1.} NC pins are not connected on the die.

^{2.} Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.



Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature-65 °C to +150 °C Ambient temperature Supply voltage to ground potential-0.5 V to 6.0 V DC voltage applied to outputs in high Z state $^{[3,\,4]}$ -0.5 V to 6.0 V DC input voltage [3, 4]-0.5 V to 6.0 V

Output current into outputs (LOW)	20 mA
Static discharge voltage	> 0004 V
(MIL-STD-883, Method 3015)	>2001 V
Latch-up current	>200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC} ^[5]	
CY62146ELL	Industrial/ Automotive-A	–40 °C to +85 °C	4.5 V–5.5 V	

Electrical Characteristics

Over the Operating Range

Dawamatan	Description	Took C	di4i	45 ns (Inc	I I mit		
Parameter	Description	lest C	onditions	Min	Typ ^[6]	Max	Unit
V _{OH}	Output high voltage	V _{CC} = 4.5 V	$I_{OH} = -1.0 \text{ mA}$	2.4	_	_	V
		V _{CC} = 5.5 V	$I_{OH} = -0.1 \text{ mA}$	_	_	3.4 ^[7]	
V _{OL}	Output low voltage	I _{OL} = 2.1 mA		_	_	0.4	V
V _{IH}	Input high voltage	4.5 ≤ V _{CC} ≤ 5.5		2.2	_	V _{CC} + 0.5	V
V _{IL}	Input low voltage	4.5 ≤ V _{CC} ≤ 5.5		-0.5	_	0.8	V
I _{IX}	Input leakage current	$GND \leq V_I \leq V_CC$		-1	_	+1	μΑ
I _{OZ}	Output leakage current	$GND \leq V_O \leq V_{CO}$, output disabled	-1	_	+1	μΑ
I _{CC}	V _{CC} operating supply current	$f = f_{max} = 1/t_{RC}$	V _{CC} = V _{CCmax}	_	15	20	mA
		f = 1 MHz	I _{OUT} = 0 mA, CMOS levels	-	3.5	6	
I _{SB2} ^[8]	Automatic CE power down current – CMOS inputs	$\overline{CE} \ge V_{CC} - 0.2$ $V_{IN} \ge V_{CC} - 0.2$ $f = 0, V_{CC} = V_{CC}$	V , V or $V_{IN} \le 0.2 V$, $C(max)$	-	2.5	7	μА

- $V_{IL}(min) = -2.0 \text{ V}$ for pulse durations less than 20 ns for I < 30 mA.
- $V_{IH}(max) = V_{CC} + 0.75 \text{ V}$ for pulse durations less than 20 ns.

- V_H(max) = V_{CC} + 0.75 V for pulse durations less trian 20 fts.
 Full Device AC operation assumes a minimum of 100 μs ramp time from 0 to V_{CC} (min) and 200 μs wait time after V_{CC} stabilization.
 Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
 Please note that the maximum V_{OH} limit does not exceed minimum CMOS V_{IH} of 3.5 V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum V_{IH} of 3.5 V, please refer to Application Note AN6081 for technical details and options you may consider.
 Chip enable (CE) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the I_{SB2}/I_{CCDR} spec. Other inputs are left floating.



Capacitance

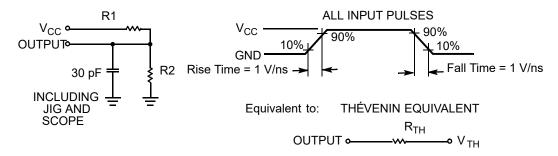
Parameter [9]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	$T_A = 25 ^{\circ}\text{C}, f = 1 \text{MHz}, V_{CC} = V_{CC(typ)}$	10	pF
C _{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [9]	Description	Test Conditions	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	55.52	°C/W
$\Theta_{\sf JC}$	Thermal resistance (junction to case)		16.03	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	5.0 V	Unit
R1	1800	Ω
R2	990	Ω
R _{TH}	639	Ω
V _{TH}	1.77	V

Note

^{9.} Tested initially after any design or process changes that may affect these parameters.



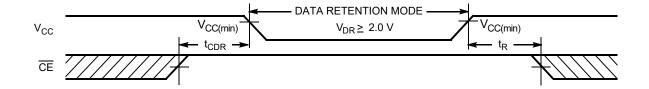
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Min	Typ [10]	Max	Unit	
V_{DR}	V _{CC} for data retention		2	-	-	V
I _{CCDR} [11]	Data retention current	$V_{CC} = 2 \text{ V}, \overline{CE} \ge V_{CC} - 0.2 \text{ V},$ $V_{IN} \ge V_{CC} - 0.2 \text{ V or } V_{IN} \le 0.2 \text{ V}$	-	3	8.8	μА
t _{CDR} ^[12]	Chip deselect to data retention time		0	_	_	ns
t _R ^[13]	Operation recovery time		45	_	_	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



^{10.} Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C. 11. Chip enable (CE) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the I_{SB2}/I_{CCDR} spec. Other inputs are left floating.

 ^{12.} Tested initially and after any design or process changes that may affect these parameters.
 13. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} ≥ 100 μs or stable at V_{CC(min)} ≥ 100 μs.



Switching Characteristics

Over the Operating Range

Parameter [14, 15]	Description	45 ns (Industria	45 ns (Industrial/Automotive-A)			
Parameter [11, 10]	Description	Min	Max	Unit		
Read Cycle				•		
t _{RC}	Read cycle time	45	_	ns		
t _{AA}	Address to data valid	-	45	ns		
t _{OHA}	Data hold from address change	10	_	ns		
t _{ACE}	CE LOW to data valid	_	45	ns		
t _{DOE}	OE LOW to data valid	_	22	ns		
t _{LZOE}	OE LOW to Low Z ^[16]	5	_	ns		
t _{HZOE}	OE HIGH to High Z ^[16, 17]	_	18	ns		
t _{LZCE}	CE LOW to Low Z ^[16]	10	_	ns		
t _{HZCE}	CE HIGH to High Z ^[16, 17]	_	18	ns		
t _{PU}	CE LOW to power-up	0	_	ns		
t _{PD}	CE HIGH to power-down	_	45	ns		
t _{DBE}	BLE/BHE LOW to data valid	_	22	ns		
t _{LZBE}	BLE/BHE LOW to Low Z ^[16]	5	_	ns		
t _{HZBE}	BLE/BHE HIGH to High Z ^[16, 17]	_	18	ns		
Write Cycle ^[18, 19]						
t _{WC}	Write cycle time	45	_	ns		
t _{SCE}	CE LOW to write end	35	_	ns		
t _{AW}	Address setup to write end	35	_	ns		
t _{HA}	Address hold from write end	0	_	ns		
t _{SA}	Address setup to write start	0	_	ns		
t _{PWE}	WE pulse width	35	_	ns		
t _{BW}	BLE/BHE LOW to write end	35	_	ns		
t _{SD}	Data setup to write end	25	_	ns		
t _{HD}	Data hold from write end	0	_	ns		
t _{HZWE}	WE LOW to High Z [16, 17]	-	18	ns		
t _{LZWE}	WE HIGH to Low Z [16]	10	_	ns		

 ^{14.} Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1 V/ns) or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3 V, and output loading of the specified l_{OL}/l_{OH} as shown in Figure 2 on page 5.
 15. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes AN13842 and AN66311. However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in

production.

16. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZDE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.

17. t_{HZOE}, t_{HZDE}, t_{HZDE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.

^{18.} The internal write time of the memory is defined by the overlap of WE, CE = V_{IL}, BHE, BLE or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

^{19.} The minimum write cycle pulse width for Write Cycle No. 3 (WE Controlled, OE LOW) should be equal to the sum of tsp and thzwe.



Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) $^{[20,\ 21]}$

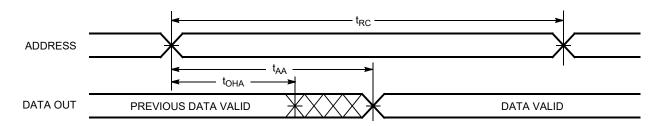
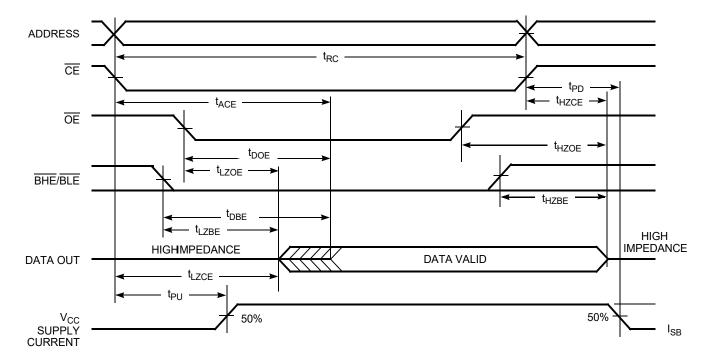


Figure 5. Read Cycle No. 2 (OE Controlled) [21, 22]



^{20.} The device is continuously selected. $\overline{\text{OE}}$, $\overline{\text{CE}} = \text{V}_{\text{IL}}$, $\overline{\text{BHE}}$, $\overline{\text{BLE}}$, or both = V_{IL} . 21. WE is HIGH for read cycle. 22. Address valid before or similar to $\overline{\text{CE}}$, $\overline{\text{BHE}}$, $\overline{\text{BLE}}$ transition LOW.



Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 (WE Controlled) [23, 24, 25]

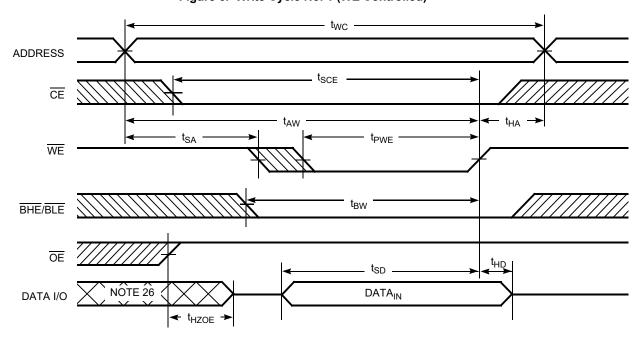
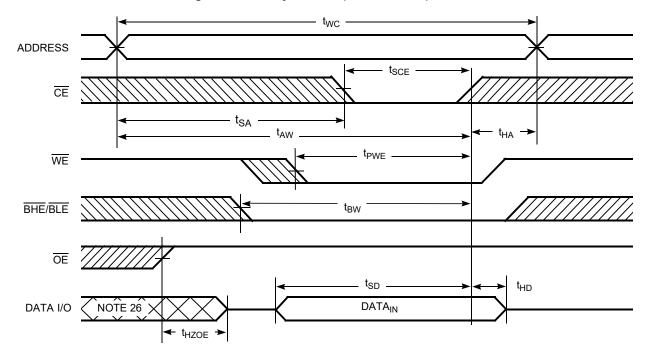


Figure 7. Write Cycle No. 2 (CE Controlled) [23, 24, 25]



Notes

- 23. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 24. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ = V_{IH} , the output remains in a high impedance state.
- 25. The internal write time of the memory is defined by the overlap of WE, $\overline{\text{CE}} = V_{\parallel L}$, $\overline{\text{BHE}}$, $\overline{\text{BLE}}$ or both = $V_{\parallel L}$. All signals must be active to initiate a write and any of these signals can terminate the write by going inactive. The input setup and hold timing must be referenced to the edge of the signal that terminate the write.

 26. During this period, the I/Os are in output state. Do not apply input signals.



Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [27, 28, 30]

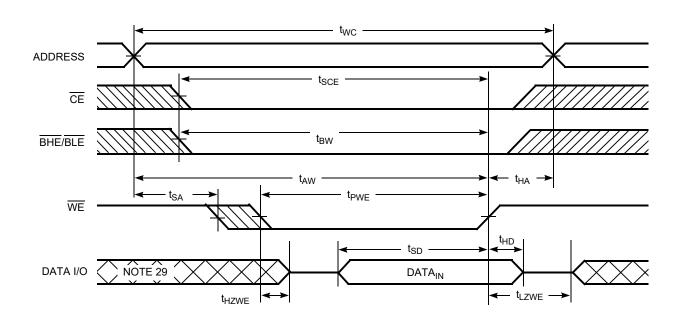
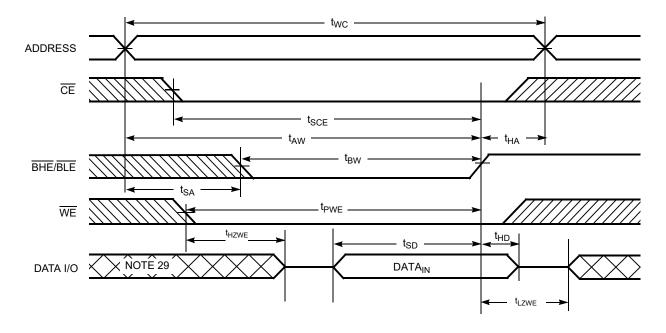


Figure 9. Write Cycle No. 4 (BHE/BLE Controlled, OE LOW) [27, 28]



- 27. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ = V_{IH} , the output remains in a high impedance state.
- 28. The internal write time of the memory is defined by the overlap of WE, $\overline{CE} = V_{\parallel}$, \overline{BHE} , \overline{BLE} or both = V_{\parallel} . All signals must be active to initiate a write and any of these signals can terminate the write by going inactive. The input setup and hold timing must be referenced to the edge of the signal that terminate the write.

 29. During this period, the I/Os are in output state. Do not apply input signals.

 30. The minimum write cycle pulse width should be equal to the sum of tsd and thzwe.



Truth Table

CE [31]	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
Н	Х	Х	X ^[31]	X ^[31]	High Z	Deselect/power down	Standby (I _{SB})
L	Χ	Χ	Н	Н	High Z	Output disabled	Active (I _{CC})
L	Н	L	L	L	Data out (I/O ₀ -I/O ₁₅)	Read	Active (I _{CC})
L	Н	L	Н	L	Data out (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High-Z	Read	Active (I _{CC})
L	Н	L	L	Н	Data out (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High-Z	Read	Active (I _{CC})
L	Н	Н	L	L	High Z	Output disabled	Active (I _{CC})
L	Н	Н	Н	L	High Z	Output disabled	Active (I _{CC})
L	Н	Н	L	Н	High Z	Output disabled	Active (I _{CC})
L	L	Χ	L	L	Data in (I/O ₀ –I/O ₁₅)	Write	Active (I _{CC})
L	L	Х	Н	L	Data in (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High Z	Write	Active (I _{CC})
L	L	Х	L	Н	Data in (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High Z	Write	Active (I _{CC})

Note
31. Chip enable ($\overline{\text{CE}}$) and byte enables ($\overline{\text{BHE}}$ and $\overline{\text{BLE}}$) must be at CMOS levels (not floating) to meet the I_{SB2} / I_{CCDR} spec. Intermediate voltage levels on these pins is not permitted.

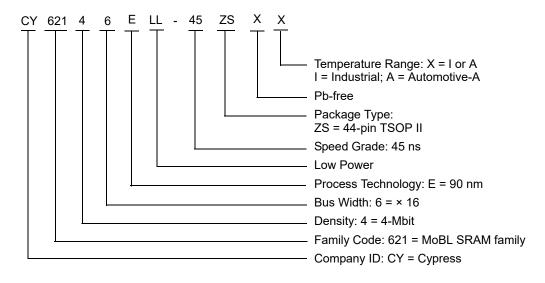


Ordering Information

;	Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
	45	CY62146ELL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	Industrial

Contact your local Cypress sales representative for availability of these parts.

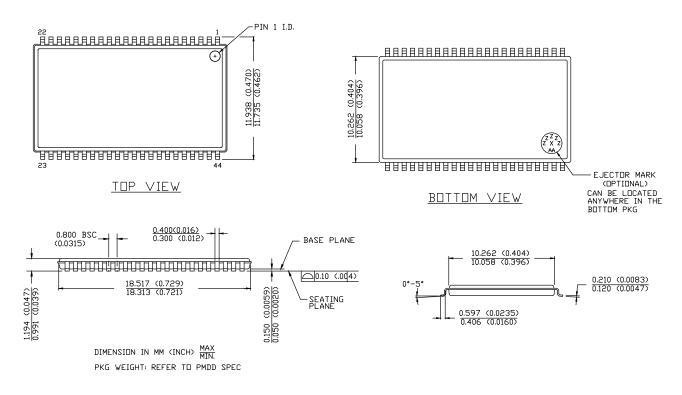
Ordering Code Definitions





Package Diagram

Figure 10. 44-pin TSOP II (18.4 × 10.2 × 1.194 mm) Package Outline, 51-85087



51-85087 *F



Acronyms

Acronym	Description
BHE	Byte High Enable
BLE	Byte Low Enable
CE	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
OE	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Gird Array
WE	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure		
°C	degree Celsius		
MHz	megahertz		
μΑ	microampere		
mA	milliampere		
ns	nanosecond		
Ω	ohm		
pF	picofarad		
V	volt		
W	watt		



Document History Page

Document Number: 001-07970					
Rev.	ECN No.	Submission Date	Description of Change		
**	463213	05/19/2006	New data sheet.		
*A	684343	01/17/2007	Added Automotive-A Temperature Range related information in all instances across the document and made the information Preliminary (by shading in required places). Updated Ordering Information: Updated part numbers.		
*B	925501	04/09/2007	Updated Electrical Characteristics: Added Note 8 and referred the same note in I _{SB2} parameter. Updated Data Retention Characteristics: Added Note 11 and referred the same note in I _{CCDR} parameter. Updated Switching Characteristics: Added Note 15 and referred the same note in "Parameter" column.		
*C	1045260	05/07/2007	Changed status of Automotive-A Temperature Range related information from Preliminary to Final (by unshading in required places). Updated Ordering Information: No change in part numbers. Unshaded the Automotive-A MPNs (Changed status from Preliminary to Final).		
*D	2073548	02/06/2008	Updated Data Retention Waveform: Updated Figure 3 (Corrected typo). Removed Note "BHE. BLE is the AND of BHE and BLE. Deselect the chip by either disabling the chip enable signals or by disabling BHE and BLE." and its reference. Updated to new template.		
*E	2943752	06/03/2010	Updated Truth Table: Added Note 31 and referred the same note in "CE" column. Updated Package Diagram: spec 51-85087 – Changed revision from *A to *C. Updated to new template.		
*F	3109050	12/13/2010	Changed Table Footnotes to Notes in all instances across the document. Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions.		
*G	3149059	01/20/2011	Updated Ordering Information: No change in part numbers. Updated Ordering Code Definitions (Corrected Errors). Added Acronyms and Units of Measure. Updated to new template. Completing Sunset Review.		
*H	3296704	06/29/2011	Updated Functional Description: Updated description (Removed "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.").		
*	3921993	03/05/2013	Updated Switching Waveforms: Added Note 25 and referred the same note in Figure 6, Figure 7. Removed Note "WE is HIGH for read cycle." and its references in Figure 6, Figure 7. Added Note 28 and referred the same note in Figure 8, Figure 9. Updated Package Diagram: spec 51-85087 – Changed revision from *C to *E. Completing Sunset Review.		



Document History Page (continued)

Rev.	ECN No.	Submission Date	Description of Change	
*J	4013949	06/04/2013	Updated Functional Description: Updated description. Updated Electrical Characteristics: Updated Electrical Characteristics: Added one more Test Condition " $V_{CC} = 5.5 \text{ V}$, $I_{OH} = -0.1 \text{ mA}$ " for V_{OH} parameter and added maximum value corresponding to that Test Condition. Added Note 7 and referred the same note in maximum value for V_{OH} parameter corresponding to Test Condition " $V_{CC} = 5.5 \text{ V}$, $I_{OH} = -0.1 \text{ mA}$ ".	
*K	4102022	08/14/2013	Updated Switching Characteristics: Updated Note 15. Updated to new template.	
*L	4576478	11/21/2014	Updated Functional Description: Added "For a complete list of related documentation, click here." at the end. Updated Switching Characteristics: Added Note 19 and referred the same note in "Write Cycle". Updated Switching Waveforms: Added Note 30 and referred the same note in Figure 8.	
*M	5196888	04/14/2016	Updated Thermal Resistance: Updated values of Θ_{JA} and Θ_{JC} parameters in "44-pin TSOP II" column. Updated to new template. Completing Sunset Review.	
*N	6049346	01/29/2018	Updated Ordering Information: Updated part numbers. Updated to new template. Completing Sunset Review.	
*O	6560791	04/29/2019	Updated to new template.	
*P	6906316	06/26/2020	Updated Features: Changed value of Typical standby current from 1 μA to 2.5 μA. Changed value of Typical active current from 2 mA to 3.5 mA. Updated Product Portfolio: Changed typical value of Operating I_{CC} from 2 mA to 3.5 mA corresponding to "f = 1 MHz". Changed maximum value of Operating I_{CC} from 2.5 mA to 6 mA corresponding to "f = 1 MHz". Changed typical value of Standby, I_{SB2} from 1 μA to 2.5 μA. Updated Electrical Characteristics: Changed typical value of I_{CC} parameter from 2 mA to 3.5 mA corresponding to Test Condition "f = 1 MHz". Changed maximum value of I_{CC} parameter from 2.5 mA to 6 mA corresponding to Test Condition "f = 1 MHz". Changed typical value of I_{SB2} parameter from 1 μA to 2.5 μA. Updated Data Retention Characteristics: Changed typical value of I_{CCDR} parameter from 1 μA to 3 μA. Changed maximum value of I_{CCDR} parameter from 7 μA to 8.8 μA. Updated Package Diagram: spec 51-85087 – Changed revision from *E to *F.	



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