X5323, X5325 (Replaces X25323, X25325)

CPU Supervisor with 32kBit SPI EEPROM

FN8131
Rev 3.00
December 9, 2015

These devices combine four popular functions, Power-on Reset Control, Watchdog Timer, Supply Voltage Supervision, and Block Lock Protect Serial EEPROM Memory in one package. This combination lowers system cost, reduces board space requirements, and increases reliability.

Applying power to the device activates the power-on reset circuit which holds $\overline{\text{RESET}}$/RESET active for a period of time. This allows the power supply and oscillator to stabilize before the processor can execute code.

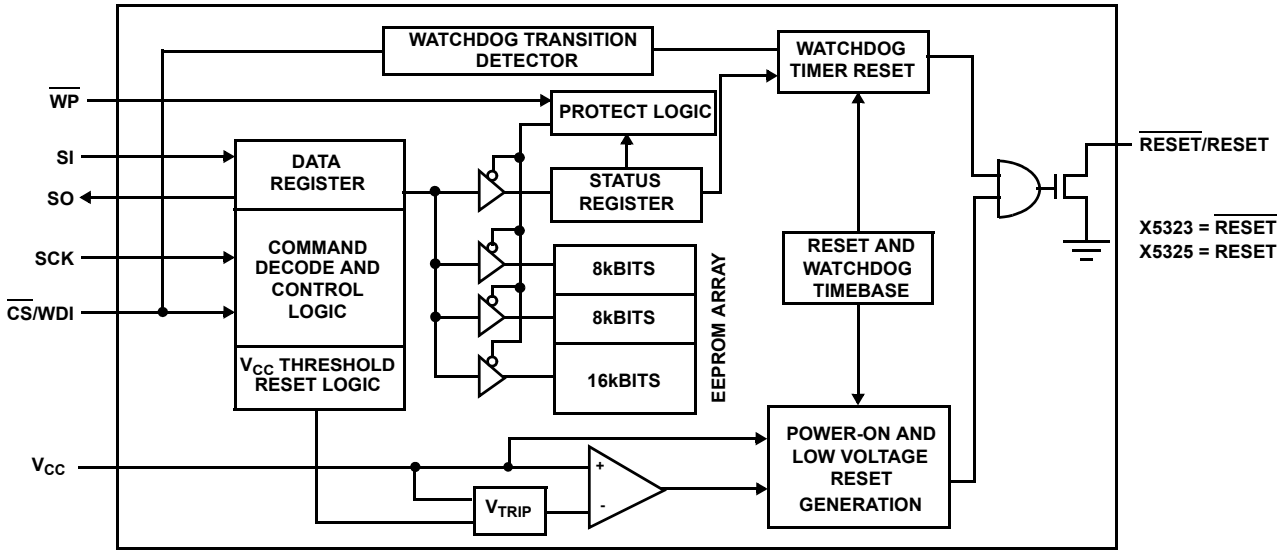
The Watchdog Timer provides an independent protection mechanism for microcontrollers. When the microcontroller fails to restart a timer within a selectable time out interval, the device activates the $\overline{\text{RESET}}$/RESET signal. The user selects the interval from three preset values. Once selected, the interval does not change, even after cycling the power.

The device's low V_{CC} detection circuitry protects the user's system from low voltage conditions, resetting the system when V_{CC} falls below the minimum V_{CC} trip point. $\overline{\text{RESET}}$/RESET is asserted until V_{CC} returns to proper operating level and stabilizes. Five industry standard V_{TRIP} thresholds are available, however, Intersil's unique circuits allow the threshold to be reprogrammed to meet custom requirements or to fine-tune the threshold for applications requiring higher precision.

Features

- Selectable watchdog timer
- Low V_{CC} detection and reset assertion
  - Five standard reset threshold voltages
  - Re-program low V_{CC} reset threshold voltage using special programming sequence
  - Reset signal valid to V_{CC} = 1V
- Determine watchdog or low voltage reset with a volatile flag bit
- Long battery life with low power consumption
  - <50µA max standby current, watchdog on
  - <1µA max standby current, watchdog off
  - <400µA max active current during read
- 32kbits of EEPROM
- Built-in inadvertent write protection
  - Power-up/power-down protection circuitry
  - Protect 0, 1/4, 1/2 or all of EEPROM array with Block Lock™ protection
  - In circuit programmable ROM mode
- 2MHz SPI interface modes (0,0 and 1,1)
- Minimize EEPROM programming time
  - 32-byte page write mode
  - Self-timed write cycle
  - 5ms write cycle time (typical)
- 2.7V to 5.5V and 4.5V to 5.5V power supply operation
- Available packages
  - 14 Ld TSSOP, 8 Ld SOIC, 8 Ld PDIP
- Pb-free (RoHS compliant)

Block Diagram



Ordering Information

PART NUMBER	PART MARKING	V_{CC} RANGE (V)	V_{TRIP} RANGE (V)	TEMP RANGE (°C)	PACKAGE
$\overline{\text{RESET}}$ (Active Low)					
X5323PZ-4.5A (Note) **(No longer available, recommended replacement: X5323S8Z-4.5A)**	X5323P ZAL	4.5 to 5.5	4.5 to 4.75	0 to +70	8 Ld PDIP** (Pb-free)
X5323PIZ-4.5A (Note) **(No longer available, recommended replacement: X5323S8IZ-4.5A)**	X5323P ZAM			-40 to +85	8 Ld PDIP** (Pb-free)
X5323S8Z-4.5A (Note)	X5323 ZAL			0 to +70	8 Ld SOIC (Pb-free)
X5323S8IZ-4.5A* (Note)	X5323 ZAM			-40 to +85	8 Ld SOIC (Pb-free)
X5323V14-4.5A	X5323 VAL			0 to +70	14 Ld TSSOP
X5323PZ (Note) **(No longer available, recommended replacement: X5323S8Z)**	X5323P Z	4.5 to 5.5	4.25 to 4.5	0 to +70	8 Ld PDIP** (Pb-free)
X5323PIZ (Note) **(No longer available, recommended replacement: X5323S8IZ)**	X5323P ZI			-40 to +85	8 Ld PDIP** (Pb-free)
X5323S8Z* (Note)	X5323 Z			0 to +70	8 Ld SOIC (Pb-free)
X5323S8IZ* (Note)	X5323 ZI			-40 to +85	8 Ld SOIC (Pb-free)
X5323PZ-2.7A (Note) **(No longer available, recommended replacement: X5323S8Z-2.7A)**	X5323P ZAN	2.7 to 5.5	2.85 to 3.0	0 to +70	8 Ld PDIP** (Pb-free)
X5323PIZ-2.7A (Note) **(No longer available, recommended replacement: X5323S8IZ-2.7A)**	X5323P ZAP			-40 to +85	8 Ld PDIP** (Pb-free)
X5323S8Z-2.7A* (Note)	X5323 ZAN			0 to +70	8 Ld SOIC (Pb-free)
X5323S8IZ-2.7A* (Note)	X5323 ZAP			-40 to +85	8 Ld SOIC (Pb-free)
X5323PZ-2.7 (Note) **(No longer available, recommended replacement: X5323S8Z-2.7)**	X5323P ZF	2.7 to 5.5	2.55 to 2.7	0 to +70	8 Ld PDIP** (Pb-free)
X5323PIZ-2.7 (Note) **(No longer available, recommended replacement: X5323S8IZ-2.7)**	X5323P ZG			-40 to +85	8 Ld PDIP** (Pb-free)
X5323S8Z-2.7* (Note)	X5323 ZF			0 to +70	8 Ld SOIC (Pb-free)
X5323S8IZ-2.7* (Note)	X5323 ZG			-40 to +85	8 Ld SOIC (Pb-free)
RESET (Active High)					
X5325S8Z-4.5A (Note)	X5325 ZAL	4.5 to 5.5	4.5 to 4.75	0 to +70	8 Ld SOIC (Pb-free)
X5325S8IZ-4.5A (Note)	X5325 ZAM			-40 to +85	8 Ld SOIC (Pb-free)
X5325S8Z* (Note)	X5325 Z	4.5 to 5.5	4.25 to 4.5	0 to +70	8 Ld SOIC (Pb-free)
X5325S8IZ* (Note)	X5325 ZI			-40 to +85	8 Ld SOIC (Pb-free)
X5325S8Z-2.7A (Note)	X5325 ZAN	2.7 to 5.5	2.85 to 3.0	0 to +70	8 Ld SOIC (Pb-free)
X5325S8IZ-2.7A (Note)	X5325 ZAP			-40 to +85	8 Ld SOIC (Pb-free)
X5325S8Z-2.7* (Note)	X5325 ZF	2.7 to 5.5	2.55 to 2.7	0 to +70	8 Ld SOIC (Pb-free)
X5325S8IZ-2.7* (Note)	X5325 ZG			-40 to +85	8 Ld SOIC (Pb-free)

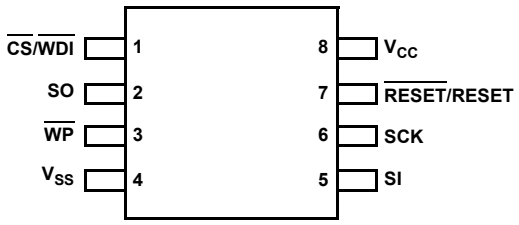
*Add “-T1” for tape and reel. Please refer to TB347 for details on reel specifications.

**Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

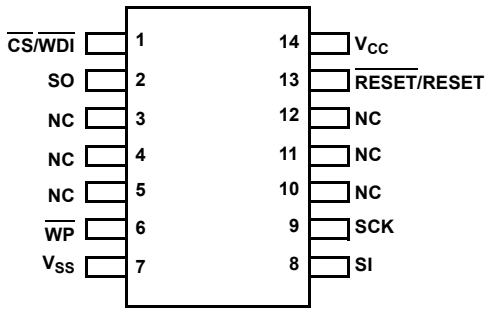
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts

X5323, X5325
(8 LD SOIC, PDIP)
TOP VIEW



X5323, X5325
(14 LD TSSOP)
TOP VIEW



Pin Descriptions

PIN NUMBER (SOIC/PDIP)	PIN NUMBER TSSOP	PIN NAME	PIN FUNCTION
1	1	$\overline{CS}$/WDI	**Chip Select Input.** $\overline{CS}$ HIGH, deselects the device and the SO output pin is at a high impedance state. Unless a nonvolatile write cycle is underway, the device will be in the stand-by power mode. $\overline{CS}$ LOW enables the device, placing it in the active power mode. Prior to the start of any operation after power-up, a HIGH to LOW transition on $\overline{CS}$ is required. **Watchdog Input.** A HIGH to LOW transition on the WDI pin restarts the watchdog timer. The absence of a HIGH to LOW transition within the watchdog time out period results in $\overline{RESET}$/RESET going active.
2	2	SO	**Serial Output.** SO is a push/pull serial data output pin. A read cycle shifts data out on this pin. The falling edge of the serial clock (SCK) clocks the data out.
5	8	SI	**Serial Input.** SI is a serial data input pin. Input all opcodes, byte addresses, and memory data on this pin. The rising edge of the serial clock (SCK) latches the input data. Send all opcodes (Table 1), addresses and data MSB first.
6	9	SCK	**Serial Clock.** The serial clock controls the serial bus timing for data input and output. The rising edge of SCK latches in the opcode, address, or data bits present on the SI pin. The falling edge of SCK changes the data output on the SO pin.
3	6	$\overline{WP}$	**Write Protect.** The $\overline{WP}$ pin works in conjunction with a nonvolatile WPEN bit to “lock” the setting of the watchdog timer control and the memory write protect bits.
4	7	V_{SS}	Ground
8	14	V_{CC}	Supply Voltage
7	13	$\overline{RESET}$/ RESET	**Reset Output**. $\overline{RESET}$/RESET is an active LOW/HIGH, open drain output which goes active whenever V_{CC} falls below the minimum V_{CC} sense level. It will remain active until V_{CC} rises above the minimum V_{CC} sense level for 200ms. $\overline{RESET}$/RESET goes active if the watchdog timer is enabled and $\overline{CS}$ remains either HIGH or LOW longer than the selectable watchdog time out period. A falling edge of $\overline{CS}$ will reset the watchdog timer. $\overline{RESET}$/RESET goes active on power-up at about 1V and remains active for 200ms after the power supply stabilizes.
	3 to 5,10 to 12	NC	No internal connections

Principles of Operation

Power-on Reset

Application of power to the X5323/X5325 activates a power-on reset circuit. This circuit goes active at about 1V and pulls the $\overline{RESET}$/RESET pin active. This signal prevents the system microprocessor from starting to operate with insufficient voltage or prior to stabilization of the oscillator. As long as $\overline{RESET}$/RESET pin is active, the device will not respond to any Read/Write instruction. When V_{CC} exceeds the device V_{TRIP} value for 200ms (nominal) the circuit releases $\overline{RESET}$/RESET, allowing the processor to begin executing code.

Low Voltage Monitoring

During operation, the X5323/X5325 monitors the V_{CC} level and asserts $\overline{RESET}$/RESET if supply voltage falls below a preset minimum V_{TRIP}. The $\overline{RESET}$/RESET signal prevents the microprocessor from operating in a power fail or brown-out condition. The $\overline{RESET}$/RESET signal remains active until the voltage drops below 1V. It also remains active until V_{CC} returns and exceeds V_{TRIP} for 200ms.

Watchdog Timer

The watchdog timer circuit monitors the microprocessor activity by monitoring the WDI input. The microprocessor must toggle the $\overline{CS}$/WDI pin periodically to prevent a $\overline{RESET}$/RESET signal. The $\overline{CS}$/WDI pin must be toggled from HIGH to LOW prior to the expiration of the watchdog time out period. The state of two nonvolatile control bits in the status register determine the watchdog timer period. The microprocessor can change these watchdog bits, or they may be "locked" by tying the $\overline{WP}$ pin LOW and setting the WPEN bit HIGH.

V_{CC} Threshold Reset Procedure

The X5323/X5325 has a standard V_{CC} threshold (V_{TRIP}) voltage. This value will not change over normal operating and storage conditions. However, in applications where the standard V_{TRIP} is not exactly right, or for higher precision in the V_{TRIP} value, the X5323/X5325 threshold may be adjusted.

Setting the V_{TRIP} Voltage

This procedure sets the V_{TRIP} to a higher voltage value. For example, if the current V_{TRIP} is 4.4V and the new V_{TRIP} is 4.6V, this procedure directly makes the change. If the new setting is lower than the current setting, then it is necessary to reset the trip point before setting the new value.

To set the new V_{TRIP} voltage, apply the desired V_{TRIP} threshold to the VCC pin and tie the $\overline{CS}$/WDI pin and the $\overline{WP}$ pin HIGH. $\overline{RESET}$/RESET and SO pins are left unconnected. Then apply the programming voltage V_P to both SCK and SI and pulse $\overline{CS}$/WDI LOW then HIGH. Remove V_P and the sequence is complete.

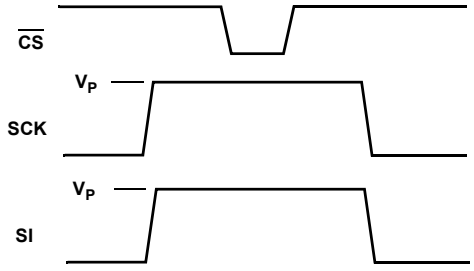


FIGURE 1. SET V_{TRIP} VOLTAGE

Resetting the V_{TRIP} Voltage

This procedure sets the V_{TRIP} to a "native" voltage level. For example, if the current V_{TRIP} is 4.4V and the V_{TRIP} is reset, the new V_{TRIP} is something less than 1.7V. This procedure must be used to set the voltage to a lower value.

To reset the V_{TRIP} voltage, apply a voltage between 2.7V and 5.5V to the VCC pin. Tie the $\overline{CS}$/WDI pin, the $\overline{WP}$ pin, and the SCK pin HIGH. $\overline{RESET}$/RESET and SO pins are left unconnected. Then apply the programming voltage V_P to the SI pin ONLY and pulse $\overline{CS}$/WDI LOW then HIGH. Remove V_P and the sequence is complete.

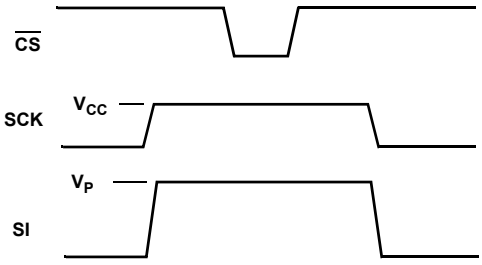


FIGURE 2. RESET V_{TRIP} VOLTAGE

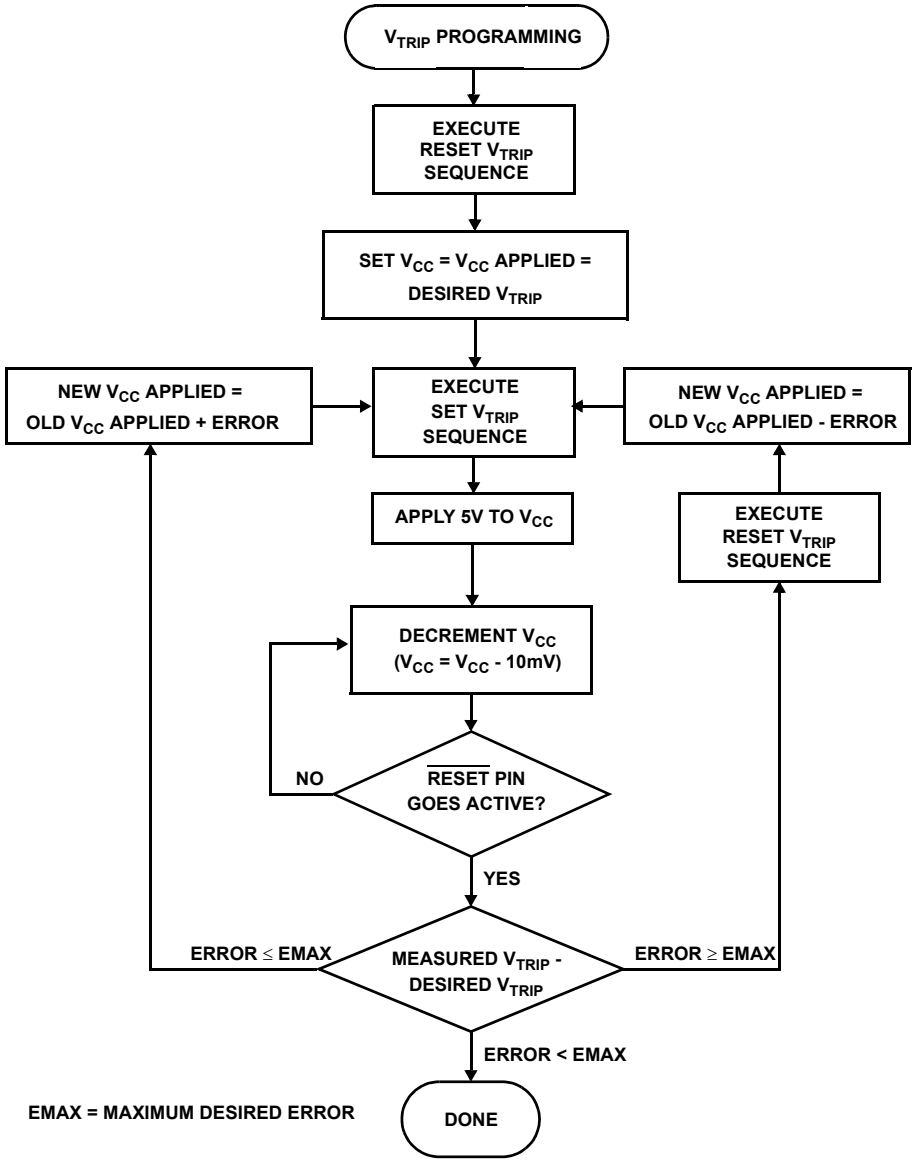


FIGURE 3. V_{TRIP} PROGRAMMING SEQUENCE FLOW CHART

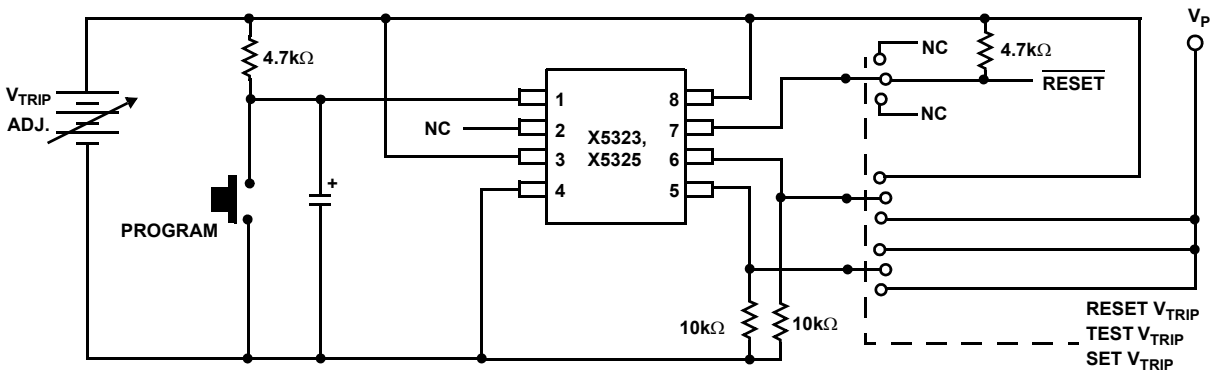


FIGURE 4. SAMPLE V_{TRIP} RESET CIRCUIT

SPI Serial Memory

The memory portion of the device is a CMOS serial EEPROM array with Intersil's block lock protection. The array is internally organized as x8. The device features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple four-wire bus.

The device utilizes Intersil's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles and a minimum data retention of 100 years.

The device is designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of many popular microcontroller families. It contains an 8-bit instruction register that is accessed via the SI input, with data being clocked in on the rising edge of SCK. $\overline{CS}$ must be LOW during the entire operation.

All instructions (Table 1), addresses and data are transferred MSB first. Data input on the SI line is latched on the first rising edge of SCK after $\overline{CS}$ goes LOW. Data is output on the SO line by the falling edge of SCK. SCK is static, allowing the user to stop the clock and then start it again to resume operations where left off.

Write Enable Latch

The device contains a write enable latch. This latch must be SET before a write operation is initiated. The WREN instruction will set the latch and the WRDI instruction will reset the latch (Figure 3). This latch is automatically reset upon a power-up condition and after the completion of a valid write cycle.

Status Register

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
WPEN	FLB	WD1	WD0	BL1	BL0	WEL	WIP

The Write-In-Progress (WIP) bit is a volatile, read only bit and indicates whether the device is busy with an internal nonvolatile write operation. The WIP bit is read using the RDSR instruction. When set to a "1", a nonvolatile write operation is in progress. When set to a "0", no write is in progress.

The Write Enable Latch (WEL) bit indicates the status of the write enable latch. When WEL = 1, the latch is set HIGH and when WEL = 0 the latch is reset LOW. The WEL bit is a volatile, read only bit. It can be set by the WREN instruction and can be reset by the WRDS instruction.

The block lock bits, BL0 and BL1, set the level of block lock protection. These nonvolatile bits are programmed using the WRSR instruction and allow the user to protect one quarter, one half, all or none of the EEPROM array. Any portion of the array that is block lock protected can be read but not written. It will remain protected until the BL bits are altered to disable block lock protection of that portion of memory.

TABLE 1. INSTRUCTION SET

INSTRUCTION NAME	INSTRUCTION FORMAT*	OPERATION
WREN	0000 0110	Set the write enable latch (enable write operations)
SFLB	0000 0000	Set flag bit
WRDI/RFLB	0000 0100	Reset the write enable latch/reset flag bit
RSDR	0000 0101	Read status register
WRSR	0000 0001	Write status register (watchdog, block lock, WPEN and flag bits)
READ	0000 0011	Read data from memory array beginning at selected address
WRITE	0000 0010	Write data to memory array beginning at selected address

NOTE: *Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

TABLE 2. BLOCK PROTECT MATRIX

WREN CMD	STATUS REGISTER	DEVICE PIN	BLOCK	BLOCK	STATUS REGISTER
WEL	WPEN	$\overline{WP}$	Protected Block	Unprotected Block	WPEN, BL0, BL1 WD0, WD1
0	X	X	Protected	Protected	Protected
1	1	0	Protected	Writable	Protected
1	0	X	Protected	Writable	Writable
1	X	1	Protected	Writable	Writable

STATUS REGISTER BITS		ARRAY ADDRESSES PROTECTED
BL1	BL0	X5323/X5325
0	0	None (factory default)
0	1	$0C00 to $0FFF
1	0	$0800 to $0FFF
1	1	$0000 to $0FFF

The watchdog timer bits, WD0 and WD1, select the watchdog time out period. These nonvolatile bits are programmed with the WRSR instruction.

STATUS REGISTER BITS		WATCHDOG TIME-OUT (TYPICAL)
WD1	WD0	
0	0	1.4s
0	1	600ms
1	0	200ms
1	1	disabled (factory default)

The FLAG bit shows the status of a volatile latch that can be set and reset by the system using the SFLB and RFLB instructions. The flag bit is automatically reset upon power-up. This flag can be used by the system to determine whether a reset occurs as a result of a watchdog time out or power failure.

Note: The Watch Dog Timer is shipped disabled. (WD1 = 1, WD0 = 1. The factory default for Memory Block Protection is ‘None’. (BL1 = 0, BL0 = 0).

The nonvolatile WPEN bit is programmed using the WRSR instruction. This bit works in conjunction with the $\overline{WP}$ pin to provide an in-circuit programmable ROM function (Table 2). $\overline{WP}$ is LOW and WPEN bit programmed HIGH disables all status register write operations.

In Circuit Programmable ROM Mode

This mechanism protects the block lock and watchdog bits from inadvertent corruption.

In the locked state (programmable ROM mode) the $\overline{WP}$ pin is LOW and the nonvolatile bit WPEN is “1”. This mode disables nonvolatile writes to the device’s status register.

Setting the $\overline{WP}$ pin LOW while WPEN is a “1” while an internal write cycle to the status register is in progress will not stop this write operation, but the operation disables subsequent write attempts to the status register.

When $\overline{WP}$ is HIGH, all functions, including nonvolatile writes to the status register operate normally. Setting the WPEN bit in the status register to “0” blocks the $\overline{WP}$ pin function, allowing writes to the status register when $\overline{WP}$ is HIGH or LOW. Setting the WPEN bit to “1” while the $\overline{WP}$ pin is LOW activates the programmable ROM mode, thus requiring a change in the $\overline{WP}$ pin prior to subsequent status register changes. This allows manufacturing to install the device in a system with $\overline{WP}$ pin grounded and still be able to program the status register. Manufacturing can then load configuration data, manufacturing time and other parameters into the EEPROM, then set the portion of memory to be protected by setting the block lock bits, and finally set the “OTP mode” by setting the WPEN bit. Data changes now require a hardware change.

Read Sequence

When reading from the EEPROM memory array, $\overline{CS}$ is first pulled low to select the device. The 8-bit READ instruction is transmitted to the device, followed by the 16-bit address. After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to address

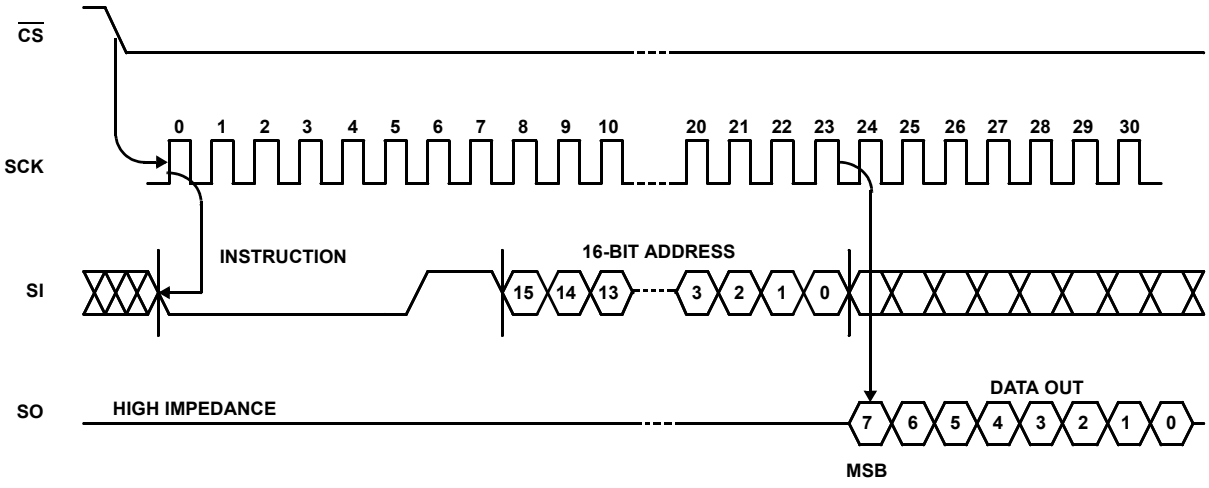


FIGURE 5. READ EEPROM ARRAY SEQUENCE

$0000 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ high. Refer to the read EEPROM Array Sequence (Figure 1).

To read the status register, the $\overline{CS}$ line is first pulled low to select the device followed by the 8-bit RDSR instruction. After the RDSR opcode is sent, the contents of the status register are shifted out on the SO line. Refer to the read status register sequence (Figure 2).

Write Sequence

Prior to any attempt to write data into the device, the “Write Enable” Latch (WEL) must first be set by issuing the WREN instruction (Figure 3). $\overline{CS}$ is first taken LOW, then the WREN instruction is clocked into the device. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the write operation without taking $\overline{CS}$ HIGH after issuing the WREN instruction, the write operation will be ignored.

To write data to the EEPROM memory array, the user then issues the WRITE instruction followed by the 16-bit address and then the data to be written. Any unused address bits are specified to be “0’s”. The WRITE operation minimally takes 32 clocks. $\overline{CS}$ must go low and remain low for the duration of the operation. If the address counter reaches the end of a page and the clock continues, the counter will roll back to the first address of the page and overwrite any data that may have been previously written.

Note: When writing more than one page, you must wait one write cycle (10ms typical) when going from one page to another. This is required for the internal nonvolatile memory to be programmed correctly.

For the page write operation (byte or page write) to be completed, $\overline{CS}$ can only be brought HIGH after bit 0 of the last data byte to be written is clocked in. If it is brought HIGH at any other time, the write operation will not be completed (Figure 4).

To write to the status register, the WRSR instruction is followed by the data to be written (Figure 5). Data bits 0 and 1 must be “0”.

While the write is in progress following a status register or EEPROM Sequence, the status register may be read to check the WIP bit. During this time the WIP bit will be high.

Operational Notes

The device powers-up in the following state:

- The device is in the low power standby state.
- A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The write enable latch is reset.
- The flag bit is reset.
- Reset signal is active for t_{PURST}.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

- A WREN instruction must be issued to set the write enable latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a nonvolatile write cycle.

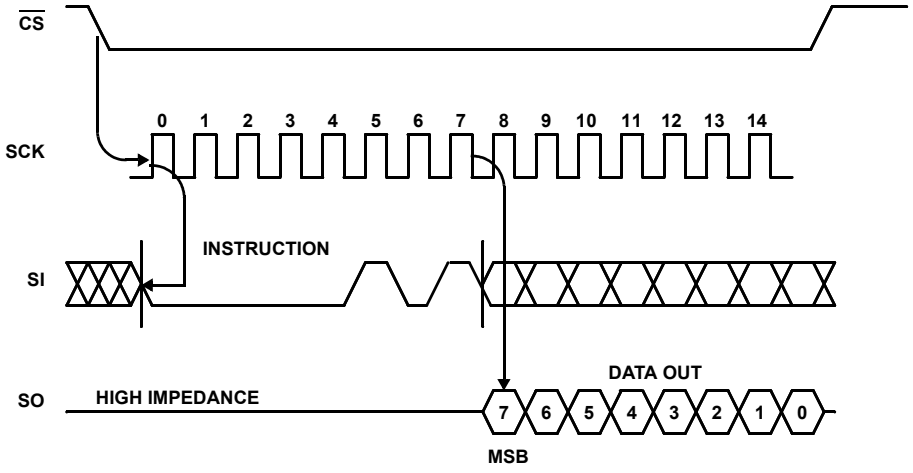


FIGURE 6. READ STATUS REGISTER SEQUENCE

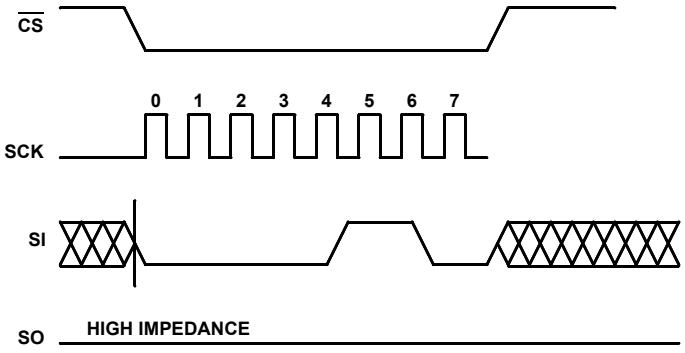


FIGURE 7. WRITE ENABLE LATCH SEQUENCE

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

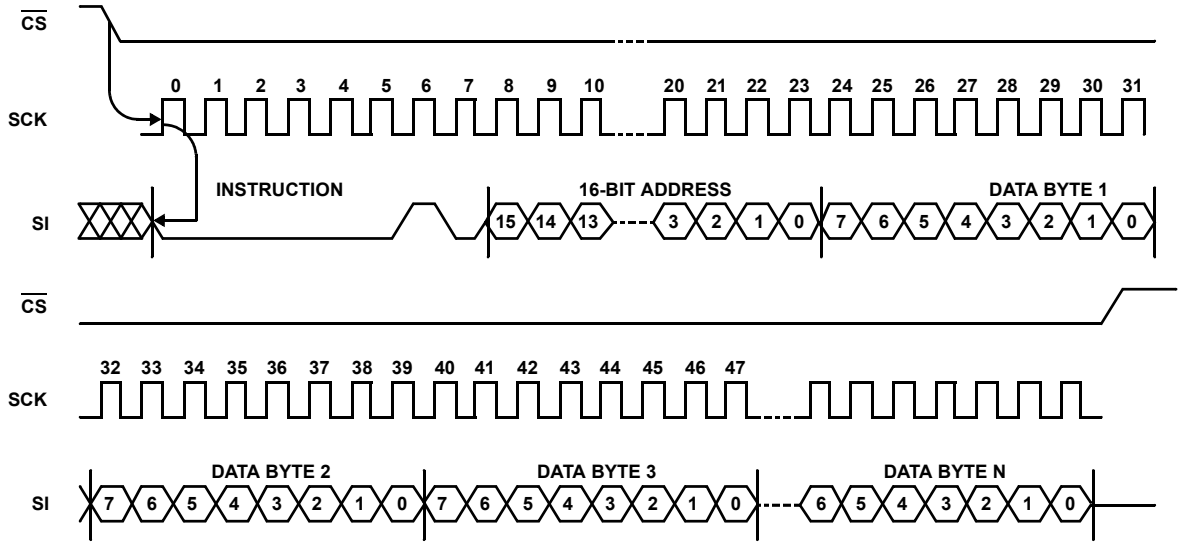


FIGURE 8. WRITE SEQUENCE

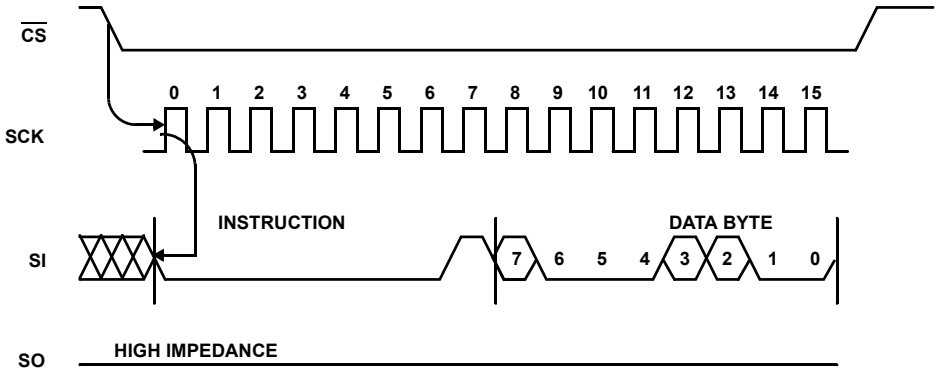


FIGURE 9. STATUS REGISTER WRITE SEQUENCE

Absolute Maximum Ratings

Temperature Under Bias . . . . . .-65°C to +135°C
Storage Temperature . . . . . .-65°C to +150°C
Voltage on any Pin with Respect to V_{SS} . . . . . .-1.0V to +7V
DC Output Current. 5mA

Operating Conditions

Temperature Range (Industrial) . . . . . .-40°C to +85°C
Temperature Range (Commercial). . . . . 0°C to +70°C
Supply Voltage Range . . . . . 2.7V to 5.5V

Thermal Information

Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

DC Electrical Specifications

Over the recommended operating conditions, unless otherwise specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} Write Current (active)	I_{CC1}	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 2MHz, SO = Open			5	mA
V_{CC} Read Current (active)	I_{CC2}	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 2MHz, SO = Open			0.4	mA
V_{CC} Standby Current WDT = OFF	I_{SB1}	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5.5V			1	µA
V_{CC} Standby Current WDT = ON	I_{SB2}	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5.5V			50	µA
V_{CC} Standby Current WDT = ON	I_{SB3}	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} =3.6V			20	µA
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}		0.1	10	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{CC}		0.1	10	µA
Input LOW Voltage	V_{IL} (Note 1)		-0.5		V_{CC} x 0.3	V
Input HIGH Voltage	V_{IH} (Note 1)		V_{CC} x 0.7		V_{CC} + 0.5	V
Output LOW Voltage	V_{OL1}	V_{CC} > 3.3V, I_{OL} = 2.1mA			0.4	V
Output LOW Voltage	V_{OL2}	2V < V_{CC} ≤ 3.3V, I_{OL} = 1mA			0.4	V
Output LOW Voltage	V_{OL3}	V_{CC} ≤ 2V, I_{OL} = 0.5mA			0.4	V
Output HIGH Voltage	V_{OH1}	V_{CC} > 3.3V, I_{OH} = -1.0mA	V_{CC} - 0.8			V
Output HIGH Voltage	V_{OH2}	2V < V_{CC} ≤ 3.3V, I_{OH} = -0.4mA	V_{CC} - 0.4			V
Output HIGH Voltage	V_{OH3}	V_{CC} ≤ 2V, I_{OH} = -0.25mA	V_{CC} - 0.2			V
Reset Output LOW Voltage	V_{OLS}	I_{OL} = 1mA			0.4	V

Capacitance

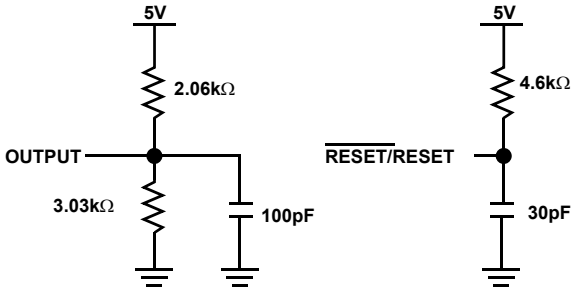
T_A = +25°C, f = 1MHz, V_{CC} = 5V

SYMBOL	TEST	CONDITIONS	MAX	UNIT
C_{OUT} (Note 2)	Output Capacitance (SO, $\overline{RESET}$/RESET)	V_{OUT} = 0V	8	pF
C_{IN} (Note 2)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$)	V_{IN} = 0V	6	pF

NOTES:

1. V_{IL} min and V_{IH} max are for reference only and are not tested.
2. This parameter is periodically sampled and not 100% tested.

Equivalent AC Load Circuit at 5V V_{CC}



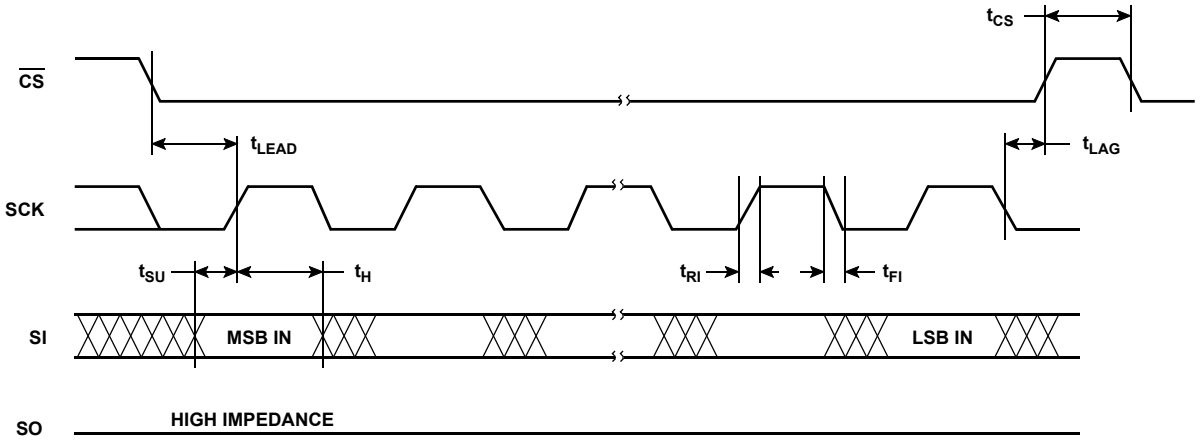
AC Test Conditions

Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing level	V_{CC} x 0.5

AC Electrical Specifications — Input pulse levels = V_{CC} x 0.1 to V_{CC} x 0.9; input rise and fall times = 10ns; input and ouput timing level = V_{CC} x 0.5. Over recommended operating conditions, unless otherwise specified.

PARAMETER	SYMBOL	2.7 TO 5.5V MIN	2.7 TO 5.5V MAX	UNIT
SERIAL INPUT TIMING				
Clock Frequency	f_{SCK}	0	2	MHz
Cycle Time	t_{CYC}	500		ns
$\overline{CS}$ Lead Time	t_{LEAD}	250		ns
$\overline{CS}$ Lag Time	t_{LAG}	250		ns
Clock HIGH Time	t_{WH}	200		ns
Clock LOW Time	t_{WL}	250		ns
Data Set-up Time	t_{SU}	50		ns
Data Hold Time	t_H	50		ns
Input Rise Time	t_{RI} (Note 3)		100	ns
Input Fall Time	t_{FI} (Note 3)		100	ns
$\overline{CS}$ Deselect Time	t_{CS}	500		ns
Write Cycle Time	t_{WC} (Note 4)		10	ms

Serial Input Timing



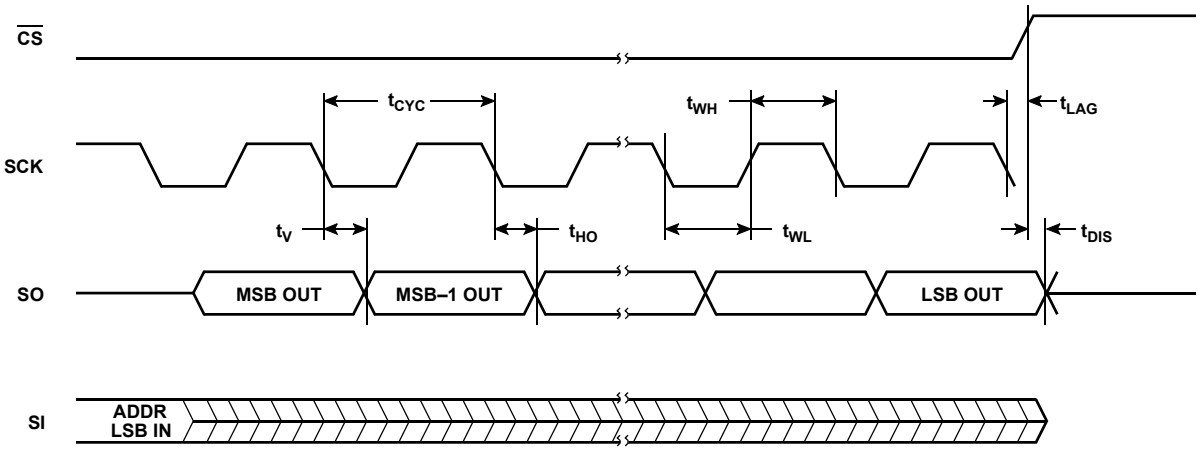
Serial Output Timing

PARAMETER	SYMBOL	2.7 TO 5.5V		UNIT
		MIN	MAX	
Clock Frequency	f_{SCK}	0	2	MHz
Output Disable Time	t_{DIS}		250	ns
Output Valid From Clock Low	t_V		250	ns
Output Hold Time	t_{HO}	0		ns
Output Rise Time	t_{RO} (Note 3)		100	ns
Output Fall Time	t_{FO} (Note 3)		100	ns

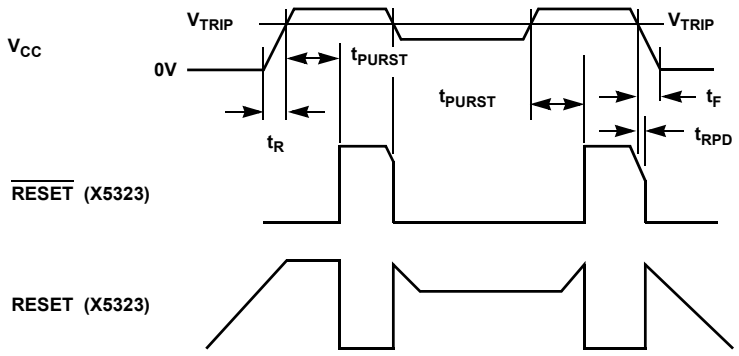
NOTES:

3. This parameter is periodically sampled and not 100% tested.
4. t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

Serial Output Timing



Power-Up and Power-Down Timing



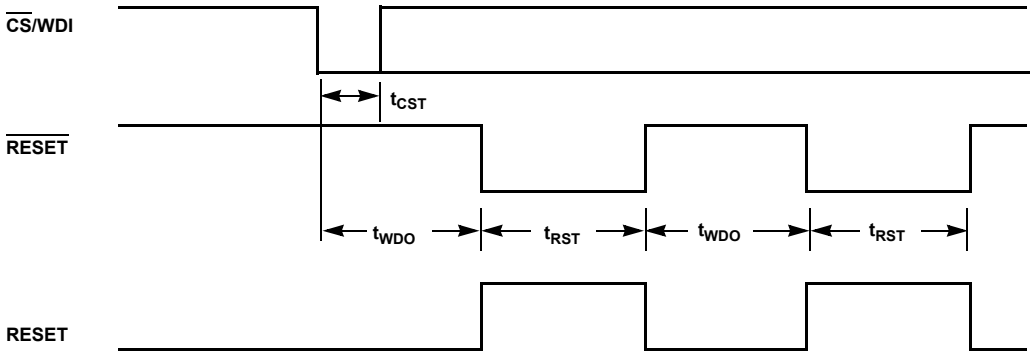
$\overline{RESET}$ Output Timing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{TRIP}	Reset Trip Point Voltage, X5323-4.5A, X5323-4.5A	4.5	4.63	4.75	V
	Reset Trip Point Voltage, X5323, X5325	4.25	4.38	4.5	V
	Reset Trip Point Voltage, X5323-2.7A, X5325-2.7A	2.85	2.92	3.0	V
	Reset Trip Point Voltage, X5323-2.7, X5325-2.7	2.55	2.63	2.7	V
V_{TH}	V_{TRIP} Hysteresis (HIGH to LOW vs LOW to HIGH V_{TRIP} Voltage)		20		mV
t_{PURST}	Power-up Reset Time-Out	100	200	280	ms
t_{RPD} (Note 5)	V_{CC} Detect To Reset/Output			500	ns
t_F (Note 5)	V_{CC} Fall Time	100			µs
t_R (Note 5)	V_{CC} Rise Time	100			µs
V_{RVALID}	Reset Valid V_{CC}	1			V

NOTE:

5. This parameter is periodically sampled and not 100% tested.

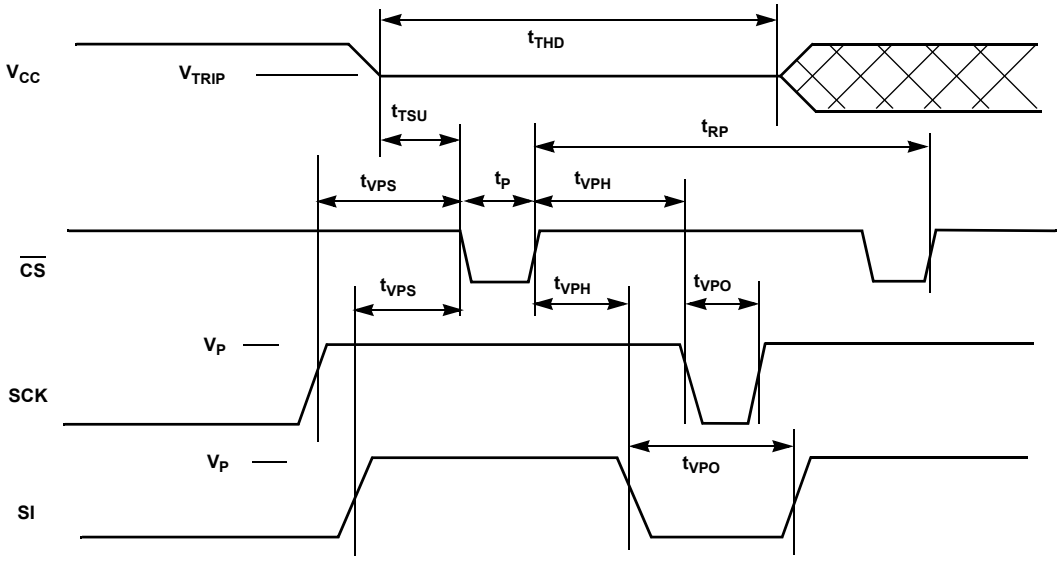
$\overline{CS}$/WDI vs RESET/$\overline{RESET}$ Timing



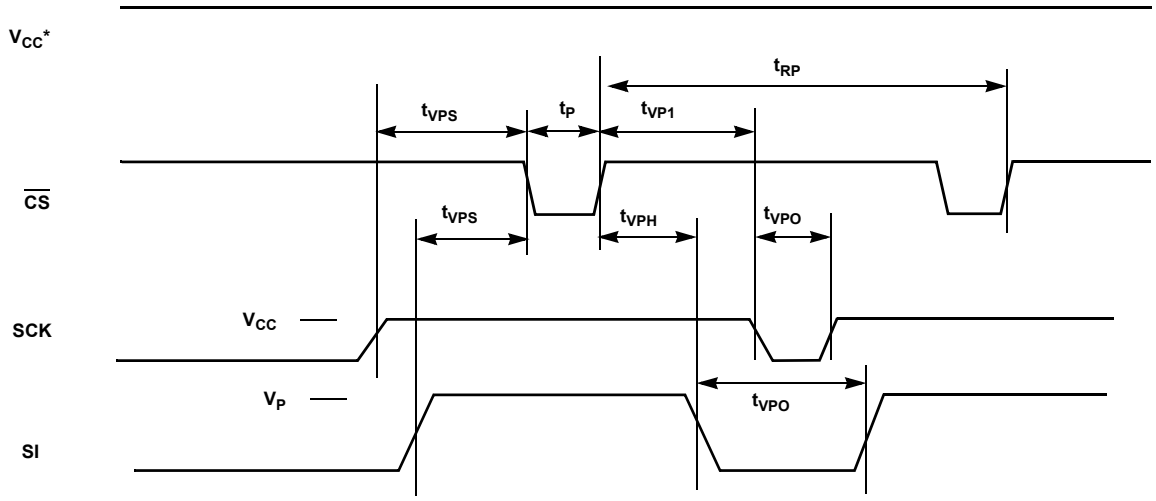
$\overline{RESET}$/RESET Output Timing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{WDO}	Watchdog Time-Out Period				
	WD1 = 1, WD0 = 0	100	200	300	ms
	WD1 = 0, WD0 = 1	450	600	800	ms
	WD1 = 0, WD0 = 0	1	1.4	2	s
t_{CST}	$\overline{CS}$ Pulse Width to Reset the Watchdog	400			ns
t_{RST}	Reset Time-Out	100	200	300	ms

V_{TRIP} Set Conditions



V_{TRIP} Reset Conditions



*V_{CC} > PROGRAMMED V_{TRIP}

V_{TRIP} Programming Specifications

V_{CC} = 1.7 to 5.5V; Temperature = 0°C to +70°C.

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
t_{VPS}	SCK V_{TRIP} Program Voltage Set-up Time	1		µs
t_{VPH}	SCK V_{TRIP} Program Voltage Hold Time	1		µs
t_P	V_{TRIP} Program Pulse Width	1		µs
t_{TSU}	V_{TRIP} Level Set-up Time	10		µs
t_{THD}	V_{TRIP} Level Hold (Stable) Time	10		ms

V_{TRIP} Programming Specifications V_{CC} = 1.7 to 5.5V; Temperature = 0°C to +70°C. **(Continued)**

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
t_{WC}	V_{TRIP} Write Cycle Time		10	ms
t_{RP}	V_{TRIP} Program Cycle Recovery Period (Between Successive Programming Cycles)	10		ms
t_{VPO}	SCK V_{TRIP} Program Voltage Off-Time Before Next Cycle	0		ms
V_P	Programming Voltage	15	18	V
V_{TRAN}	V_{TRIP} Programed Voltage Range	1.7	5.0	V
V_{ta1}	Initial V_{TRIP} Program Voltage Accuracy (V_{CC} Applied-V_{TRIP}) (Programmed at +25°C)	-0.1	+0.4	V
V_{ta2}	Subsequent V_{TRIP} Program Voltage Accuracy [(V_{CC} Applied-V_{ta1})-V_{TRIP}] (Programmed at +25°C)	-25	+25	mV
V_{tr}	V_{TRIP} Program Voltage Repeatability (Successive Program Operations; Programmed at +25°C)	-25	+25	mV
V_{tv}	V_{TRIP} Program Variation After Programming (0°C to +75°C; Programmed at +25°C)	-25	+25	mV

NOTE:

6. V_{TRIP} programming parameters are periodically sampled and are not 100% tested.

Typical Performance Curves

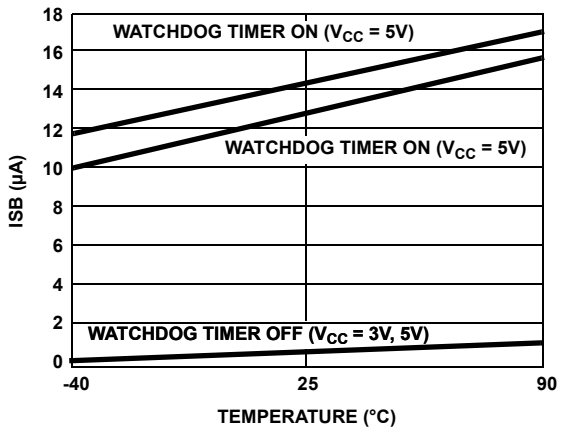


FIGURE 10. V_{CC} SUPPLY CURRENT vs TEMPERATURE (I_{SB})

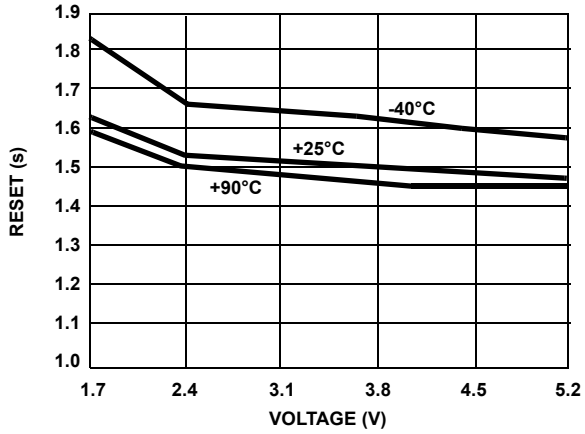


FIGURE 11. T_{WDO} vs VOLTAGE/TEMPERATURE (WD1, 0 = 1, 1)

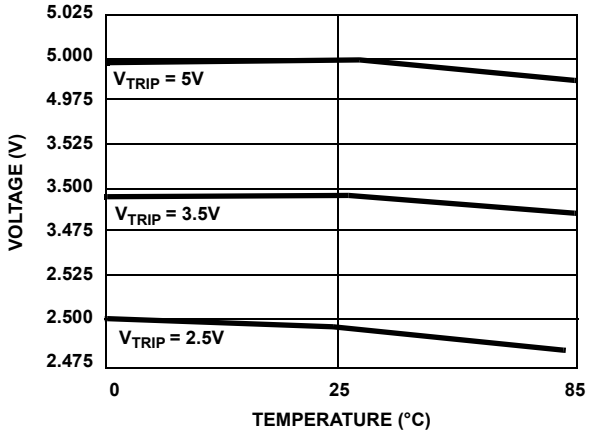


FIGURE 12. V_{TRIP} vs TEMPERATURE (PROGRAMMED AT +25°C)

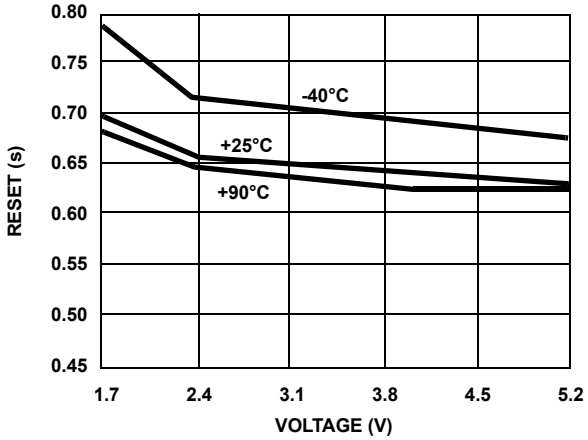


FIGURE 13. T_{WDO} vs VOLTAGE/TEMPERATURE (WD1, 0 = 1, 0)

Typical Performance Curves

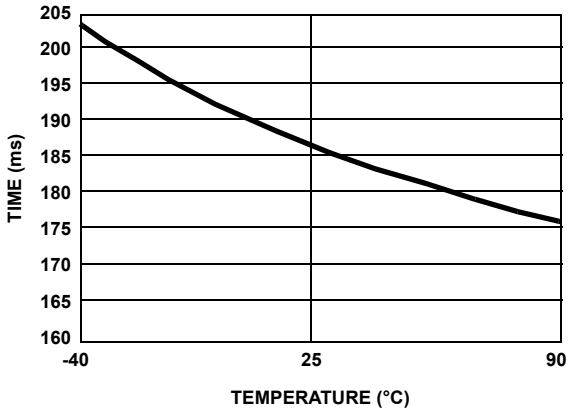


FIGURE 14. T_{PURST} vs TEMPERATURE

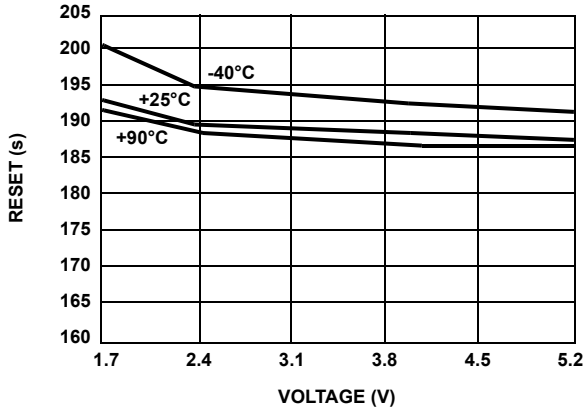


FIGURE 15. T_{WDO} vs VOLTAGE/TEMPERATURE (WD1, 0 0 = 0, 1)

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
December 9, 2015	FN8131.3	Updated Ordering Information Table on page 2. Added Revision History and About Intersil sections. Replaced POD MDP0027 with M8.15E

About Intersil

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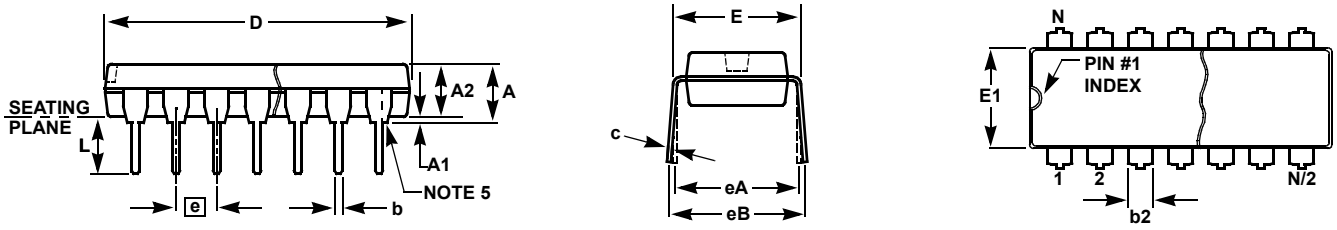
For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

Plastic Dual-In-Line Packages (PDIP)



MDP0031

PLASTIC DUAL-IN-LINE PACKAGE

SYMBOL	INCHES					TOLERANCE	NOTES
	PDIP8	PDIP14	PDIP16	PDIP18	PDIP20		
A	0.210	0.210	0.210	0.210	0.210	MAX	
A1	0.015	0.015	0.015	0.015	0.015	MIN	
A2	0.130	0.130	0.130	0.130	0.130	±0.005	
b	0.018	0.018	0.018	0.018	0.018	±0.002	
b2	0.060	0.060	0.060	0.060	0.060	+0.010/-0.015	
c	0.010	0.010	0.010	0.010	0.010	+0.004/-0.002	
D	0.375	0.750	0.750	0.890	1.020	±0.010	1
E	0.310	0.310	0.310	0.310	0.310	+0.015/-0.010	
E1	0.250	0.250	0.250	0.250	0.250	±0.005	2
e	0.100	0.100	0.100	0.100	0.100	Basic	
eA	0.300	0.300	0.300	0.300	0.300	Basic	
eB	0.345	0.345	0.345	0.345	0.345	±0.025	
L	0.125	0.125	0.125	0.125	0.125	±0.010	
N	8	14	16	18	20	Reference	

Rev. C 2/07

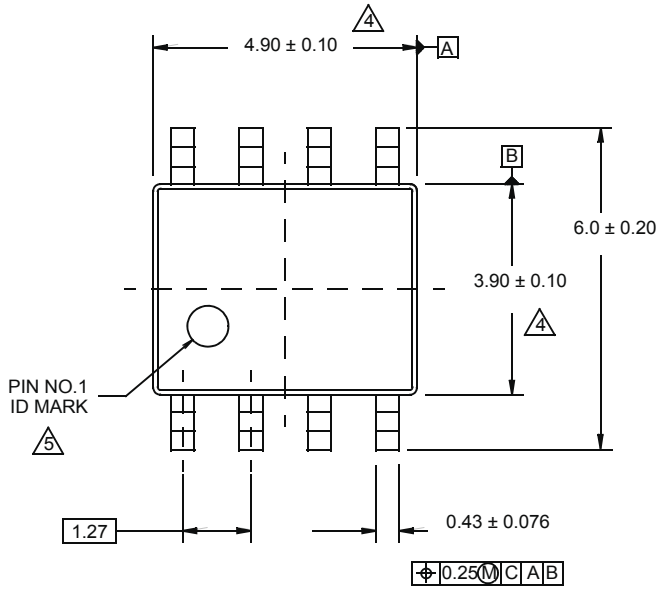
NOTES:

1. Plastic or metal protrusions of 0.010” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
4. Dimension eB is measured with the lead tips unconstrained.
5. 8 and 16 lead packages have half end-leads as shown.

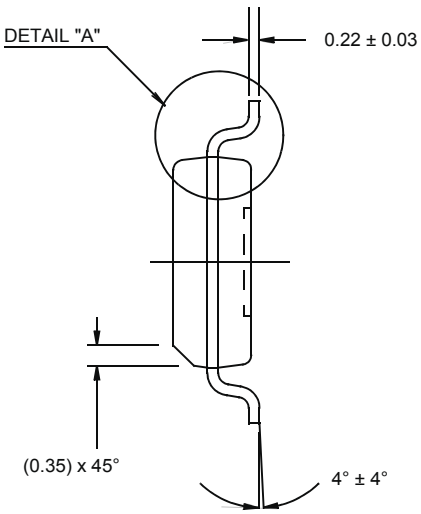
Package Outline Drawing

M8.15E

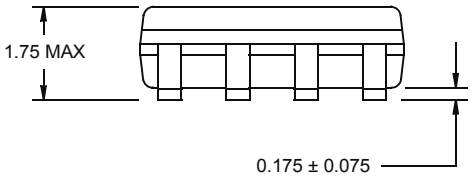
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 0, 08/09



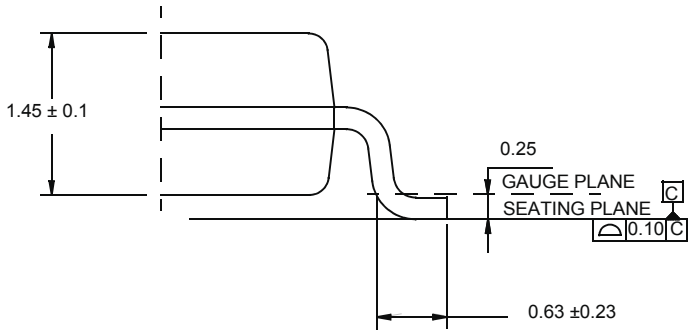
TOP VIEW



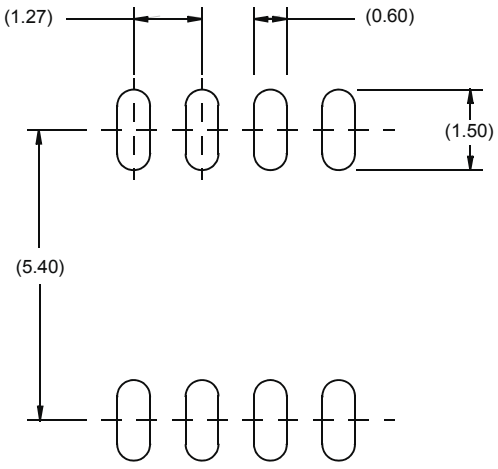
SIDE VIEW "B"



SIDE VIEW "A"



DETAIL "A"

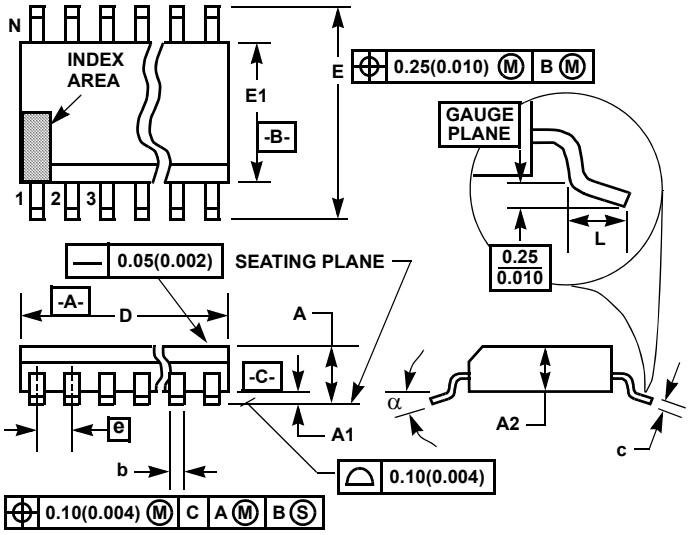


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M14.173

14 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.041	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.195	0.199	4.95	5.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	14		14		7
α	0°	8°	0°	8°	-

Rev. 2 4/06

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