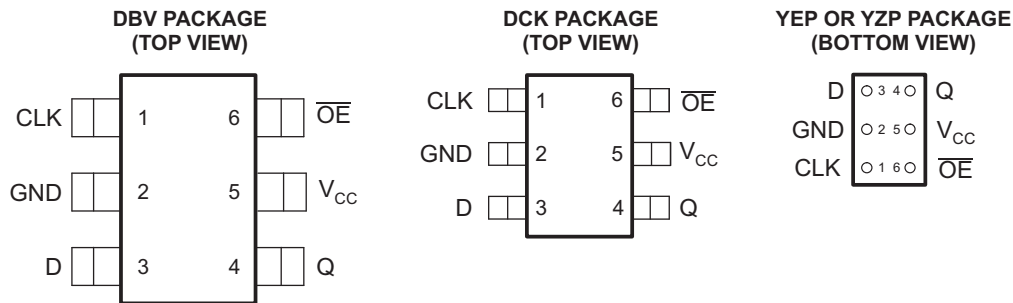


## FEATURES

- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Supports 5-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 4 ns at 3.3 V
- Low Power Consumption, 10- $\mu$ A Max  $I_{CC}$
- $\pm 24$ -mA Output Drive at 3.3 V
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

## DESCRIPTION/ORDERING INFORMATION

This single D-type latch is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC1G374 features a 3-state output designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, input/output (I/O) ports, bidirectional bus drivers, and working registers.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

On the positive transition of the clock (CLK) input, the Q output is set to the logic level set up at the data (D) input.

## ORDERING INFORMATION

| $T_A$         | PACKAGE <sup>(1)</sup>  |              | ORDERING PART NUMBER | TOP-SIDE MARKING <sup>(2)</sup> |
|---------------|---|--------------|----------------------|---------------------------------|
| –40°C to 85°C | NanoStar – WCSP (DSBGA)<br>0.23-mm Large Bump – YEP           | Reel of 3000 | SN74LVC1G374YEPR     | ___D4_                          |
|               | NanoFree – WCSP (DSBGA)<br>0.23-mm Large Bump – YZP (Pb-free) |              | SN74LVC1G374YZPR     |                                 |
|               | SOT (SOT-23) – DBV  | Reel of 3000 | SN74LVC1G374DBVR     | CA4___                          |
|               |   | Reel of 250  | SN74LVC1G374DBVT     |                                 |
|               | SOT (SC-70) – DCK   | Reel of 3000 | SN74LVC1G374DCKR     | D4_                             |
|               |   | Reel of 250  | SN74LVC1G374DCKT     |                                 |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

(2) DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.  
YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition(1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar, NanoFree are trademarks of Texas Instruments.

# SN74LVC1G374 SINGLE D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

SCES520B–DECEMBER 2003–REVISED SEPTEMBER 2006

## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the output in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the output neither loads nor drives the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

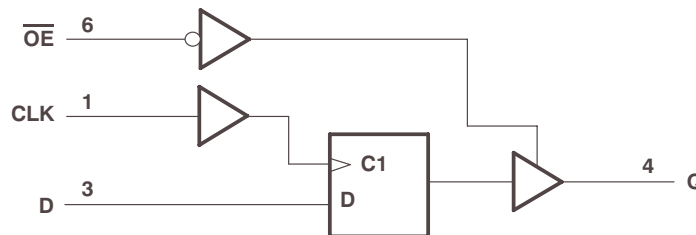
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

FUNCTION TABLE

| INPUTS          |        |   | OUTPUT |
|-----------------|--------|---|--------|
| $\overline{OE}$ | CLK    | D | Q      |
| L               | ↑      | L | L      |
| L               | ↑      | H | H      |
| L               | H or L | X | Q      |
| H               | X      | X | Z      |

LOGIC DIAGRAM (POSITIVE LOGIC)



### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                  |   | MIN                | MAX                   | UNIT |
|------------------|---|--------------------|-----------------------|------|
| V <sub>CC</sub>  | Supply voltage range  | –0.5               | 6.5                   | V    |
| V <sub>I</sub>   | Input voltage range <sup>(2)</sup>  | –0.5               | 6.5                   | V    |
| V <sub>O</sub>   | Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup> | –0.5               | 6.5                   | V    |
| V <sub>O</sub>   | Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>              | –0.5               | V <sub>CC</sub> + 0.5 | V    |
| I <sub>IK</sub>  | Input clamp current   | V <sub>I</sub> < 0 | –50                   | mA   |
| I <sub>OK</sub>  | Output clamp current  | V <sub>O</sub> < 0 | –50                   | mA   |
| I <sub>O</sub>   | Continuous output current   |                    | ±50                   | mA   |
|                  | Continuous current through V <sub>CC</sub> or GND   |                    | ±100                  | mA   |
| θ <sub>JA</sub>  | Package thermal impedance <sup>(4)</sup>  | DBV package        | 165                   | °C/W |
|                  |   | DCK package        | 259                   |      |
|                  |   | YEP/YZP package    | 123                   |      |
| T <sub>stg</sub> | Storage temperature range   | –65                | 150                   | °C   |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

# SN74LVC1G374

## SINGLE D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

SCES520B–DECEMBER 2003–REVISED SEPTEMBER 2006

### Recommended Operating Conditions<sup>(1)</sup>

|                 |                                    | MIN   | MAX                    | UNIT                   |      |
|-----------------|------------------------------------|---|------------------------|------------------------|------|
| V <sub>CC</sub> | Supply voltage                     | Operating                                       | 1.65                   | 5.5                    | V    |
|                 |                                    | Data retention only                             | 1.5                    |                        |      |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 1.65 V to 1.95 V              | 0.65 × V <sub>CC</sub> |                        | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V                | 1.7                    |                        |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V                  | 2                      |                        |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V                | 0.7 × V <sub>CC</sub>  |                        |      |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 1.65 V to 1.95 V              |                        | 0.35 × V <sub>CC</sub> | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V                |                        | 0.7                    |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V                  |                        | 0.8                    |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V                |                        | 0.3 × V <sub>CC</sub>  |      |
| V <sub>I</sub>  | Input voltage                      | 0   | 5.5                    | V                      |      |
| V <sub>O</sub>  | Output voltage                     | 0   | V <sub>CC</sub>        | V                      |      |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 1.65 V                        |                        | –4                     | mA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V                         |                        | –8                     |      |
|                 |                                    | V <sub>CC</sub> = 3 V                           |                        | –16                    |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V                         |                        | –24                    |      |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 1.65 V                        |                        | 4                      | mA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V                         |                        | 8                      |      |
|                 |                                    | V <sub>CC</sub> = 3 V                           |                        | 16                     |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V                         |                        | 24                     |      |
| Δt/Δv           | Input transition rise or fall rate | V <sub>CC</sub> = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V |                        | 20                     | ns/V |
|                 |                                    | V <sub>CC</sub> = 3.3 V ± 0.3 V                 |                        | 10                     |      |
|                 |                                    | V <sub>CC</sub> = 5 V ± 0.5 V                   |                        | 5                      |      |
| T <sub>A</sub>  | Operating free-air temperature     | –40   | 85                     | °C                     |      |

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        | TEST CONDITIONS  | V <sub>CC</sub> | MIN                   | TYP <sup>(1)</sup> | MAX  | UNIT |
|------------------|--|-----------------|-----------------------|--------------------|------|------|
| V <sub>OH</sub>  | I <sub>OH</sub> = -100 μA  | 1.65 V to 5.5 V | V <sub>CC</sub> - 0.1 |                    |      | V    |
|                  | I <sub>OH</sub> = -4 mA  | 1.65 V          | 1.2                   |                    |      |      |
|                  | I <sub>OH</sub> = -8 mA  | 2.3 V           | 1.9                   |                    |      |      |
|                  | I <sub>OH</sub> = -16 mA   | 3 V             | 2.4                   |                    |      |      |
|                  | I <sub>OH</sub> = -24 mA   |                 | 2.3                   |                    |      |      |
|                  | I <sub>OH</sub> = -32 mA   | 4.5 V           | 3.8                   |                    |      |      |
| V <sub>OL</sub>  | I <sub>OL</sub> = 100 μA   | 1.65 V to 5.5 V |                       |                    | 0.1  | V    |
|                  | I <sub>OL</sub> = 4 mA   | 1.65 V          |                       |                    | 0.45 |      |
|                  | I <sub>OL</sub> = 8 mA   | 2.3 V           |                       |                    | 0.3  |      |
|                  | I <sub>OL</sub> = 16 mA  | 3 V             |                       |                    | 0.4  |      |
|                  | I <sub>OL</sub> = 24 mA  |                 |                       |                    | 0.55 |      |
|                  | I <sub>OL</sub> = 32 mA  | 4.5 V           |                       |                    | 0.55 |      |
| I <sub>I</sub>   | V <sub>I</sub> = 5.5 V or GND  | 0 to 5.5 V      |                       |                    | ±1   | μA   |
| I <sub>OZ</sub>  | V <sub>O</sub> = 0 to 5.5 V  |                 |                       |                    | ±5   | μA   |
| I <sub>off</sub> | V <sub>I</sub> or V <sub>O</sub> = 5.5 V                                     | 0               |                       |                    | ±10  | μA   |
| I <sub>CC</sub>  | V <sub>I</sub> = 5.5 V or GND, I <sub>O</sub> = 0                            | 1.65 V to 5.5 V |                       |                    | 10   | μA   |
| ΔI <sub>CC</sub> | One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND | 3 V to 5.5 V    |                       |                    | 500  | μA   |
| C <sub>i</sub>   | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.3 V           |                       |                    | 3    | pF   |
| C <sub>o</sub>   | V <sub>O</sub> = V <sub>CC</sub> or GND                                      | 3.3 V           |                       |                    | 6    | pF   |

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

|                    |                                 | V <sub>CC</sub> = 1.8 V<br>± 0.15 V |     | V <sub>CC</sub> = 2.5 V<br>± 0.2 V |     | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |     | V <sub>CC</sub> = 5 V<br>± 0.5 V |     | UNIT |
|--------------------|---------------------------------|-------------------------------------|-----|------------------------------------|-----|------------------------------------|-----|----------------------------------|-----|------|
|                    |                                 | MIN                                 | MAX | MIN                                | MAX | MIN                                | MAX | MIN                              | MAX |      |
| f <sub>clock</sub> | Clock frequency                 | 100                                 |     | 125                                |     | 150                                |     | 175                              |     | MHz  |
| t <sub>w</sub>     | Pulse duration, CLK high or low | 3.3                                 |     | 3                                  |     | 2.8                                |     | 2.5                              |     | ns   |
| t <sub>su</sub>    | Setup time, data before CLK ↑   | 3.5                                 |     | 2.5                                |     | 2                                  |     | 1.5                              |     | ns   |
| t <sub>h</sub>     | Hold time, data after CLK ↑     | 3.4                                 |     | 1.6                                |     | 1.5                                |     | 1.5                              |     | ns   |

## Switching Characteristics

over recommended operating free-air temperature range, C<sub>L</sub> = 15 pF (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM INPUT      | TO (OUTPUT) | V <sub>CC</sub> = 1.8 V<br>± 0.15 V |     | V <sub>CC</sub> = 2.5 V<br>± 0.2 V |     | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |     | V <sub>CC</sub> = 5 V<br>± 0.5 V |     | UNIT |
|------------------|-----------------|-------------|-------------------------------------|-----|------------------------------------|-----|------------------------------------|-----|----------------------------------|-----|------|
|                  |                 |             | MIN                                 | MAX | MIN                                | MAX | MIN                                | MAX | MIN                              | MAX |      |
| f <sub>max</sub> |                 |             | 100                                 |     | 125                                |     | 150                                |     | 175                              |     | MHz  |
| t <sub>pd</sub>  | CLK             | Q           | 2.5                                 | 15  | 2                                  | 6   | 1.4                                | 4   | 1                                | 3   | ns   |
| t <sub>en</sub>  | $\overline{OE}$ | Q           | 2.2                                 | 12  | 2                                  | 4.8 | 1.3                                | 3.8 | 1.1                              | 2.5 | ns   |
| t <sub>dis</sub> | $\overline{OE}$ | Q           | 2.2                                 | 11  | 2                                  | 4.8 | 1.6                                | 4.5 | 1.2                              | 3.1 | ns   |

# SN74LVC1G374

## SINGLE D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

SCES520B–DECEMBER 2003–REVISED SEPTEMBER 2006

### Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 30$  pF or 50 pF (unless otherwise noted) (see [Figure 2](#))

| PARAMETER | FROM INPUT      | TO (OUTPUT) | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$ |      | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ |     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |     | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ |     | UNIT |
|-----------|-----------------|-------------|---|------|--|-----|--|-----|--|-----|------|
|           |                 |             | MIN                                       | MAX  | MIN                                      | MAX | MIN                                      | MAX | MIN                                    | MAX |      |
| $f_{max}$ |                 |             | 100                                       |      | 125                                      |     | 150                                      |     | 175                                    |     | MHz  |
| $t_{pd}$  | CLK             | Q           | 2.7                                       | 18.3 | 1.8                                      | 8.2 | 1.6                                      | 6   | 1                                      | 4   | ns   |
| $t_{en}$  | $\overline{OE}$ | Q           | 2   | 13   | 1.5                                      | 6.3 | 0.9                                      | 5   | 0.7                                    | 3.5 | ns   |
| $t_{dis}$ | $\overline{OE}$ | Q           | 2   | 14   | 1.1                                      | 5.3 | 1.4                                      | 4.5 | 0.8                                    | 3.1 | ns   |

### Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER |                   | TEST CONDITIONS                     | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | $V_{CC} = 5\text{ V}$ | UNIT |    |
|-----------|-------------------|-------------------------------------|-------------------------|-------------------------|-------------------------|-----------------------|------|----|
|           |                   |                                     | TYP                     | TYP                     | TYP                     | TYP                   |      |    |
| $C_{pd}$  | Power dissipation | Outputs enabled<br>Outputs disabled | f = 10 MHz              | 24                      | 24                      | 25                    | 27   | pF |
|           | capacitance       |                                     |                         | 8                       | 8                       | 9                     | 11   |    |

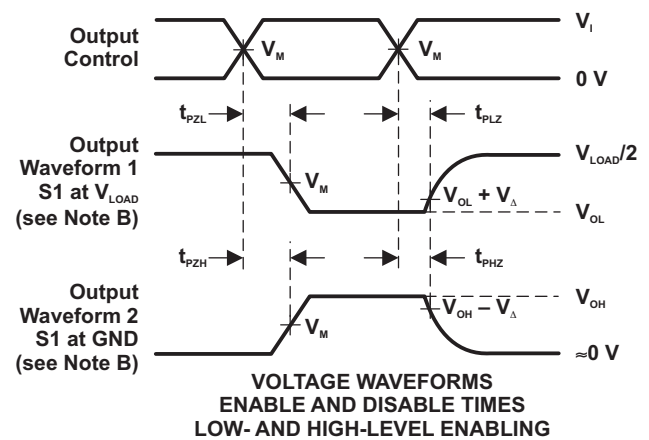
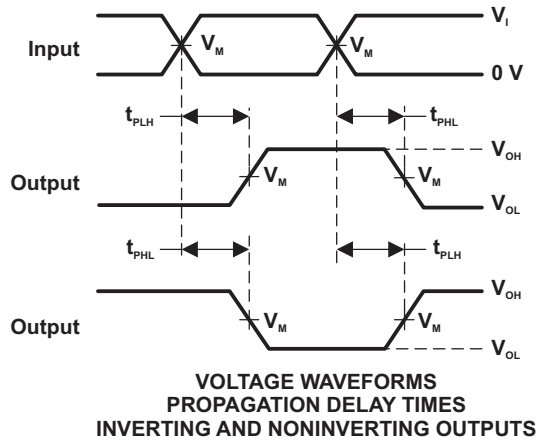
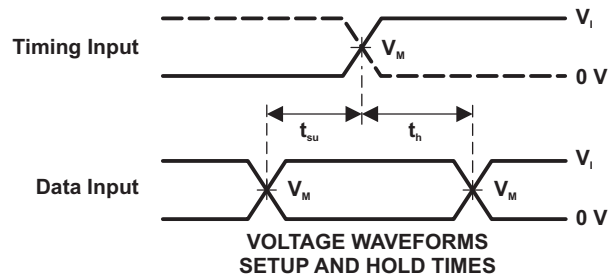
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

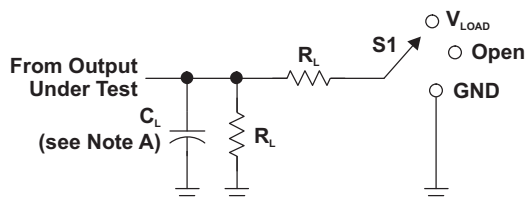
| $V_{CC}$                         | INPUTS   |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_I$    | $t/t_i$              |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M $\Omega$ | 0.15 V       |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M $\Omega$ | 0.15 V       |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 3 V      | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 15 pF | 1 M $\Omega$ | 0.3 V        |
| $5\text{ V} \pm 0.5\text{ V}$    | $V_{CC}$ | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M $\Omega$ | 0.3 V        |



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_o = 50\ \Omega$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

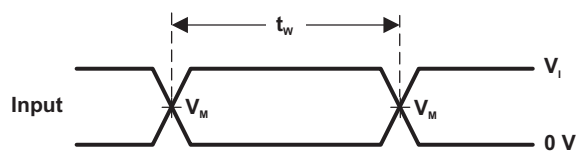
PARAMETER MEASUREMENT INFORMATION (continued)



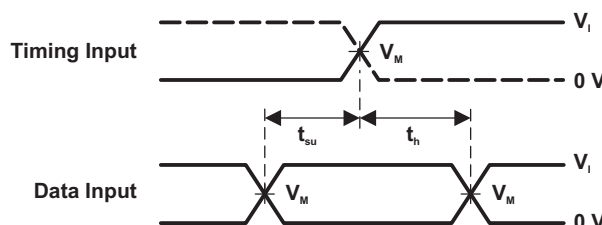
LOAD CIRCUIT

| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PZL}/t_{PZH}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PHZ}$ | GND        |

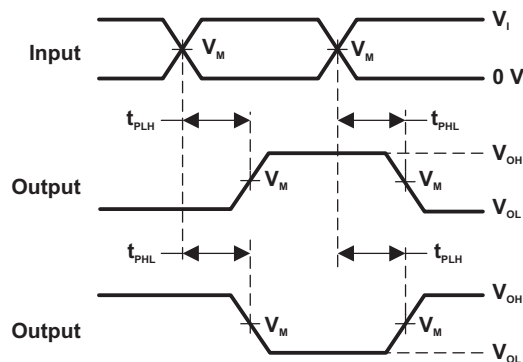
| $V_{CC}$                         | INPUTS   |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_I$    | $t_f/t_r$            |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k $\Omega$ | 0.15 V       |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 3 V      | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |
| $5\text{ V} \pm 0.5\text{ V}$    | $V_{CC}$ | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 $\Omega$ | 0.3 V        |



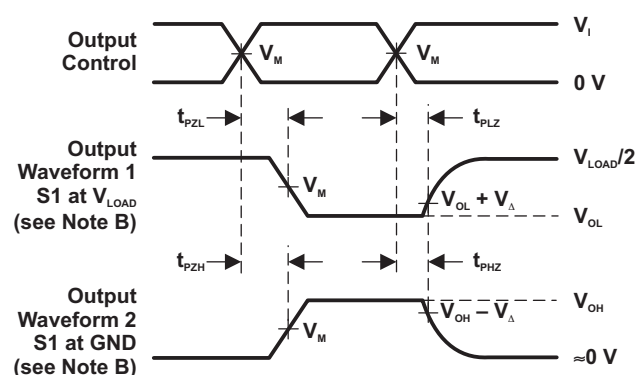
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_o = 50\ \Omega$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms



**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| 74LVC1G374DBVRE4 | ACTIVE        | SOT-23       | DBV             | 6    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | (CA45 ~ CA4R)            | <a href="#">Samples</a> |
| 74LVC1G374DBVRG4 | ACTIVE        | SOT-23       | DBV             | 6    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | (CA45 ~ CA4R)            | <a href="#">Samples</a> |
| 74LVC1G374DCKRE4 | ACTIVE        | SC70         | DCK             | 6    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | (D45 ~ D4R)              | <a href="#">Samples</a> |
| 74LVC1G374DCKRG4 | ACTIVE        | SC70         | DCK             | 6    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | (D45 ~ D4R)              | <a href="#">Samples</a> |
| SN74LVC1G374DBVR | ACTIVE        | SOT-23       | DBV             | 6    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | (CA45 ~ CA4R)            | <a href="#">Samples</a> |
| SN74LVC1G374DCKR | ACTIVE        | SC70         | DCK             | 6    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | (D45 ~ D4R)              | <a href="#">Samples</a> |
| SN74LVC1G374YZPR | ACTIVE        | DSBGA        | YZP             | 6    | 3000        | Green (RoHS & no Sb/Br) | SNAGCU           | Level-1-260C-UNLIM   | -40 to 85    | (D47 ~ D4N)              | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN74LVC1G374 :**

- Automotive: [SN74LVC1G374-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC1G374DBVR | SOT-23       | DBV             | 6    | 3000 | 180.0              | 8.4                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| SN74LVC1G374DBVR | SOT-23       | DBV             | 6    | 3000 | 178.0              | 9.2                | 3.3     | 3.2     | 1.55    | 4.0     | 8.0    | Q3            |
| SN74LVC1G374DCKR | SC70         | DCK             | 6    | 3000 | 178.0              | 9.2                | 2.4     | 2.4     | 1.22    | 4.0     | 8.0    | Q3            |
| SN74LVC1G374YZPR | DSBGA        | YZP             | 6    | 3000 | 178.0              | 9.2                | 1.02    | 1.52    | 0.63    | 4.0     | 8.0    | Q1            |

## TAPE AND REEL BOX DIMENSIONS

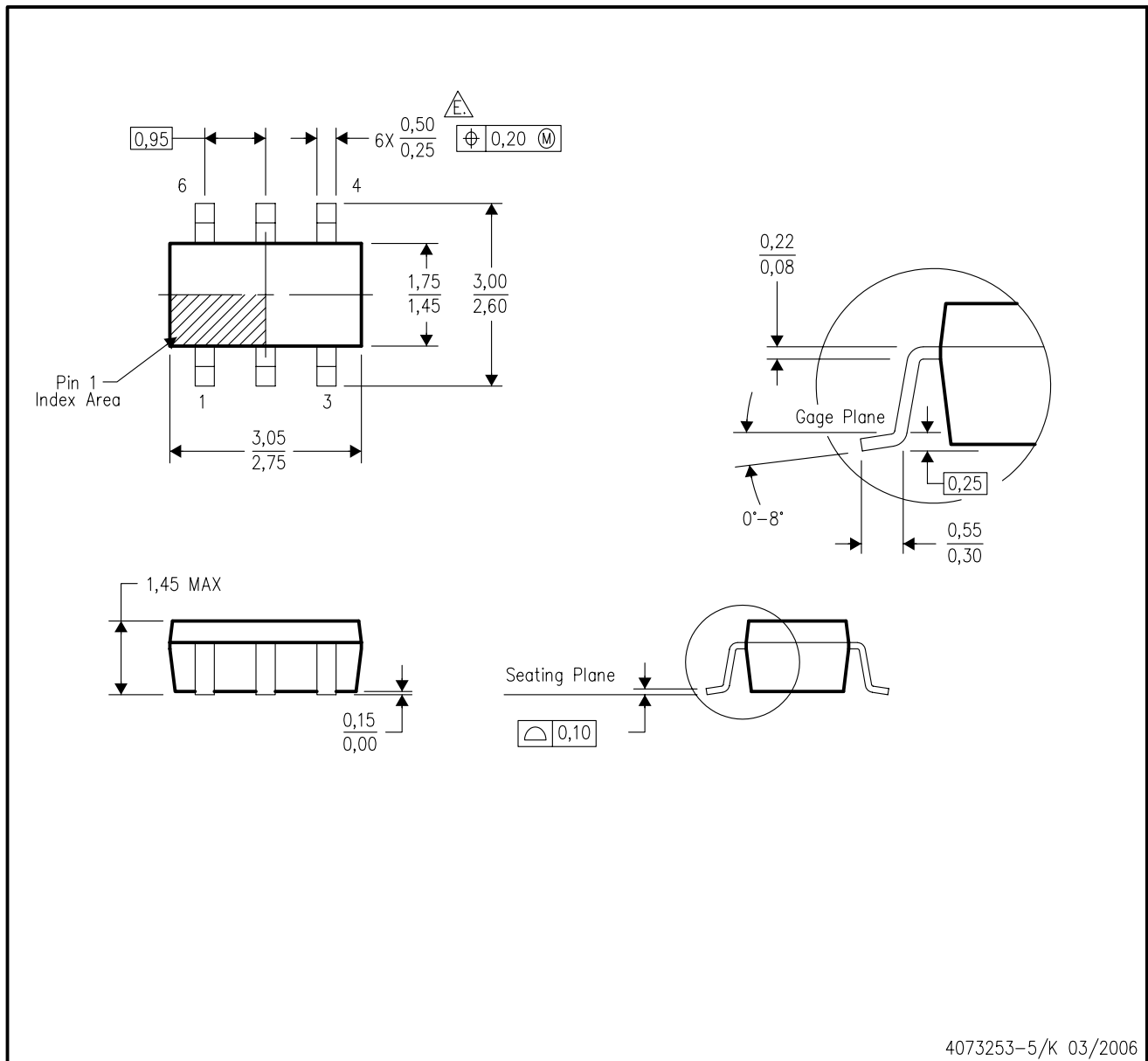


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC1G374DBVR | SOT-23       | DBV             | 6    | 3000 | 202.0       | 201.0      | 28.0        |
| SN74LVC1G374DBVR | SOT-23       | DBV             | 6    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74LVC1G374DCKR | SC70         | DCK             | 6    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74LVC1G374YZPR | DSBGA        | YZP             | 6    | 3000 | 220.0       | 220.0      | 35.0        |

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- $\triangle E$  Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE

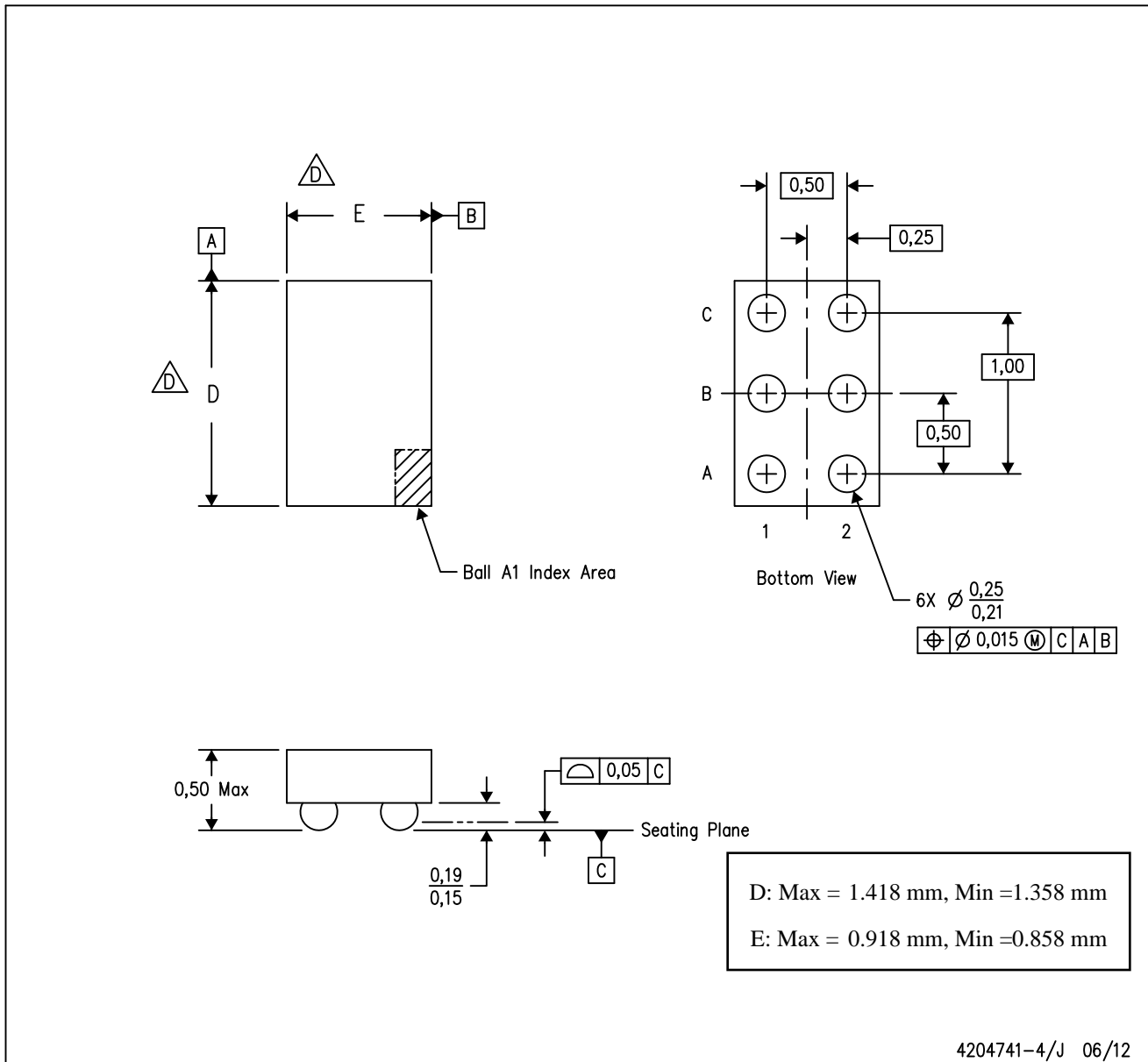


- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



YZP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.
  - The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
  - E. This package is a Pb-free solder ball design. Refer to the 6 YEP package (drawing 4204725) for tin-lead (SnPb).

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**Телефон:** +7 812 627 14 35

**Электронная почта:** [sales@st-electron.ru](mailto:sales@st-electron.ru)

**Адрес:** 198099, Санкт-Петербург,  
Промышленная ул, дом № 19, литера Н,  
помещение 100-Н Офис 331