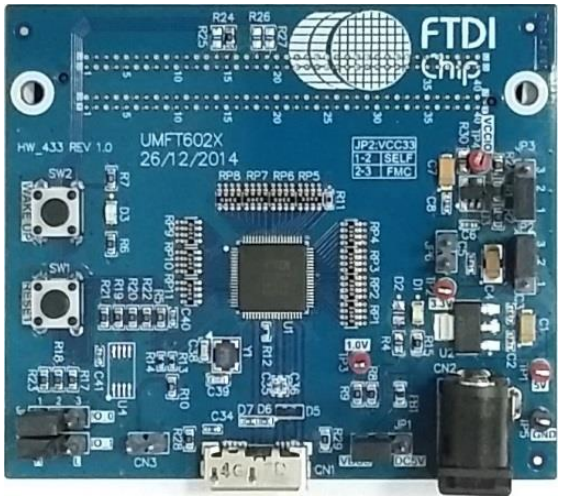
Future Technology Devices International Ltd

UMFT602A/ UMFT602X



The UMFT602A/X is an evaluation/development module with either HSMC or FMC (LPC) connectors for interfacing FTDI's FT602 32bit FIFO bus to USB 3.1 GEN 1 USB video class (UVC) bridge IC with external hardware. The UMFT602A/X allows for bridging a FIFO bus to a USB3.0 host and evaluating the functionality of the FT602.

As a daughter card, the UMFT602A/X must work with a FIFO master board which has either a HSMC or FMC connector. There are 2 models which provide different FIFO bus interfaces with 32bit data width.

The modules are designed such that they can plug into most FPGA development platforms supplied by vendors such as Xilinx or Altera. Refer to Ordering Information for module options.

The UMFT602A/X supports 2 parallel slave FIFO bus protocols (Multi-Channel FIFO / 245 Synchronous FIFO) with a data "burst" rate of up to 400MB/s. For a full list of the FT602's features refer to the FT602 datasheet.

The UMFT602A/X module has the following features:

- Supports USB 3.1 GEN 1 Super Speed (5Gbps)/USB 2.0 High Speed (480Mbps) transfer
- UVC 1.1, Raw YUV422, support 14 UVC resolutions
- Up to 4 video input channels. One I2C bus master interface for video source device configuration
- Supports multi voltage I/O: 1.8V, 2.5V and 3.3V
- High speed connector for FIFO bus : FMC(Field Programmable Mezzanine Card) or HSMC (High Speed Mezzanine Card)
- FMC connector is compatible with most Xilinx FPGA reference design boards
- HSMC is compatible with most Altera FPGA reference design boards
- Multi powered options: external DC powered, BUS powered, FMC/HSMC powered
- Hardware Reset
- Micro-USB3.0 receptacle, USB3.0 compliant and certified

1 Ordering Information

Part No.	Description
UMFT602A-B	32 Bit FIFO bus, HSMC connector
UMFT602X-B	32 Bit FIFO bus, FMC(Low Pin Count) connector

Table 1.1 UMFT60xx Ordering Information

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2 Hardware Description

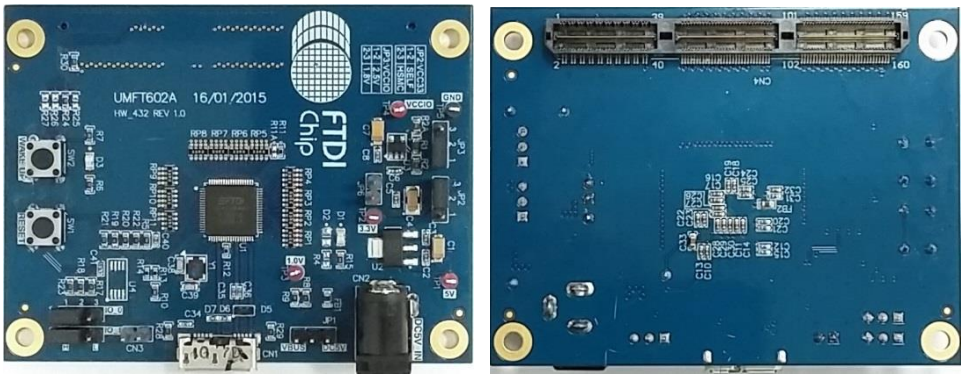

Figure 2-1 UMFT602A Module Top and Bottom View

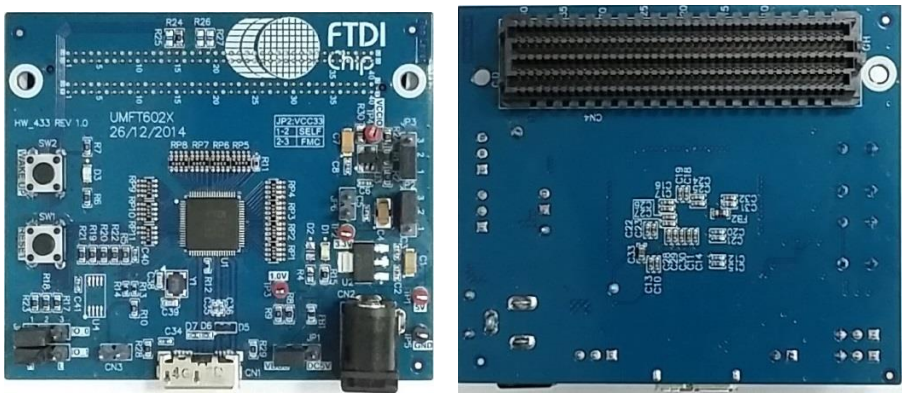

Figure 2-2 UMFT602X Module Top and Bottom View

The main functions of the UMFT602A/X module are as follows:

- Provides Multi-channel FIFO mode and 245 Synchronous FIFO mode Protocols.
- YUV422 uncompressed format is supported.
- FIFO clock: 100MHz, driven by FT602.
- High speed FIFO bus interface: FMC (Low Pin Count) and HSMC optional. See Ordering Information.
- Jumper's selection allowing powered options: VBUS-powered, External DC-powered, FIFO master board-powered.
- Multi voltage VCCIO option: 1.8V, 2.5V, 3.3V, default is 2.5V.
- Hardware reset and System wake up.

2.1 Physical Description

The UMFT602A and UMFT602X modules dimensions are illustrated in Figure 2.5 to Figure 2.8.

2.1.1 Dimensions

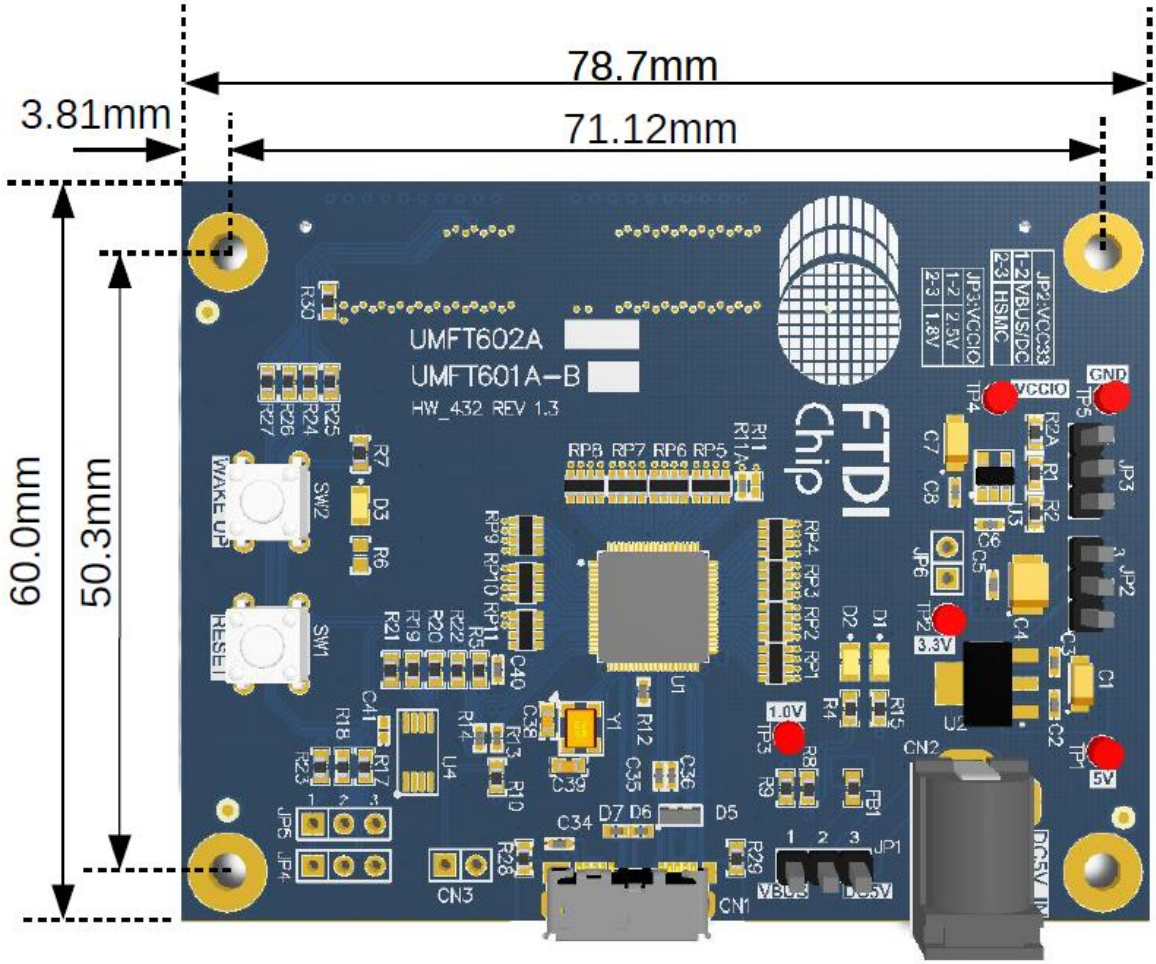

Figure 2-3 UMFT602A Dimensions (Top view)

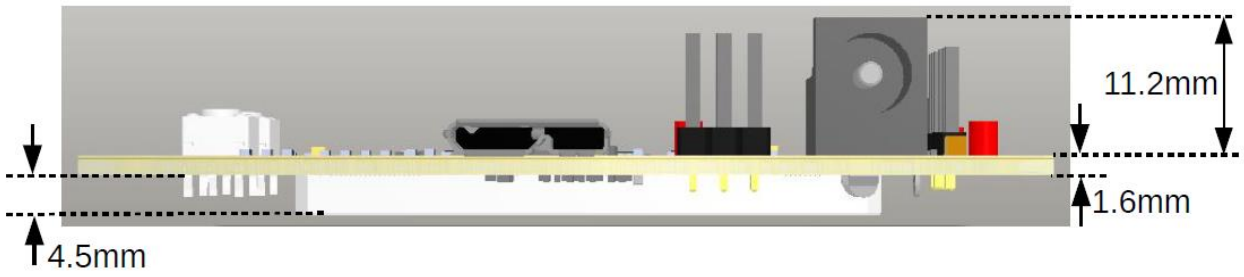

Figure 2-4 UMFT602A Dimensions (Side view)

±0.10mm Tolerance

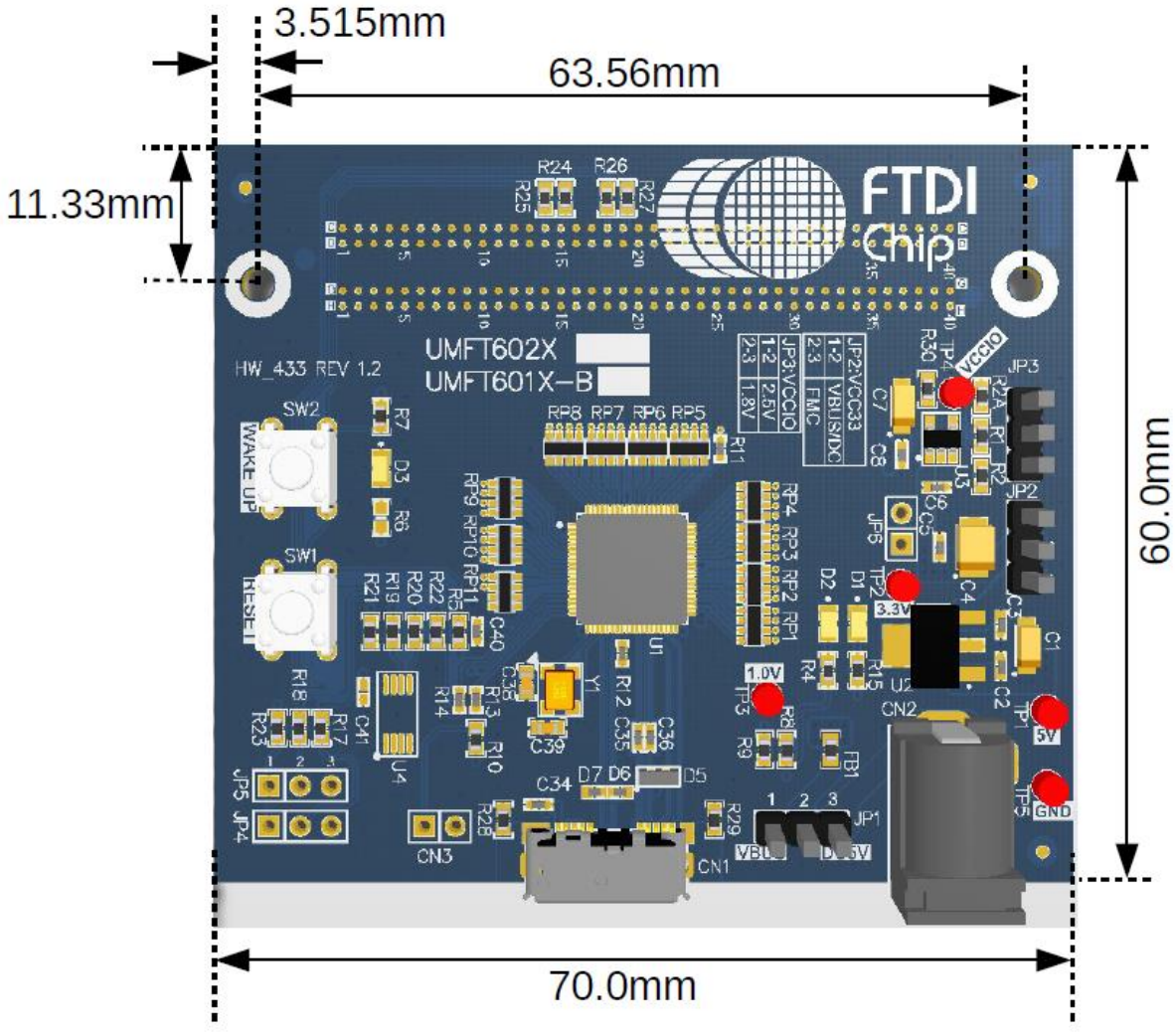

Figure 2-5 UMFT602X Dimensions (Top view)

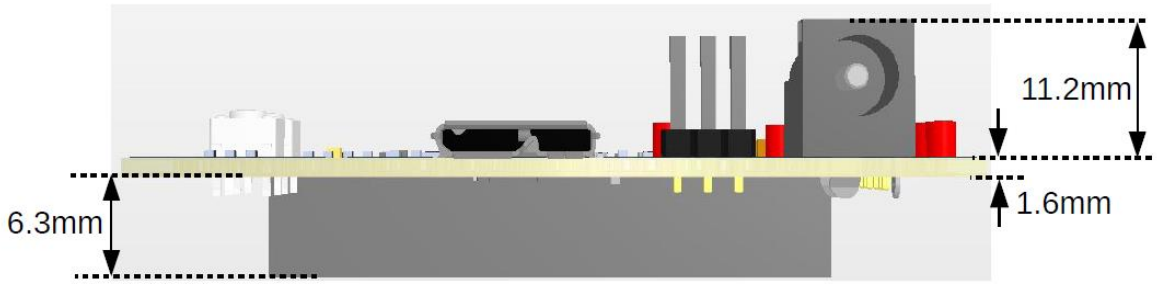

Figure 2-6 UMFT602X Dimensions (Side view)

±0.10mm Tolerance

2.2 Connectors, Jumpers and Push Buttons

Connectors, jumpers and push buttons are described in the following sections.

2.2.1 CN1 - Micro USB3.0 Receptacle

Pin No.	Name	Type	Description
1	VBUS	P	5V DC power supply
2	D-	IO	USB D- line
3	D+	IO	USB D+ line
4	ID	IO	OTG identification(N.C.)
5	GND	P	Ground
6	SSTX-	O	Super Speed USB transmitter differential pair (-)
7	SSTX+	O	Super Speed USB transmitter differential pair(+)
8	GND	P	Ground
9	SSRX-	I	Super Speed USB receiver differential pair (-)
10	SSRX+	I	Super Speed USB receiver differential pair (+)

Table 2.1 CN1 - Micro USB3.0 Pin-out

2.2.2 CN2 – POWER JACK 2.1MM

Optional external DC 5V input.

Pin No.	Name	Type	Description
1	5V	P	5V power supply
2	GND	P	Ground
3	GND	P	Ground

Table 2.2 CN2 – POWER JACK 2.1MM

2.2.3 JP1 – External/VBUS Powered Selection

Select whether the module power is supplied by an external DC 5V or VBUS. Note this setting must be chosen in conjunction with the JP2 setting. Default is open. [Note]

Jumper position	Description
Short pin 1-2	Select VBUS Power
Short pin 2-3	Select external DV 5V

Table 2.3 JP1 – 5V input Options

2.2.4 JP2 – VCC33 Selection

Select whether the module main power is supplied by DC5V or the FIFO master board DC3.3V.[Note]

Jumper position	Description
Short pin 1-2	Select powered by external DV5V or VBUS
Short pin 2-3	Select powered by FIFO master Board(default)

Table 2.4 JP3 – VCC33 Option

2.2.5 JP3, JP6– VCCIO Selection

Select the IO voltage level. [Note]

Jumper position		Description
JP3	JP6	
Short pin 1-2	Open	VCCIO=2.5V(default)
Short pin 2-3	Open	VCCIO=1.8V
Open	Short	VCCIO=3.3V

Table 2.5 JP3 – VCCIO Option

Note: Refer to section 4 Hardware setup guide for more details on power configuration options and jumpers positions.

JP6 is not fitted on the PCB.

2.2.6 SW1, SW2 – Push Buttons for Reset and Remote Wake Up

SW1 – Reset, module hardware reset, mapped to FMC/HSMC connector, can be used for FIFO master reset. Drive low when press down.

SW2 – FT602 device Wake Up, driven low when pressed down. This pin mapped is to the FMC/HSMC connector, and is normally used for I^2C interrupt.

2.2.7 CN4 – FMC / HSMC FIFO bus interface connector

2.2.7.1 FMC connector configurations- UMFT602X Module

FMC Pin#/Name	UMFT602X U1: FT602 Pin#/Name
C14/LA10_P	16 /INT_N/Wake Up_N
C15/LA10_N	15 /RESET_N
C18/LA14_P	17 /I2C_SCL
C19/LA14_N	18 /I2C_SDA

FMC Pin#/Name	UMFT602X U1: FT602 Pin#/Name
C22/LA18_P_CC	68 /D_CLK (FIFO bus clock,FT602 output)
C26/LA27_P	62 /DATA18
C27_LA27_N	60 /DATA16
D14/LA09_P	8 /BE_N_3
D15/LA09_N	7 /BE_N_2
D20/LA17_P_CC	76 /DATA31
D21/LA17_N_CC	75 /DATA30
D23/LA23_P	70 /DATA25
D24/LA23_N	69 /DATA24
D26/LA26_P	63 /DATA19
D27/LA26_N	61 /DATA17
G6/LA00_P_CC	13 /RESERVE3
G7/LA00_N_CC	12 /RESERVE2
G12/LA08_P	11 /WR_N
G13/LA08_N	10 /RESERVE1
G21/LA20_P	74 /DATA29
G22/LA20_N	73 /DATA28
G24/LA22_P	67 /DATA23
G25/_LA22_N	65 /DATA21
G27/LA25_P	57 /DATA15
G28/LA25_N	55 /DATA13
G30/LA29_P	53 /DATA11
G31/LA29_N	51 /DATA9
G33/LA31_P	47 /DATA7
G34/LA31_N	45 /DATA5
G36/LA33_P	43 /DATA3
G37/LA33_N	41 /DATA1
H13/LA07_P	9 /RXF_N

FMC Pin#/Name	UMFT602X U1: FT602 Pin#/Name
H14/LA07_N	8 /TXE_N
H19/LA15_P	5 /BE_N_1
H20/LA15_N	4 /BE_N_0
H22/LA19_P	72 /DATA27
H23/LA19_N	71 /DATA26
H25/LA21_P	66 /DATA22
H26/LA21_N	64 /DATA20
H28/LA24_P	56 /DATA14
H29/LA24_N	54 /DATA12
H31/LA28_P	52 /DATA10
H32/LA28_N	50 /DATA8
H34/LA30_P	46 /DATA6
H35/LA30_N	44 /DATA4
H37/LA32_P	42 /DATA2
H38/LA32_N	40 /DATA0

Table 2.6 CN4 – FMC connector configuration for FIFO bus

2.2.7.2 CN4 – HSMC connector configurations-UMFT602A Module

HSMC Pin#/Name	UMFT602A U1: FT602 Pin#/Name
40 /CLKIN0	68 /D_CLK (FIFO bus clock,FT602 output)
41 /D0	40 /DATA0
42 /D1	60 /DATA16
43 /D2	41 /DATA1
44 /D3	61 /DATA17
47 /D4	42 /DATA2
48 /D5	62 /DATA18
49 /D6	43 /DATA3

HSMC Pin#/Name	UMFT602A U1: FT602 Pin#/Name
50 /D7	63 /DATA19
53 /D8	44 /DATA4
54 /D9	64 /DATA20
55 /D10	45 /DATA5
56 /D11	65 /DATA21
59 /D12	46 /DATA6
60 /D13	66 /DATA22
61 /D14	47 /DATA7
62 /D15	67 /DATA23
65 /D16	50 /DATA8
66 /D17	69 /DATA24
67 /D18	51 /DATA9
68 /D19	70 /DATA25
71 /D20	52 /DATA10
72 /D21	71 /DATA26
73 /D22	53 /DATA11
74 /D23	72 /DATA27
77 /D24	54 /DATA12
78 /D25	73 /DATA28
79 /D26	55 /DATA13
80 /D27	74 /DATA29
83 /D28	56 /DATA14
84 /D29	75 /DATA30
85 /D30	57 /DATA15
86 /D31	76 /DATA31
101 /D40	4 /BE_N_0
102 /D41	8 /TXE_N
103 /D42	5 /BE_N_1

HSMC Pin#/Name	UMFT602A U1: FT602 Pin#/Name
104 /D43	9 /RXF_N
107 /D44	7 /BE_N_2
108 /D45	10 /RESERVE1
109 /D46	8 /BE_N_3
110 /D47	11 /WR_N
113 /D48	18 /I2C_SDA
114 /D49	12 /RESERVE2
115 /D50	17 /I2C_SCL
116 /D51	13 /RESERVE3
119 /D52	15 /RESET_N
121 /D54	16 / INT_N/Wake up_N

Table 2.7 CN4 – HSMC connector configuration for FIFO bus

Note: Refer to the FT602 device datasheet section 3 for details of the device pin out and signal descriptions.

The reserved pins (Pin10, Pin12, and Pin13) are connected to the FIFO master via the FMC/HSMC connector, the FIFO master IOs whose connect to these pins should be configured to pull up in the normal operation.

3 Board Schematics

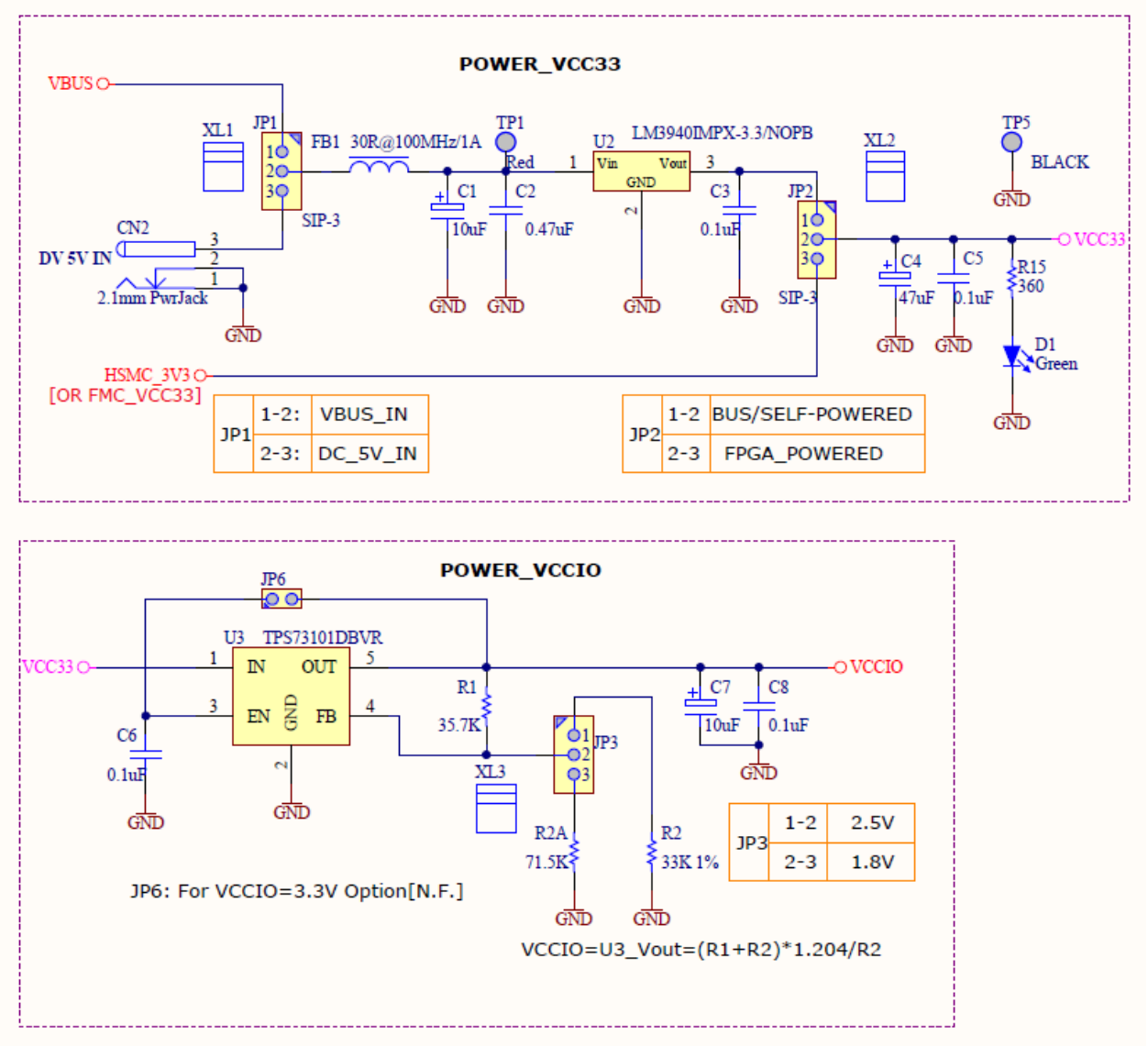

Figure 3-1 Schematics: Power Supply for UMFT602A/UMFT602X

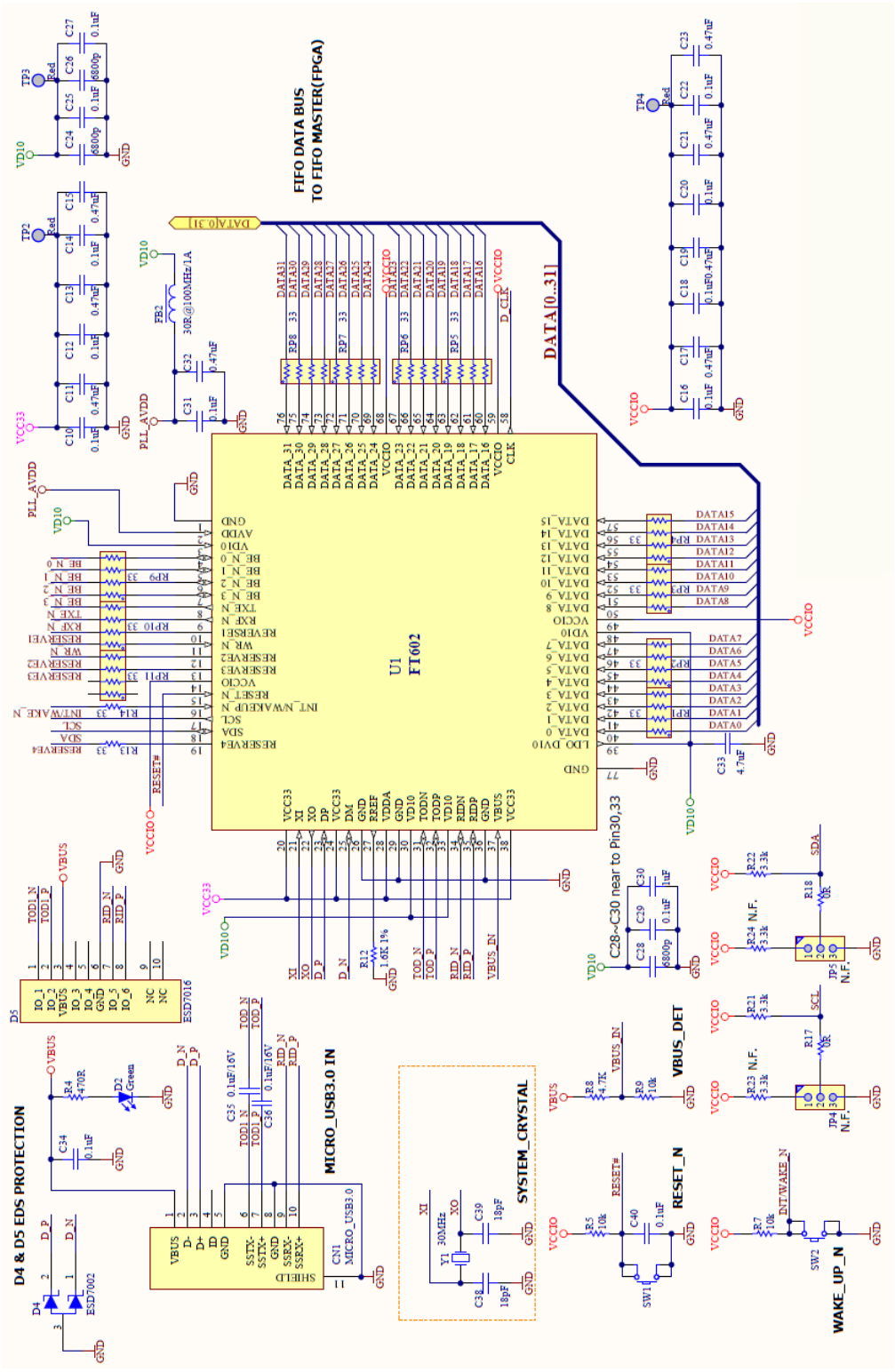

Figure 3-2 Schematics: FIFO TO USB3.0 UVC Bridge_UMFT602A/UMFT602X

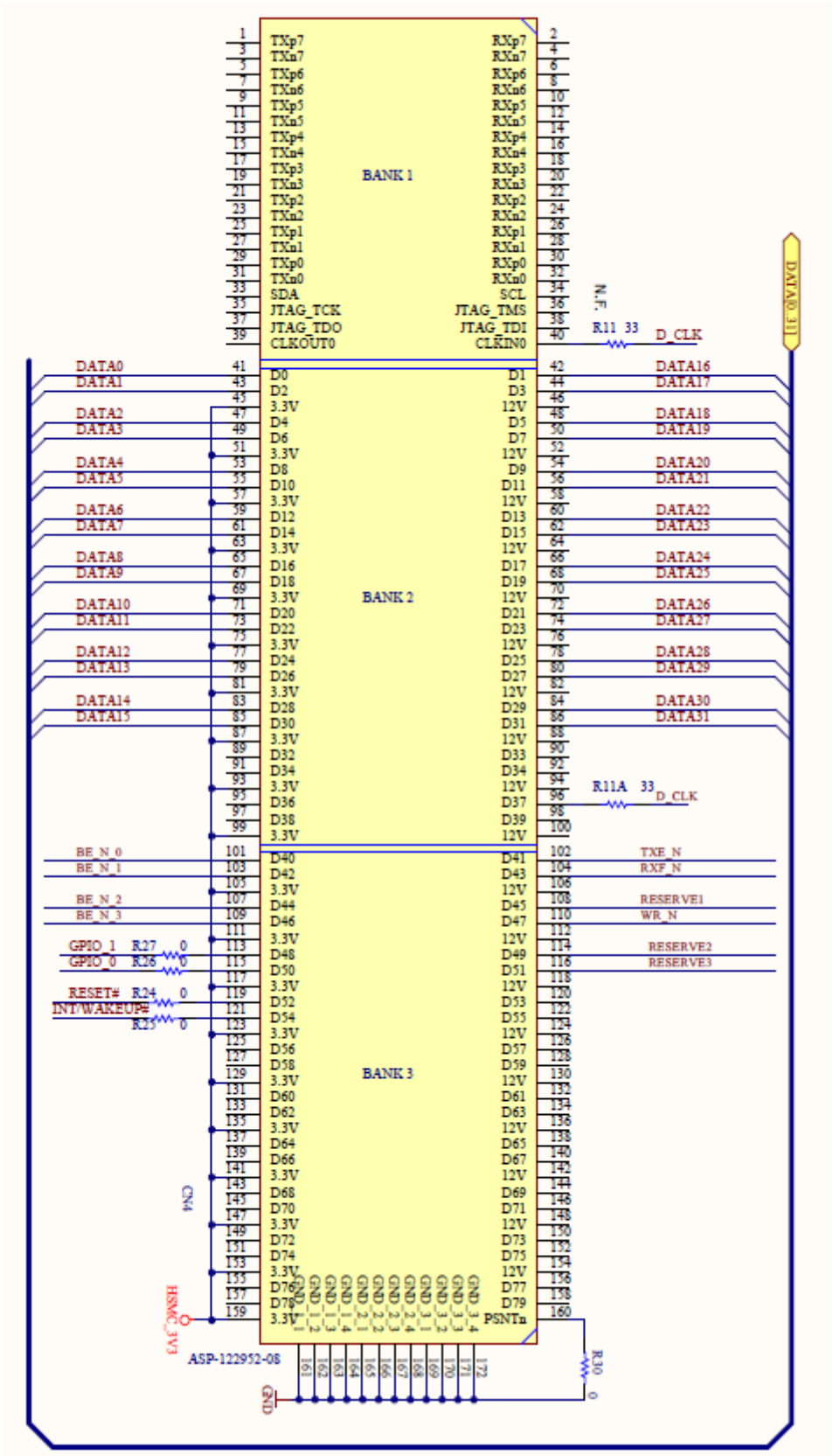

Figure 3-3 Schematics: HSMC_UMFT602A

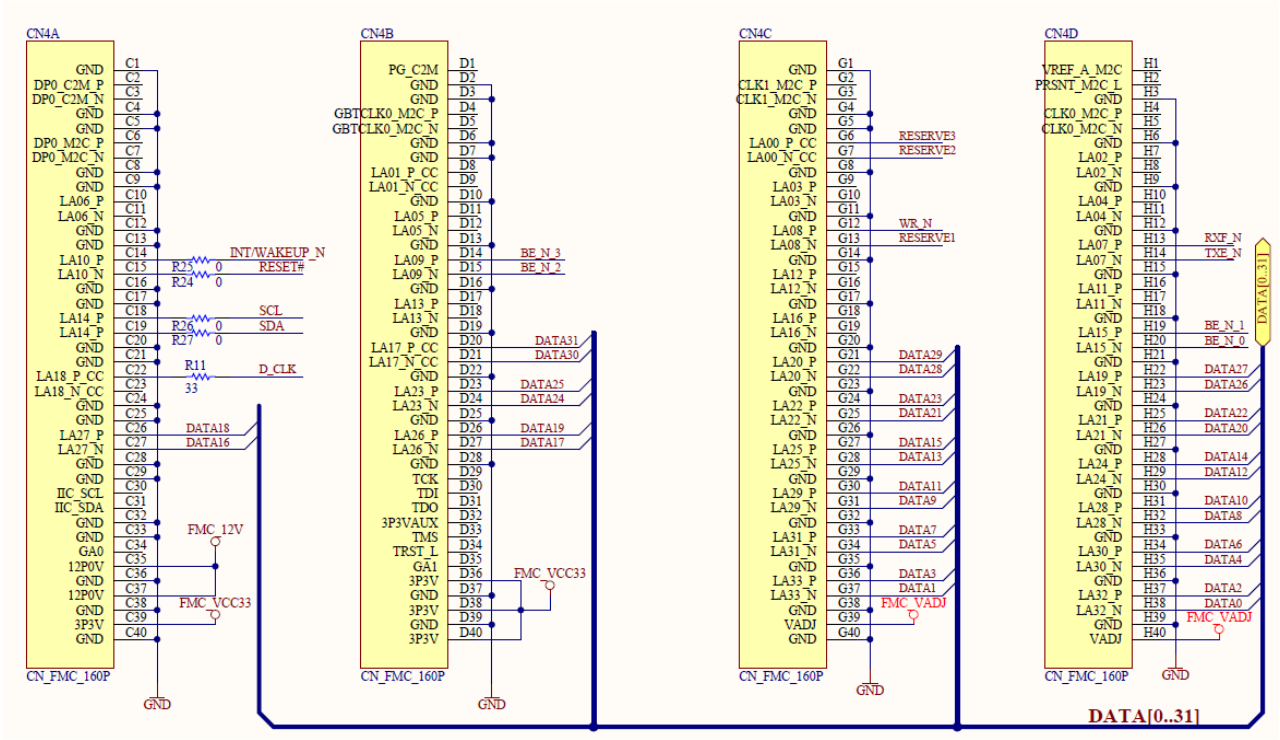

Figure 3-4 Schematics: FMC_UMFT602X

4 Hardware Setup Guide

4.1 Power Configuration

There are 3 methods of powering the UMFT602A/UMFT602X module.

1) FIFO master board Power (3.3V)-Connect the UMFT602A/UMFT602X board to the FIFO master board that has the standard configuration HSMC female or FMC (LPC or HPC) connector. This method is the default setting and is recommended.
2) USB Power (5V) - Connect USB power by micro-USB3.0 or micro-USB2.0 cable to CN1.
3) DC IN (5V) - Connect DC 5V to CN2.

The following table summarizes how to power the UMFT60xx module using the various methods.

Power Method	CN1	CN2	JP1	JP2	JP3 and JP6
FIFO master board Power(Default and Recommended)	-	N.C.	Open	Short pin 2-3	Follow FIFO master IO voltage. Default: JP3 short pin1-2 VCCIO=2.5V
USB Power	5V	N.C.	Short pin1-2	Short pin1-2	
DC IN(5V)	-	5V	Short pin2-3	Short pin1-2	

Table 4.1 Board Power Configuration

4.2 Jumpers Default Position

Jumper	JP1	JP2	JP3
Default Position	Open	2-3	1-2

Table 4.2 Jumpers Default Position

Figure 4.1 shows the Jumpers' locations on the PCBs.

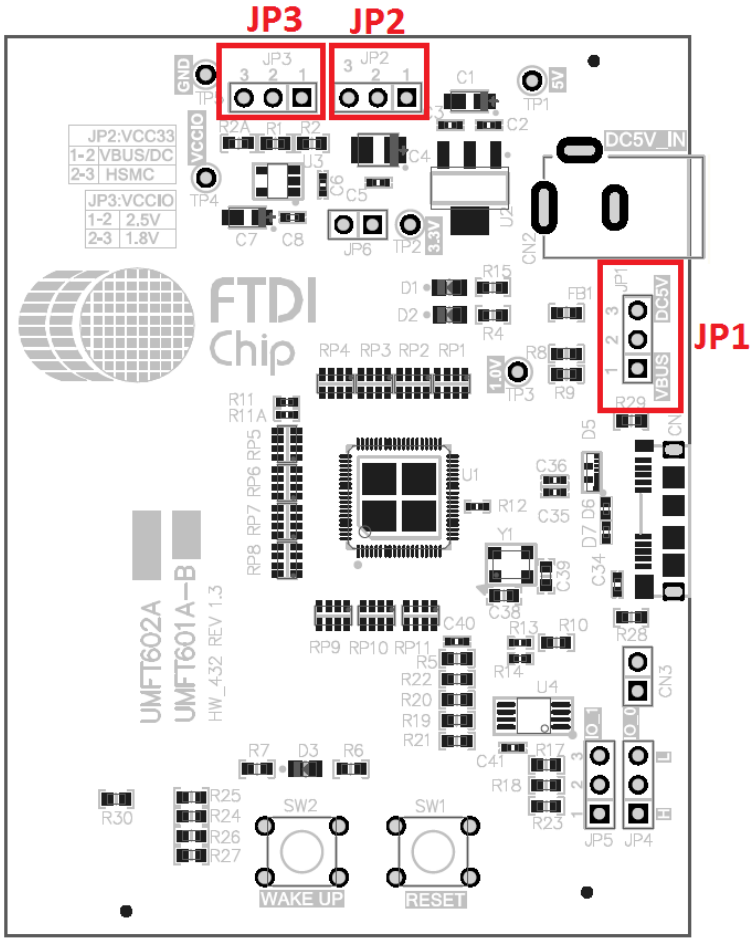

Figure 4-1 Jumpers Locations

4.3 Power Consumption

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
I_{VCC_1}	VCC Operating Supply Current	-	195	-	mA	Function Mode
I_{VCC_2}	VCC Operating Supply Current	-	7.0	-	mA	Suspend Mode
I_{VBUS1}	VBUS Operating Current	-	0.34	-	mA	DC/HSMC/FMC Powered, Function and Suspend Mode
I_{VBUS2}	VBUS Operating Current	-	191	-	mA	VBUS-Powered Powered, Function Mode
I_{VBUS3}	VBUS Operating Current	-	7.3	-	mA	VBUS-Powered Powered, Suspend Mode

Table 4.3 Power Consumption

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Distributor and Sales Representatives

Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A – References

Document References

FT602 datasheet: DS_FT602Q

FT60X PCB Layout Guidelines: AN_430 FT60X PCB Layout Guidelines

FT602 Chip Configuration Utility

Acronyms and Abbreviations

Terms	Description
FIFO	First In First Out
FMC	Field Programmable Mezzanine Card
HPC	High Pin Count
HSMC	High Speed Mezzanine Card
IO	Input Output
LPC	Low Pin Count
USB	Universal Serial Bus

Appendix B – List of Tables & Figures

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Appendix C – Revision History

Document Title: UMFT602X Module Datasheet

Document Reference No.: FT_001390

Clearance No.: FTDI#518

Product Page: http://www.ftdichip.com/Products/Modules/

Document Feedback: Send Feedback

Revision	Changes	Date
1.0	Initial Release	2017-02-21
1.1	Updated features/part numbers according to FT602Q Rev-B change	2017-11-23

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