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DELIVERY SPECIFICATIONS

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Panasonic Global Part Number AN41919A-VB

Vendor Issue Number 1203028

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Product Standards

Part No.	AN41919A
Package Code No.	∗QFN044-P-0606D

Semiconductor Company
Panasonic Corporation

Established by	Applied by	Checked by	Prepared by
	M. Hiramatsu	K. Tan	M. Nakahara

Contents

AN41919A

DC IRIS Control LSI for IP Camera and Network Camera

■ Overview

AN41919A is a DC IRIS control LSI for IP camera and security camera. It integrates digital PID control circuit and is able to control various IRIS motors.

■ Features

- Built-in DC IRIS controller
- DC IRIS control by 4-line serial data communication

■ Applications

- IP camera, security camera

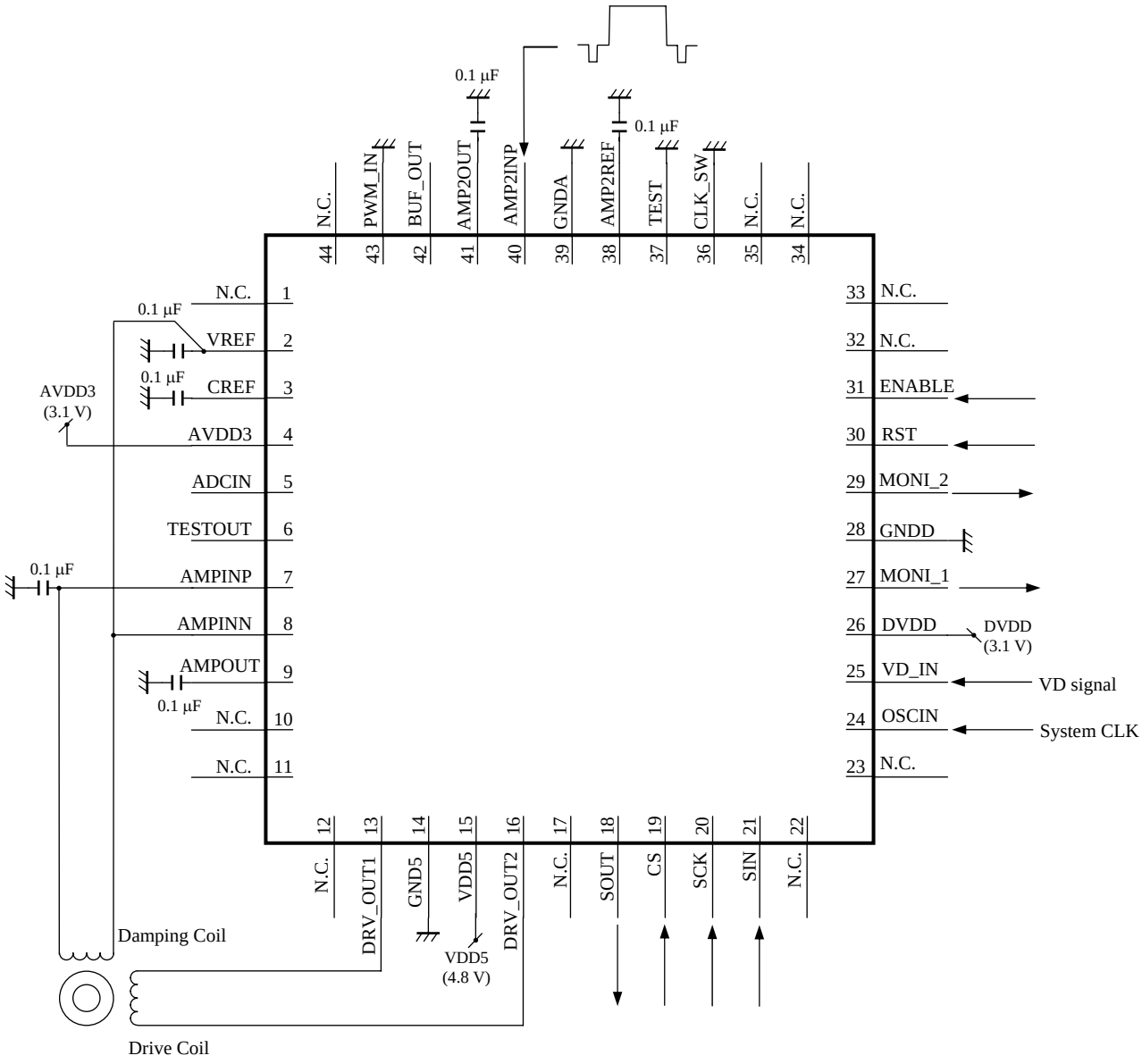
■ Package

- 44 pin Plastic Quad Flat Non-leaded Package (QFN Type)

■ Type

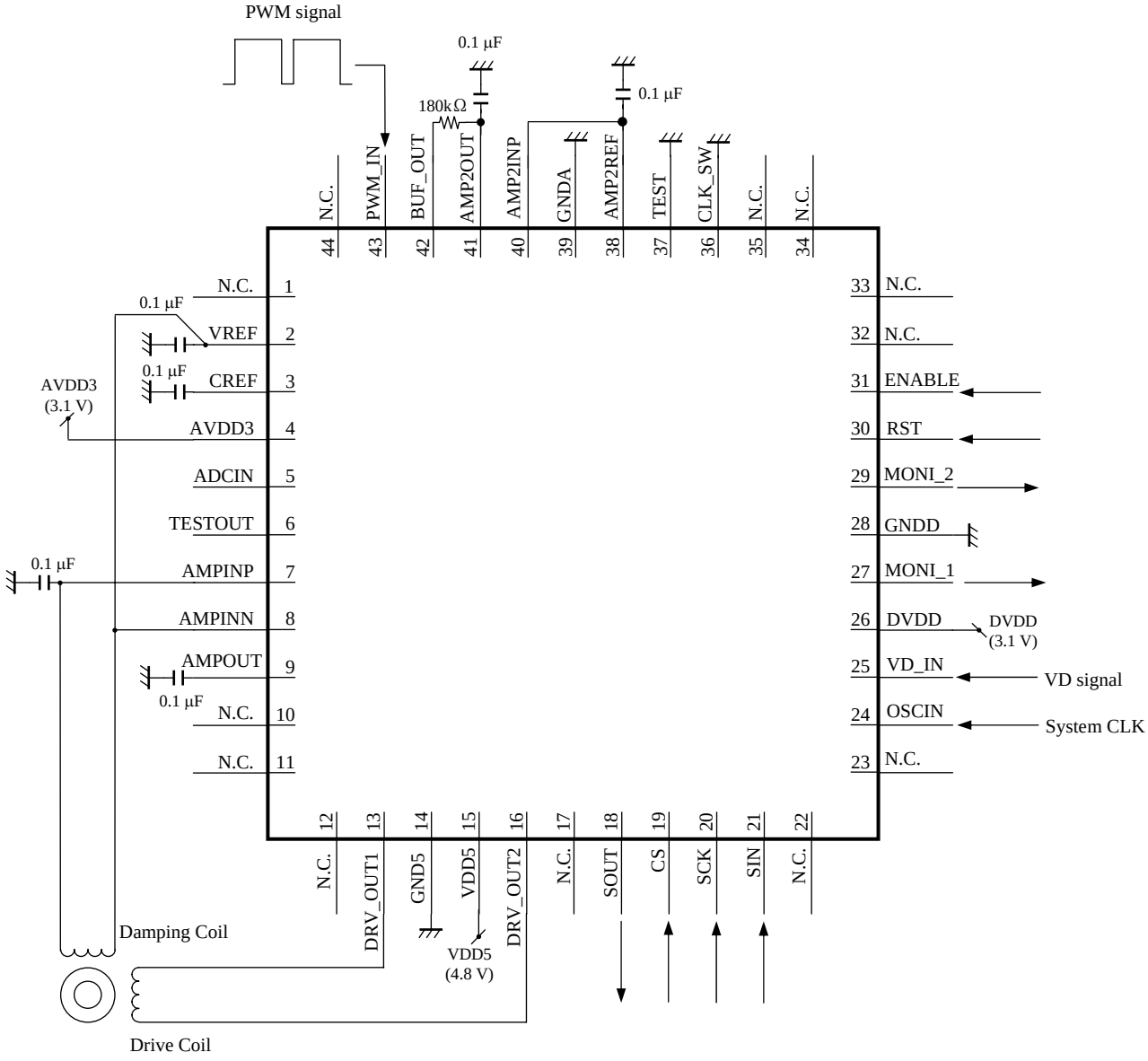
- Bi-COMS IC

■ Application Circuit Example1 (Analog Luminance signal)



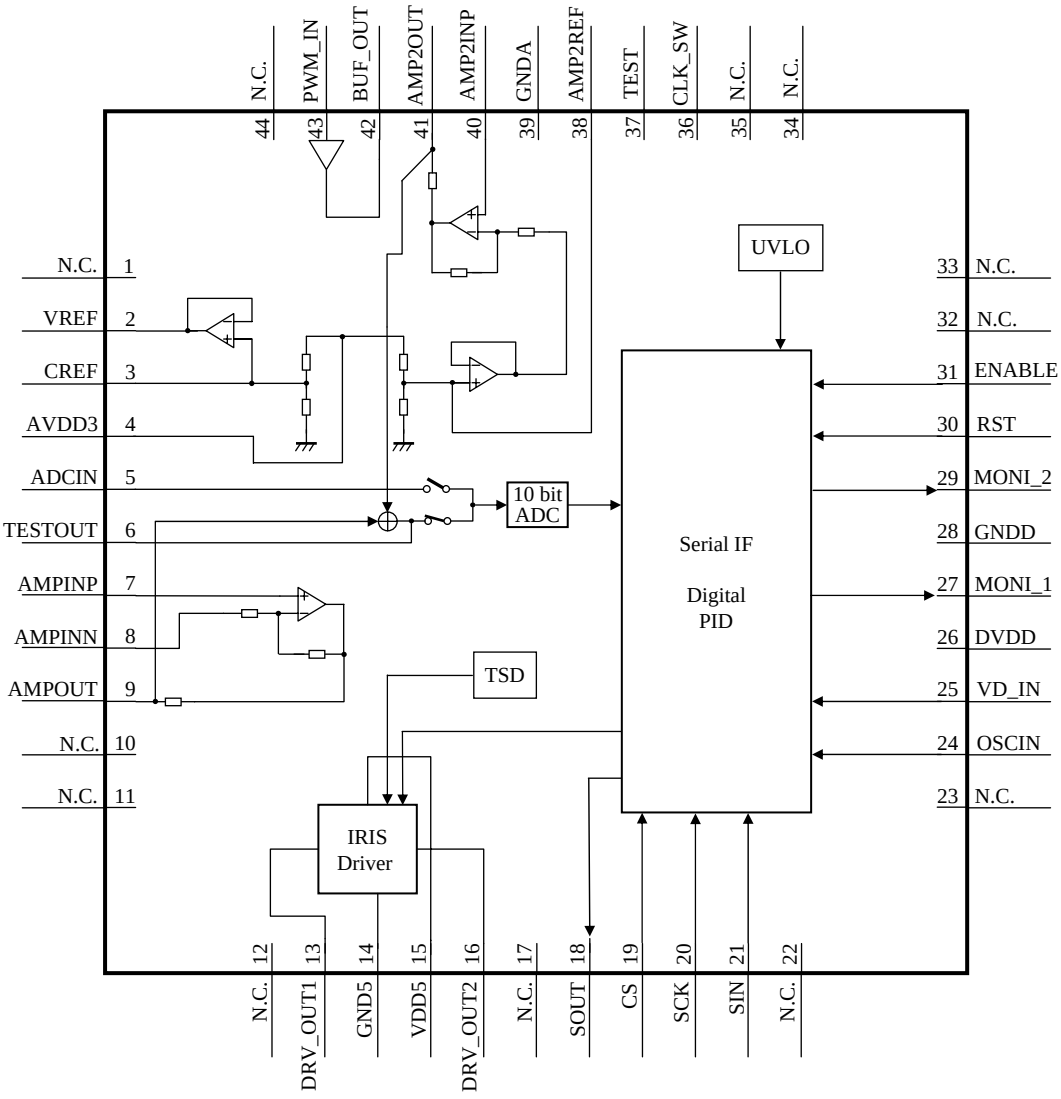
Notes) • This application circuit is an example. The operation of mass production set is not guaranteed. Perform enough evaluation and verification on the design of mass production set.

■ Application Circuit Example2 (continued) (PWM signal)



Notes) • This application circuit is an example. The operation of mass production set is not guaranteed. Perform enough evaluation and verification on the design of mass production set.

■ Block Diagram



Note) This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

■ Pin Descriptions

Pin No.	Pin name	Type	Description
1	N. C.	—	N. C.
2	VREF	Output	Reference voltage for damping coil signal amplifier
3	CREF	—	(AVDD3)/2 capacitor connection pin
4	AVDD3	Power supply	3 V analog power supply
5	ADCIN	Input	ADC test input
6	TESTOUT	Output	Test output
7	AMPINP	Input	Damping coil signal amplifier non-inverting input
8	AMPINN	Input	Damping coil signal amplifier inverting input
9	AMPOUT	Output	Damping coil signal amplifier output
10	N. C.	—	N. C.
11	N. C.	—	N. C.
12	N. C.	—	N. C.
13	DRV_OUT1	Output	Motor output 1
14	GND5	Ground	GND for motor
15	VDD5	Power supply	Power supply for motor
16	DRV_OUT2	Output	Motor output 2
17	N. C.	—	N. C.
18	SOUT	Output	Serial data output
19	CS	Input	Chip select signal input
20	SCK	Input	Serial clock input
21	SIN	Input	Serial data input
22	N. C.	—	N. C.
23	N. C.	—	N. C.
24	OSCIN	Input	System clock input
25	VD_IN	Input	IRIS video sync signal input
26	DVDD	Power supply	3 V digital power supply
27	MONI_1	Output	Monitor output 1
28	GNDD	Ground	Digital GND
29	MONI_2	Output	Monitor output 2
30	RST	Input	Reset signal input
31	ENABLE	Input	Enable signal input
32	N. C.	—	N. C.
33	N. C.	—	N. C.
34	N. C.	—	N. C.
35	N. C.	—	N. C.

■ Pin Descriptions (continued)

Pin No.	Pin name	Type	Description
36	CLK_SW	Input	System clock frequency select
37	TEST	Input	Test mode input
38	AMP2REF	—	Reference voltage for CDS signal amplifier
39	GNDA	Ground	3 V analog GND
40	AMP2INP	Input	CDS signal input
41	AMP2OUT	Output	CDS signal amplifier output
42	BUF_OUT	Output	PWM signal output
43	PWM_IN	Input	PWM signal input
44	N. C.	—	N. C.

■ Absolute Maximum Ratings

Note) Absolute maximum ratings are limit values which do not result in damages to this IC, and IC operation is not guaranteed at these limit values.

A No.	Parameter	Symbol	Rating	Unit	Notes
1	Controller supply voltage	AVDD3	–0.3 to +4.0	V	*1
		DVDD	–0.3 to +4.0		
2	Supply voltage for motor controller	VDD5	–0.3 to +6.0	V	*1
3	Power dissipation	P_D	141.4	mW	*2
4	Operating ambient temperature	T_{opr}	–20 to +85	°C	*3
5	Storage temperature	T_{stg}	–55 to +125	°C	*3
6	Motor driver H bridge drive current	I_M	±0.15	A/ch	—
7	Digital input voltage	V_{in}	–0.3 to (DVDD + 0.3)	V	*4

Notes) *1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2 : The power dissipation shown is the value at T_a = 85°C for the independent (unmounted) IC package without a heat sink. When using this IC, refer to the P_D-T_a diagram of the package standard and design the heat radiation with sufficient margin so that the allowable value might not be exceeded based on the conditions of power supply voltage, load, and ambient temperature.

*3 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.

*4 : (DVDD + 0.3) V must not be exceeded 4.0 V.

■ Operating Supply Voltage Range

Parameter	Symbol	Range			Unit	Notes
		Min	Typ	Max		
Supply voltage range	AVDD3	2.7	3.1	3.6	V	*1
	DVDD	2.7	3.1	3.6		
	VDD5	3.0	4.8	5.5		

Note) *1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

■ Allowable Current and Voltage Range

Notes)
- Allowable current and voltage ranges are limit ranges which do not result in damages to this IC, and IC operation is not guaranteed within these limit ranges.
- Voltage values, unless otherwise specified, are with respect to GND.
  GND is voltage for GNDA, GNDD, and GND5. GND = GNDA = GNDD = GND5
- VCC3V is voltage for AVDD3 and DVDD. AVDD3 = DVDD
- Do not apply external currents or voltages to any pin not specifically mentioned.
- For the circuit currents, "+" denotes current flowing into the IC, and "–" denotes current flowing out of the IC.

Pin No.	Pin name	Rating	Unit	Notes
5	ADCIN	–0.3 to (AVDD3 + 0.3)	V	*1
7	AMPINP	–0.3 to (AVDD3 + 0.3)	V	*1
8	AMPINN	–0.3 to (AVDD3 + 0.3)	V	*1
19	CS	–0.3 to (DVDD + 0.3)	V	*1
20	SCK	–0.3 to (DVDD + 0.3)	V	*1
21	SIN	–0.3 to (DVDD + 0.3)	V	*1
24	OSCIN	–0.3 to (DVDD + 0.3)	V	*1
25	VD_IN	–0.3 to (DVDD + 0.3)	V	*1
30	RST	–0.3 to (DVDD + 0.3)	V	*1
31	ENABLE	–0.3 to (DVDD + 0.3)	V	*1
36	CLK_SW	–0.3 to (DVDD + 0.3)	V	*1
37	TEST	–0.3 to (DVDD + 0.3)	V	*1
40	AMP2INP	–0.3 to (AVDD3 + 0.3)	V	*1
43	PWM_IN	–0.3 to (DVDD + 0.3)	V	*1

Pin No.	Pin name	Rating	Unit	Notes
13	DRV_OUT1	±0.15	A	—
16	DRV_OUT2	±0.15	A	—

Note) *1 : (AVDD3 + 0.3) V must not be exceeded 4.0 V, and (DVDD + 0.3) V must not be exceeded 4.0 V.

■ Electrical Characteristics at VDD5 = 4.8 V, DVDD = AVDD3 = 3.1 V

Note) T_a = 25°C±2°C unless otherwise specified.

B No.	Parameter	Symbol	Test circuits	Conditions	Limits			Unit	Notes
					Min	Typ	Max		
Current circuit									
P1	3 V supply current on Reset	$Icc3_{reset}$	1	RST = Low, No 27 MHz input	—	0	10.0	μA	—
P2	3 V supply current on Enable	$Icc3_{enable}$	1	RST = High, ENABLE = High, 27 MHz input, Output open	—	7	14	mA	—
P3	VDD5 supply current on Reset	$Icc5_{reset}$	1	RST = Low, No 27 MHz input	—	0	3.0	μA	—
P4	VDD5 supply current on Enable	$Icc5_{enable}$	1	RST = High, ENABLE = High, 27 MHz input, Output open	—	0.2	0.4	mA	—
P5	Supply current on Standby	$Icc_{standby}$	1	RST = High, ENABLE = Low, 27 MHz input, output open Total current	—	2	4	mA	—
Digital input / output									
D1	High-level input	$V_{in(H)}$	2	RST	0.54 × DVDD	—	DVDD + 0.3	V	—
D2	Low-level input	$V_{in(L)}$	2	RST	–0.3	—	0.2 × DVDD	V	—
D3	SOUT High-level output	$V_{out(H)}$: SDATA	2	[SOUT] 1 mA Source	DVDD – 0.5	—	—	V	—
D4	SOUT Low-level output	$V_{out(L)}$: SDATA	2	[SOUT] 1 mA Sink	—	—	0.5	V	—
D5	MONI_1 to 2 High-level output	$V_{out(H)}$: MUX	2	—	0.9 × DVDD	—	—	V	—
D6	MONI_1 to 2 Low-level output	$V_{out(L)}$: MUX	2	—	—	—	0.1 × DVDD	V	—
D7	Input pull-down resistance	$R_{pullret}$	3	RST, ENABLE	50	100	200	kΩ	—
Motor driver									
H1	H bridge ON resistance	R_{onIR}	4	IM = 50 mA	—	—	5	Ω	—
H2	H bridge leak current	I_{leakIR}	5	—	—	—	0.8	μA	—

■ Electrical Characteristics (continued) at VDD5 = 4.8 V, DVDD = AVDD3 = 3.1 V

Note) T_a = 25°C±2°C unless otherwise specified.

B No.	Parameter	Symbol	Test circuits	Conditions	Limits			Unit	Notes
					Min	Typ	Max		
AMP (Damping Coil signal Amplifier)									
O1	Input voltage range	V_{IN}	6	AMPINN = 1.55 V	1.05	—	2.05	V	—
O2	Input offset voltage	V_{OF}	6	—	–15	—	15	mV	—
O3	Output voltage (Low)	V_{OL}	7	ILOAD = –100 μA	—	0.2	0.4	V	—
O4	Output voltage (High)	V_{OH}	7	ILOAD = 100 μA	AVDD3 – 0.4	AVDD3 – 0.2	—	V	—
O5	Gain	V_{OG}	6	Gain setting value : 0h	19.7	21.9	24.1	V/V	—
AMP2 (CDS signal Amplifier)									
O6	Input offset voltage	V_{OF2}	9	—	–20	—	20	mV	—
O7	Output voltage (Low)	V_{OL2}	8	ILOAD = –100 μA	—	0.2	0.4	V	—
O8	Output voltage (High)	V_{OH2}	8	ILOAD = 100 μA	AVDD3 – 0.4	AVDD3 – 0.2	—	V	—
O9	Gain	V_{OG2}	9	Gain setting value : 9h	1.75	2	2.25	V/V	—
Reference voltage output block									
O10	Output voltage	VREF	6	ILOAD = 0 A, CVREF = 0.1 μF	1.45	1.55	1.65	V	—

■ Electrical Characteristics (Reference values for design) at VDD5 = 4.8 V, DVDD = AVDD3 = 3.1 V

Notes) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

B No.	Parameter	Symbol	Test circuits	Conditions	Reference values			Unit	Notes
					Min	Typ	Max		
Serial port input									
S1	Serial clock	Sclock	—	—	1	—	5	MHz	—
S2	SCK low time	T1	—	—	100	—	—	ns	—
S3	SCK high time	T2	—	—	100	—	—	ns	—
S4	CS setup time	T3	—	—	60	—	—	ns	—
S5	CS hold time	T4	—	—	60	—	—	ns	—
S6	CS disable high time	T5	—	—	100	—	—	ns	—
S7	SIN setup time	T6	—	—	50	—	—	ns	—
S8	SIN hold time	T7	—	—	50	—	—	ns	—
S9	SOUT delay time	T8	—	—	—	—	60	ns	—
S10	SOUT hold time	T9	—	—	60	—	—	ns	—
S11	SOUT Enable-Hi-Z time	T10	—	—	—	—	60	ns	—
S12	SOUT Hi-Z-Enable time	T11	—	—	—	—	60	ns	—
S13	SOUT C load	T_{SC}	—	—	—	—	40	pF	—
Digital input / output									
D8	High-level input threshold voltage	$V_{in(H)}$	—	SCK, SIN, CS, OSCIN, VD_IN, ENABLE, CLK_SW TEST	—	1.36	—	V	—
D9	Low-level input threshold voltage	$V_{in(L)}$	—	SCK, SIN, CS, OSCIN, VD_IN, ENABLE, CLK_SW TEST	—	1.02	—	V	—
D10	RST signal pulse width	T_{rst}	—	—	100	—	—	µs	—
D11	Input hysteresis width	V_{hysin}	—	SCK, SIN, CS, OSCIN, VD_IN, ENABLE, CLK_SW TEST	—	0.34	—	V	—
D12	CS signal wait time 1	$T_{(VD-CS)}$	—	—	400	—	—	ns	—
D13	CS signal wait time 2	$T_{(CS-DT1)}$	—	—	5	—	—	µs	—

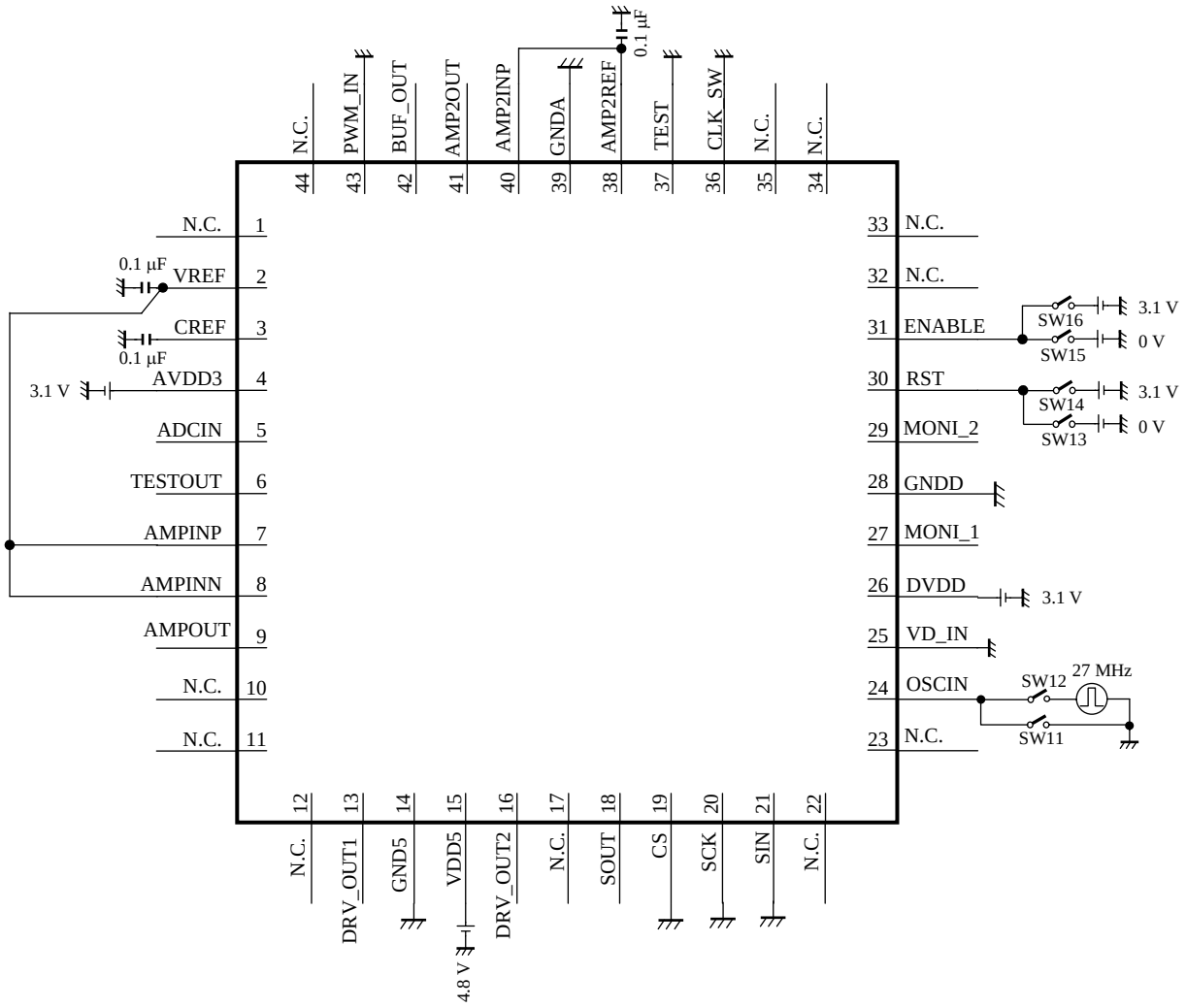
■ Electrical Characteristics (Reference values for design) (continued) at VDD5 = 4.8 V, DVDD = AVDD3 = 3.1 V

Notes) T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

B No.	Parameter	Symbol	Test circuits	Conditions	Reference values			Unit	Notes
					Min	Typ	Max		
IRIS control									
IR1	AD sampling frequency	$IRIS_{Sample}$	—	OSCIN = 27 MHz	—	500	—	kHz	—
Thermal shutdown									
T1	Thermal shutdown operation temperature	T_{tsd}	—	—	—	150	—	°C	—
T2	Thermal shutdown hysteresis width	ΔT_{tsd}	—	—	—	40	—	°C	—
Supply voltage monitor circuit									
R1	AVDD3 Reset operation	V_{rston}	—	—	—	2.27	—	V	—
R2	AVDD3 Reset hysteresis width	V_{rsthys}	—	—	—	0.2	—	V	—
R3	VDD5 Reset operation	$V_{rstISon}$	—	—	—	2.2	—	V	—
R4	VDD5 Reset hysteresis width	$V_{rstIShys}$	—	—	—	0.2	—	V	—
8 bit DAC for Damping Coil signal Amplifier Offset adjustment									
DA1	Adjustment range (High)	DAOTHof	—	—	—	AVDD3	—	V	—
DA2	Adjustment range (Low)	DAOTLof	—	—	—	0	—	V	—
10 bit ADC									
AD1	Input Range (High)	$V_{in(H)}$	—	—	—	—	AVDD3 – 0.2	V	—
AD2	Input Range (Low)	$V_{in(L)}$	—	—	0.2	—	—	V	—
AD3	DNLE (Differential linearity error)	DNL10A	—	—	—	1.0	—	LSB	—
AD4	INLE (Integral linearity error)	INL10A	—	—	—	2.0	—	LSB	—
Reference voltage output block									
O11	Output voltage 1	VREFH	—	ILOAD = 100 μA, CVREF = 0.1 μF	—	—	VREF + 0.1	V	—
O12	Output voltage 2	VREFL	—	ILOAD = –100 μA, CVREF = 0.1 μF	VREF – 0.1	—	—	V	—

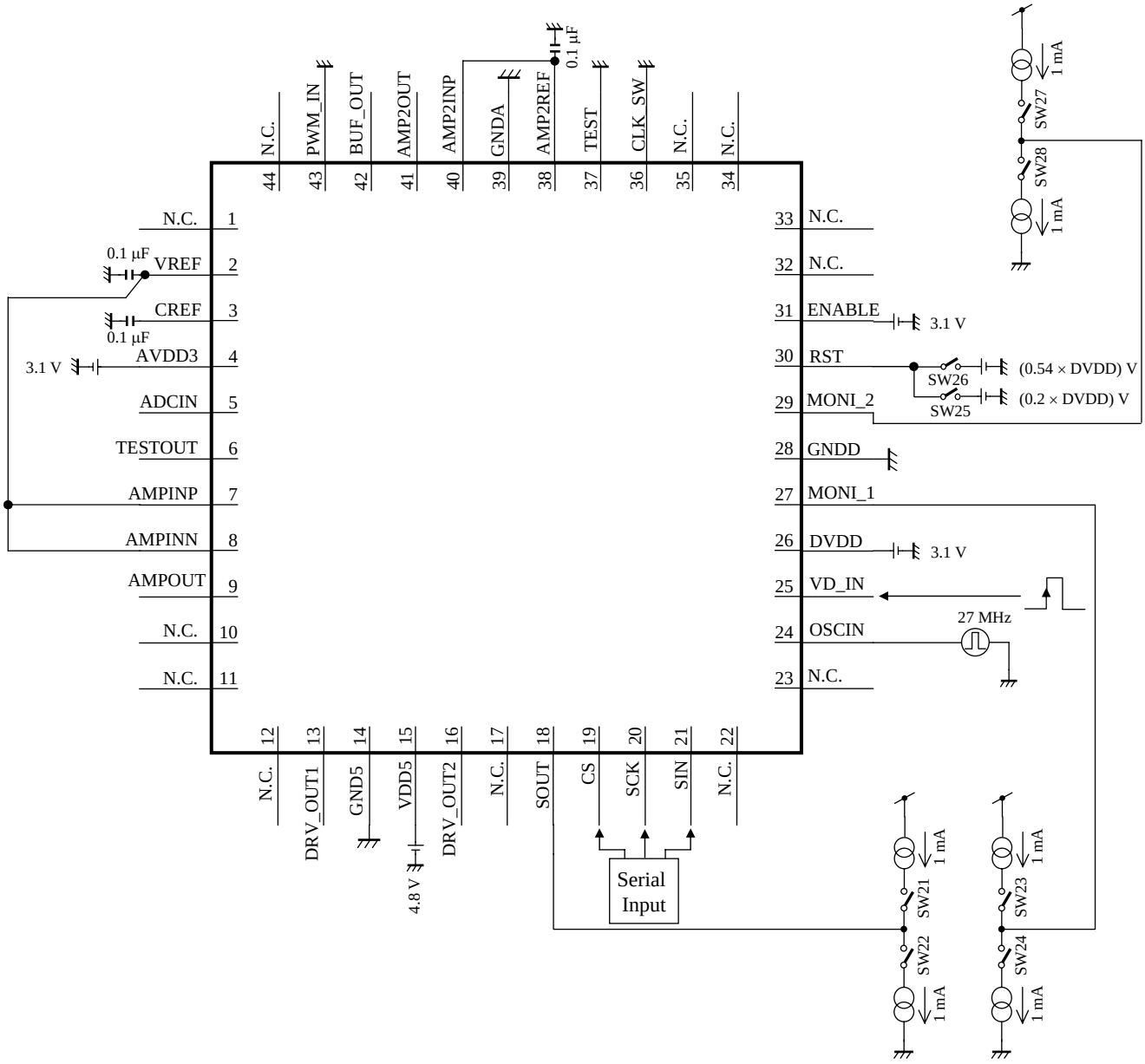
■ Test Circuit Diagram

1. Test Circuit 1 (Circuit current)



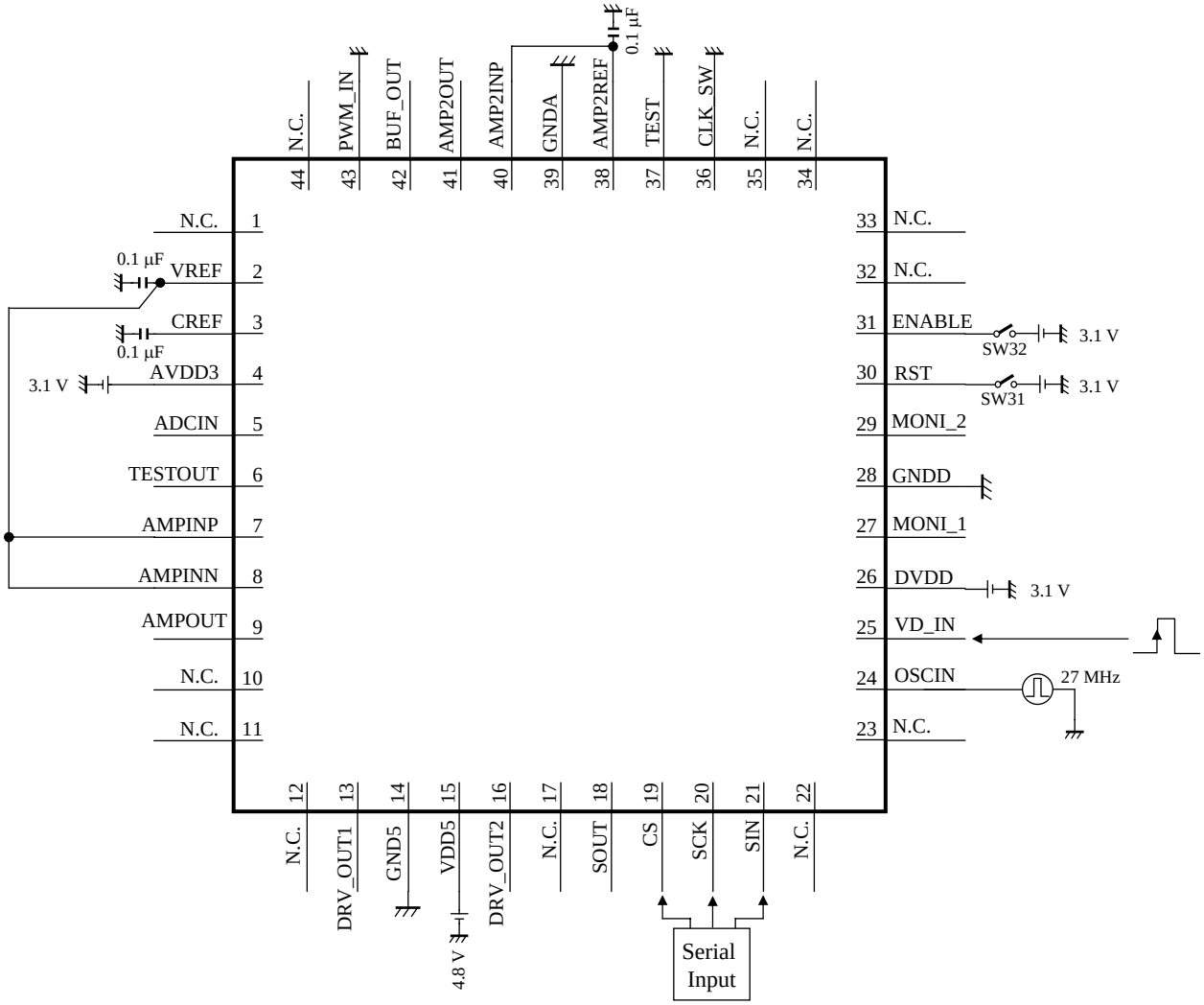
■ Test Circuit Diagram (continued)

2. Test Circuit 2 (Digital input / output)



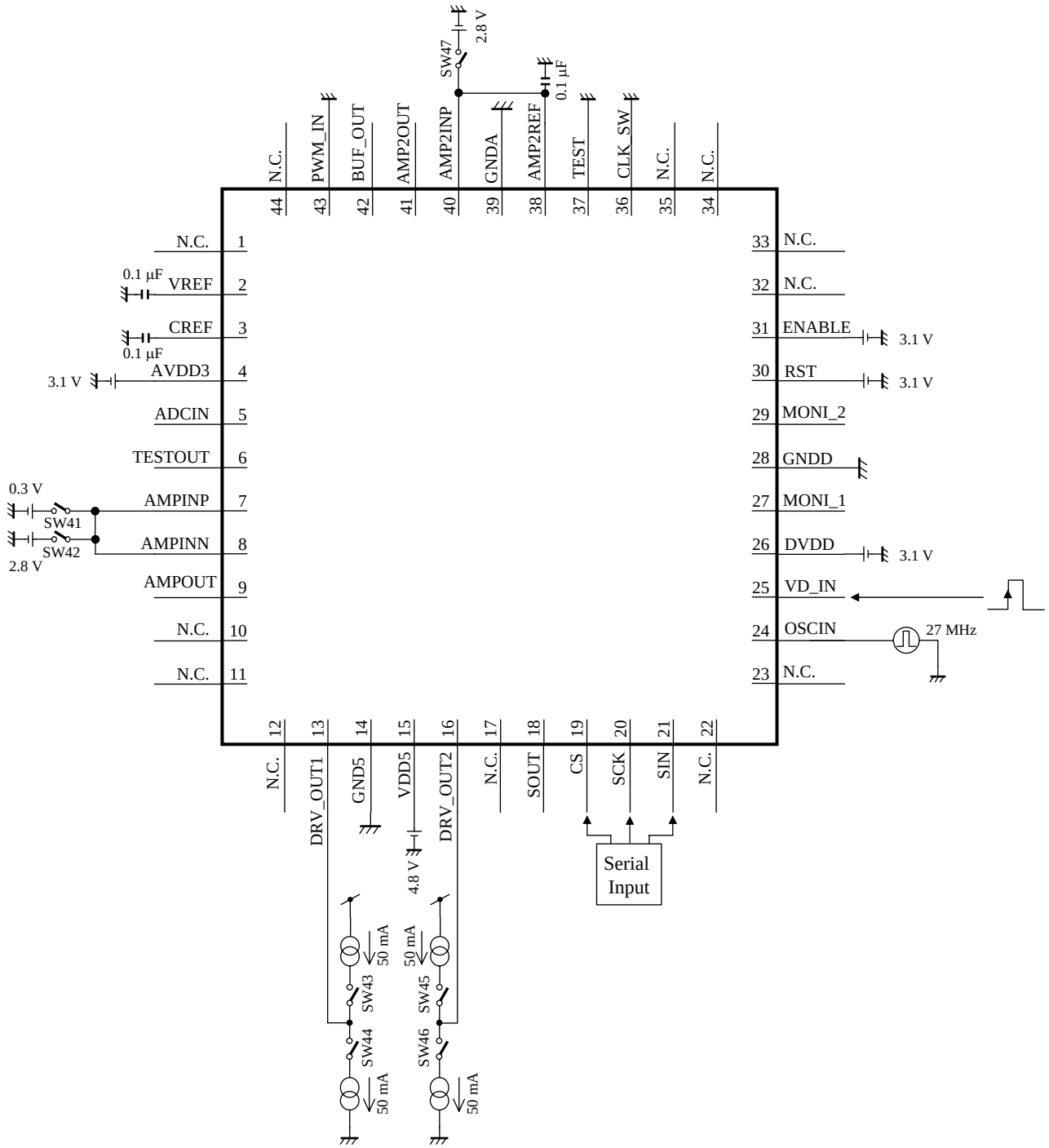
■ Test Circuit Diagram (continued)

3. Test Circuit 3 (Digital input / output : Input pull-down resistance)



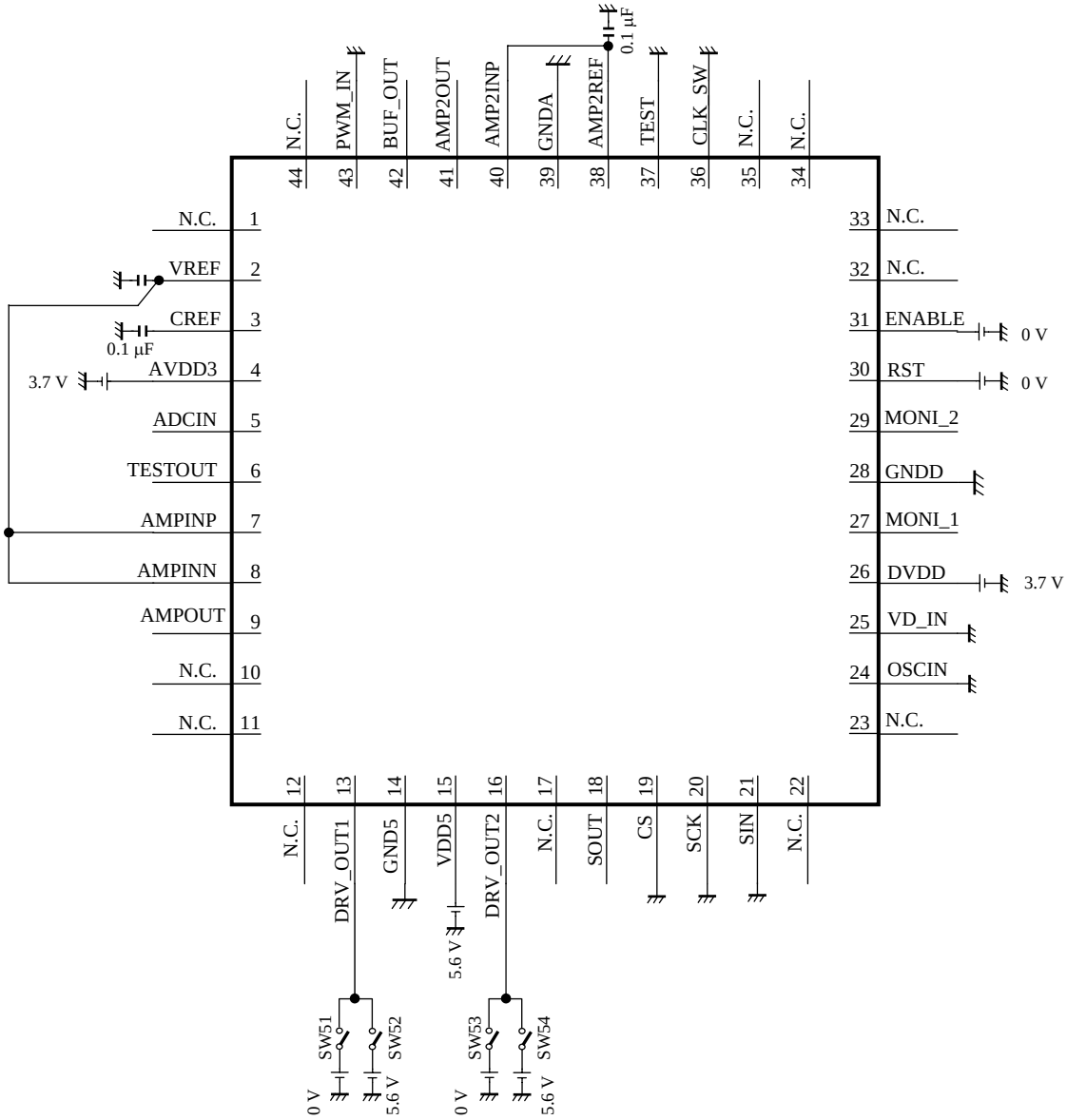
■ Test Circuit Diagram (continued)

4. Test Circuit 4 (Motor driver : IRIS H bridge ON resistance)



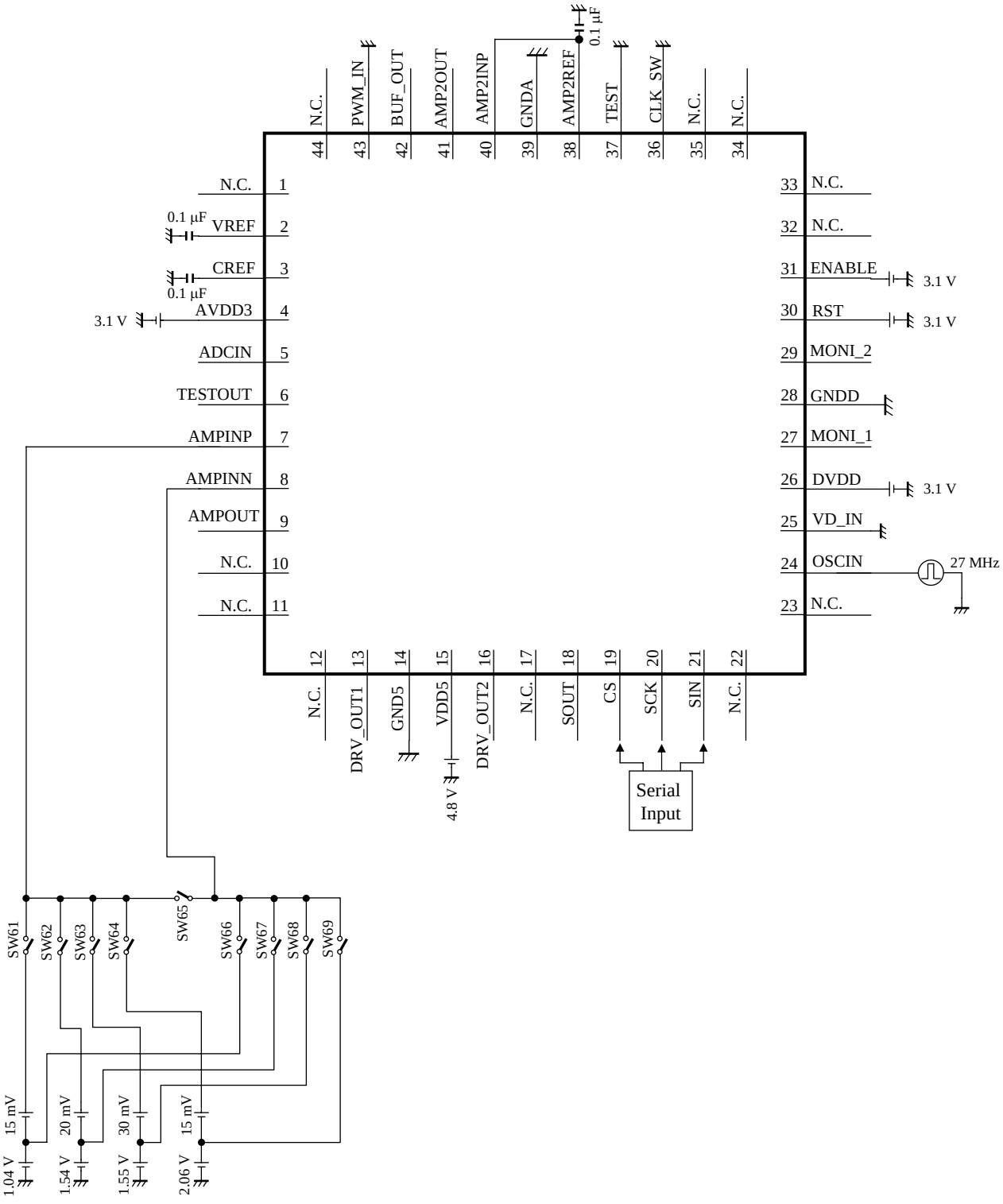
■ Test Circuit Diagram (continued)

5. Test Circuit 5 (Motor driver : H bridge leak current)



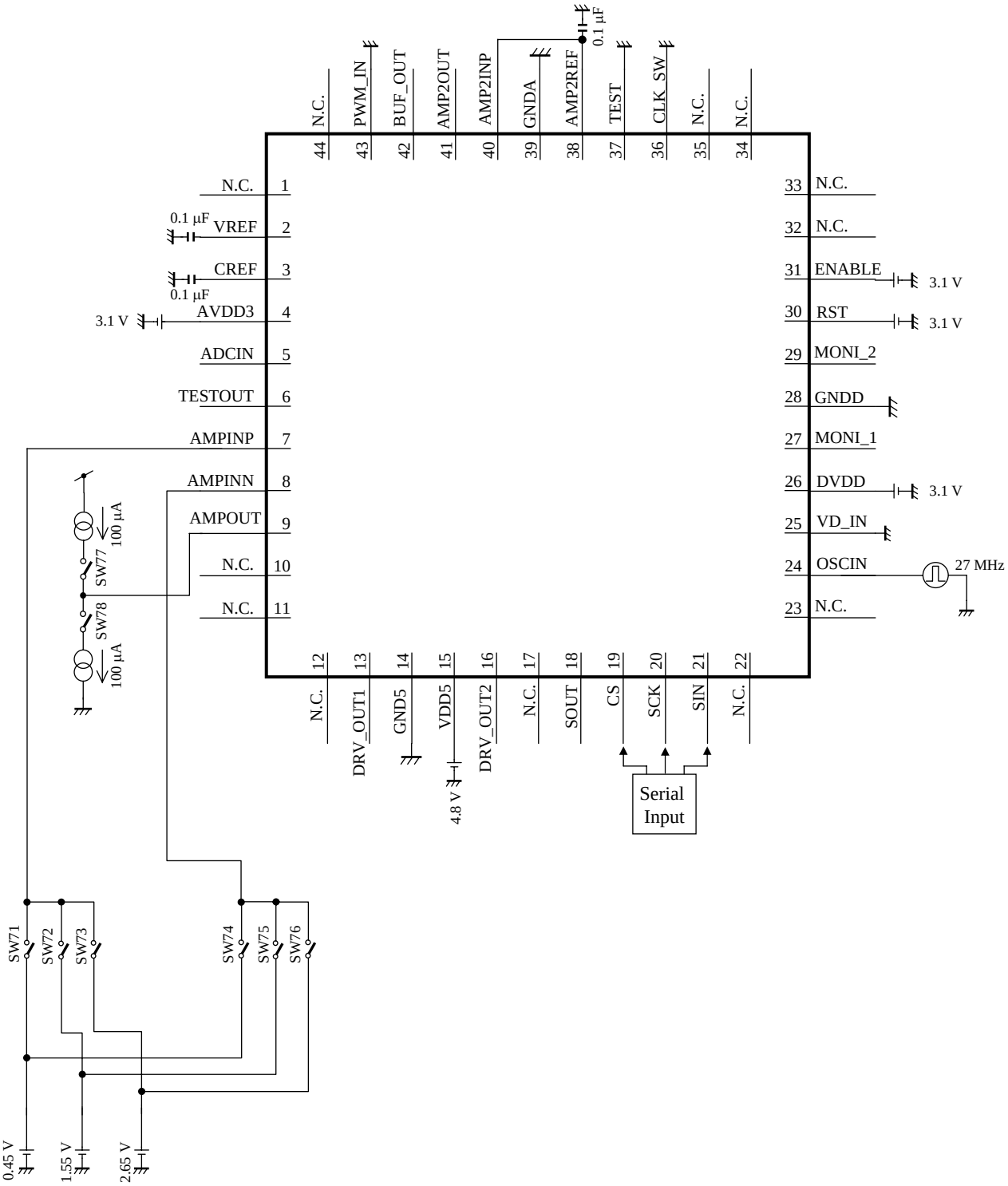
■ Test Circuit Diagram (continued)

6. Test Circuit 6 (Damping Coil signal Amplifier1, Reference voltage output block)



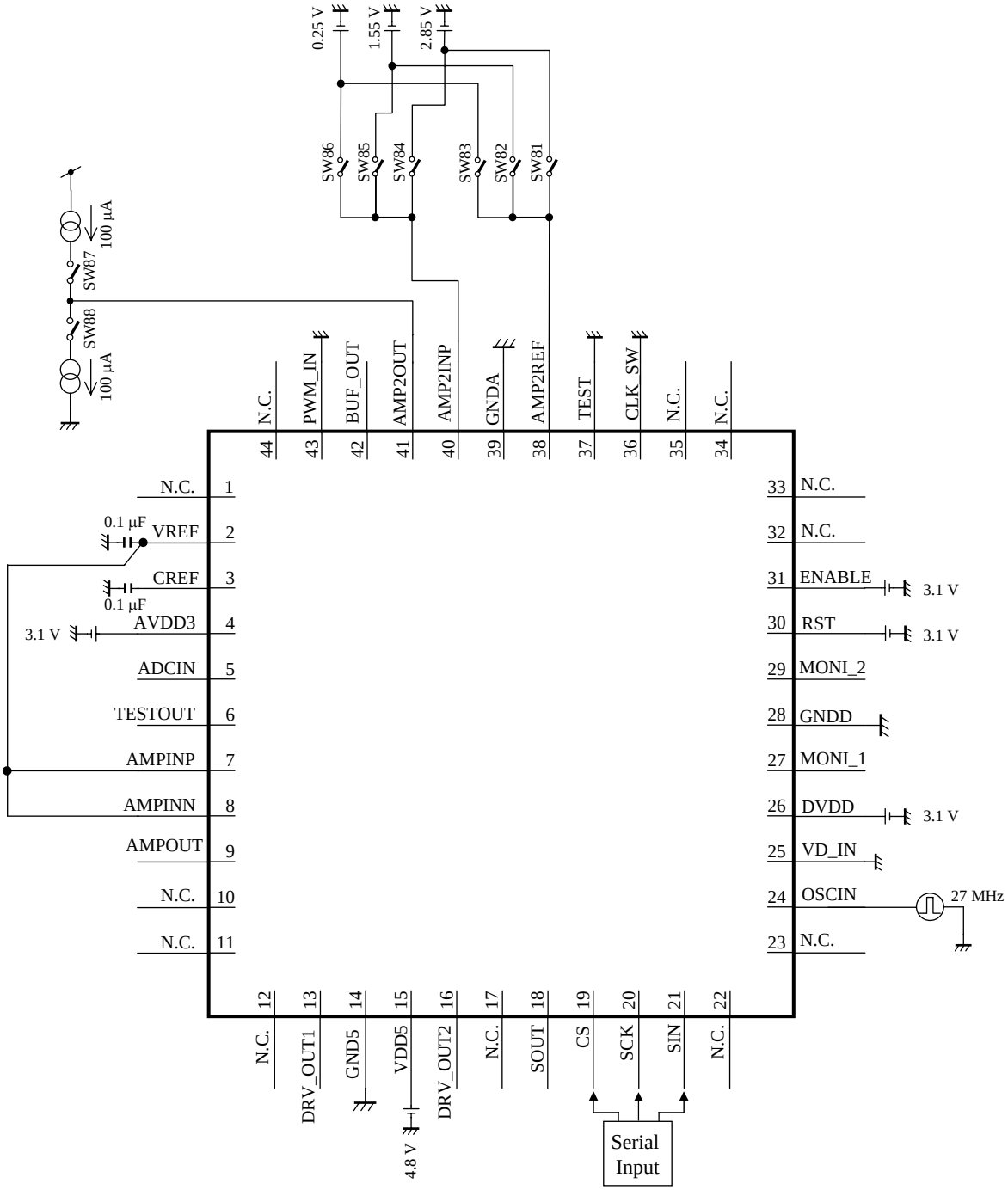
■ Test Circuit Diagram (continued)

7. Test Circuit 7 (Damping Coil signal Amplifier2)



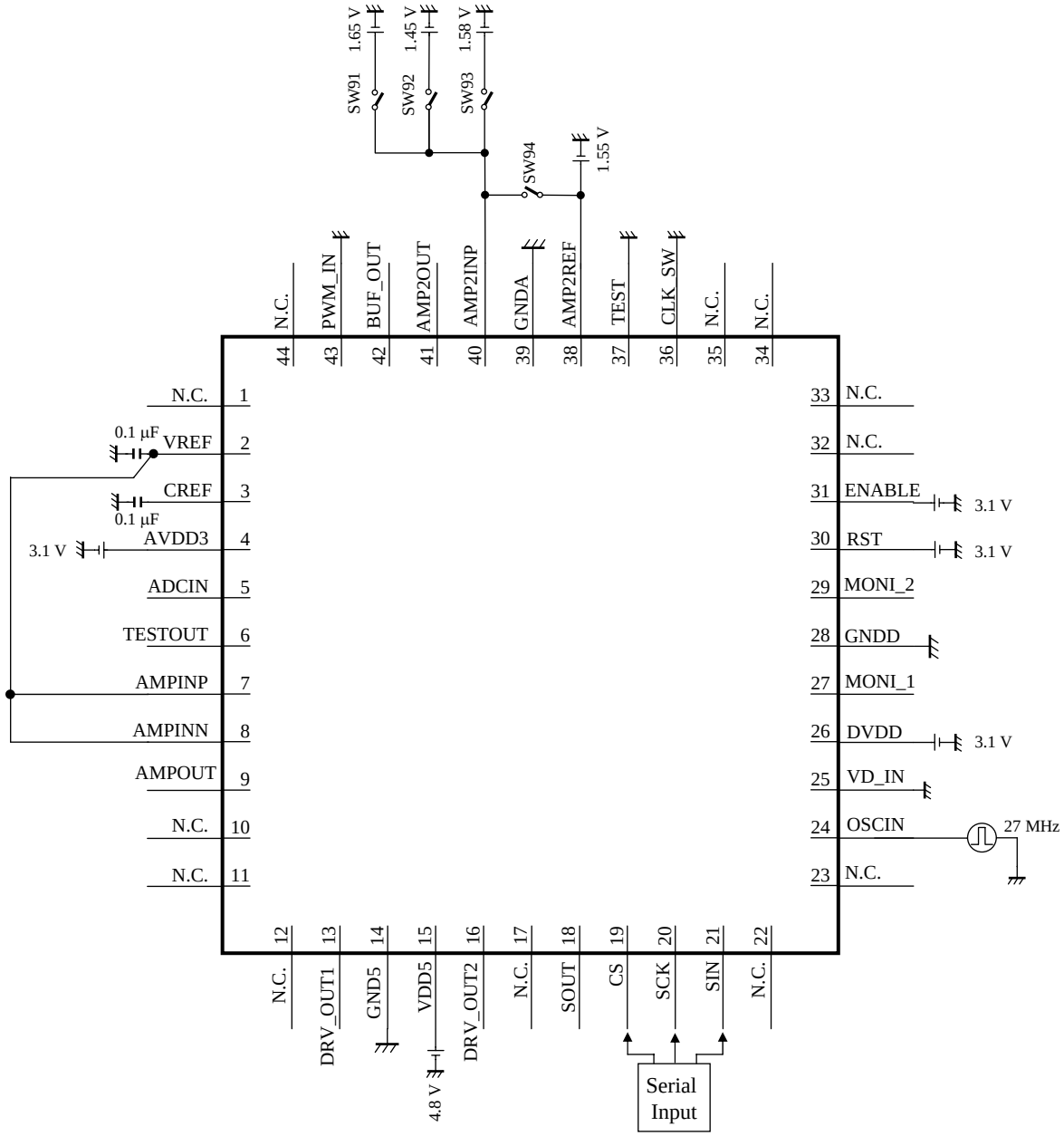
■ Test Circuit Diagram (continued)

8. Test Circuit 8 (CDS signal Amplifier1)



■ Test Circuit Diagram (continued)

9. Test Circuit 9 (CDS signal Amplifier2)



■ Electrical Characteristics Test Procedures

C No.	Parameter	Input		Output		Pin settings					
		Pin No.	Conditions	Pin No.	Conditions	SW11	SW12	SW13	SW14	SW15	SW16
Circuit current, Common circuit											
P1	3 V supply current on Reset	15	4.8 V	4 26	Measure the current	ON	OFF	ON	OFF	ON	OFF
		4 26	3.1 V								
		24	0 V								
		30	0 V								
P2	3 V supply current on Enable	15	4.8 V	4 26	Measure the current	OFF	ON	OFF	ON	OFF	ON
		4 26	3.1 V								
		24	27 MHz, 0 V / 3.1 V								
		30	3.1 V								
		31	3.1 V								
P3	VDD5 supply current on Reset	15	4.8 V	15	Measure the current	ON	OFF	ON	OFF	ON	OFF
		4 26	3.1 V								
		24	0 V								
		30	0 V								
P4	VDD5 supply current on Enable	15	4.8 V	15	Measure the current	OFF	ON	OFF	ON	OFF	ON
		4 26	3.1 V								
		24	27 MHz, 0 V / 3.1 V								
		30	3.1 V								
		31	3.1 V								
P5	Supply current on Standby	15	4.8 V	4 15 26	Measure the current	OFF	ON	OFF	ON	ON	OFF
		4 26	3.1 V								
		24	27 MHz, 0 V / 3.1 V								
		30	3.1 V								
		31	0 V								

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings					
		Pin No.	Conditions	Pin No.	Conditions	SW21	SW22	SW23 SW27	SW24 SW28	SW25	SW26
Digital input / output											
D1	High-level input	4 26	3.1 V	3	Measure the voltage (Confirm 1/2 × AVDD3)	OFF	OFF	OFF	OFF	OFF	ON
		15	4.8 V								
		30	0.54 × DVDD								
		24	27 MHz, 0 V / 3.1 V								
D2	Low-level input	4 26	3.1 V	3	Measure the voltage (Confirm AVDD3)	OFF	OFF	OFF	OFF	ON	OFF
		15	4.8 V								
		30	0.2 × DVDD								
		24	27 MHz, 0 V / 3.1 V								
D3	SOUT High-level output	4 26	3.1 V	18	Measure the voltage (Read Mode)	OFF	ON	OFF	OFF	OFF	ON
		15	4.8 V								
		30	0.54 × DVDD								
		18	–1 mA								
		24	27 MHz, 0 V / 3.1 V								
		21	*1								
D4	SOUT Low-level output	4 26	3.1 V	18	Measure the voltage (Read Mode)	ON	OFF	OFF	OFF	OFF	ON
		15	4.8 V								
		30	0.54 × DVDD								
		18	1 mA								
		24	27 MHz, 0 V / 3.1 V								
		21	*2								

	address		Data
*1 : Serial setting	04h	=	FFFFh
*2 : Serial setting	04h	=	0000h

Note）Serial settings are reflected on the rising edge of VD_IN.

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings					
		Pin No.	Conditions	Pin No.	Conditions	SW21	SW22	SW23 SW27	SW24 SW28	SW25	SW26
Digital input / output (continued)											
D5	MONI_1 to 2 High-level output	4 26	3.1 V	27 29	Measure the voltage	OFF	OFF	OFF	ON	OFF	ON
		15	4.8 V								
		30	0.54 × DVDD								
		27	–1 mA								
		29	–1 mA								
		24	27 MHz, 0 V / 3.1 V								
		21	*3								
D6	MONI_1 to 2 Low-level output	4 26	3.1 V	27 29	Measure the voltage	OFF	OFF	ON	OFF	OFF	ON
		15	4.8 V								
		30	0.54 × DVDD								
		27	1 mA								
		29	1 mA								
		24	27 MHz, 0 V / 3.1 V								
		21	*4								

	address		Data
*3 : Serial setting	09h	=	8000h
	20h	=	8000h
*4 : Serial setting	20h	=	8004h

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings	
		Pin No.	Conditions	Pin No.	Conditions	SW31	SW32
Digital input / output (continued)							
D7	Input pull-down resistance	4 26	3.1 V	30 31	Measure the current(I30, I31) $R_{pullret}$ = 3.1 V/I30(or I31)	ON	ON
		15	4.8 V				
		30	3.1 V				
		31	3.1 V				

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings						
		Pin No.	Conditions	Pin No.	Conditions	SW41	SW42	SW43	SW44	SW45	SW46	SW47
Motor driver												
H1	H bridge ON resistance DRV_OUT (DRV_OUT1_UP + DRV_OUT2_DOWN)	4 26	3.1 V	13 14 15 16	Measure the voltage Ron = {(Pin15 – Pin13) + (Pin16 – Pin14)} / 50 mA	ON	OFF	OFF	ON	ON	OFF	OFF
		15	4.8 V									
		30 31	3.1 V									
		24	27 MHz, 0 V / 3.1 V									
		21	*5									
		7 8	0.3 V									
		38 40	SW47 OPEN									
		13	–50 mA									
		16	50 mA									
H1	H bridge DRV_OUT (DRV_OUT2_UP + DRV_OUT1_DOWN)	4 26	3.1 V	13 14 15 16	Measure the voltage Ron = {(Pin15 – Pin16) + (Pin13 – Pin14)} / 50 mA	OFF	ON	ON	OFF	OFF	ON	ON
		15	4.8 V									
		30 31	3.1 V									
		24	27 MHz, 0 V / 3.1 V									
		21	*6									
		7 8	2.8 V									
		38 40	2.8 V									
		13	50 mA									
		16	–50 mA									

	address		Data
*5 : Serial setting	00h	=	0200h
	03h	=	1040h
	07h	=	0F0Fh
	09h	=	0700h
	20h	=	8000h
	21h	=	07FFh
*6 : Serial setting	21h	=	05FFh

Note） Serial settings are reflected on the rising edge of VD_IN

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings			
		Pin No.	Conditions	Pin No.	Conditions	SW51	SW52	SW53	SW54
Motor driver (continued)									
H2	H bridge leak current upper	4 26	3.7 V	13 16	Measure the current	ON	OFF	ON	OFF
		15	5.6 V						
		30	0 V						
		31	0 V						
H2	H bridge leak current lower	4 26	3.7 V	13 16	Measure the current	OFF	ON	OFF	ON
		15	5.6 V						
		30	0 V						
		31	0 V						

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings								
		Pin No.	Conditions	Pin No.	Conditions	SW61	SW62	SW63	SW64	SW65	SW66	SW67	SW68	SW69
AMP (Damping Coil signal Amplifier)														
O1	Input voltage range Low	4 26	3.1 V	9	Measure the voltage ; Vo1 : Output voltage when inputting 1.04 V to Pin 7 and Pin 8 Vo2 : Output voltage when inputting 1.055 V to Pin 7, 1.04 V to Pin 8 Calculation (Vo1 – 1.04) × 0.015 / (Vo2 – Vo1) Confirm that the calculational result is within input offset rating.	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
		15	4.8 V											
		24	27 MHz, 0 V / 3.1 V											
		30 31	3.1 V											
		21	*7											
		7 8	1.04 V											
		7	1.055 V			ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
O1	Input voltage range High	4 26	3.1 V	9	Measure the voltage ; Vo1 : Output voltage when inputting 2.06 V to Pin 7 and Pin 8 Vo2 : Output voltage when inputting 2.075 V to Pin 7, 2.06 V to Pin 8 Calculation (Vo1 – 2.06) × 0.015 / (Vo2 – Vo1) Confirm that the calculational result is within input offset rating.	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON
		15	4.8 V											
		24	27 MHz, 0 V / 3.1 V											
		30 31	3.1 V											
		21	*7											
		7 8	2.06 V											
		7	2.075 V			OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON
O2	Input offset voltage	4 26	3.1 V	9	Measure the voltage Vo1 : Output voltage when inputting 1.55 V to Pin 7 and Pin 8 Vo2 : Output voltage when inputting 1.58 V to Pin 7, 1.55 V to Pin 8 Calculation (Vo1 – 1.55) × 0.03 / (Vo2 – Vo1)	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF
		15	4.8 V											
		24	27 MHz, 0 V / 3.1 V											
		30 31	3.1 V											
		21	*7											
		7 8	1.55 V											
		7	1.58 V			OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF

*7 : Serial setting

address		Data
01h	=	1000h
08h	=	0003h
3Fh	=	0100h

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings							
		Pin No.	Conditions	Pin No.	Conditions	SW71	SW72	SW73	SW74	SW75	SW76	SW77	SW78
AMP (Damping Coil signal Amplifier) (continued)													
O3	Output voltage Low	4 26	3.1 V	9	Measure the voltage	OFF	ON	OFF	OFF	OFF	ON	ON	OFF
		15	4.8 V										
		24	27 MHz, 0 V / 3.1 V										
		30 31	3.1 V										
		21	*8										
		7	1.55 V										
		8	2.65 V										
		9	100 μA										
O3	Output voltage Low	4 26	3.1 V	9	Measure the voltage	ON	OFF	OFF	OFF	ON	OFF	ON	OFF
		15	4.8 V										
		24	27 MHz, 0 V / 3.1 V										
		30 31	3.1 V										
		21	*8										
		7	0.45 V										
		8	1.55 V										
		9	100 μA										

	address		Data
*8 : Serial setting	01h	=	1000h
	06h	=	0080h
	08h	=	0003h

Note）Serial settings are reflected on the rising edge of VD_IN

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings							
		Pin No.	Conditions	Pin No.	Conditions	SW71	SW72	SW73	SW74	SW75	SW76	SW77	SW78
AMP (Damping Coil signal Amplifier) (continued)													
O4	Output voltage High	4 26	3.1 V	9	Measure the voltage	OFF	OFF	ON	OFF	ON	OFF	OFF	ON
		15	4.8 V										
		24	27 MHz, 0 V / 3.1 V										
		30 31	3.1 V										
		21	*9										
		7	2.65 V										
		8	1.55 V										
		9	–100 μA										
O4	Output voltage High	4 26	3.1 V	9	Measure the voltage	OFF	ON	OFF	ON	OFF	OFF	OFF	ON
		15	4.8 V										
		24	27 MHz, 0 V / 3.1 V										
		30 31	3.1 V										
		21	*9										
		7	1.55 V										
		8	0.45 V										
		9	–100 μA										

	address		Data
*9 : Serial setting	01h	=	1000h
	06h	=	0080h
	08h	=	0003h

Note）Serial settings are reflected on the rising edge of VD_IN

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings								
		Pin No.	Conditions	Pin No.	Conditions	SW61	SW62	SW63	SW64	SW65	SW66	SW67	SW68	SW69
AMP (Damping Coil signal Amplifier) (continued)														
O5	Gain	4 26	3.1 V	9	Measure the voltage Vo1 : Output voltage when inputting 1.54 V to Pin 7 and Pin 8 Vo2 : Output voltage when inputting 1.56 V to Pin 7, 1.54 V to Pin 8 Calculation (Vo2 – Vo1)/0.02	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF
		15	4.8 V											
		24	27 MHz, 0 V / 3.1 V											
		30 31	3.1 V											
		21	*10											
		7 8	1.54 V											
		7	1.56 V			OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF

	address		Data
*10 : Serial setting	01h	=	1000h
	06h	=	0080h
	08h	=	0030h

Note）Serial settings are reflected on the rising edge of VD_IN

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings							
		Pin No.	Conditions	Pin No.	Conditions	SW81	SW82	SW83	SW84	SW85	SW86	SW87	SW88
AMP2 (CDS signal Amplifier)													
O7	Output voltage Low	4 26	3.1 V	41	Measure the voltage	OFF	ON	OFF	OFF	OFF	ON	ON	OFF
		15	4.8 V										
		24	27 MHz, 0 V / 3.1 V										
		30 31	3.1 V										
		21	*11										
		38	1.55 V										
		40	0.25 V										
		41	100 μA										
O7	Output voltage Low	4 26	3.1 V	41	Measure the voltage	ON	OFF	OFF	OFF	ON	OFF	ON	OFF
		15	4.8 V										
		24	27 MHz, 0 V / 3.1 V										
		30 31	3.1 V										
		21	*11										
		38	2.85 V										
		40	1.55 V										
		41	100 μA										

*11 : Serial setting

address		Data
01h	=	1000h
08h	=	B003h

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Pin settings							
		Pin No.	Conditions	Pin No.	Conditions	SW81	SW82	SW83	SW84	SW85	SW86	SW87	SW88
AMP2 (CDS signal Amplifier) (continued)													
O8	Output voltage High	4 26	3.1 V	41	Measure the voltage	OFF	ON	OFF	ON	OFF	OFF	OFF	ON
		15	4.8 V										
		24	27 MHz, 0 V / 3.1 V										
		30 31	3.1 V										
		21	*12										
		38	1.55 V										
		40	2.85 V										
		41	–100 μA										
O8	Output voltage High	4 26	3.1 V	41	Measure the voltage	OFF	OFF	ON	OFF	ON	OFF	OFF	ON
		15	4.8 V										
		24	27 MHz, 0 V / 3.1 V										
		30 31	3.1 V										
		21	*12										
		38	0.25 V										
		40	1.55 V										
		41	–100 μA										

*12 : Serial setting

address		Data
01h	=	1000h
08h	=	B030h

■ Electrical Characteristics Test Procedures (continued)

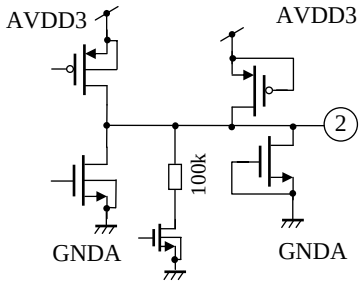
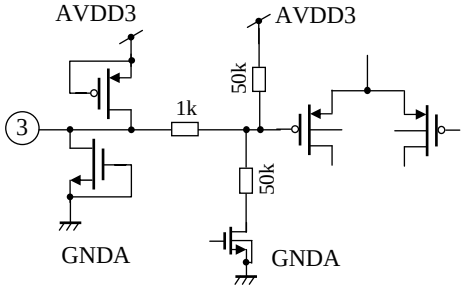
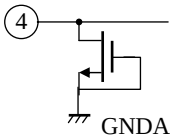
C No.	Parameter	Input		Output		Pin settings			
		Pin No.	Conditions	Pin No.	Conditions	SW91	SW92	SW93	SW94
AMP2 (CDS signal Amplifier) (continued)									
O6	Input offset voltage	4 26	3.1 V	41	Measure the voltage Vo1 : Output voltage when inputting 1.55 V to Pin 38 and Pin 40 Vo2 : Output voltage when inputting 1.58 V to Pin 40, 1.55 V to Pin 38 Calculation (Vo1 – 1.55) × 0.03 / (Vo2 – Vo1)	OFF	OFF	OFF	ON
		15	4.8 V						
		24	27 MHz, 0 V / 3.1 V						
		30 31	3.1 V						
		21	*13						
		38 40	1.55 V						
		40	1.58 V			OFF	OFF	ON	OFF
O9	Gain	4 26	3.1 V	41	Measure the voltage Vo1 : Output voltage when inputting 1.55V to Pin 38, 1.45V to Pin 40 Vo2 : Output voltage when inputting 1.55 V to Pin 38, 1.65V to Pin 40 Calculation (Vo2 – Vo1)/0.2	OFF	ON	OFF	OFF
		15	4.8 V						
		24	27 MHz, 0 V / 3.1 V						
		30 31	3.1 V						
		21	*14						
		38	1.55V						
		40	1.45 V						
		40	1.65 V			ON	OFF	OFF	OFF

	address		Data
*13 : Serial setting	01h	=	1000h
	08h	=	0030h
*14 : Serial setting	08h	=	9030h

■ Technical Data

1. I/O block circuit diagrams and pin function descriptions

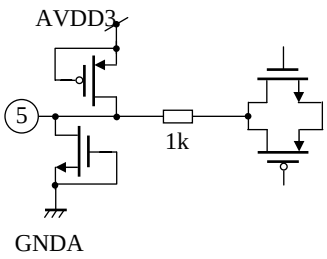
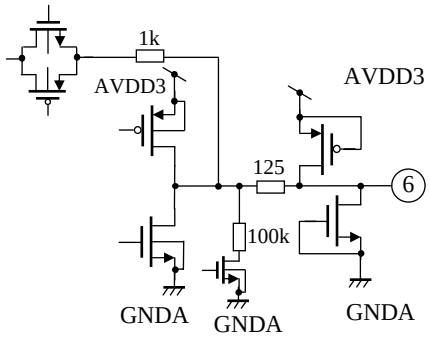
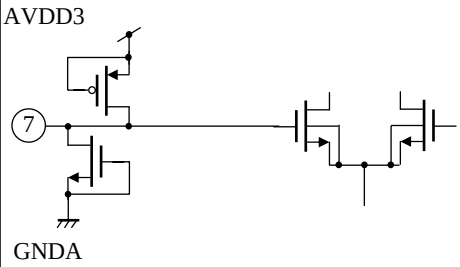
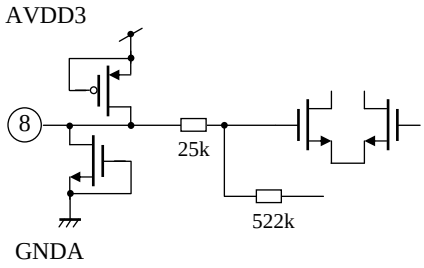
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
1	—	—	—	N.C.
2	—		—	VREF Reference voltage for Damping Coil signal amplifier
3	—		25 kΩ	CREF (AVDD3)/2 capacitor connection pin
4	AVDD3		—	AVDD3 3 V analog power supply pin

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

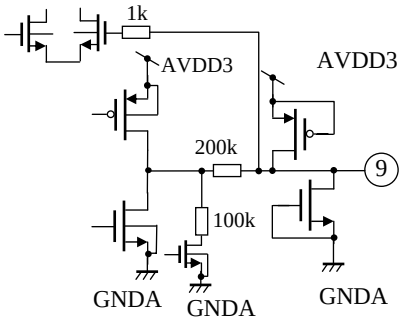
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
5	—		—	ADCIN ADC test input pin
6	—		—	TESTOUT Test output pin
7	—		—	AMPINP Damping Coil signal amplifier non-inverting input pin
8	—		—	AMPINN Damping Coil signal amplifier inverting input pin

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

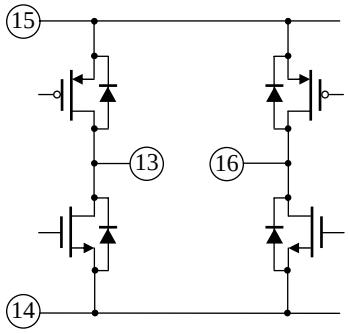
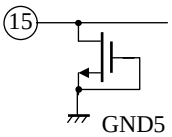
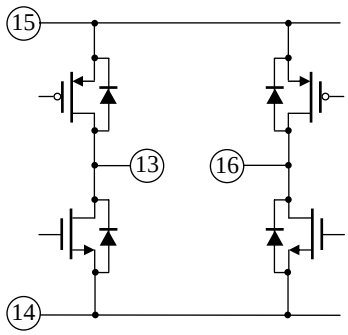
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
9	—		—	AMPOUT Damping Coil signal amplifier output pin
10	—	—	—	N.C.
11	—	—	—	N.C.
12	—	—	—	N.C.

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

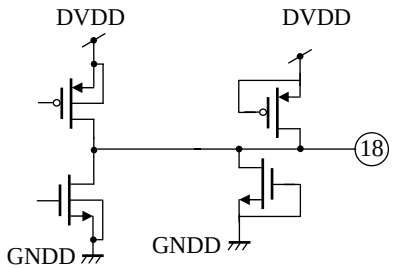
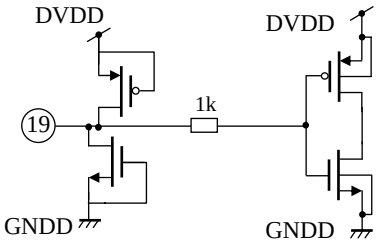
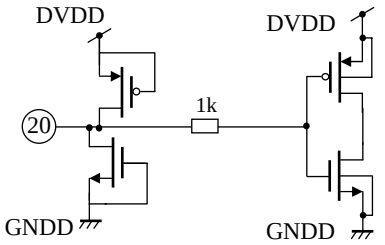
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
13	—		—	DRV_OUT1 Motor output pin 1
14	GND5		—	GND5 5 V GND pin
15	VDD5		—	VDD5 5 V power supply pin
16	—		—	DRV_OUT2 Motor output pin 2

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

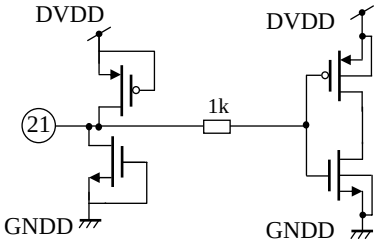
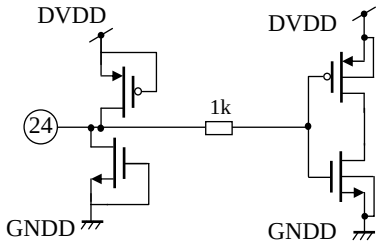
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
17	—	—	—	N.C.
18	GNDD to DVDD logic signal output / Hi-Z		—	SOUT Serial data output pin
19	GNDD to DVDD logic signal input		Hi-Z	CS Chip select signal input pin (Schmidt)
20	GNDD to DVDD logic signal input		Hi-Z	SCK Serial clock input pin (Schmidt)

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

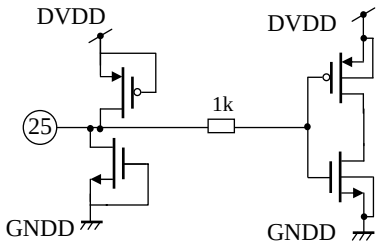
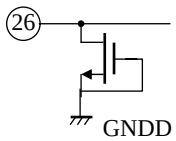
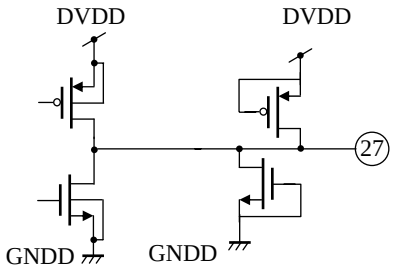
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
21	GNDD to DVDD logic signal input		Hi-Z	SIN Serial data input pin (Schmidt)
22	—	—	—	N.C.
23	—	—	—	N.C.
24	GNDD to DVDD logic signal input		Hi-Z	OSCIN System clock input pin

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

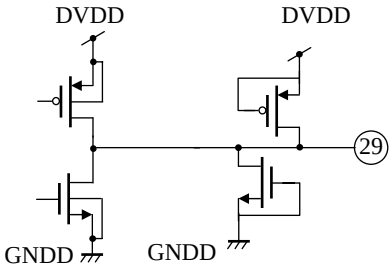
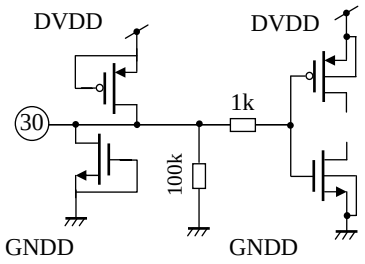
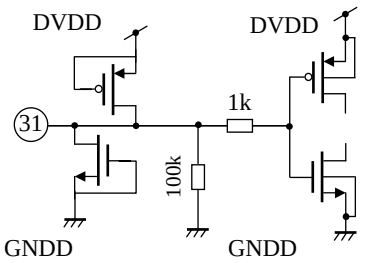
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
25	GNDD to DVDD logic signal input		Hi-Z	VD_IN IRIS video sync. signal input pin (Schmidt)
26	—		—	DVDD 3 V digital power supply pin
27	GNDD to DVDD logic signal output		—	MONI_1 Monitor 1 output pin
28	—		—	GNDD Digital GND pin

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

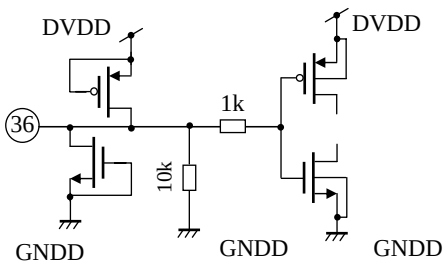
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
29	GNDD to DVDD logic signal output		—	MONI_2 Monitor 2 output pin
30	Logic signal input		100 kΩ	RST Reset signal input pin
31	Logic signal input		100 kΩ	ENABLE Enable signal input pin
32	—	—	—	N.C.

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

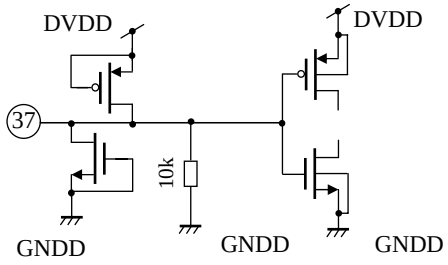
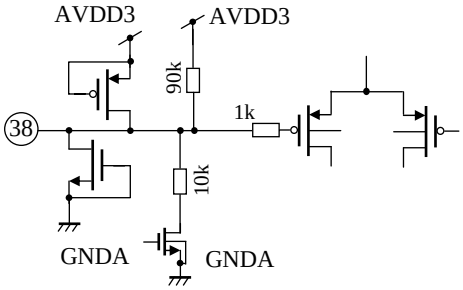
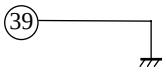
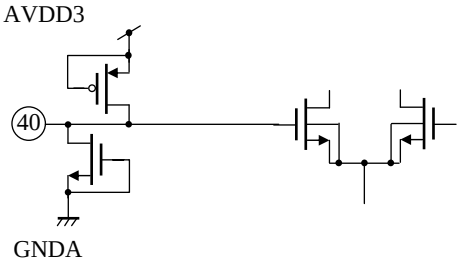
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
33	—	—	—	N.C.
34	—	—	—	N.C.
35	—	—	—	N.C.
36	—		10 kΩ	CLK_SW System clock frequency select

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

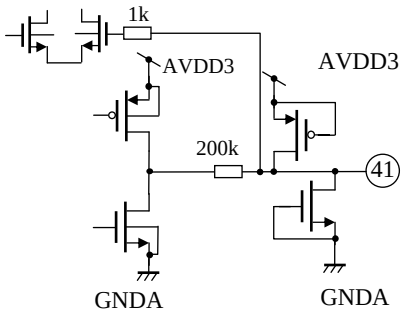
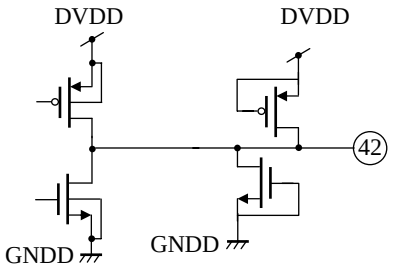
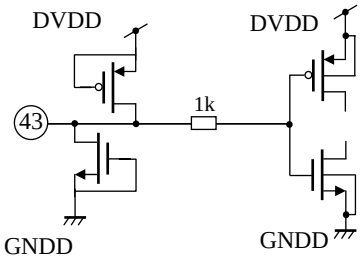
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
37	—		10 kΩ	TEST Test mode input pin TEST
38	—		9 kΩ	AMP2REF Reference voltage for CDS signal amplifier
39	—		—	GNDA 3 V analog GND
40	—		—	AMP2INP CDS signal input pin

■ Technical Data (continued)

1. I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
41	—		—	AMP2OUT CDS signal amplifier output pin
42	—		—	BUF_OUT PWM signal output pin
43	—		—	PWM_IN PWM signal input pin
44	—	—	—	N.C.

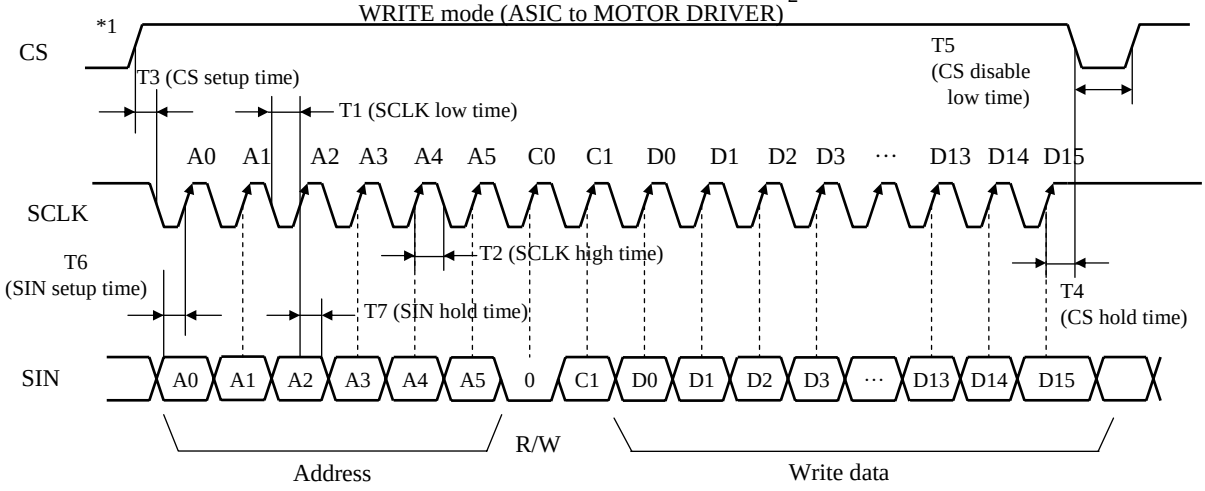
■ Technical Data (continued)

2. Read / Write of serial data

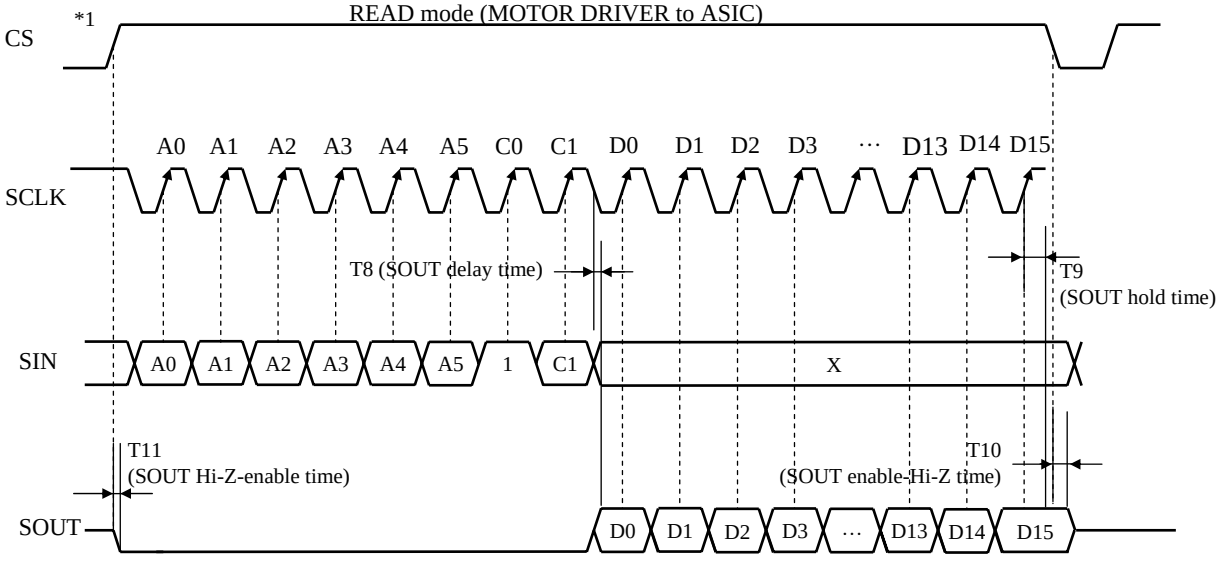
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Register input / output signal specification

WRITE mode (ASIC to MOTOR DRIVER)*2



READ mode (MOTOR DRIVER to ASIC)



Notes) *1 : CS default value of each cycle (Write / Read mode) starts from Low-level.

*2 : It is necessary to input the system clock OSCIN in write mode.

■ Technical Data (continued)

3. Register table

Register table

Address	Register name	Bit															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00h	Luminance Target	—	—	—	—	—	—	Y_TGT[9:0]									
01h	Target Update Timing	Y_PWM_POL	Y_PWM_ON	CDS_AMP_OFF	Reserved	—	—	—	—	TGT_UPDATE[7:0]							
02h	PID Filter(1)	—	—	—	TGT_FLT_OFF	TGT_LPF_FC[3:0]				—	—	DEC_AVE	AVE_SPEED[4:0]				
03h	PID(1)	PID_INV	—	—	LMT_ENB	ARW[3:0]				—	DGAIN[6:0]						
04h	PID(2)	PID_POLE[3:0]				PID_ZERO[3:0]				IRIS_ROUND[3:0]				IRIS_CALC_NR[3:0]			
05h	PID Filter(2)	—	—	—	—	PWM_FIL_OFF	PWM_LPF_FC[2:0]			AS_FLT_OFF	ASOUND_LPF_FC[2:0]			OVER_LPF_FC_2ND[1:0]		OVER_LPF_FC_1ST[1:0]	
06h	Offset DAC	—	—	—	—	—	—	—	—	DAMP_OFFSET_DAC[7:0]							
07h	Analog Adder	—	—	—	—	Y_MIX[3:0]				—	—	—	—	DAMP_MIX[3:0]			
08h	Analog LPF/Gain	Y_GAIN[3:0]				DAMP_GAIN[3:0]				—	—	Y_FLT[1:0]		—	—	DAMP_FLT[1:0]	
09h	PWM/Enable	TEST EN1	—	DT_ADJ_IRIS[1:0]		—	PWM_IRIS[2:0]			PID_CLIP[3:0]				ASWMODE[1:0]		VD_POL	ENABLE
0Ah	ADC Read	—	—	—	—	—	—	IRSAD[9:0] read only									
0Bh	Reserved	Panasonic Reserved															
0Ch	Pulse Generator	—	—	—	—	—	—	START1[9:0]									
0Dh	Pulse Generator	P1EN	—	—	—	WIDTH1[11:0]											
0Eh	Pulse Generator	—	—	—	—	—	—	START2[9:0]									
0Fh	Pulse Generator	P2EN	—	—	—	—	—	—	—	—	—	WIDTH2[5:0]					
20h	Test mode selection	TEST EN2	—	—	—	—	—	Panasonic Reserved		—	—	—	—	PLS_SEL[3:0]*			
21h	Test mode selection	—	—	—	—	—	DUTY_TEST	TGT_IN_TEST[9:0]									
22h	Reserved	Panasonic Reserved															
3Fh	Reserved	Panasonic Reserved															

— : Use prohibited

■ Technical Data (continued)

4. Register function table

Address	Register name / Bit wide	Function
00h	Y_TGT[9:0]	Luminance target
01h	TGT_UPDATE[7:0]	Y_TGT update delay time
	CDS_AMP_OFF	Luminance signal amplifier enable / disable
	Y_PWM_ON	PWM (luminance signal modulation) buffer enable / disable
	Y_PWM_POL	PWM_IN polarity selection
02h	AVE_SPEED[3:0]	DEC_AVE time controller
	DEC_AVE	Moving average of Luminance target
	TGT_LPF_FC[3:0]	Luminance target value LPF cut-off frequency
	TGT_FLT_OFF	IRIS target value LPF function enable / disable
03h	DGAIN[6:0]	PID controller digital gain
	ARW[3:0]	Number of bits in PID controller integrator
	LMT_ENB	PID controller integral stop
	PID_INV	PID controller polarity
04h	IRIS_CALC_NR[3:0]	PID controller integral error cumulative prevention level
	IRIS_ROUND[3:0]	PID controller differential error cumulative prevention level
	PID_ZERO[3:0]	PID controller zero point
	PID_POLE[3:0]	PID controller pole
05h	OVER_LPF_FC_1ST[1:0]	ADC feedback filter (1) cut-off frequency
	OVER_LPF_FC_2ND[1:0]	ADC feedback filter (2) cut-off frequency
	ASOUND_LPF_FC[2:0]	Filter cut-off frequency before PID controller
	AS_FLT_OFF	Filter before PID controller enable / disable
	PWM_LPF_FC[2:0]	LPF cut-off frequency after PID controller
	PWM_FLT_OFF	LPF after PID controller enable / disable
06h	DAMP_OFFSET_DAC[7:0]	Offset adjustment for damping coil output amplifier
07h	DAMP_MIX[3:0]	Damping coil signal mixed gain
	Y_MIX[3:0]	Luminance signal mixed gain
08h	DAMP_FLT[1:0]	Damping coil signal LPF cut-off frequency
	Y_FLT[1:0]	Luminance signal LPF cut-off frequency
	DAMP_GAIN[3:0]	Damping coil signal amplifier gain
	Y_GAIN[3:0]	Luminance signal amplifier gain

■ Technical Data (continued)

4. Register function table (continued)

Address	Register name / Bit wide	Function
09h	ENABLE	Enable / Disable CTL
	VD_POL	VD_IN polarity selection
	ASWMODE[1:0]	ADCIN pin connection selection
	PID_CLIP[3:0]	PWM max-duty control
	PWM_IRIS[2:0]	PWM frequency of IRIS block output
	DT_ADJ_IRIS[1:0]	Dead time correction of IRIS block output
	TESTEN1	Test mode enable 1
0Ah	IRSAD[9:0]	ADC output for IRIS (read only)
0Ch	START1[9:0]	Pulse 1 start time
0Dh	WIDTH1[11:0]	Pulse 1 width
	P1EN	Pulse 1 output enable
0Eh	START2[9:0]	Pulse 2 start time
0Fh	WIDTH2[5:0]	Pulse 2 width
	P2EN	Pulse 2 output enable
20h	PLS_SEL[3:0]*	Monitor output selection
	TESTEN2	Test mode enable 2
21h	DUTY_TEST	IRIS test mode 1
	TGT_IN_TEST[9:0]	IRIS test mode 2

■ Usage Notes

- Special attention and precaution in using

1. This IC is intended to be used for general electronic equipment [IP camera and network camera].
   Consult our sales staff in advance for information on the following applications:
   - Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
   - Any applications other than the standard applications intended.
     (1) Space appliance (such as artificial satellite, and rocket)
     (2) Traffic control equipment (such as for automobile, airplane, train, and ship)
     (3) Medical equipment for life support
     (4) Submarine transponder
     (5) Control equipment for power plant
     (6) Disaster prevention and security device
     (7) Weapon
     (8) Others : Applications of which reliability equivalent to (1) to (7) is required

   It is to be understood that our company shall not be held responsible for any damage incurred as a result of or in connection with your using the IC described in this book for any special application, unless our company agrees to your using the IC in this book for any special application.
2. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.
3. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
4. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.
5. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin-V_{CC} short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short) .
   And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.
6. When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
   Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.
7. When using the LSI for new models, verify the safety including the long-term reliability for each product.
8. When the application system is designed by using this LSI, be sure to confirm notes in this book.
   Be sure to read the notes to descriptions and the usage notes in the book.

■ Usage Notes (continued)

- Notes of Power LSI

1. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
   Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to V_{CC} short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.

2. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.

3. The product which has specified ASO (Area of Safe Operation) should be operated in ASO.

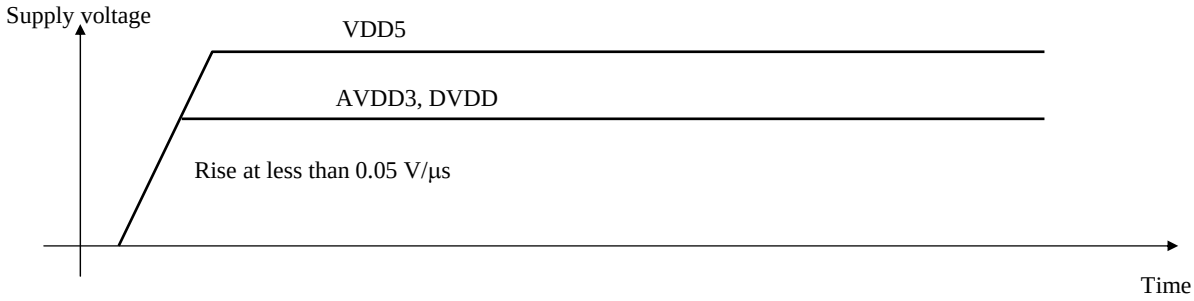
4. Verify the risks which might be caused by the malfunctions of external components.

5. Apply voltage from a low-impedance to power supply pins and connect a bypass capacitor to the LSI as near as possible.

- Notes for this LSI

Power-on and Supply voltage

When supplying to AVDD3 (Pin 4) ,VDD5 (Pin 15) , and DVDD (Pin 26), or raising supply voltage for these pins, set the rising speed of supply voltage to less than 0.05 V/μs. AVDD3, VDD5, and DVDD can be powered on in any sequence.



Connections to VREF and CREF

To VREF (Pin 2), do not connect other than recommended capacitor and damp coil.
To CREF (Pin 3), do not connect other than recommended capacitor.

Package Standards

Package Code	∗QFN044-P-0606D

Semiconductor Company
Panasonic Corporation

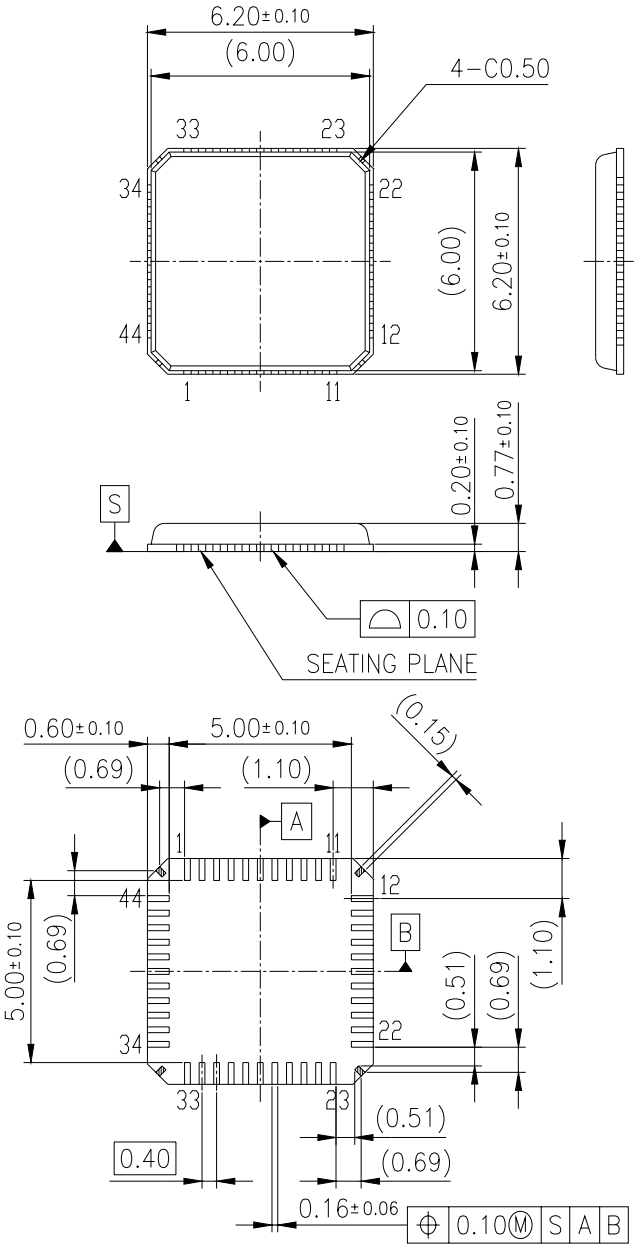
Established by	Applied by	Checked by	Prepared by
H.Shidooka	H.Yoshida	M.Okajima	M.Itoh

Established: 2009-06-01
Revised : 2009-06-17

1. Outline Drawing

Unit:mm

Package Code : ∗QFN044-P-0606D



Body Material	:	Br / Sb Free Epoxy Resin
Lead Material	:	Cu Alloy
Lead Finish Method	:	Pd Plating

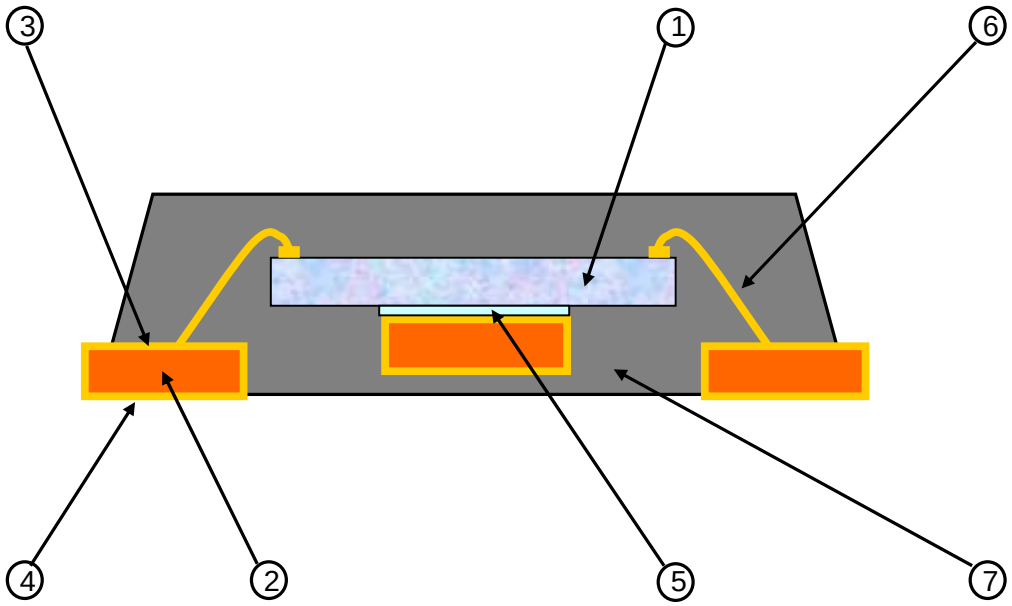
Established	Revised
-	-

Established: 2009-06-01
Revised : 2009-06-17

2. Package Structure (Technical Report : Reference Value)

Package Code : ∗QFN044-P-0606D

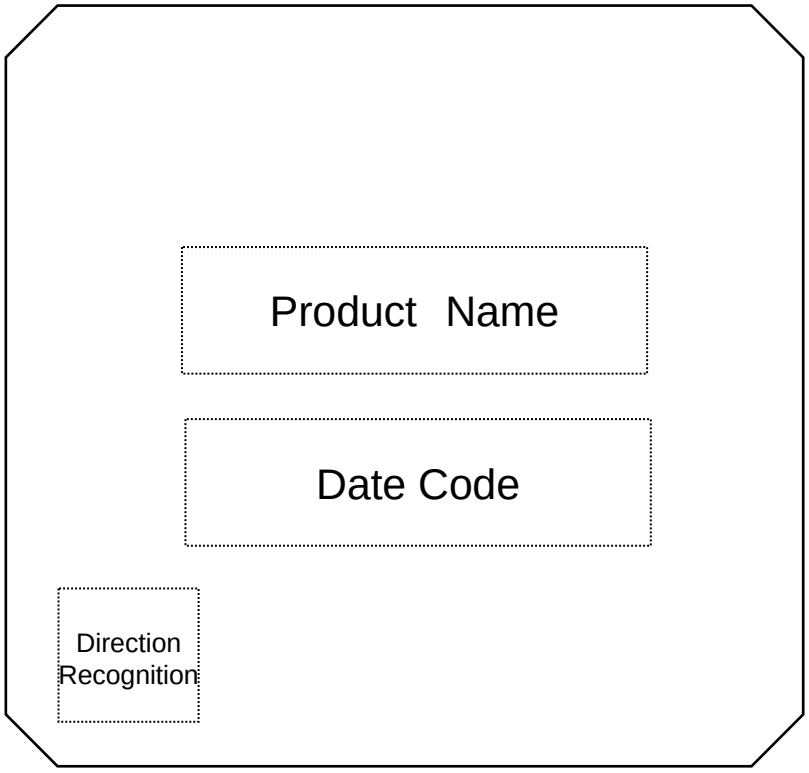
Chip Material		Si	①
Leadframe material		Cu alloy	②
Inner lead surface		Pd plating	③
Outer lead surface		Pd plating	④
Die attach	Method	Resin adhesive method	⑤
	Material	Adhesive material	
Wirebond	Method	Thermo-compression bonding	⑥
	Material	Au	
Molding	Method	Transfer molding	⑦
	Material	Br/Sb Free Epoxy resin	
Mass		67 mg	



Established: 2009-06-01
Revised : 2009-06-17

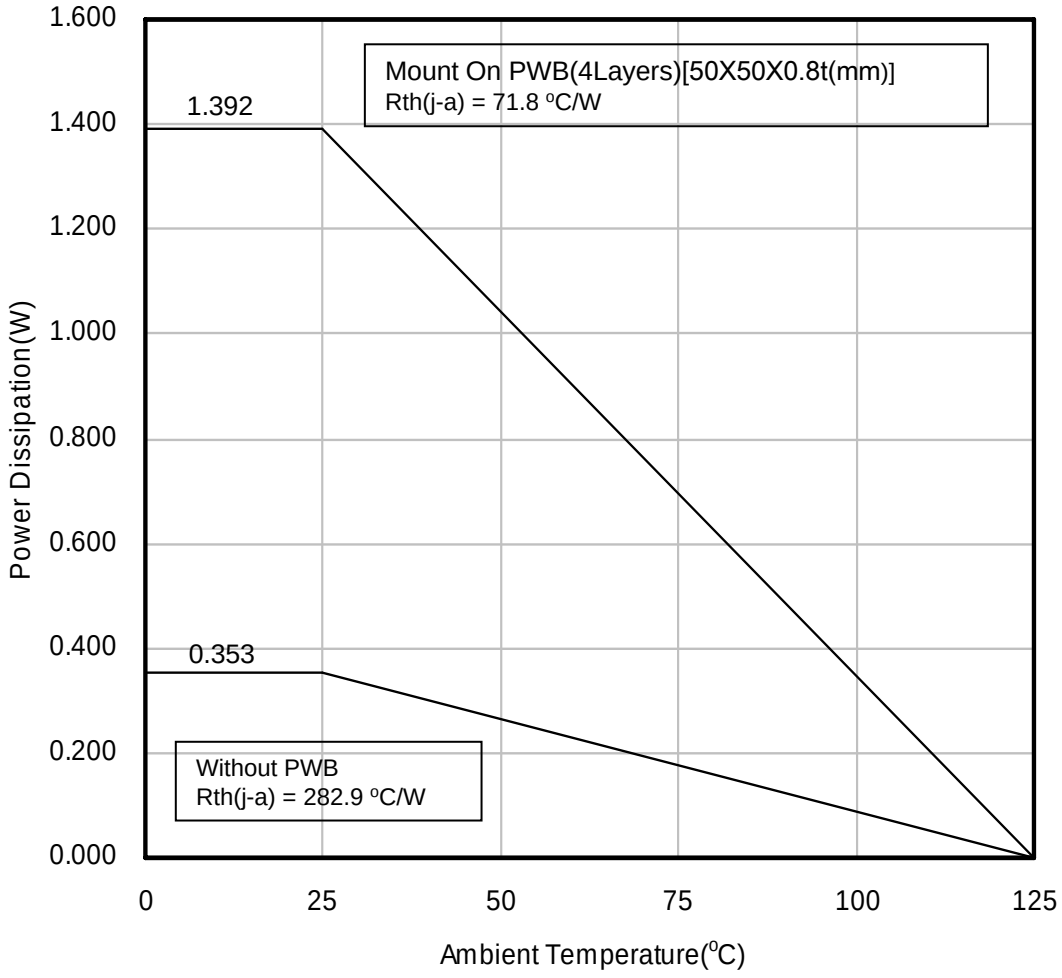
3. Mark Layout

Package Code : ∗QFN044-P-0606D



4. Power Dissipation (Technical Report)

Package Code : ∗QFN044-P-0606D



Established: 2009-06-01
Revised : 2009-06-17

5. Power Dissipation (Supplementary Explanation)

[Experiment environment]

Power Dissipation（Technical Report）is a result in the experiment environment of SEMI standard conformity. （Ambient air temperature (Ta) is 25 degrees C）

[Supplementary information of PWB to be used for measurement]

The supplement of PWB information for Power Dissipation data (Technical Report）are shown below.

Indication	Total Layer	Resin Material
Glass-Epoxy	1-layer	FR-4
4-layer	4-layer	FR-4

[Notes about Power Dissipation（Thermal Resistance）]

Power Dissipation values（Thermal Resistance）depend on the conditions of the surroundings, such as specification of PWB and a mounting condition , and a ambient temperature. (Power Dissipation (Thermal Resistance) is not a fixed value.)

The Power Dissipation value（Technical Report）is the experiment result in specific conditions (evaluation environment of SEMI standard conformity) ,and keep in mind that Power Dissipation values (Thermal resistance) depend on circumference conditions and also change.

[Definition of each temperature and thermal resistance]

Ta ：Ambient air temperature

※The temperature of the air is defined at the position where the convection, radiation, etc. don't affect the temperature value, and it's separated from the heating elements.

Tc ：It's the temperature near the center of a package surface. The package surface is defined at the opposite side if the PWB.

Tj ：Semiconductor element surface temperature (Junction temperature.)

Rth(j-c)：The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the package surface

Rth(c-a)：The thermal resistance (difference of temperature of per 1 Watts) between the package surface and the ambient air

Rth(j-a)：The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the ambient air

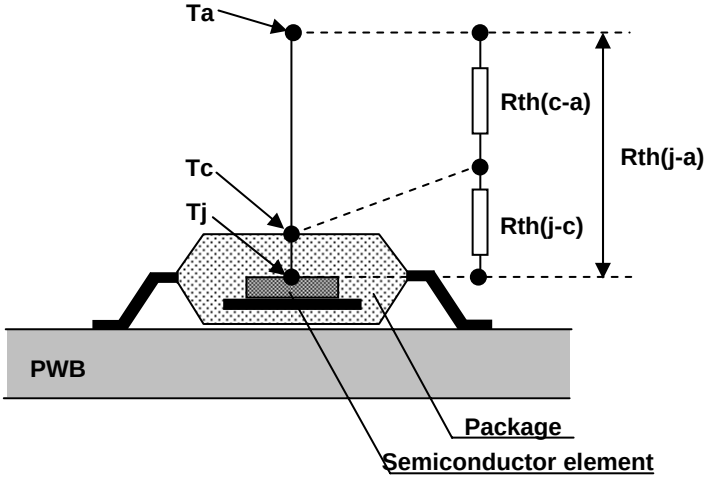


Fig1. Definition image

[Definition formula]

$$Tj=\{Rth(j\text{-}c)+Rth(c\text{-}a)\}\times P+Ta$$

$$=Rth(j\text{-}a)\times P+Ta$$

$$Rth(j\text{-}c)=\frac{Tj-Tc}{P}\ (℃/W)$$

$$Rth(c\text{-}a)=\frac{Tc-Ta}{P}\ (℃/W)$$

$$Rth(j\text{-}a)=\frac{Tj-Ta}{P}\ (℃/W)$$

$$=Rth(j\text{-}c)+Rth(c\text{-}a)$$

P:power(W)

Established: 2009-06-01
Revised : 2009-06-17

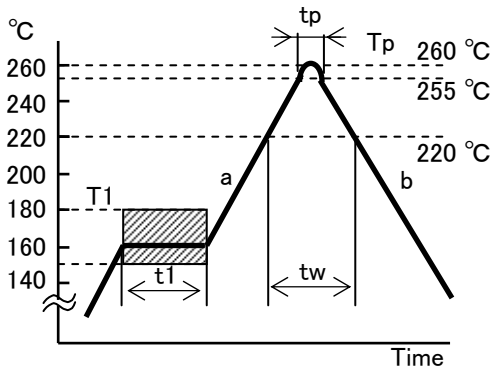
Product name : AN41919A-VB
Package : *QFN044-P-0606D

1. Recommended Soldering Conditions

In case that the semiconductor packages are mounted on the PCB, the soldering should be performed under the following conditions.

① Reflow soldering

Reflow peak temp. :	max. 260 ℃

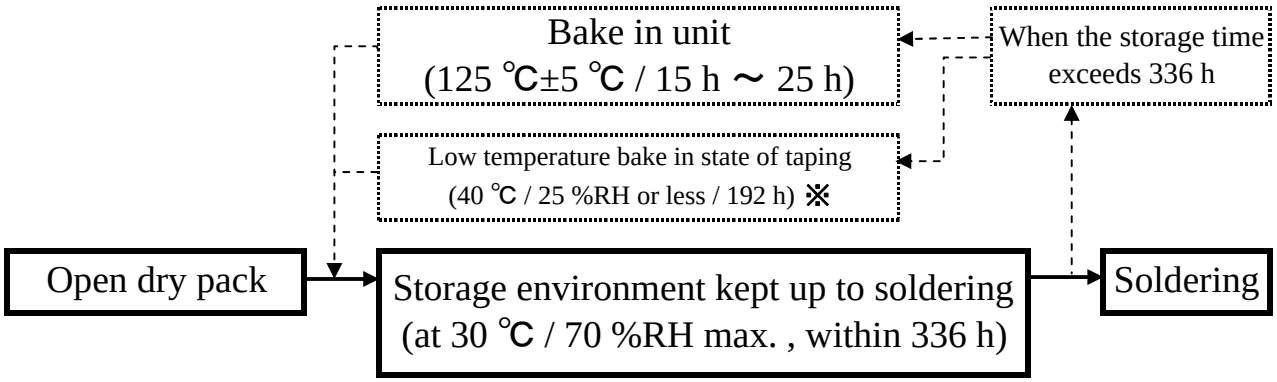


No.	mark	contents	value
1	T1	Pre-heating temp.	150 ℃～180 ℃
2	t1	Pre-heating temp. hold time	60 s～120 s
3	a	Rising rate	2 ℃/s～5 ℃/s
4	Tp	Peak temp.	255 ℃+5 ℃、-0 ℃
5	tp	Peak temp. hold time	10 s±3 s
6	tw	High temp. region hold time	within 60 s (≧220 ℃)
7	b	Down rate	2 ℃/s～5 ℃/s
8	-	Number of reflow	within 2 times

＊Peak temperature : less than 260 ℃

＊Temperature is measured at package surface point

2. Storage environment after dry pack opening



※ Because the taping and the magazine materials are not the heat-resistant materials, the bake at 125℃ cannot be done.
Therefore, please solder everything or control everything in the rule time.
Please keep them in an equal environment with the moisture-proof packaging or dry box.
(Temperature: room temperature, relative humidity: 30% or less.)
To control storage time, when bake in the taping and the magazine is necessary, it is necessary for each type to set a bake condition. Please inquire of our company.

☆ **AN41919A-VB limitation, low temperature bake condition : 40 ℃ / 25 %RH or less / 192 h**

3. Note

① Storage environment conditions: keep the following conditions Ta=5 ℃～30 ℃、RH=30 %～70 %.
② Storage period before opening dry pack shall be 1year from a shipping day under Ta=5 ℃～30 ℃、RH=30 %～70 %.
③ Baking cycle should be only one time. Please be cautious of solderability at baking.
④ Reflow soldering : max. two times. (1st reflow must be finished within 336 hours.)
⑤ Remove flux sufficiently from product in the washing process.
(Flux : Chlorineless rosin flux is recommended.)
⑥ In case that use ultrasonic for product washing,
There is the possibility that the resonance may occur due to the frequency and shape of PCB.
It may be affected to the strength of lead. Please be cautious of this matter.

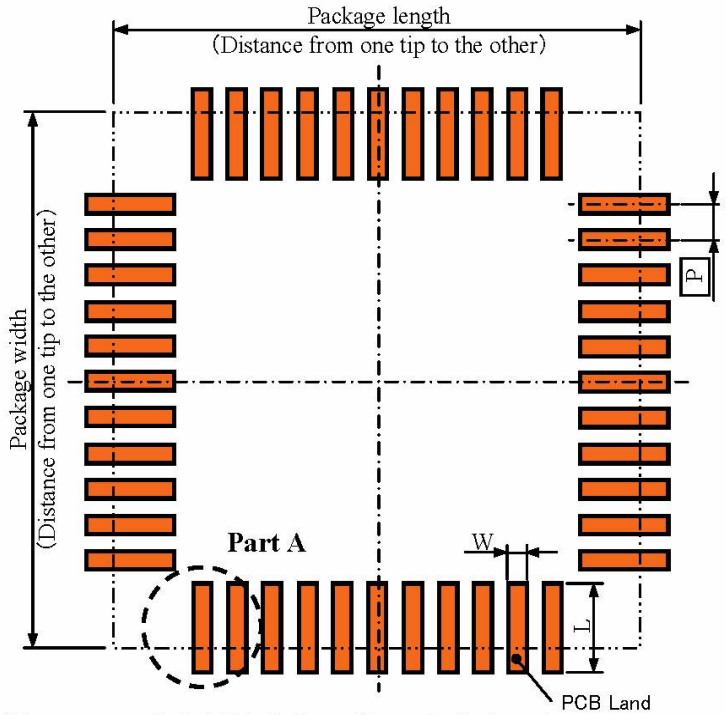
Referential PCB & Mask spec. for QFN

Application Specific Standard Products BU
Semiconductor Company
Panasonic Corporation

Reference

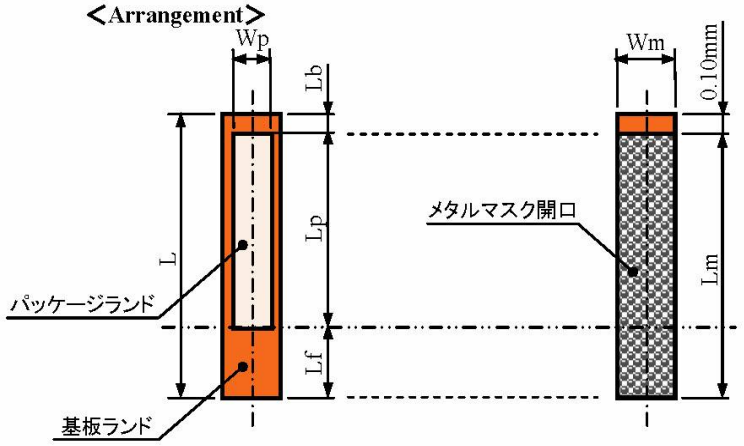
【Whole PCB land figure】

(Reference figure)Package Code：QFN044-P-0606（0.40mmP/44pin、6.2mm□）



【Expansion of part A】

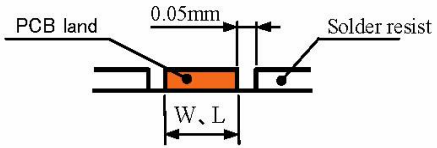
<Arrangement>



PCB land and package land

PCB land and mask opening

【Cross-sectional figure of PCB land】



Solder resist：Normal resist structure（NSMD）

（PCB land size＋0.10mm（One side＋0.05mm））

*Stencil mask thickness
：0.11～0.13mmt

■Recommended PCB & Stencil mask design size

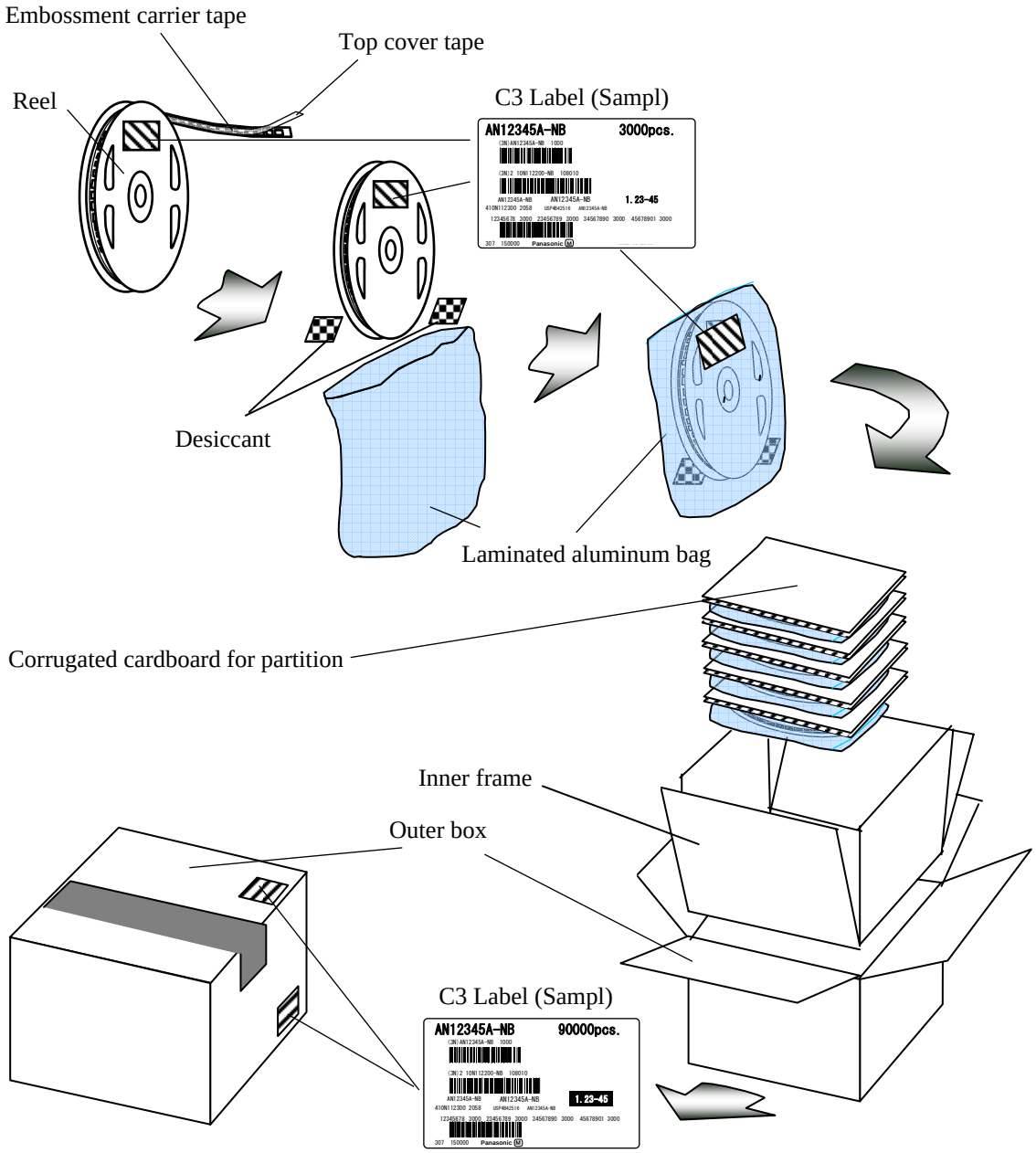
（Unit：mm）

Terminal pitch P	Package land		PCB Land				Metal Mask Opening	
	Width Wp	Length Lp	Width W	Length L	Front fillet Lf	Back fillet Lb	Width Wm	Length Lm
0.40mmP	0.16	0.60	0.20	1.00	0.30	0.10	0.20	0.90
0.50mmP	0.20	0.60	0.25	1.00	0.30	0.10	0.25	0.90

*The above size is calculated based on the experiment results by Panasonic Corporation and is not intended as a guarantee of mounting reliability. Mounting reliability can vary depending on factors such as the equipment specifications and conditions, material specifications and properties, and environmental conditions. To ensure satisfactory results, your company should evaluate and confirm actual mounting performance.

Specifications of packing by the embossment tape

(Specifications for dampproof packing of the reel without the inner carton)



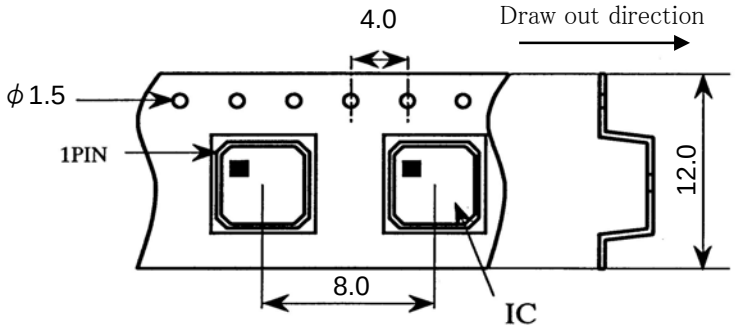
Package : *QFN044-P-0606D

Unit : mm

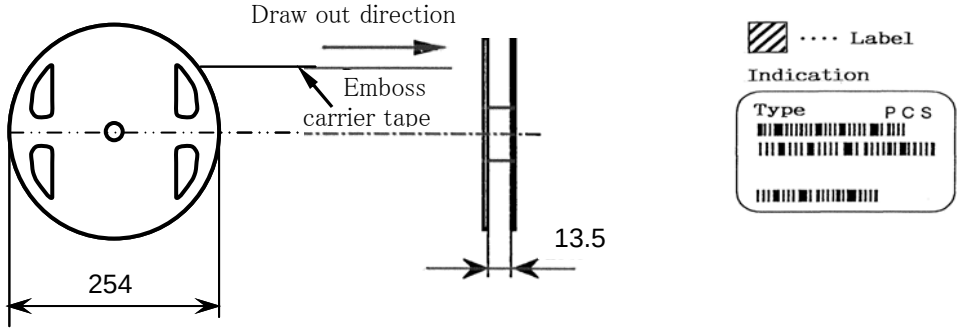
1 Packing

1) Tape

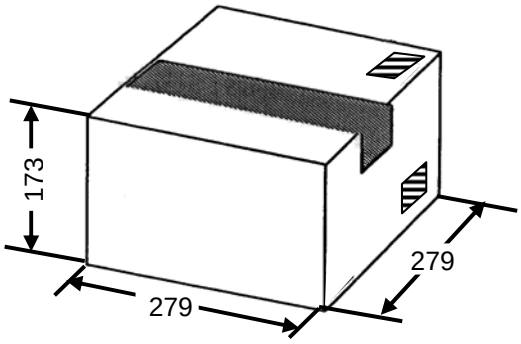
V B



2) Reel



3) Packing case

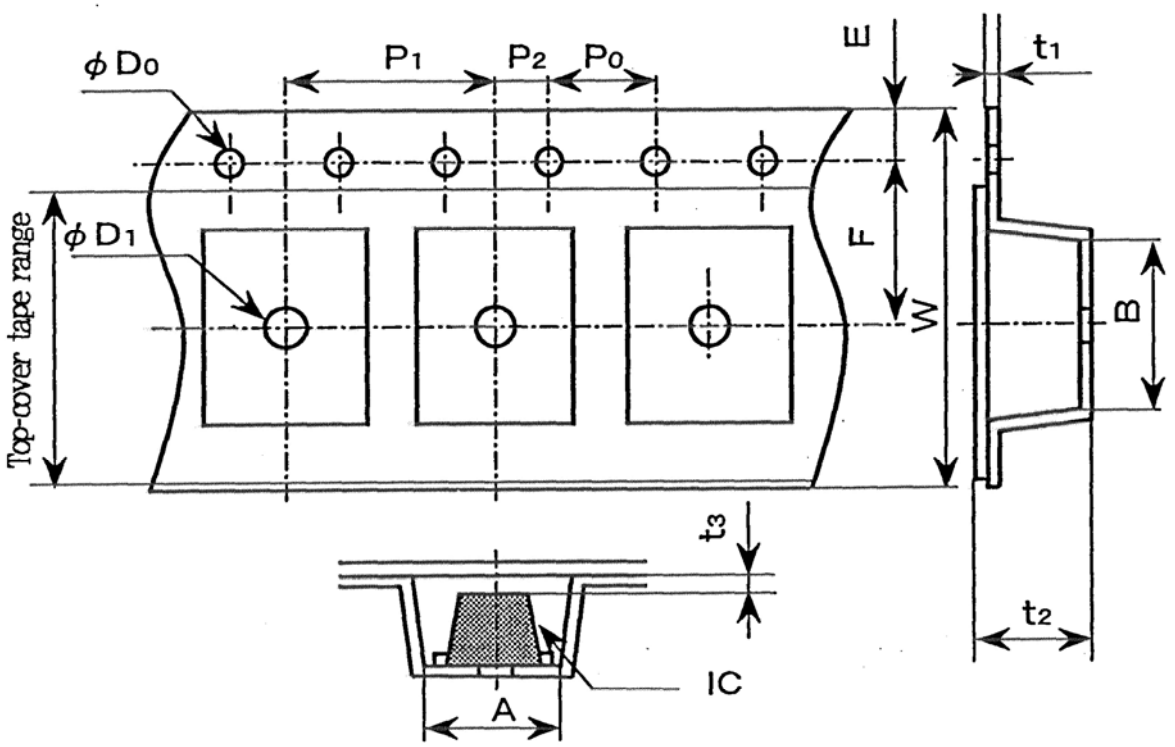


2 Packing quantity

Form	IC quantity	Contents
Reel	2000 Pcs	Reel × 1Pcs
Packing case	10000 Pcs	Reel × 5Pcs

Package : *QFN044-P-0606D

Unit : mm



Unit:mm

Dimension & Tolerance					
W	A	B	E	F	P_1
12.0±0.2	6.5±0.1	6.5±0.1	1.75±0.1	5.5±0.05	8.0±0.1
P_2	P_0	ϕD_1	ϕD_0	t_1	t_2
2.0±0.05	4.0±0.1	$1.5^{+0.3}_{-0}$	1.55±0.05	0.3±0.05	1.8max
t_3					
(0.4)					

Panasonic

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