

74AHC74-Q100; 74AHCT74-Q100

Dual D-type flip-flop with set and reset; positive-edge trigger

Rev. 3 — 22 April 2020

Product data sheet

1. General description

The 74AHC74-Q100; 74AHCT74-Q100 is a high-speed Si-gate CMOS device and is pin compatible with Low-Power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC74-Q100; 74AHCT74-Q100 is a dual positive-edge triggered, D-type flip-flop with individual data inputs (D), clock inputs (CP), set inputs (\overline{SD}) and reset inputs (\overline{RD}). It also has complementary outputs (Q and \overline{Q}).

The set and reset are asynchronous active LOW inputs that operate independent of the clock input. Information on the data input is transferred to the Q output on the LOW to HIGH transition of the clock pulse. The data inputs must be stable one set-up time prior to the LOW to HIGH clock transition for predictable operation.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than V_{CC}
- Input levels:
 - For 74AHC74-Q100: CMOS level
 - For 74AHCT74-Q100: TTL level
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|-----------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | |
| 74AHC74D-Q100 | -40 °C to +125 °C | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74AHCT74D-Q100 | | | | |
| 74AHC74PW-Q100 | -40 °C to +125 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |
| 74AHCT74PW-Q100 | | | | |
| 74AHC74BQ-Q100 | -40 °C to +125 °C | DHFQFN14 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm | SOT762-1 |
| 74AHCT74BQ-Q100 | | | | |

4. Functional diagram

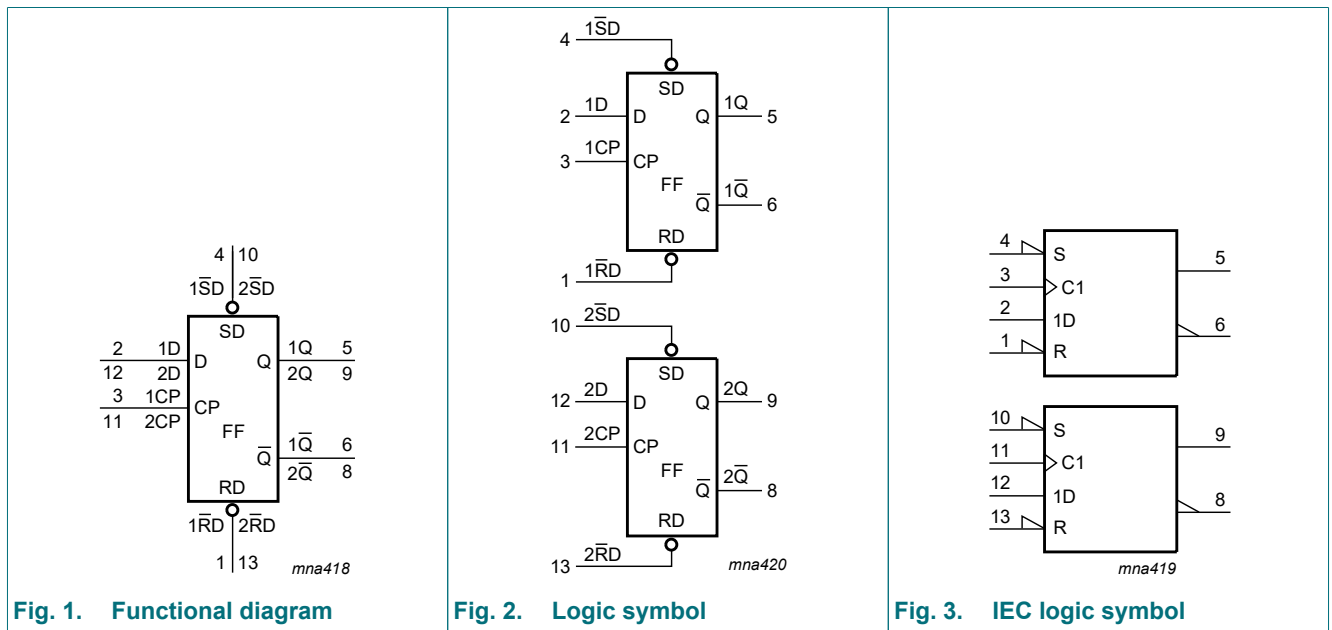


Fig. 1. Functional diagram

Fig. 2. Logic symbol

Fig. 3. IEC logic symbol

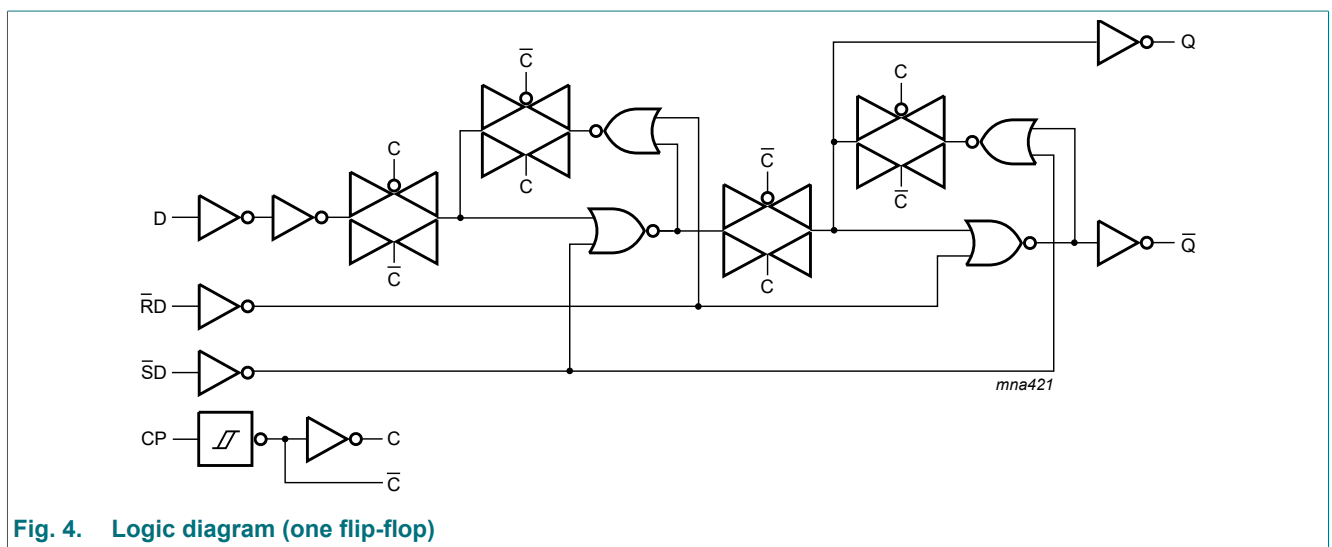
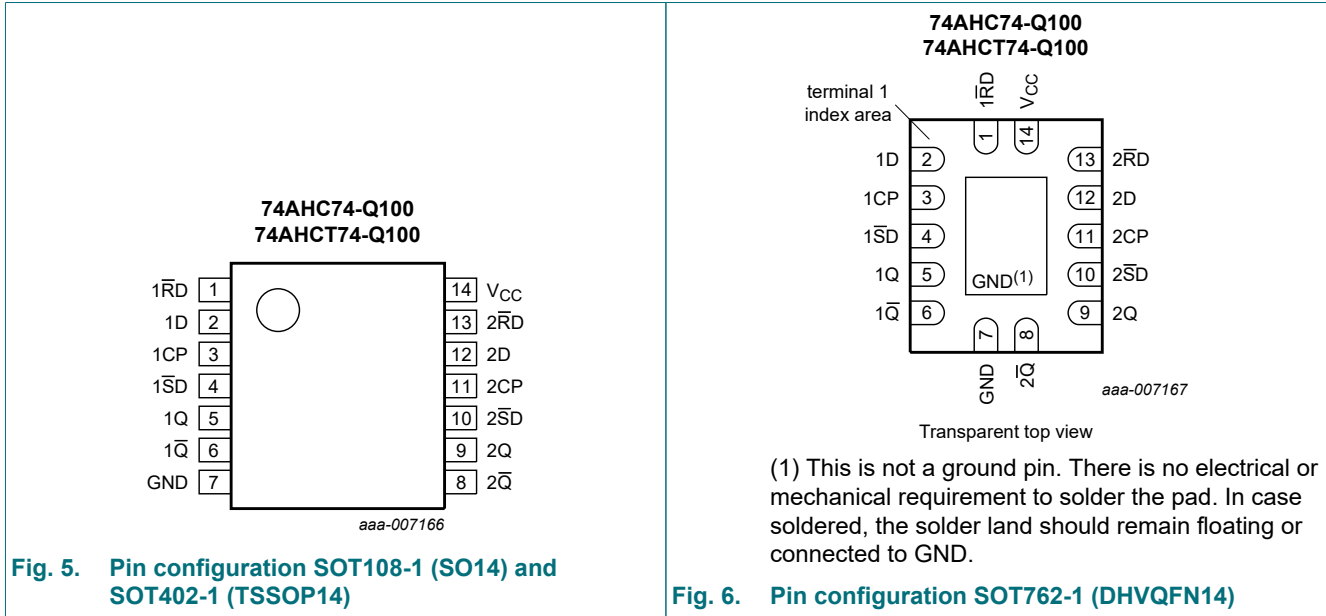


Fig. 4. Logic diagram (one flip-flop)

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-------------------|-----|--|
| 1 \overline{RD} | 1 | asynchronous reset direct input (active LOW) |
| 1D | 2 | data input |
| 1CP | 3 | clock input (LOW to HIGH, edge-triggered) |
| 1 \overline{SD} | 4 | asynchronous set direct input (active LOW) |
| 1Q | 5 | true flip-flop output |
| 1 \overline{Q} | 6 | complement flip-flop output |
| GND | 7 | ground (0 V) |
| 2 \overline{Q} | 8 | complement flip-flop output |
| 2Q | 9 | true flip-flop output |
| 2 \overline{SD} | 10 | asynchronous set direct input (active LOW) |
| 2CP | 11 | clock input (LOW to HIGH, edge-triggered) |
| 2D | 12 | data input |
| 2 \overline{RD} | 13 | asynchronous reset direct input (active LOW) |
| V _{CC} | 14 | supply voltage |

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care;

↑ = LOW to HIGH transition; Q_{n+1} = state after the next LOW to HIGH CP transition.

| Control | | | Input | Output | | | |
|---------|-----|-----|-------|--------|-----|-------------------|--------------------|
| nSD | nRD | nCP | nD | nQ | nQ̄ | nQ _{n+1} | nQ̄ _{n+1} |
| L | H | X | X | H | L | - | - |
| H | L | X | X | L | H | - | - |
| L | L | X | X | H | H | - | - |
| H | H | ↑ | L | - | - | L | H |
| H | H | ↑ | H | - | - | H | L |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|---|------|------|------|
| V _{CC} | supply voltage | | -0.5 | +7.0 | V |
| V _I | input voltage | | -0.5 | +7.0 | V |
| I _{IK} | input clamping current | V _I < -0.5 V [1] | -20 | - | mA |
| I _{OK} | output clamping current | V _O < -0.5 V or V _O > V _{CC} + 0.5 V [1] | -20 | +20 | mA |
| I _O | output current | V _O = -0.5 V to (V _{CC} + 0.5 V) | -25 | +25 | mA |
| I _{CC} | supply current | | - | +75 | mA |
| I _{GND} | ground current | | -75 | - | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| P _{tot} | total power dissipation | T _{amb} = -40 °C to +125 °C [2] | - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Operating conditions

| Symbol | Parameter | Conditions | 74AHC74-Q100 | | | 74AHCT74-Q100 | | | Unit |
|------------------|-------------------------------------|----------------------------------|--------------|-----|-----------------|---------------|-----|-----------------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V _{CC} | supply voltage | | 2.0 | 5.0 | 5.5 | 4.5 | 5.0 | 5.5 | V |
| V _I | input voltage | | 0 | - | 5.5 | 0 | - | 5.5 | V |
| V _O | output voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| T _{amb} | ambient temperature | | -40 | +25 | +125 | -40 | +25 | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 3.0 V to 3.6 V | - | - | 100 | - | - | - | ns/V |
| | | V _{CC} = 4.5 V to 5.5 V | - | - | 20 | - | - | 20 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|----------------------|---------------------------|--|-------|-----|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74AHC74-Q100 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | V _{CC} = 3.0 V | 2.1 | - | - | 2.1 | - | 2.1 | - | V |
| | | V _{CC} = 5.5 V | 3.85 | - | - | 3.85 | - | 3.85 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | V _{CC} = 3.0 V | - | - | 0.9 | - | 0.9 | - | 0.9 | V |
| | | V _{CC} = 5.5 V | - | - | 1.65 | - | 1.65 | - | 1.65 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = -50 μA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | I _O = -50 μA; V _{CC} = 3.0 V | 2.9 | 3.0 | - | 2.9 | - | 2.9 | - | V |
| | | I _O = -50 μA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -4.0 mA; V _{CC} = 3.0 V | 2.58 | - | - | 2.48 | - | 2.40 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 50 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 50 μA; V _{CC} = 3.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 50 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 3.0 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| I _I | input leakage current | V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | μA |
| | | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 2.0 | - | 20 | - | 40 | μA |
| C _I | input capacitance | V _I = V _{CC} or GND | - | 3 | 10 | - | 10 | - | 10 | pF |
| 74AHCT74-Q100 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | - | - | 2.0 | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = -50 μA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| V _{OL} | LOW-level output voltage | I _O = -8.0 mA | 3.94 | - | - | 3.80 | - | 3.70 | - | V |
| | | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| I _I | input leakage current | I _O = 50 μA | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 8.0 mA | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| I _I | input leakage current | V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 2.0 | - | 20 | - | 40 | μA |

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|---------------------------|--|-------|-----|------|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| ΔI_{CC} | additional supply current | per input pin; $V_I = V_{CC} - 2.1$ V; other pins at V_{CC} or GND; $I_O = 0$ A; $V_{CC} = 4.5$ V to 5.5 V | - | - | 1.35 | - | 1.5 | - | 1.5 | mA |
| C_I | input capacitance | $V_I = V_{CC}$ or GND | - | 3 | 10 | - | 10 | - | 10 | pF |

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit, see Fig. 9.

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|--|-------------------|--|-------|---------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ [1] | Max | Min | Max | Min | Max | |
| 74AHC74-Q100 | | | | | | | | | | |
| t_{pd} | propagation delay | nCP to nQ, n \bar{Q} ; see Fig. 7 [2] | | | | | | | | |
| | | $V_{CC} = 3.0$ V to 3.6 V; $C_L = 15$ pF | - | 5.2 | 11.9 | 1.0 | 14.0 | 1.0 | 15.0 | ns |
| | | $V_{CC} = 3.0$ V to 3.6 V; $C_L = 50$ pF | - | 7.4 | 15.4 | 1.0 | 17.5 | 1.0 | 19.5 | ns |
| | | $V_{CC} = 4.5$ V to 5.5 V; $C_L = 15$ pF | - | 3.7 | 7.3 | 1.0 | 8.5 | 1.0 | 9.5 | ns |
| | | $V_{CC} = 4.5$ V to 5.5 V; $C_L = 50$ pF | - | 5.2 | 9.3 | 1.0 | 10.5 | 1.0 | 12.0 | ns |
| | | n $\bar{S}D$, n $\bar{R}D$ to nQ, n \bar{Q} ; see Fig. 8 | | | | | | | | |
| | | $V_{CC} = 3.0$ V to 3.6 V; $C_L = 15$ pF | - | 5.4 | 12.3 | 1.0 | 14.5 | 1.0 | 15.5 | ns |
| | | $V_{CC} = 3.0$ V to 3.6 V; $C_L = 50$ pF | - | 7.7 | 15.8 | 1.0 | 18.0 | 1.0 | 20.0 | ns |
| | | $V_{CC} = 4.5$ V to 5.5 V; $C_L = 15$ pF | - | 3.7 | 7.7 | 1.0 | 9.0 | 1.0 | 10.0 | ns |
| $V_{CC} = 4.5$ V to 5.5 V; $C_L = 50$ pF | - | 5.3 | 9.7 | 1.0 | 11.0 | 1.0 | 12.5 | ns | | |
| f_{max} | maximum frequency | see Fig. 7 | | | | | | | | |
| | | $V_{CC} = 3.0$ V to 3.6 V; $C_L = 15$ pF | 80 | 125 | - | 70 | - | 70 | - | MHz |
| | | $V_{CC} = 3.0$ V to 3.6 V; $C_L = 50$ pF | 50 | 75 | - | 45 | - | 45 | - | MHz |
| | | $V_{CC} = 4.5$ V to 5.5 V; $C_L = 15$ pF | 130 | 170 | - | 110 | - | 110 | - | MHz |
| | | $V_{CC} = 4.5$ V to 5.5 V; $C_L = 50$ pF | 90 | 115 | - | 75 | - | 75 | - | MHz |
| t_W | pulse width | CP HIGH or LOW; n $\bar{S}D$, n $\bar{R}D$ LOW; see Fig. 7 and Fig. 8 | | | | | | | | |
| | | $V_{CC} = 3.0$ V to 3.6 V | 6.0 | - | - | 7.0 | - | 7.0 | - | ns |
| | | $V_{CC} = 4.5$ V to 5.5 V | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| t_{su} | set-up time | nD to nCP; see Fig. 7 | | | | | | | | |
| | | $V_{CC} = 3.0$ V to 3.6 V | 6.0 | - | - | 7.0 | - | 7.0 | - | ns |
| | | $V_{CC} = 4.5$ V to 5.5 V | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| t_h | hold time | nD to nCP; see Fig. 7 | | | | | | | | |
| | | $V_{CC} = 3.0$ V to 3.6 V | 0.5 | - | - | 0.5 | - | 0.5 | - | ns |
| | | $V_{CC} = 4.5$ V to 5.5 V | 0.5 | - | - | 0.5 | - | 0.5 | - | ns |

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|----------------------|-------------------------------|---|-------|---------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ [1] | Max | Min | Max | Min | Max | |
| t _{rec} | recovery time | nRD to nCP; see Fig. 8 | | | | | | | | |
| | | V _{CC} = 3.0 V to 3.6 V | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| | | V _{CC} = 4.5 V to 5.5 V | 3.0 | - | - | 3.0 | - | 3.0 | - | ns |
| C _{PD} | power dissipation capacitance | f _i = 1 MHz; V _I = GND to V _{CC} [3] | - | 12 | - | - | - | - | - | pF |
| 74AHCT74-Q100 | | | | | | | | | | |
| t _{pd} | propagation delay | nCP to nQ, nQ̄; see Fig. 7 [2] | | | | | | | | |
| | | V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF | - | 3.3 | 7.8 | 1.0 | 9.0 | 1.0 | 10.0 | ns |
| | | V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF | - | 4.8 | 8.8 | 1.0 | 10.0 | 1.0 | 11.0 | ns |
| | | nSD, nRD to nQ, nQ̄; see Fig. 8 | | | | | | | | |
| | | V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF | - | 3.7 | 10.4 | 1.0 | 12.0 | 1.0 | 13.0 | ns |
| | | V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF | - | 5.3 | 11.4 | 1.0 | 13.0 | 1.0 | 14.5 | ns |
| f _{max} | maximum frequency | see Fig. 7 | | | | | | | | |
| | | V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF | 100 | 160 | - | 80 | - | 80 | - | MHz |
| | | V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF | 80 | 140 | - | 65 | - | 65 | - | MHz |
| t _W | pulse width | CP HIGH or LOW; nSD, nRD LOW; V _{CC} = 4.5 V to 5.5 V; see Fig. 7 and Fig. 8 | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| t _{su} | set-up time | nD to nCP; V _{CC} = 4.5 V to 5.5 V; see Fig. 7 | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| t _h | hold time | nD to nCP; V _{CC} = 4.5 V to 5.5 V; see Fig. 7 | 0 | - | - | 0 | - | 0 | - | ns |
| t _{rec} | recovery time | nRD to nCP; V _{CC} = 4.5 V to 5.5 V; see Fig. 8 | 3.5 | - | - | 3.5 | - | 3.5 | - | ns |
| C _{PD} | power dissipation capacitance | f _i = 1 MHz; V _I = GND to V _{CC} [3] | - | 16 | - | - | - | - | - | pF |

[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

10.1. Waveforms

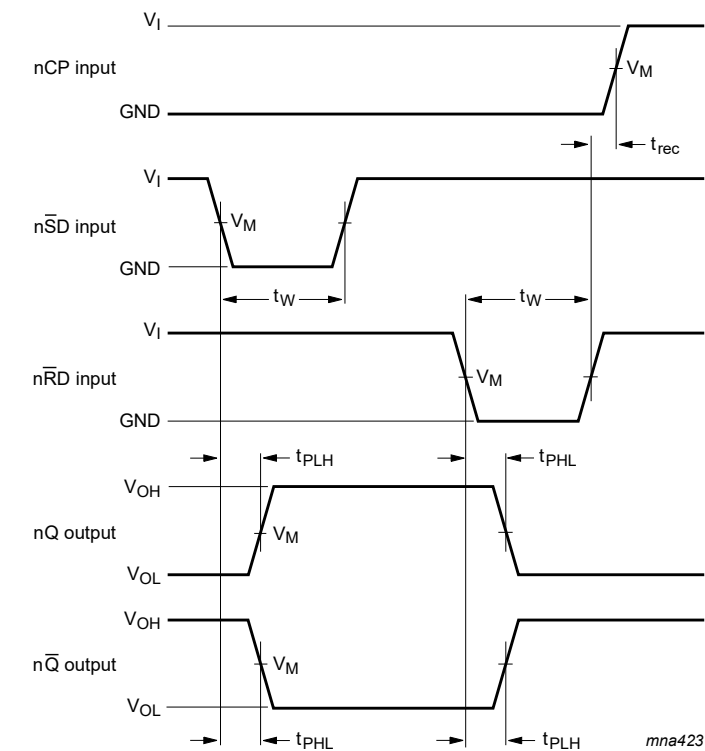


Measurement points are given in [Table 8](#).

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 7. Clock pulse width, maximum frequency, set-up times, hold times and input to output propagation delays



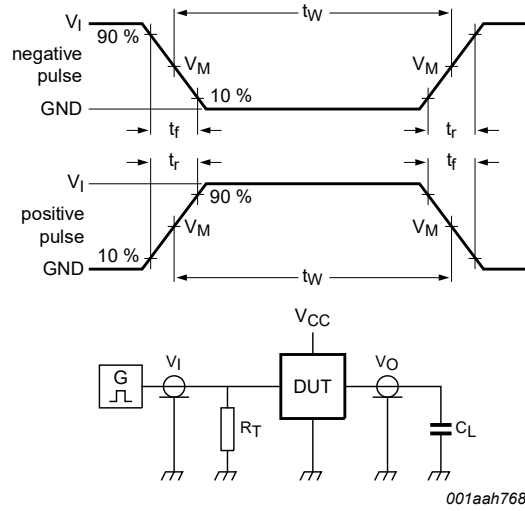
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 8. Set and reset pulse widths, recovery time and input to output propagation delays

Table 8. Measurement points

| Type | Input | Output |
|---------------|---------------------|---------------------|
| | V_M | V_M |
| 74AHC74-Q100 | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ |
| 74AHCT74-Q100 | 1.5 V | $0.5 \times V_{CC}$ |



001aah768

For test data, see [Table 9](#).

Definitions for test circuit:

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig. 9. Test circuit for measuring switching times

Table 9. Test data

| Type | Input | | Load | Test |
|---------------|----------|---------------|--------------|--------------------|
| | V_I | t_r, t_f | C_L | |
| 74AHC74-Q100 | V_{CC} | ≤ 3.0 ns | 50 pF, 15 pF | t_{PLH}, t_{PHL} |
| 74AHCT74-Q100 | 3.0 V | ≤ 3.0 ns | 50 pF, 15 pF | t_{PLH}, t_{PHL} |

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Fig. 10. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

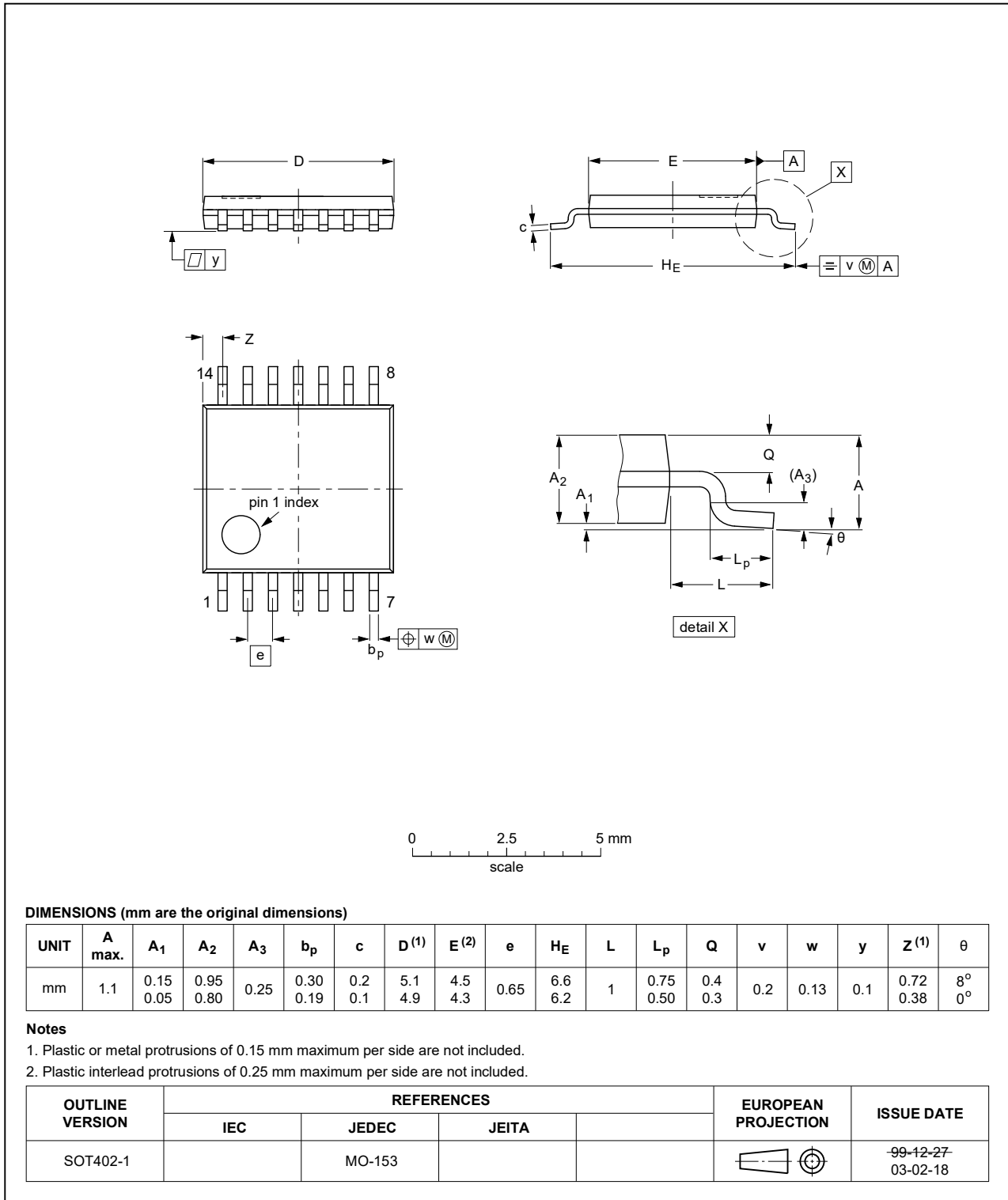


Fig. 11. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



Fig. 12. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|--|
| CMOS | Complementary Metal-Oxide Semiconductor |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| LSTTL | Low-power Schottky Transistor-Transistor Logic |
| MIL | Military |
| MM | Machine Model |

13. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------------|--|--------------------|---------------|-----------------------|
| 74AHC_AHCT74_Q100 v.3 | 20200422 | Product data sheet | - | 74AHC_AHCT74_Q100 v.2 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 2 updated. Table 4: Derating values for P_{tot} total power dissipation updated. Table 7: minimum f_{max} values at 3.0 V to 3.6 V for 74AHC74 corrected (errata). Fig. 12: Package outline drawing SOT762-1 (DHVQFN14) updated. | | | |
| 74AHC_AHCT74_Q100 v.2 | 20150421 | Product data sheet | - | 74AHC_AHCT74_Q100 v.1 |
| Modifications: | <ul style="list-style-type: none"> Table 3 corrected (errata). | | | |
| 74AHC_AHCT74_Q100 v.1 | 20130416 | Product data sheet | - | - |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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