ZL50020
Enhanced 2 K Digital Switch

Data Sheet

Features

November 2006

- 2048 channel x 2048 channel non-blocking digital Time Division Multiplex (TDM) switch at 8.192 Mbps and 16.384 Mbps or using a combination of ports running at 2.048, 4.096, 8.192 and 16.384 Mbps
- 32 serial TDM input, 32 serial TDM output streams
- Output streams can be configured as bi-directional for connection to backplanes
- Exceptional input clock cycle to cycle variation tolerance (20 ns for all rates)
- Per-stream input and output data rate conversion selection at 2.048, 4.096, 8.192 or 16.384 Mbps. Input and output data rates can differ
- Per-stream high impedance control outputs (STOHZ) for 16 output streams
- Per-stream input bit delay with flexible sampling point selection
- Per-stream output bit and fractional bit advancement

Ordering Information

ZL50020GAC	256 Ball PBGA	Trays
ZL50020QCC	256 Lead LQFP	Trays
ZL50020QCG1	256 Lead LQFP*	Trays, Bake & Drypack
ZL50020GAG2	256 Ball PBGA**	Trays, Bake & Drypack

*Pb Free Matte Tin
**Pb Free Tin/Silver/Copper

-40°C to +85°C

- Per-channel ITU-T G.711 PCM A-Law/μ-Law Translation
- Four frame pulse and four reference clock outputs
- Three programmable delayed frame pulse outputs
- Input clock: 4.096 MHz, 8.192 MHz, 16.384 MHz
- Input frame pulses:61 ns, 122 ns, 244 ns
- Per-channel constant or variable throughput delay for frame integrity and low latency applications
- Per Stream (32) Bit Error Rate Test circuits complying to ITU-O.151

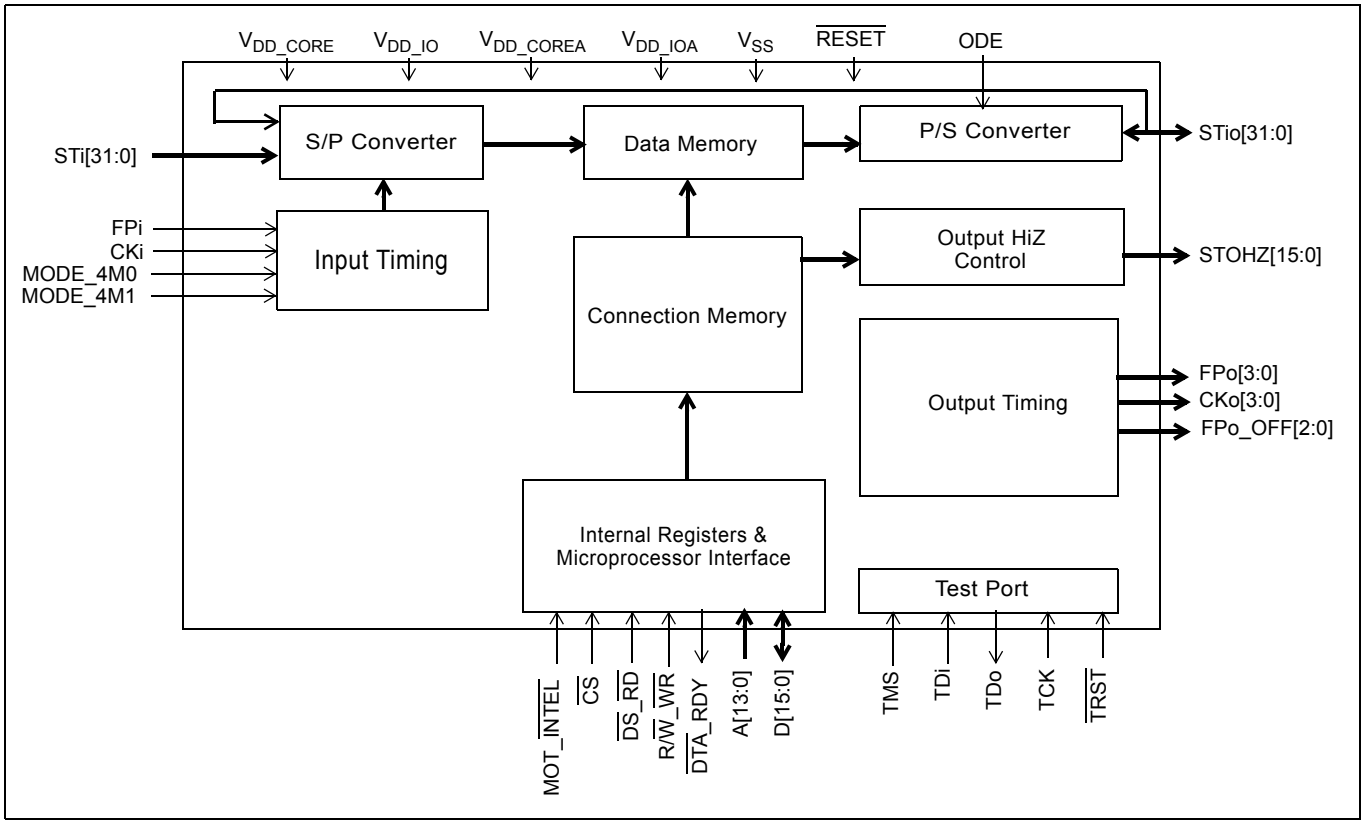

Figure 1 - ZL50020 Functional Block Diagram

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- Per-channel high impedance output control
- Per-channel message mode
- Control interface compatible with Intel and Motorola 16-bit non-multiplexed buses
- Connection memory block programming
- Supports ST-BUS and GCI-Bus standards for input and output timing
- IEEE-1149.1 (JTAG) test port
- 3.3 V I/O with 5 V tolerant inputs; 1.8 V core voltage

Applications

- PBX and IP-PBX
- Small and medium digital switching platforms
- Remote access servers and concentrators
- Wireless base stations and controllers
- Multi service access platforms
- Digital Loop Carriers
- Computer Telephony Integration

Description

The ZL50020 is a maximum 2048 x 2048 channel non-blocking digital Time Division Multiplex (TDM) switch. It has thirty-two input streams (STi0 - 31) and thirty-two output streams (STio0 - 31). The device can switch 64 kbps and Nx64 kbps TDM channels from any input stream to any output stream. Each of the input and output streams can be independently programmed to operate at any of the following data rates: 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps. The ZL50020 provides up to sixteen high impedance control outputs (STOHZ0 - 15) to support the use of external tristate drivers for the first sixteen output streams (STio0 - 15). The output streams can be configured to operate in bi-directional mode, in which case STi0 - 31 will be ignored.

The device contains two types of internal memory - data memory and connection memory. There are four modes of operation - Connection Mode, Message Mode, BER mode and high impedance mode. In Connection Mode, the contents of the connection memory define, for each output stream and channel, the source stream and channel (the actual data to be output is stored in the data memory). In Message Mode, the connection memory is used for the storage of microprocessor data. Using Zarlink's Message Mode capability, microprocessor data can be broadcast to the data output streams on a per-channel basis. This feature is useful for transferring control and status information for external circuits or other TDM devices. In BER mode the output channel data is replaced with a pseudorandom bit sequence (PRBS) from one of 32 PRBS generators that generates a 2^{15}-1 pattern. On the input side channels can be routed to one of 32 bit error detectors. In high impedance mode the selected output channel can be put into a high impedance state.

The configurable non-multiplexed microprocessor port allows users to program various device operating modes and switching configurations. Users can employ the microprocessor port to perform register read/write, connection memory read/write, and data memory read operations. The port is configurable to interface with either Motorola or Intel-type microprocessors.

The device also supports the mandatory requirements of the IEEE-1149.1 (JTAG) standard via the test port.

Table of Contents

Features 1
Applications 2
Description 2
Changes Summary 7
1.0 Pinout Diagrams 8
1.1 BGA Pinout 8
1.2 QFP Pinout 9
2.0 Pin Description 10
3.0 Device Overview 16
4.0 Data Rates and Timing 16
4.1 Input Clock (CKi) and Input Frame Pulse (FPi) Timing 17
5.0 ST-BUS and GCI-Bus Timing 19
6.0 Output Timing Generation 19
7.0 Data Input Delay and Data Output Advancement 22
7.1 Input Bit Delay Programming 23
7.2 Input Bit Sampling Point Programming 24
7.3 Output Advancement Programming 26
7.4 Fractional Output Bit Advancement Programming 27
7.5 External High Impedance Control Advancement 28
8.0 Data Delay Through the Switching Paths 28
8.1 Variable Delay Mode 28
8.2 Constant Delay Mode 29
9.0 Connection Memory Description 30
10.0 Connection Memory Block Programming 31
10.1 Memory Block Programming Procedure 31
11.0 Device Operation in Divided Clock and Multiplied Clock Modes 31
11.1 Divided Clock Mode Operation 32
11.2 Multiplied Clock Mode Operation 32
11.3 Output Clock Frequencies 32
12.0 Microprocessor Port 33
13.0 Device Reset and Initialization 33
13.1 Power-up Sequence 33
13.2 Device Initialization on Reset 33
13.3 Software Reset 34
14.0 Pseudo Random Bit Generation and Error Detection 34
15.0 PCM A-law/m-law Translation 35
16.0 Quadrant Frame Programming 35
17.0 JTAG Port 36
17.1 Test Access Port (TAP) 36
17.2 Instruction Register 37
17.3 Test Data Registers 37
17.4 BSDL 37
18.0 Register Address Mapping 38
19.0 Detailed Register Description 39
20.0 Memory 57
20.1 Memory Address Mappings 57
20.2 Connection Memory Low (CM_L) Bit Assignment 57
20.3 Connection Memory High (CM_H) Bit Assignment 59
21.0 DC Parameters 61

Table of Contents

22.0 AC Parameters 62

List of Figures

Figure 1 - ZL50020 Functional Block Diagram . . . 1
Figure 2 - ZL50020 256-Ball 17 mm x 17 mm PBGA (as viewed through top of package) . . . 8
Figure 3 - ZL50020 256-Lead 28 mm x 28 mm LQFP (top view). . . . 9
Figure 4 - Input Timing when CKIN1 - 0 bits = “10” in the CR . . . 18
Figure 5 - Input Timing when CKIN1 - 0 bits = “01” in the CR . . . 18
Figure 6 - Input Timing when CKIN1 - 0 = “00” in the CR . . . 19
Figure 7 - Output Timing for CKo0 and FPo0 . . . 20
Figure 8 - Output Timing for CKo1 and FPo1 . . . 21
Figure 9 - Output Timing for CKo2 and FPo2 . . . 21
Figure 10 - Output Timing for CKo3 and FPo3 with CKoFPo3SEL1-0=”11” . . . 22
Figure 11 - Input Bit Delay Timing Diagram (ST-BUS). . . . 23
Figure 12 - Input Bit Sampling Point Programming . . . 24
Figure 13 - Input Bit Delay and Factional Sampling Point . . . 25
Figure 14 - Output Bit Advancement Timing Diagram (ST-BUS). . . . 26
Figure 15 - Output Fractional Bit Advancement Timing Diagram (ST-BUS) . . . 27
Figure 16 - Channel Switching External High Impedance Control Timing . . . 28
Figure 17 - Data Throughput Delay for Variable Delay . . . 29
Figure 18 - Data Throughput Delay for Constant Delay. . . . 30
Figure 19 - Timing Parameter Measurement Voltage Levels. . . . 62
Figure 20 - Motorola Non-Multiplexed Bus Timing - Read Access . . . 63
Figure 21 - Motorola Non-Multiplexed Bus Timing - Write Access. . . . 64
Figure 22 - Intel Non-Multiplexed Bus Timing - Read Access . . . 65
Figure 23 - Intel Non-Multiplexed Bus Timing - Write Access . . . 66
Figure 24 - JTAG Test Port Timing Diagram . . . 67
Figure 25 - Frame Pulse Input and Clock Input Timing Diagram (ST-BUS). . . . 69
Figure 26 - Frame Pulse Input and Clock Input Timing Diagram (GCI-Bus) . . . 69
Figure 27 - ST-BUS Input Timing Diagram when Operated at 2, 4, 8 Mbps . . . 70
Figure 28 - ST-BUS Input Timing Diagram when Operated at 16 Mbps . . . 71
Figure 29 - GCI-Bus Input Timing Diagram when Operated at 2, 4, 8 Mbps . . . 71
Figure 30 - GCI-Bus Input Timing Diagram when Operated at 16 Mbps . . . 72
Figure 31 - ST-BUS Output Timing Diagram when Operated at 2, 4, 8 or 16 Mbps . . . 73
Figure 32 - GCI-Bus Output Timing Diagram when Operated at 2, 4, 8 or 16 Mbps . . . 73
Figure 33 - Serial Output and External Control . . . 74
Figure 34 - Output Drive Enable (ODE). . . . 74
Figure 35 - Input and Output Frame Boundary Offset . . . 75
Figure 36 - FPo0 and CKo0 Timing Diagram. . . . 76
Figure 37 - FPo1 and CKo1 Timing Diagram. . . . 77
Figure 38 - FPo2 and CKo2 Timing Diagram. . . . 78
Figure 39 - FPo3 and CKo3 Timing Diagram. . . . 79
Figure 40 - Output Timing (ST-BUS Format) . . . 80

List of Tables

Table 1 - CKi and FPi Configurations for Divided Clock Modes . . . 17
Table 2 - CKi and FPi Configurations for Multiplied Clock Mode . . . 17
Table 3 - Output Timing Generation . . . 19
Table 4 - Delay for Variable Delay Mode . . . 29
Table 5 - Connection Memory Low After Block Programming . . . 31
Table 6 - Connection Memory High After Block Programming . . . 31
Table 7 - ZL50020 Operating Modes . . . 32
Table 8 - Generated Output Frequencies . . . 32
Table 9 - Input and Output Voice and Data Coding . . . 35
Table 10 - Definition of the Four Quadrant Frames . . . 35
Table 11 - Quadrant Frame Bit Replacement . . . 36
Table 12 - Address Map for Registers (A13 = 0) . . . 38
Table 13 - Control Register (CR) Bits . . . 39
Table 14 - Internal Mode Selection Register (IMS) Bits . . . 41
Table 15 - Software Reset Register (SRR) Bits . . . 43
Table 16 - Output Clock and Frame Pulse Control Register (OCFCR) Bits . . . 44
Table 17 - Output Clock and Frame Pulse Selection Register (OCFSR) Bits . . . 45
Table 18 - FPo_OFF[n] Register (FPo_OFF[n]) Bits . . . 47
Table 19 - Internal Flag Register (IFR) Bits - Read Only . . . 48
Table 20 - BER Error Flag Register 0 (BERFR0) BIts - Read Only . . . 48
Table 21 - BER Error Flag Register 1 (BERFR1) Bits - Read Only . . . 49
Table 22 - BER Receiver Lock Register 0 (BERLR0) Bits - Read Only . . . 49
Table 23 - BER Receiver Lock Register 1 (BERLR1) Bits - Read Only . . . 50
Table 24 - Stream Input Control Register 0 - 31 (SICR0 - 31) Bits . . . 50
Table 25 - Stream Input Quadrant Frame Register 0 - 31 (SIQFR0 - 31) Bits . . . 52
Table 26 - Stream Output Control Register 0 - 31 (SOCR0 - 31) Bits . . . 54
Table 27 - BER Receiver Start Register [n] (BRSR[n]) Bits . . . 55
Table 28 - BER Receiver Length Register [n] (BRLR[n]) Bits . . . 55
Table 29 - BER Receiver Control Register [n] (BRCR[n]) Bits . . . 56
Table 30 - BER Receiver Error Register [n] (BRER[n]) Bits - Read Only . . . 56
Table 31 - Address Map for Memory Locations (A13 = 1) . . . 57
Table 32 - Connection Memory Low (CM_L) Bit Assignment when CMM = 0 . . . 57
Table 33 - Connection Memory Low (CM_L) Bit Assignment when CMM = 1 . . . 58
Table 34 - Connection Memory High (CM_H) Bit Assignment . . . 59

Changes Summary

The following table captures the changes from January 2006 to November 2006.

Page	Item	Change
1		Updated Ordering Information.

The following table captures the changes from the October 2004 issue.

Page	Item	Change
13	Pin Description “CKi” on page 13	• Clarified pin description for CKi.
32	11.3, “Output Clock Frequencies“	• Added new section to describe output clock frequencies.

1.0 Pinout Diagrams

1.1 BGA Pinout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	V_{SS}	STi29	STi28	STi27	STi25	STi26	STi24	NC	NC	STio22	STio23	STio21	STio20	NC	NC	V_{SS}	A
B	STi31	STi10	STi5	STi4	CKo2	STi0	CKo0	NC	V_{DD_COREA}	FPi	CKi	IC_Open	IC_Open	IC_GND	ODE	STio19	B
C	STi30	STi9	V_{SS}	STi7	STi6	STi1	CKo1	NC	V_{SS}	IC_Open	IC_Open	IC_Open	IC_GND	V_{SS}	STio15	STio18	C
D	STi17	STi11	V_{DD_IO}	STi3	STi2	NC	NC	NC	NC	V_{SS}	FPo_OFF1	IC_GND	STio13	V_{DD_IO}	STio14	STio16	D
E	STi16	STi14	STi8	V_{DD_IO}	V_{SS}	V_{DD_CORE}	NC	NC	NC	NC	V_{DD_CORE}	V_{SS}	V_{DD_IO}	STio12	FPo2	STio17	E
F	STi19	STi15	STi12	STi13	V_{DD_IO}	V_{DD_CORE}	V_{DD_CORE}	V_{SS}	V_{SS}	V_{DD_CORE}	V_{DD_CORE}	V_{DD_IO}	IC	FPo3	FPo_OFF2	STOHZ15	F
G	STi18	$\overline{RESET}$	IC_GND	IC_Open	TDo	V_{DD_IO}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_IO}	A12	A13	FPo1	FPo0	STOHZ14	G
H	STi21	V_{SS}	V_{SS}	V_{DD_COREA}	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	A7	A9	A10	FPo_OFF0	A11	STOHZ12	H
J	STi20	V_{DD_IOA}	V_{DD_IOA}	V_{SS}	V_{SS}	CKo3	V_{SS}	V_{SS}	V_{SS}	V_{SS}	A3	A4	A5	A8	A6	STOHZ13	J
K	STi22	V_{SS}	TMS	V_{SS}	V_{DD_COREA}	V_{DD_IO}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_IO}	IC_Open	A0	A2	A1	STOHZ11	K
L	STi23	V_{DD_COREA}	$\overline{TRST}$	TCK	V_{DD_IO}	V_{DD_CORE}	V_{DD_CORE}	V_{SS}	V_{SS}	V_{DD_CORE}	V_{DD_CORE}	V_{DD_IO}	STio10	STio11	STio9	STOHZ10	L
M	STio25	NC	TDi	D0	V_{SS}	V_{DD_CORE}	V_{DD_CORE}	D6	D10	V_{DD_CORE}	V_{DD_CORE}	V_{SS}	MOT_INTEL	MODE_4M0	STio8	STOHZ9	M
N	STio24	NC	V_{DD_IO}	STio0	STOHZ3	D1	D5	D7	D11	D13	R/$\overline{W}$_$\overline{WR}$	$\overline{DTA}$_RDY	STio4	V_{DD_IO}	STOHZ5	STOHZ8	N
P	STio26	NC	V_{SS}	STio1	STio3	STOHZ1	D3	D8	D14	NC	STio5	STOHZ4	STOHZ6	V_{SS}	STOHZ7	NC	P
R	STio27	NC	STOHZ0	STio2	STOHZ2	D2	D4	D9	D12	D15	$\overline{CS}$	$\overline{DS}$_$\overline{RD}$	MODE_4M1	STio6	STio7	NC	R
T	V_{SS}	STio28	STio29	STio31	STio30	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	V_{SS}	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Note: A1 corner identified by metallized marking.
Note: Pinout is shown as viewed through top of package.

Figure 2 - ZL50020 256-Ball 17 mm x 17 mm PBGA (as viewed through top of package)

1.2 QFP Pinout

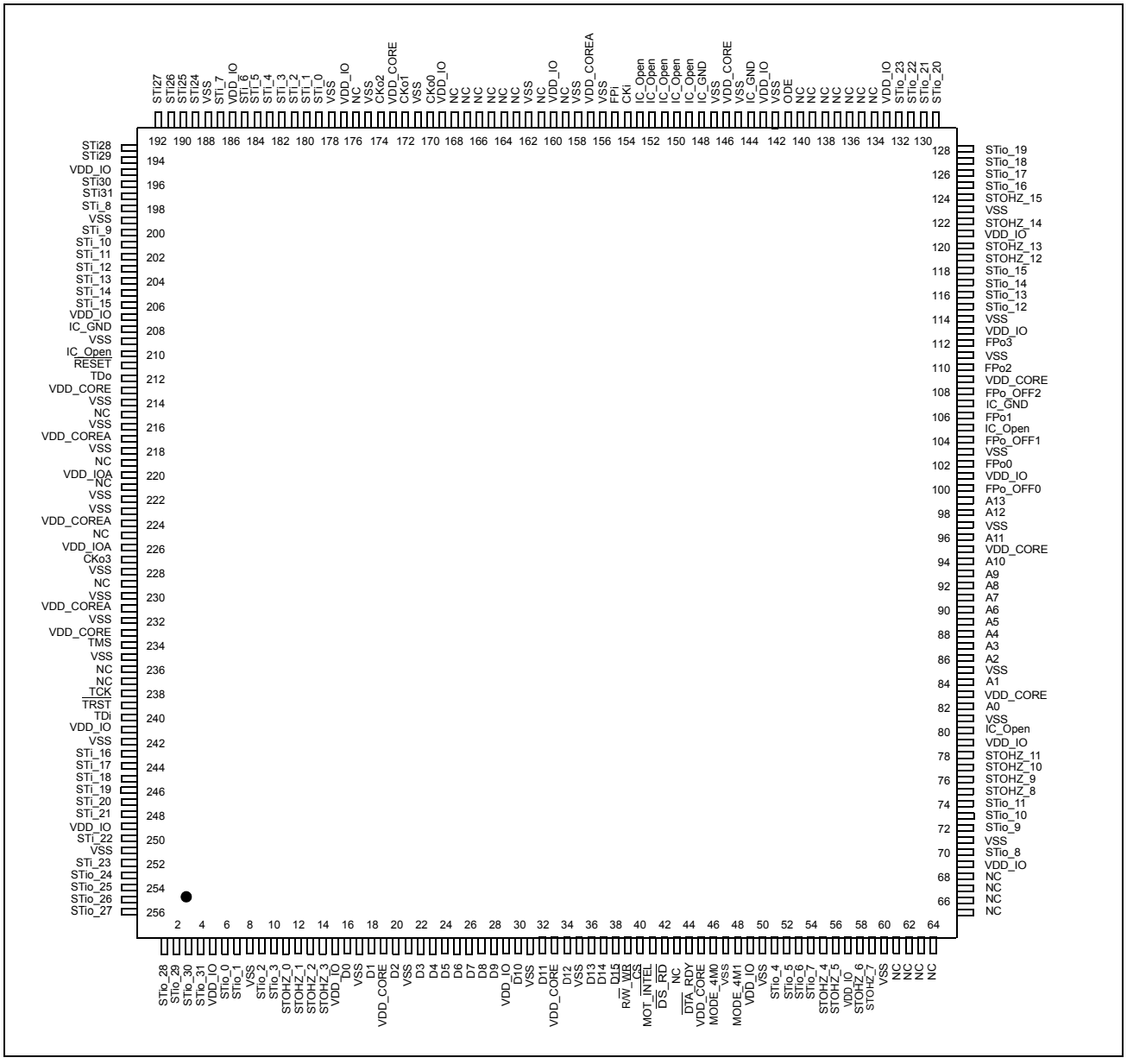


Figure 3 - ZL50020 256-Lead 28 mm x 28 mm LQFP (top view)

2.0 Pin Description

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
E6, E11, F6, F7, F10, F11, L6, L7, L10, L11, M6, M7, M10, M11	19, 33, 45, 83, 95, 109, 146, 173, 213, 233	V_{DD_CORE}	**Power Supply for the core logic:** +1.8 V
H4, K5, B9, L2	217, 231, 157, 224	V_{DD_COREA}	**Power Supply for analog circuitry:** +1.8 V
D3, D14, E4, E13, F5, F12, G6, G11, K6, K11, L5, L12, N3, N14	5, 15, 29, 49, 57, 69, 79, 101, 113, 121, 133, 143, 160, 169, 177, 186, 195, 207, 241, 249	V_{DD_IO}	**Power Supply for I/O:** +3.3 V
J2, J3	220, 226	V_{DD_IOA}	**Power Supply for the CKo5 and CKo3 outputs:** +3.3 V
A1, A16, C3, C9, C14, D10, E5, E12, F8, F9, G7, G8, G9, G10, H2, H3, H6, H7, H8, H9, H10, J4, J5, J7, J8, J9, J10, K2, K4, K7, K8, K9, K10, L8, L9, M5, M12, P3, P14, T1, T16	8, 17, 21, 31, 35, 47, 50, 60, 71, 81, 85, 97, 103, 111, 114, 123, 142, 145, 147, 156, 158, 162, 171, 175, 178, 188, 199, 209, 214, 216, 218, 222, 223, 228, 230, 232, 235, 242, 251	V_{SS}	**Ground**

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
K3	234	TMS	**Test Mode Select (5 V-Tolerant Input with Internal Pull-up)** JTAG signal that controls the state transitions of the TAP controller. This pin is pulled high by an internal pull-up resistor when it is not driven.
L4	238	TCK	**Test Clock (5 V-Tolerant Schmitt-Triggered Input with Internal Pull-up)** Provides the clock to the JTAG test logic.
L3	239	$\overline{\text{TRST}}$	**Test Reset (5 V-Tolerant Input with Internal Pull-up)** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low during power-up to ensure that the device is in the normal functional mode. When JTAG is not being used, this pin should be pulled low during normal operation.
M3	240	TDi	**Test Serial Data In (5 V-Tolerant Input with Internal Pull-up)** JTAG serial test instructions and data are shifted in on this pin. This pin is pulled high by an internal pull-up resistor when it is not driven.
G5	212	TDo	**Test Serial Data Out (5 V-Tolerant Three-state Output)** JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high impedance state when JTAG is not enabled.
B12, B13, C10, C11, F13, G4, K12, C12,	80, 105, 150, 151, 152, 153, 210, 149	IC_Open	**Internal Test Mode (5 V-Tolerant Input with Internal Pull-down)** These pins may be left unconnected.
G3, D12, B14, C13	144, 107, 148, 208	IC_GND	**Internal Test Mode Enable (5 V-Tolerant Input)** These pins **MUST** be low.

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
A8, A9, A14, A15, E10, M2, N2, P2, P16, R2, R16, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, D9, E8, C8, E7, D6, H5, P10, E9, D8, B8, D7	61, 62, 63, 64, 65, 66, 67, 68, 134, 135, 136, 137, 138, 139, 140, 152, 215, 219, 225, 229, 236, 237159, 163, 165, 167, 176, 221, 43, 161, 164, 166, 168	NC	**No Connect** These pins **MUST** be left unconnected.
M14, R13	46, 48	MODE_4M0, MODE_4M1	**4M Input Clock Mode 0 to 1 (5 V-Tolerant Input with internal pull-down)** These two pins should be tied together and are typically used to select CKi = 4.096 MHz operation. See Table 7, “ZL50020 Operating Modes” on page 32 for a detailed explanation. See Table 13, “Control Register (CR) Bits” on page 39 for CKi and FPi selection using the CKIN1 - 0 bits.
G15, G14, E15, F14	102, 106, 110, 112	FPo0 - 3	**ST-BUS/GCI-Bus Frame Pulse Outputs 0 to 3 (5 V-Tolerant Three-state Outputs)** FPo0: 8 kHz frame pulse corresponding to the 4.096 MHz output clock of CKo0. FPo1: 8 kHz frame pulse corresponding to the 8.192 MHz output clock of CKo1. FPo2: 8 kHz frame pulse corresponding to 16.384 MHz output clock of CKo2. FPo3: Programmable 8 kHz frame pulse corresponding to 4.096 MHz, 8.192 MHz, 16.384 MHz, or 32.768 MHz output clock of CKo3.
H14, D11, F15	100, 104, 108	FPo_OFF0 - 2	**Generated Offset Frame Pulse Outputs 0 to 2 (5 V-Tolerant Three-state Outputs)** Individually programmable 8 kHz frame pulses, offset from the output frame boundary by a programmable number of channels.
B7, C7, B5, J6	170, 172, 174, 227	CKo0 - 3	**ST-BUS/GCI-Bus Clock Outputs 0 to 3 (5 V-Tolerant Three-state Outputs)** CKo0: 4.096 MHz output clock. CKo1: 8.192 MHz output clock. CKo2: 16.384 MHz output clock. CKo3: 4.096 MHz, 8.192 MHz or 16.384 MHz programmable output clock. 32.768 MHz if in multiplied clock mode.

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
B10	155	FPi	**ST-BUS/GCI-Bus Frame Pulse Input (5 V-Tolerant Schmitt-Triggered Input)** This pin accepts the frame pulse which stays active for 61 ns, 122 ns or 244 ns at the frame boundary. The frame pulse frequency is 8 kHz. The frame pulse associated with the CKi must be applied to this pin. If the data rate is 16.384 Mbps, a 61 ns wide frame pulse must be used. By default, the device accepts a negative frame pulse in ST-BUS format, but it can accept a positive frame pulse instead if the FPINP bit is set high in the Control Register (CR). It can accept a GCI-formatted frame pulse by programming the FPINPOS bit in the Control Register (CR) to high.
B11	154	CKi	**ST-BUS/GCI-Bus Clock Input (5 V-Tolerant Schmitt-Triggered Input)** This pin accepts a 4.096 MHz, 8.192 MHz or 16.384 MHz clock. In divided clock mode the clock frequency applied to this pin must be **twice the highest input or output** data rate. In multiplied clock mode the clock frequency applied to this pin must be **twice the highest input** data rate. The exception is, when data is running at 16.384 Mbps, a 16.384 MHz clock must be used. By default, the clock falling edge defines the input frame boundary, but the device allows the clock rising edge to define the frame boundary by programming the CKINP bit in the Control Register (CR).
B6, C6, D5, D4, B4, B3, C5, C4, E3, C2, B2, D2, F3, F4, E2, F2, E1, D1, G1, F1, J1, H1, K1, L1, A7, A5, A6, A4, A3, A2, C1, B1	179, 180, 181, 182, 183, 184, 185, 187, 198, 200, 201, 202, 203, 204, 205, 206, 243, 244, 245, 246, 247, 248, 250, 252, 189, 190, 191, 192, 193, 194, 196, 197	STi0 - 31	**Serial Input Streams 0 to 31 (5 V-Tolerant Inputs with Internal Pull-downs)** The data rate of each input stream can be selected independently using the Stream Input Control Registers (SICR[n]). In the 2.048 Mbps mode, these pins accept serial TDM data streams at 2.048 Mbps with 32 channels per frame. In the 4.096 Mbps mode, these pins accept serial TDM data streams at 4.096 Mbps with 64 channels per frame. In the 8.192 Mbps mode, these pins accept serial TDM data streams at 8.192 Mbps with 128 channels per frame. In the 16.384 Mbps mode, these pins accept TDM data streams at 16.384 Mbps with 256 channels per frame.

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
N4, P4, R4, P5, N13, P11, R14, R15, M15, L15, L13, L14, E14, D13, D15, C15, D16, E16, C16, B16, A13, A12, A10, A11, N1, M1, P1, R1, T2, T3, T5, T4	6, 7, 9, 10, 51, 52, 53, 54, 70, 72, 73, 74, 115, 116, 117, 118, 125, 126, 127, 128, 129, 130, 131, 132, 253, 254, 255, 256, 1, 2, 3, 4	STio0 - 31	**Serial Output Streams 0 to 31 (5 V-Tolerant Slew-Rate-Limited Three-state I/Os with Enabled Internal Pull-downs)** The data rate of each output stream can be selected independently using the Stream Output Control Registers (SOCR[n]). In the 2.048 Mbps mode, these pins output serial TDM data streams at 2.048 Mbps with 32 channels per frame. In the 4.096 Mbps mode, these pins output serial TDM data streams at 4.096 Mbps with 64 channels per frame. In the 8.192 Mbps mode, these pins output serial TDM data streams at 8.192 Mbps with 128 channels per frame. In the 16.384 Mbps mode, these pins output serial TDM data streams at 16.384 Mbps with 256 channels per frame.These output streams can be used as bi-directionals by programming BDH (bit 7) and BDL (bit 6) of Internal Mode Selection (IMS) register.
R3, P6, R5, N5, P12, N15, P13, P15, N16, M16, L16, K16, H16, J16, G16, F16	11, 12, 13, 14, 55, 56, 58, 59, 75, 76, 77, 78, 119, 120, 122, 124	STOHZ0 - 15	**Serial Output Streams High Impedance Control 0 to 15 (5 V-Tolerant Slew-Rate-Limited Three-state Outputs)** These pins are used to enable (or disable) external three-state buffers. When an output channel is in the high impedance state, the STOHZ drives high for the duration of the corresponding output channel. When the STio channel is active, the STOHZ drives low for the duration of the corresponding output channel. STOHZ outputs are available for STio0 - 15 only.
B15	141	ODE	**Output Drive Enable (5 V-Tolerant Input with Internal Pull-up)** This is the output enable control for STio0 - 31 and the output-driven-high control for STOHZ0 - 15. When it is high, STio0 - 31 and STOHZ0 - 15 are enabled. When it is low, STio0 - 31 are tristated and STOHZ0 - 15 are driven high.
M4, N6, R6, P7, R7, N7, M8, N8, P8, R8, M9, N9, R9, N10, P9, R10	16, 18, 20, 22, 23, 24, 25, 26, 27, 28, 30, 32, 34, 36, 37, 38	D0 - 15	**Data Bus 0 to 15 (5 V-Tolerant Slew-Rate-Limited Three-state I/Os)** These pins form the 16-bit data bus of the microprocessor port.

PBGA Pin Number	LQFP Pin Number	Pin Name	Description
N12	44	$\overline{\text{DTA}}$_RDY	**Data Transfer Acknowledgment_Ready (5 V-Tolerant Three-state Output)** This active low output indicates that a data bus transfer is complete for the Motorola interface. For the Intel interface, it indicates a transfer is completed when this pin goes from low to high. An external pull-up resistor **MUST** hold this pin at HIGH level for the Motorola mode. An external pull-down resistor **MUST** hold this pin at LOW level for the Intel mode.
R11	40	$\overline{\text{CS}}$	**Chip Select (5 V-Tolerant Input)** Active low input used by the Motorola or Intel microprocessor to enable the microprocessor port access.
N11	39	R/$\overline{\text{W}}$_$\overline{\text{WR}}$	**Read/Write_Write (5 V-Tolerant Input)** This input controls the direction of the data bus lines (D0 - 15) during a microprocessor access. For the Motorola interface, this pin is set high and low for the read and write access respectively. For the Intel interface, a write access is indicated when this pin goes low.
R12	42	$\overline{\text{DS}}$_$\overline{\text{RD}}$	**Data Strobe_Read (5 V-Tolerant Input)** This active low input works in conjunction with $\overline{\text{CS}}$ to enable the microprocessor port read and write operations for the Motorola interface. A read access is indicated when it goes low for the Intel interface.
K13, K15, K14, J11, J12, J13, J15, H11, J14, H12, H13, H15, G12, G13	82, 84, 86, 87, 88, 89, 90, 91, 92, 93, 94, 96, 98, 99	A0 - 13	**Address 0 to 13 (5 V-Tolerant Inputs)** These pins form the 14-bit address bus to the internal memories and registers.
M13	41	MOT_$\overline{\text{INTEL}}$	**Motorola_Intel (5 V-Tolerant Input with Internal Pull-up)** This pin selects the Motorola or Intel microprocessor interface to be connected to the device. When this pin is unconnected or connected to high, Motorola interface is assumed. When this pin is connected to ground, Intel interface should be used.
G2	211	$\overline{\text{RESET}}$	**Device Reset (5 V-Tolerant Input with Internal Pull-up)** This input (active LOW) puts the device in its reset state that disables the STio0 - 31 drivers and drives the STOHZ0 - 15 outputs to high. It also preloads registers with default values and clears all internal counters. To ensure proper reset action, the reset pin must be low for longer than 1 μs. Upon releasing the reset signal to the device, the first microprocessor access cannot take place for at least 600 μs due to the time required to stabilize the device from the power-down state. Refer to Section Section 13.2 on page 33 for details.

3.0 Device Overview

The device has thirty-two ST-BUS/GCI-Bus inputs (STi0 - 31) and thirty-two ST-BUS/GCI-Bus outputs (STio0 - 31). STio0 - 31 can also be configured as bi-directional pins, in which case STi0 - 31 will be ignored. It is a non-blocking digital switch with 2048 64 kbps channels and is capable of performing rate conversion between ST-BUS/GCI-Bus inputs and ST-BUS/GCI-Bus outputs. The ST-BUS/GCI-Bus inputs accept serial input data streams with data rates of 2.048 Mbps, 4.096 Mbps, 8.192 Mbps and 16.384 Mbps on a per-stream basis. The ST-BUS/GCI-Bus outputs deliver serial data streams with data rates of 2.048 Mbps, 4.096 Mbps and, 8.192 Mbps and 16.384 Mbps on a per-stream basis. The device also provides sixteen high impedance control outputs (STOHZ0 - 15) to support the use of external ST-BUS/GCI-Bus tristate drivers for the first sixteen ST-BUS/GCI-Bus outputs (STio0 -15).

By using Zarlink's message mode capability, microprocessor data stored in the connection memory can be broadcast to the output streams on a per-channel basis. This feature is useful for transferring control and status information for external circuits or other ST-BUS/GCI-Bus devices.

The device uses the ST-BUS/GCI-Bus input frame pulse (FPi) and the ST-BUS/GCI-Bus input clock (CKi) to define the input frame boundary and timing for sampling the ST-BUS/GCI-Bus input streams with various data rates. The output data streams will be driven by and have their timing defined by FPi and CKi in Divided Clock mode (CLKM bit 11 Table 13, Control Register (CR) Bits. In Multiplied Clock mode, the output data streams will be driven by an internally generated clock, which is multiplied from CKi internally. In Multiplied Clock mode, the output data streams will be driven by an internally generated clock, which is multiplied from CKi internally. Refer to Application Note ZLAN-120 for further explanation of the different modes of operation.

There are two clock modes for this device:

The first is the Divided Clock mode. In this mode, output streams are clocked by input CKi. Therefore the output streams have exactly the same jitter as the input streams. The output data rate can be the same as or lower than the input data rate, but the output data rate cannot be higher than what CKi can drive. For example, if CKi is 4.096 MHz, the output data rate cannot be higher than 2.048 Mbps.The second clock mode is called Multiplied Clock mode. In this mode, CKi is used to generate a 16.384 MHz clock internally, and output streams are driven by this internal clock. In Multiplied Clock mode, the data rate of output streams can be any rate, but output jitter may not be exactly the same as input jitter.

A Motorola or Intel compatible non-multiplexed microprocessor port allows users to program the device to operate in various modes under different switching configurations. Users can use the microprocessor port to perform internal register and memory read and write operations. The microprocessor port has a 16-bit data bus, a 14-bit address bus and six control signals (MOT_INTEL, CS, DS_RD, R/W_WR and DTA_RDY).

The device supports the mandatory requirements of the IEEE-1149.1 (JTAG) standard via the test port.

4.0 Data Rates and Timing

The ZL50020 has 32 serial data inputs and 32 serial data outputs. Each stream can be individually programmed to operate at 2.048 Mbps, 4.096 Mbps, 8.192 Mbps or 16.384 Mbps. Depending on the data rate there will be 32 channels, 64 channels, 128 channels or 256 channels, respectively, during a 125 μs frame.

The output streams can be programmed to operate as bi-directional streams. The output streams are divided into two groups to be programmed into bi-directional mode. By setting BDL (bit 6) in the Internal Mode Selection (IMS) register, input streams 0 - 15 (STi0 - 15) are internally tied low, and output streams 0 - 15 (STio0 - 15) are set to operate in a bi-directional mode. Similarly, when BDH (bit 7) in the Internal Mode Selection (IMS) register is set, input streams 16 - 31 (STi16 - 31) are internally tied low, and output streams 16 - 31 (STio16 - 31) are set to operate in bi-directional mode. The groups do not have to be set into the same mode. Therefore it is possible to have half of the streams operating in bi-directional mode while the other half is operating in normal input/output mode.

The input data rate is set on a per-stream basis by programming STIN[n]DR3 - 0 (bits 3 - 0) in the Stream Input Control Register 0 - 31 (SICR0 - 31). The output data rate is set on a per-stream basis by programming STO[n]DR3 - 0 (bits 3 - 0) in the Stream Output Control Register 0 - 31 (SOCR0 - 31). The output data rates do not have to match or follow the input data rates. he maximum number of channels switched is limited to 2048 channels. If all 32

input streams were operating at 16.384 Mbps (256 channels per stream), this would result in 8192 channels. Memory limitations prevent the device from operating at this capacity. A maximum capacity of 2048 channels will occur if eight of the streams are operating at 16.384 Mbps, half of the streams are operating at 8.192 Mbps or all streams operating at 4.096 Mbps. With all streams operating at 2.048 Mbps, the capacity will be reduced to 1024 channels. However, as each stream can be programmed to a different data rate, any combination of data rates can be achieved, as long as the total channel count does not exceed 2048 channels. It should be noted that only full stream can be programmed for use. The device does not allow fractional streams. External High Impedance Control, STOHZ0 - 15.

There are 16 external high impedance control signals, STOHZ0 - 15, that are used to control the external drivers for per-channel high impedance operations. Only the first sixteen ST-BUS/GCI-Bus (STio0 - 15) outputs are provided with corresponding STOHZ signals. The STOHZ outputs deliver the appropriate number of control timeslot channels based on the output stream data rate. Each control timeslot lasts for one channel time. When the ODE pin is high and the OSB (bit 2) of the Control Register (CR) is also high, STOHZ0 - 15 are enabled. When the ODE pin, OSB (bit 2) of the Control Register (CR) or the $\overline{\text{RESET}}$ pin is low, STOHZ0 - 15 are driven high, together with all the ST-BUS/GCI-Bus outputs being tristated. Under normal operation, the corresponding STOHZ outputs of any unused ST-BUS/GCI-Bus channel (high impedance) are driven high. Refer to Figure 16 on page 28 for a diagrammatical explanation.

4.1 Input Clock (CKi) and Input Frame Pulse (FPi) Timing

The frequency of the input clock (CKi) for the ZL50020 depends on the operation mode selected. In divided clock mode, CKi must be at least twice the highest input or output data rate. For example, if the highest input data rate is 4.096 Mbps and the highest output data rate is 8.192 Mbps, the input clock, CKi, must be 16.384 MHz, which is twice the highest overall data rate. The only exception to this is for 16.384 Mbps input or output data. In this case, the input clock, CKi, is equal to the data rate. The input frame pulse, FPi, must always follow CKi. In multiplied clock mode the frequency of CKi must be at least twice the highest input data rate regardless of the output data rate. An APLL is used to multiple CKi to generate an internal clock that is used to output clocks and STio streams. Following the example above, if the highest input data rate is 4.096 Mbps, the input clock, CKi, must be 8.192 MHz, regardless of the output data rate. The only exception to this is for 16.384 Mbps input or output data. In this case, the input clock, CKi, is equal to the data rate. The input frame pulse, FPi, must always follow CKi.

In either mode the user has to program the CKIN1 - 0 (bits 6 - 5) in the Control Register (CR) to indicate the width of the input frame pulse and the frequency of the input clock supplied to the device.

Highest ***Input or Output*** Data Rate	CKIN 1-0 Bits	Input Clock Rate (CKi)	Input Frame Pulse (FPi)
8.192 Mbps or 16.384 Mbps	00	16.384 MHz	8 kHz (61 ns wide pulse)
4.096 Mbps	01	8.192 MHz	8 kHz (122 ns wide pulse)
2.048 Mbps	10	4.096 MHz	8 kHz (244 ns wide pulse)

Table 1 - CKi and FPi Configurations for Divided Clock Modes

Highest ***Input*** Data Rate	CKIN 1-0 Bits	Input Clock Rate (CKi)	Input Frame Pulse (FPi)
8.192 Mbps or 16.384 Mbps	00	16.384 MHz	8 kHz (61 ns wide pulse)
4.096 Mbps	01	8.192 MHz	8 kHz (122 ns wide pulse)
2.048 Mbps	10	4.096 MHz	8 kHz (244 ns wide pulse)

Table 2 - CKi and FPi Configurations for Multiplied Clock Mode

The ZL50020 accepts positive and negative ST-BUS/GCI-Bus input clock and input frame pulse formats via the programming of CKINP (bit 8) and FPINP (bit 7) in the Control Register (CR). By default, the device accepts the negative input clock format and ST-BUS format frame pulses. However, the switch can also accept a positive-going clock format by programming CKINP (bit 8) in the Control Register (CR). A GCI-Bus format frame pulse can be used by programming FPINPOS (bit 9) and FPINP (bit 7) in the Control Register (CR).

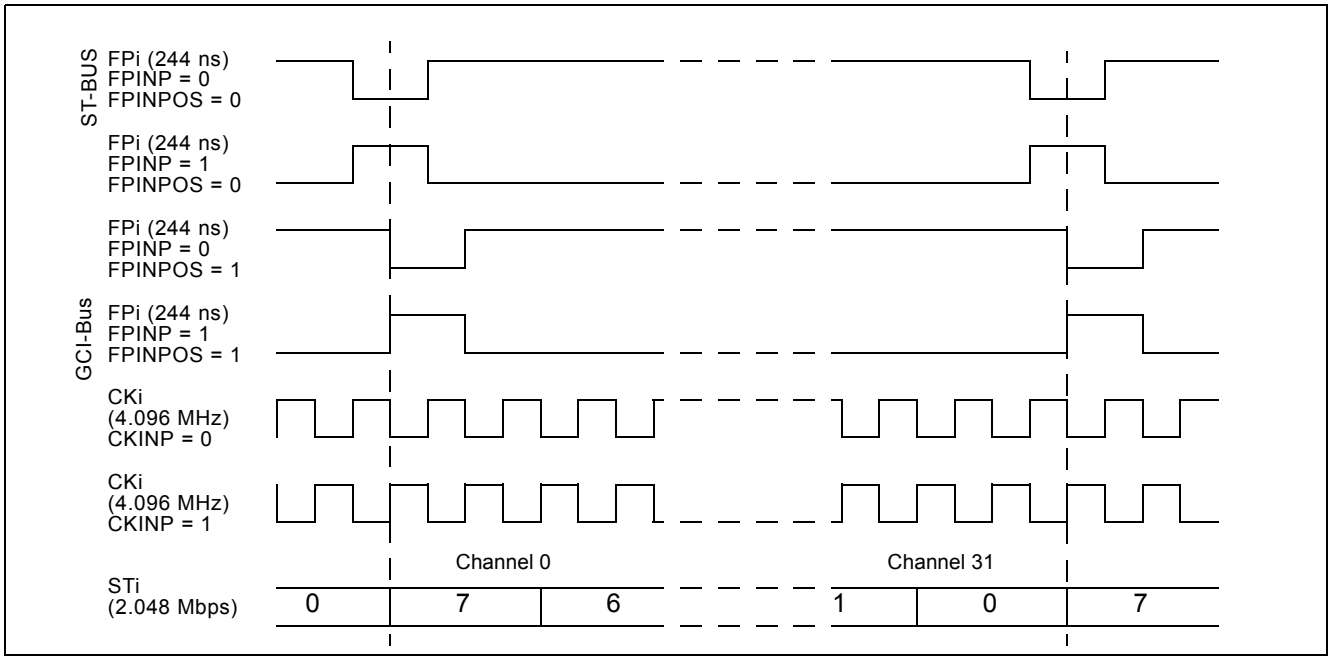


Figure 4 - Input Timing when CKIN1 - 0 bits = “10” in the CR

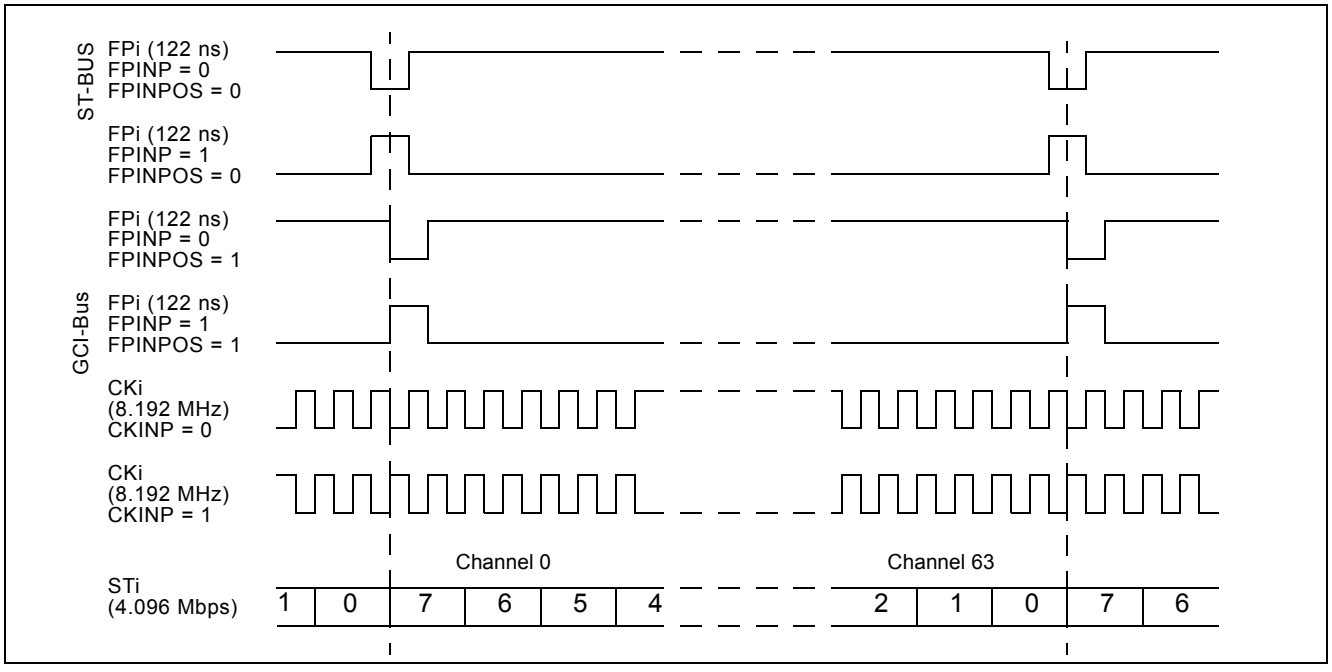


Figure 5 - Input Timing when CKIN1 - 0 bits = “01” in the CR

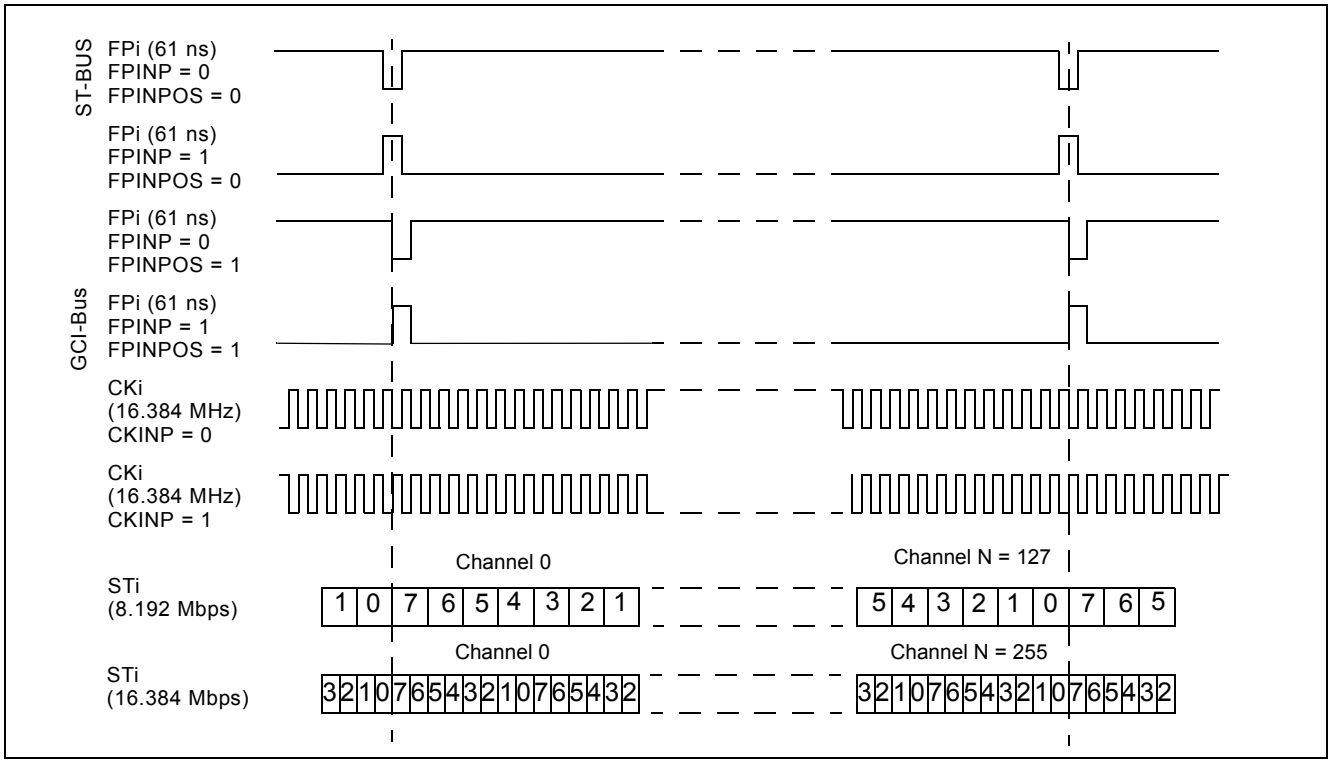


Figure 6 - Input Timing when CKIN1 - 0 = “00” in the CR

5.0 ST-BUS and GCI-Bus Timing

The ZL50020 is capable of operating using either the ST-BUS or GCI-Bus standards. The output timing that the device generates is defined by the bus standard. In the ST-BUS standard, the output frame boundary is defined by the falling edge of CKo while FPo is low. In the GCI-Bus standard, the frame boundary is defined by the rising edge of CKo while FPo goes high. The data rates define the number of channels that are available in a 125 µs frame pulse period.

By default, the ZL50020 is configured for ST-BUS input and output timing. To set the input timing to conform to the GCI-Bus standard, FPINPOS (bit 9) and FPINP (bit 7) in the Control Register (CR) must be set. To set output timing to conform to the GCI-Bus standard, FPO[n]P and FPO[n]POS must be set in the Output Clock and Frame Pulse Selection Register (OCFSR). The CKO[n]P bits in the Output Clock and Frame Pulse Selection Register control the polarity (positive-going or negative-going) of the output clocks.

6.0 Output Timing Generation

The ZL50020 generates frame pulse and clock timing. There are four output frame pulse pins (FPo0 - 3) and four output clock pins (CKo0 - 3). All output frame pulses are 8 kHz output signals. By default, the output frame boundary is defined by the falling edge of the CKo0, while FPo0 is low. At the output frame boundary, the CKo1, CKo2 and CKo3 output clocks will by default have a falling edge, while FPo1, FPo2 and FPo3 will be low. The duration of the frame pulse low cycle and the frequency of the corresponding output clock are shown in Table 3 on page 19. Every frame pulse and clock output can be tristated by programming the enable bits in the Internal Mode Selection (IMS) register.

Pin Name	Output Timing Rate	Output Timing Unit

Table 3 - Output Timing Generation

FPo0 pulse width	244	ns
CKo0	4.096	MHz
FPo1 pulse width	122	ns
CKo1	8.192	MHz
FPo2 pulse width	61	ns
CKo2	16.384	MHz
FPo3 pulse width	244, 122, 61 or 30	ns
CKo3	4.096, 8.192, 16.384 or 32.768	MHz

Table 3 - Output Timing Generation

The output timing is dependent on the operation mode that is selected. When the device is in Divided Clock mode, the frequencies on CKo0 - 3 cannot be greater than the input clock, CKi. For example, if the input clock is 8.192 MHz, the CKo2 pin will not produce a valid output clock and the CKo3 pin can only be programmed to output a 4.096 MHz or 8.192 MHz clock signal.

The device also delivers positive or negative output frame pulse and ST-BUS/GCI-Bus output clock formats via the programming of various bits in the Output Clock and Frame Pulse Selection Register (OCFSR). By default, the device delivers the negative output clock format. The ZL50020 can also deliver GCI-Bus format output frame pulses by programming bits of the Output Clock and Frame Pulse Selection Register (OCFSR). As there is a separate bit setting for each frame pulse output, some of the outputs can be set to operate in ST-BUS mode and others in GCI-Bus mode.

The following figures describe the usage of the FPO0P, FPO1P, FPO2P, FPO3P, CKO0P, CKO1P, CKO2P and CKO3P bits to generate the FPo0 - 3 and CKo0 - 3 timing.

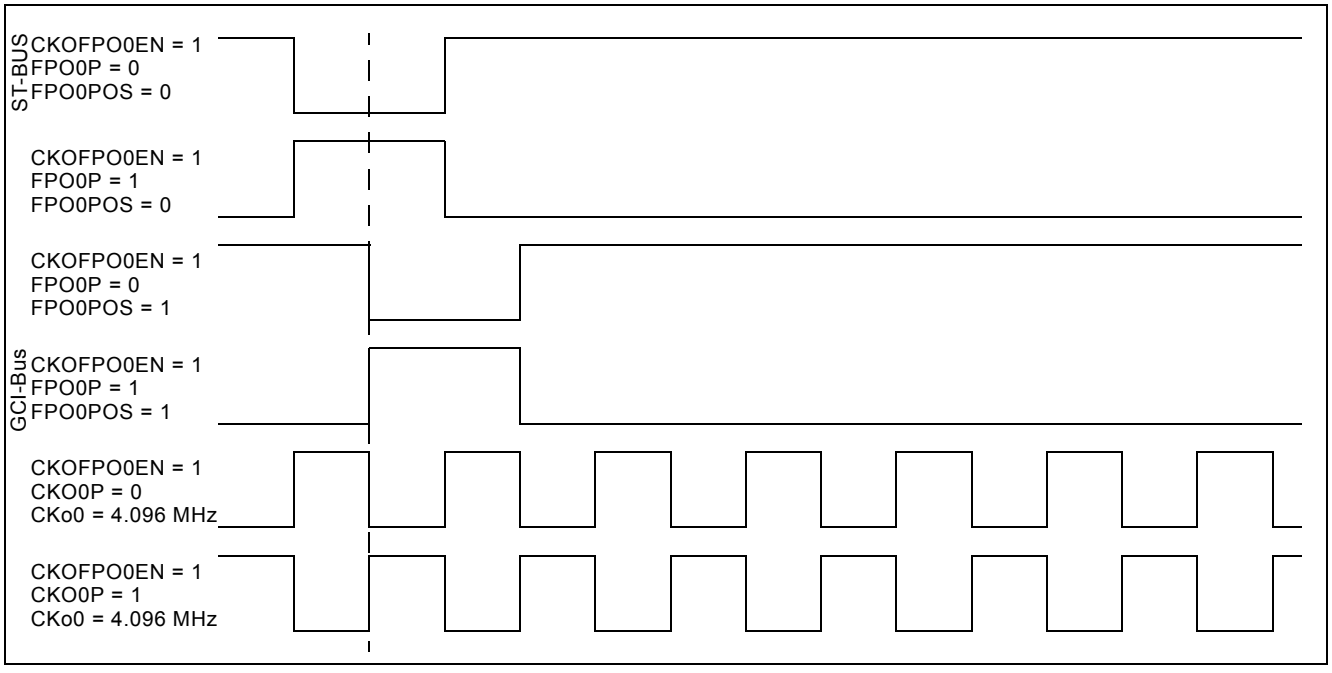


Figure 7 - Output Timing for CKo0 and FPo0

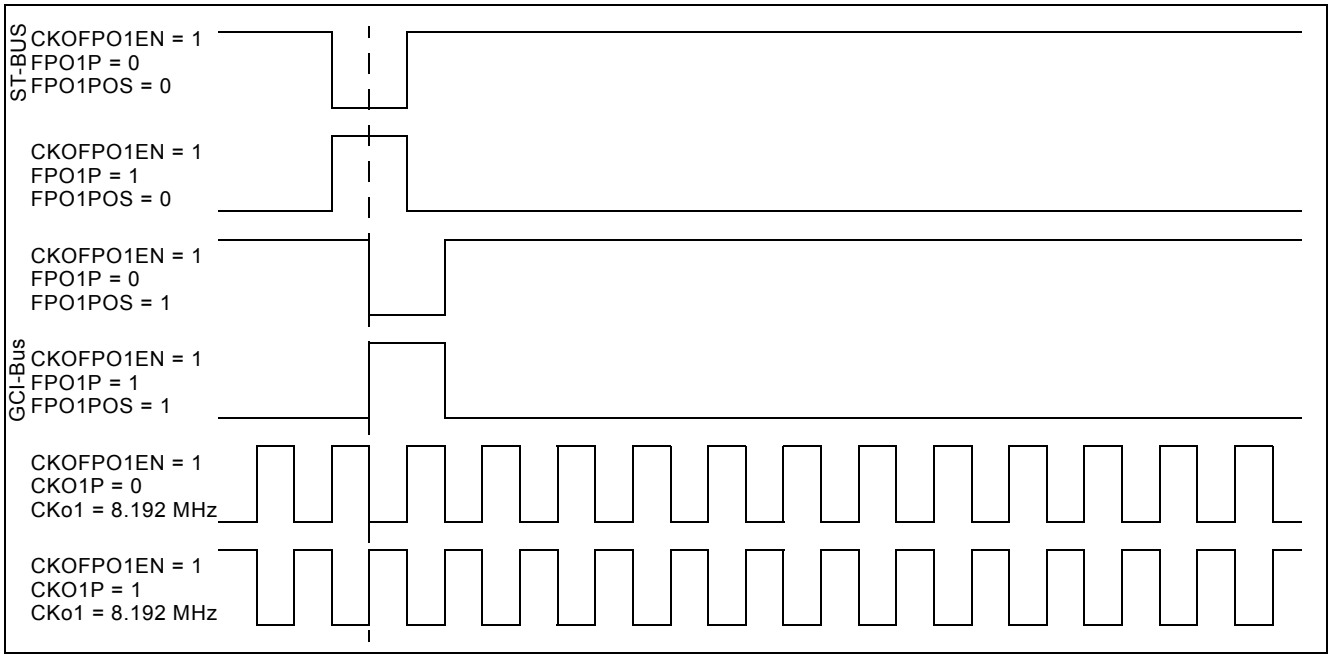


Figure 8 - Output Timing for CKo1 and FPo1

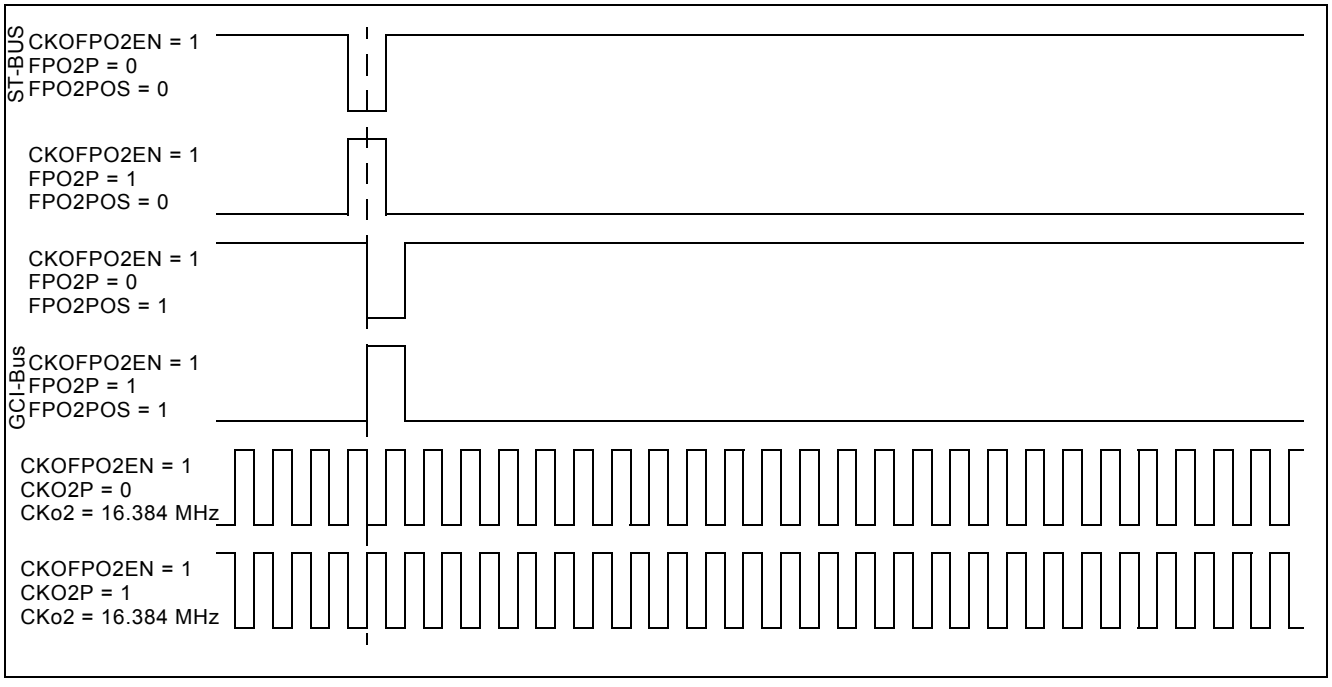
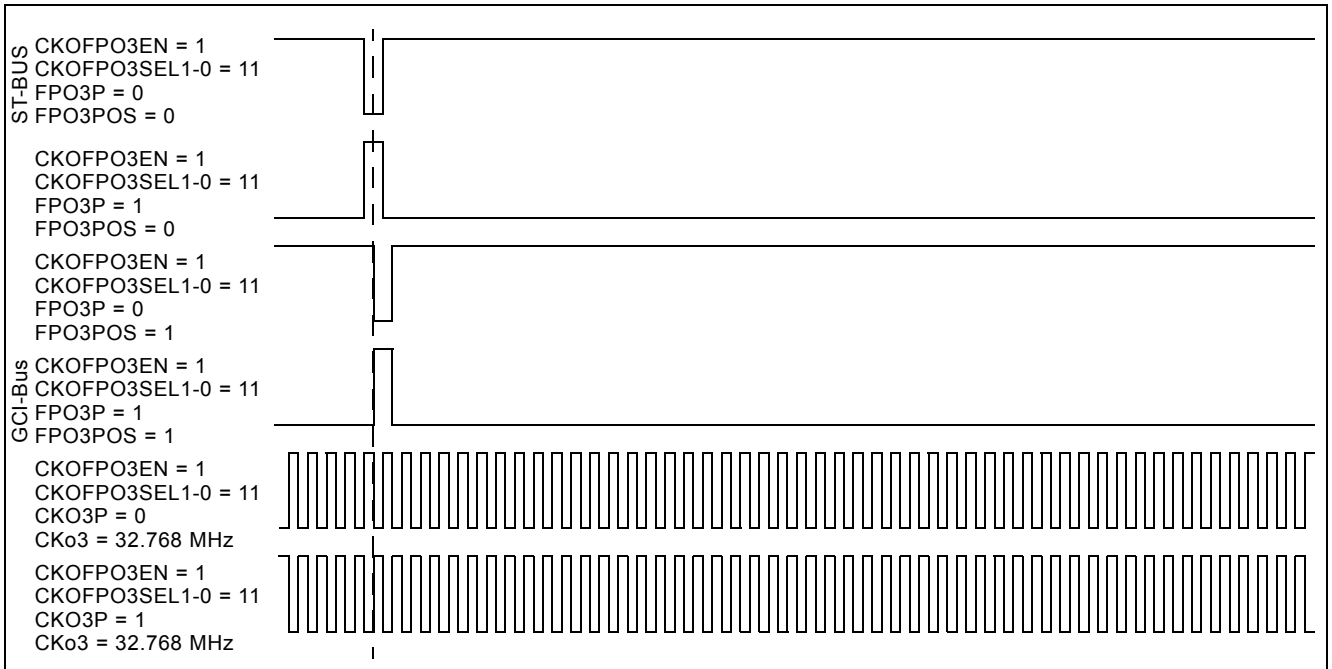


Figure 9 - Output Timing for CKo2 and FPo2



NOTE:
When CKOFPO3SEL1-0 = “00,” the output for FPo3 and CKo3 follow the same as Figure 7: Output Timing for CKo0 and FPo0
When CKOFPO3SEL1-0 = “01,” the output for FPo3 and CKo3 follow the same as Figure 8: Output Timing for CKo1 and FPo1
When CKOFPO3SEL1-0 = “10,” the output for FPo3 and CKo3 follow the same as Figure 9: Output Timing for CKo2 and FPo2

Figure 10 - Output Timing for CKo3 and FPo3 with CKoFPo3SEL1-0=”11”

7.0 Data Input Delay and Data Output Advancement

Various registers are provided to adjust the input delay and output advancement for each input and output data stream. The input bit delay and output bit advancement can vary from 0 to 7 bits for each individual stream.

If input delay of less than a bit is desired, different sampling points can be used to handle the adjustments. The sampling point can vary from 1/4 to 4/4 with a 1/4-bit increment for all input streams, unless the stream is operating at 16.384 Mbps, in which case the fractional bit delay has a 1/2-bit increment. By default, the sampling point is set to the 3/4-bit location for non-16.384 Mbps data rates and the 1/2-bit location for the 16.384 Mbps data rate.

The fractional output bit advancement can vary from 0 to 3/4 bits, again with a 1/4-bit increment unless the output stream is operating at 16.384 Mbps, in which case the output bit advancement has a 1/2-bit increment from 0 to 1/2 bit. By default, there is 0 output bit advancement.

Although input delay or output advancement features are available on streams which are operating in bi-directional mode it is not recommended, as it can easily cause bus contention. If users require this function, special attention must be given to the timing to ensure contention is minimized.

7.1 Input Bit Delay Programming

The input bit delay programming feature provides users with the flexibility of handling different wire delays when designing with source streams for different devices.

By default, all input streams have zero bit delay, such that bit 7 is the first bit that appears after the input frame boundary (assuming ST-BUS formatting). The input delay is enabled by STIN[n]BD2-0 (bits 8 - 6) in the Stream Input Control Register 0 - 31 (SICR0 - 31) as described in Table 24 on page 50. The input bit delay can range from 0 to 7 bits.

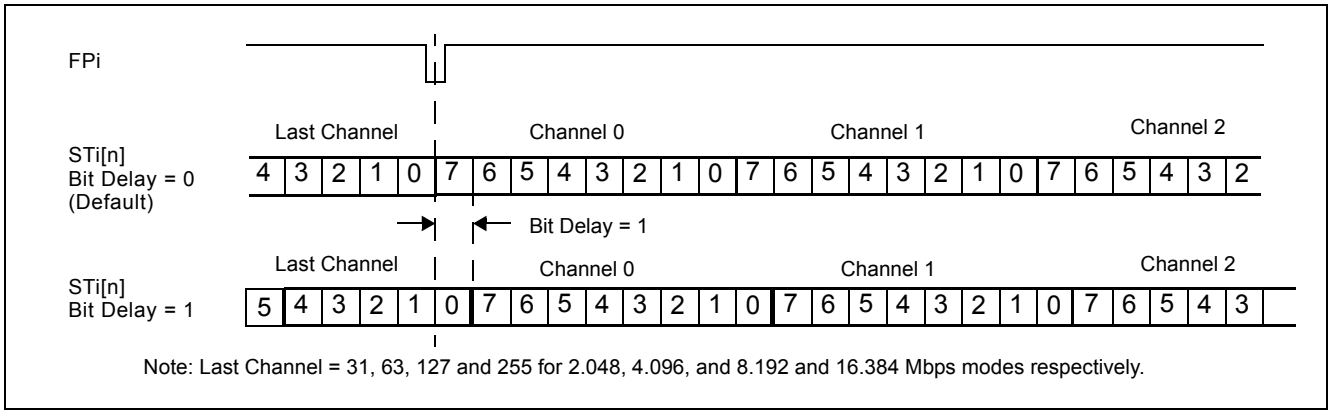


Figure 11 - Input Bit Delay Timing Diagram (ST-BUS)

7.2 Input Bit Sampling Point Programming

In addition to the input bit delay feature, theZL50020 allows users to change the sampling point of the input bit by programming STIN[n]SMP 1-0 (bits 5 - 4) in the Stream Input Control Register 0 - 31 (SICR0 - 31). For input streams operating at any rate except 16.384 Mbps, the default sampling point is at 3/4 bit and users can change the sampling point to 1/4, 1/2, 3/4 or 4/4 bit position. When the stream is operating at 16.384 Mbps, the default sampling point is 1/2 bit and can be adjusted to a 4/4 bit position.

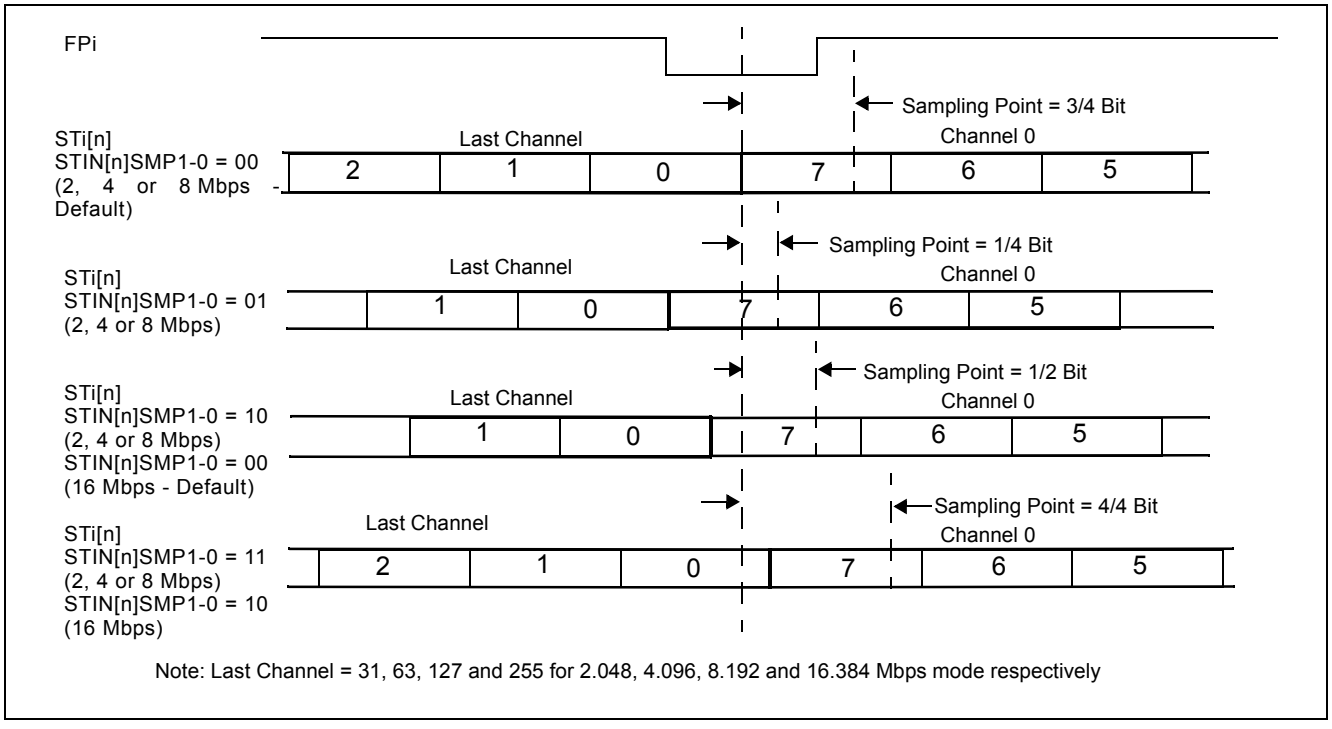


Figure 12 - Input Bit Sampling Point Programming

The input delay is controlled by STIN[n]BD2-0 (bits 8 - 6) to control the bit shift and STIN[n]SMP1 - 0 (bits 5 - 4) to control the sampling point in the Stream Input Control Register 0 - 31 (SICR0 - 31).

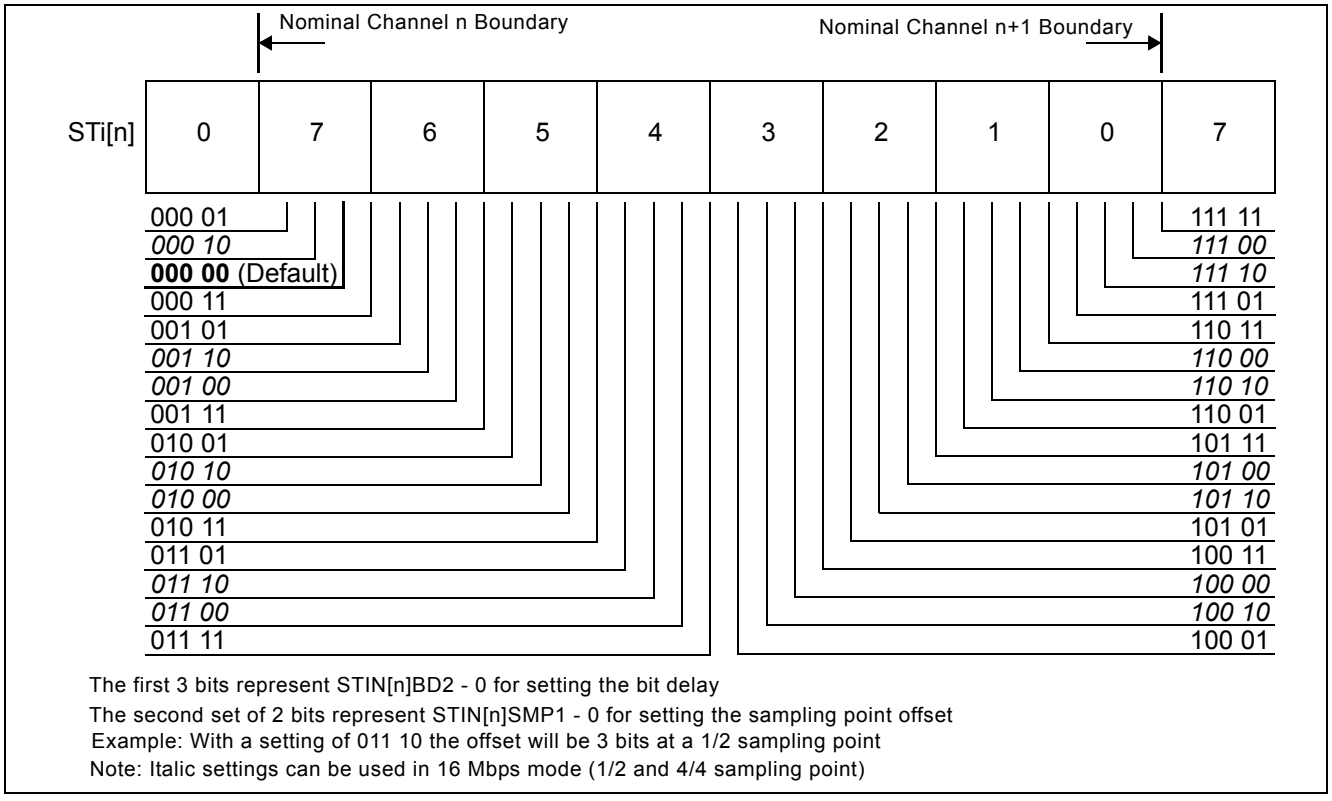


Figure 13 - Input Bit Delay and Factional Sampling Point

7.3 Output Advancement Programming

This feature is used to advance the output data of individual output streams with respect to the output frame boundary. Each output stream has its own bit advancement value which can be programmed in the Stream Output Control Register 0 - 31 (SOCR0 - 31).

By default, all output streams have zero bit advancement such that bit 7 is the first bit that appears after the output frame boundary (assuming ST-BUS formatting). The output advancement is enabled by STO[n]AD 2 - 0 (bits 6 - 4) of the Stream Output Control Register 0 - 31 (SOCR0 - 31) as described in Table 26 on page 54. The output bit advancement can vary from 0 to 7 bits.

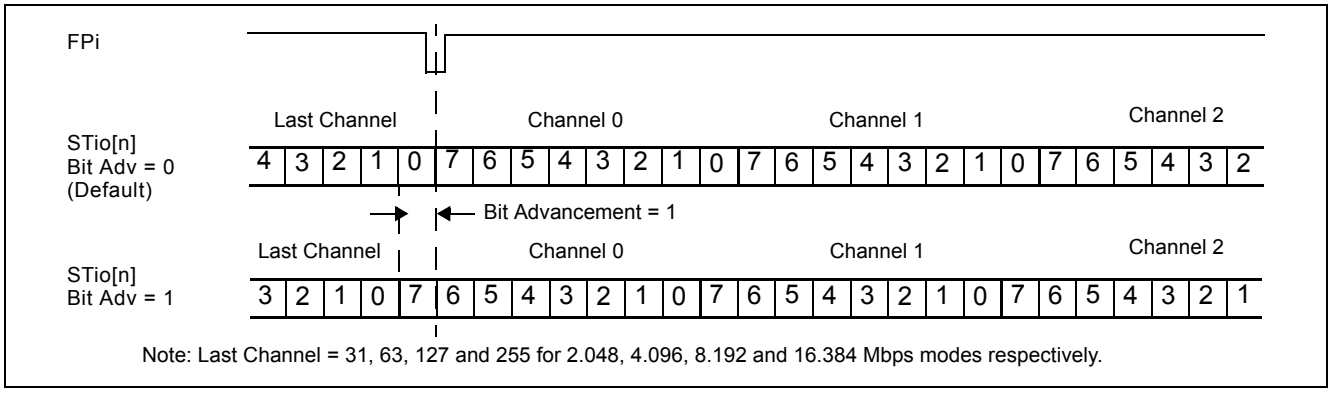


Figure 14 - Output Bit Advancement Timing Diagram (ST-BUS)

7.4 Fractional Output Bit Advancement Programming

In addition to the output bit advancement, the device has a fractional output bit advancement feature that offers better resolution. The fractional output bit advancement is useful in compensating for varying parasitic load on the serial data output pins.

By default all of the streams have zero fractional bit advancement such that bit 7 is the first bit that appears after the output frame boundary. The fractional output bit advancement is enabled by STO[n]FA 1 - 0 (bits 8 - 7) in the Stream Output Control Register 0 - 31 (SOCR0 - 31). For all streams running at any data rate except 16.384 Mbps the fractional bit advancement can vary from 0, 1/4, 1/2 to 3/4 bits. For streams operating at 16.384 Mbps, the fractional bit advancement can be set to either 0 or 1/2 bit.

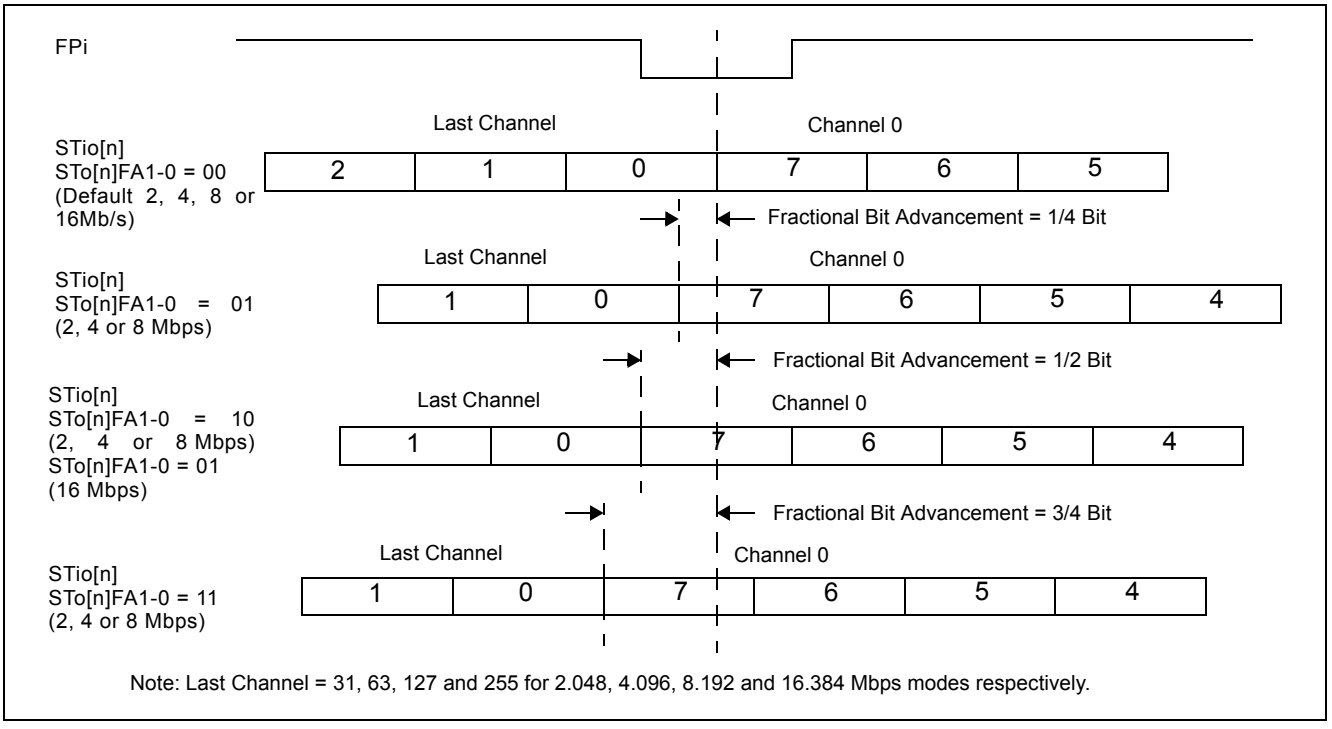


Figure 15 - Output Fractional Bit Advancement Timing Diagram (ST-BUS)

7.5 External High Impedance Control Advancement

The external high impedance signals can be programmed to better match the timing required by the external buffers. By default, the output timing of the STOHZ signals follows the programmed channel delay and bit offset of their corresponding ST-BUS/GCI-Bus output streams. In addition, for all high impedance streams operating at any data rate except 16.384 Mbps, the user can advance the STOHZ signals a further 0, 1/4, 1/2, 3/4 or 4/4 bits by programming STOHZ[n]A 2 - 0 (bit 11 - 9) in the Stream Output Control Register. When the stream is operating at 16.384 Mbps, the additional STOHZ advancement can be set to 0, 1/2 or 4/4 bits by programming the same register.

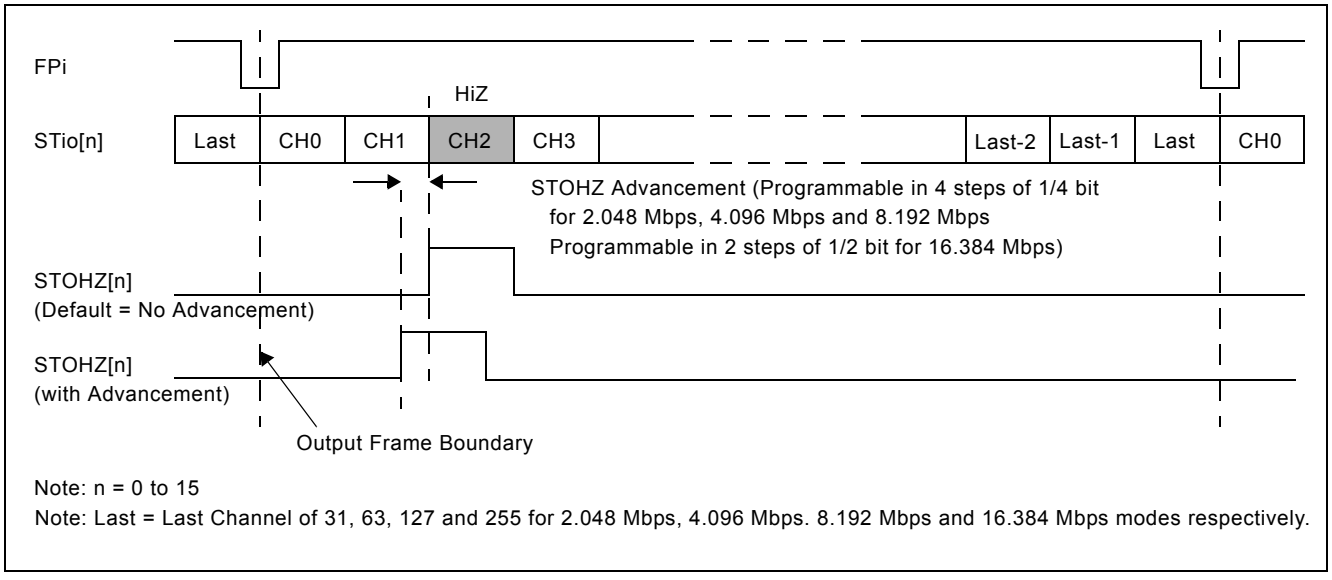


Figure 16 - Channel Switching External High Impedance Control Timing

8.0 Data Delay Through the Switching Paths

The switching of information from the input serial streams to the output serial streams results in a throughput delay. The device can be programmed to perform timeslot interchange functions with different throughput delay capabilities on a per-channel basis. For voice applications, select variable throughput delay to ensure minimum delay between input and output data. In wideband data applications, select constant delay to maintain the frame integrity of the information through the switch. The delay through the device varies according to the type of throughput delay selected by the V/$\overline{C}$ (bit 14) in the Connection Memory Low when CMM = 0.

8.1 Variable Delay Mode

Variable delay mode causes the output channel to be transmitted as soon as possible. This is a useful mode for voice applications where the minimum throughput delay is more important than frame integrity. The delay through the switch can vary from 7 channels to 1 frame + 7 channels. To set the device into variable delay mode, VAREN (bit 4) in the Control Register (CR) must be set before V/$\overline{C}$ (bit 14) in the Connection Memory Low when CMM = 0. If the VAREN bit is not set and the device is programmed for variable delay mode, the information read on the output stream will not be valid.

In variable delay mode, the delay depends on the combination of the source and destination channels of the input and output streams.

m = input channel number n = output channel number	n-m <= 0	0 < n-m < 7	n-m = 7		n-m > 7
			STio < STi	STio >= STi	
T = Delay between input and output	1 frame - (m-n)	1 frame + (n-m)		n-m	

Table 4 - Delay for Variable Delay Mode

For example, if Stream 4 Channel 2 is switched to Stream 5 Channel 9 with variable delay, the data will be output in the same 125 µs frame. Contrarily, if Stream 6 Channel 1 is switched to Stream 9 Channel 3, the information will appear in the following frame.

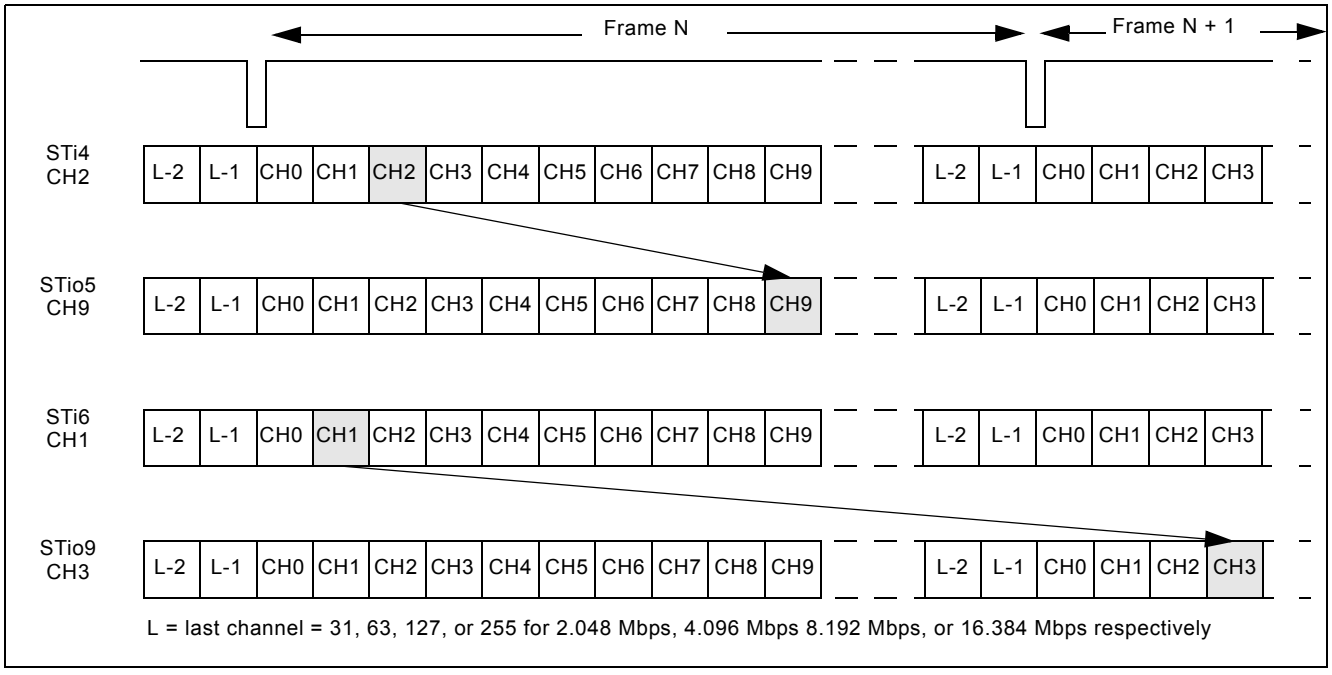


Figure 17 - Data Throughput Delay for Variable Delay

8.2 Constant Delay Mode

In this mode, frame integrity is maintained in all switching configurations. The delay though the switch is 2 frames - Input Channel + Output Channel. This can result in a minimum of 1 frame + 1 channel delay if the last channel on a stream is switched to the first channel of a stream. The maximum delay is 3 frames - 1 channel. This occurs when the first channel of a stream is switched to the last channel of a stream. The constant delay mode is available for all output channels.

The data throughput delay is expressed as a function of ST-BUS/GCI-Bus frames, input channel number (m) and output channel number (n). The data throughput delay (T) is:

T = 2 frames + (n - m)

The constant delay mode is controlled by V/$\overline{C}$ (bit 14) in the Connection Memory Low when CMM = 0. When this bit is set low, the channel is in constant delay mode. If VAREN (bit 4) in the Control Register (CR) is set (to enable variable throughput delay on a chip-wide basis), the device can still be programmed to operate in constant delay mode.

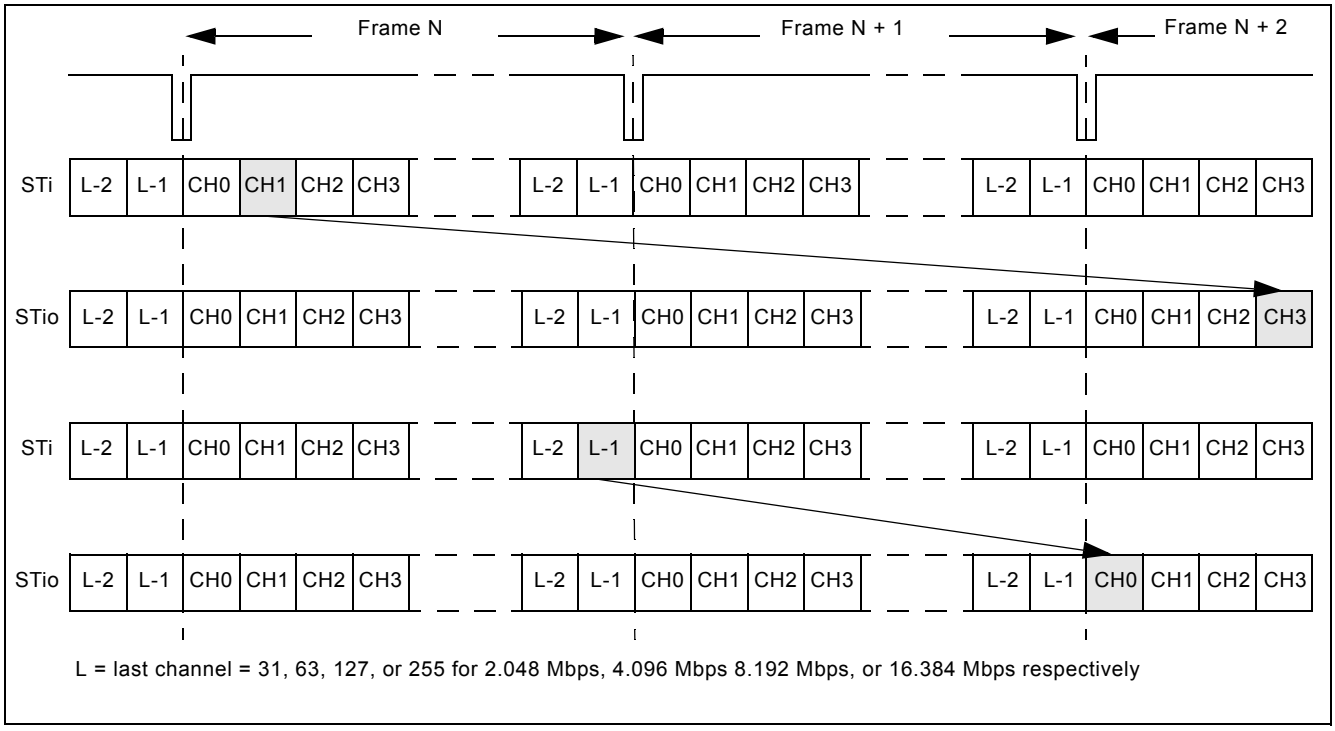


Figure 18 - Data Throughput Delay for Constant Delay

9.0 Connection Memory Description

The connection memory consists of two blocks, Connection Memory Low (CM_L) and Connection Memory High (CM_H). The CM_L is 16 bits wide and is used for channel switching and other special modes. The CM_H is 5 bits wide and is used for the voice coding function. When UAEN (bit 15) of the Connection Memory Low (CM_L) is low, μ-law/A-law conversion will be turned off and the contents of CM_H will be ignored. Each connection memory location of the CM_L or CM_H can be read or written via the 16 bit microprocessor port within one microprocessor access cycle. See Table 31 on page 57 for the address mapping of the connection memory. Any unused bits will be reset to zero on the 16-bit data bus.

For the normal channel switching operation, CMM (bit 0) of the Connection Memory Low (CM_L) is programmed low. SCA7 - 0 (bits 8 - 1) indicate the source (input) channel address and SSA4 - 0 (bits 13 - 9) indicate the source (input) stream address. The 5-bit contents of the CM_H will be ignored during the normal channel switching mode without the μ-law/A-law conversion when UAEN (bit 15) of the Connection Memory Low (CM_L) is set to zero. If μ-law/A-law conversion is required, the CM_H bits must be programmed first to provide the voice/data information, the input coding law and the output coding law before the assertion of UAEN (bit 15) in the Connection Memory Low.

When CMM (bit 0) of the Connection Memory Low (CM_L) is programmed high, the ZL50020 will operate in one of the special modes described in Table 33 on page 58. When the per-channel message mode is enabled, MSG7 - 0 (bit 10 - 3) in the Connection Memory Low (CM_L) will be output via the serial data stream as message output data. When the per-channel message mode is enabled, the μ-law/A-law conversion can also be enabled as required.

10.0 Connection Memory Block Programming

This feature allows for fast initialization of the connection memory after power up.

10.1 Memory Block Programming Procedure

1. Set MBPE (bit 3) in the Control Register (CR) from low to high.
2. Configure BPD2 - 0 (bits 3 - 1) in the Internal Mode Selection (IMS) register to the desired values to be loaded into CM_L.
3. Start the block programming by setting MBPS (bit 0) in the Internal Mode Selection Register (IMS) high. The values stored in BPD2 - 0 will be loaded into bits 2 - 0 of all CM_L positions. The remaining CM_L locations (bits 15 - 3) and the programmable values in the CM_H (bits 4 - 0) will be loaded with zero values.

The following tables show the resulting values that are in the CM_L and CM_H connection memory locations.

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	BPD2	BPD1	BPD0

Table 5 - Connection Memory Low After Block Programming

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6 - Connection Memory High After Block Programming

Note: Bits 15 to 5 are reserved in Connection Memory High and should always be 0.

It takes at least two frame periods (250 μs) to complete a block program cycle.

MBPS (bit 0) in the Control Register (CR) will automatically reset to a low position after the block programming process has completed.

MBPE (bit 3) in the Internal Mode Selection (IMS) register must be cleared from high to low to terminate the block programming process. This is not an automatic action taken by the device and must be performed manually.

Note: Once the block program has been initiated, it can be terminated at any time prior to completion by setting MBPS (bit 0) in the Control Register (CR) or MBPE (bit 3) in the Internal Mode Selection (IMS) register to low. If the MBPE bit was used to terminate the block programming, the MBPS bit will have to be set low before enabling other device operations.

11.0 Device Operation in Divided Clock and Multiplied Clock Modes

This device has two main operating modes - Divided Clock mode and Multiplied Clock mode.

In Multiplied Clock mode, output clocks and frame pulses are generated from an internal high-speed clock synchronized to CKi and FPi. Therefore, all specified output clock rates and data rates are available on CKo0-3 and STio0-31. In Divided Clock mode, output clocks and frame pulses are directly divided from CKi/FPi. Therefore, the output clock rate cannot exceed the CKi rate (the output data rates are also limited as per Table 1). The input data rate cannot exceed the CKi rate in either Multiplied or Divided Clock modes, because input data are always sampled directly by CKi.

Table 7, “ZL50020 Operating Modes” on page 32 summarizes the different modes of operation available within the ZL50020. Each Major mode (explained below) has an associated Minor mode that is determined by setting the MODE_4M Input Control pins and the OPM bit in the Control Register (Table 13, “Control Register (CR) Bits” on page 39) indicated in the table.

Device		Input Pins		CR Register	Output Clock Pins		Data Pins	
Operating Mode		Control	Signal	Bit	Reference Lock	Enabled	Clock Source	
Major	Minor	MODE_4M [1:0]	CKi	OPM	CKo0-3	CKo0-3	STi	STo
Divided Clock	4 M	11	4 M	0	CKi	Yes	CKi	CKo0-3 (CKi)
	8/16 M	00	8/16 M					
Multiplied Clock	4 M	11	4 M	1	CKi MULT			CKo0-3 (CKi MULT)
	8/16 M	00	8/16 M					

Legend:

X Don’t care or not applicable.

Reference Lock Refers to what signal the output pins are locked to:
Cki = Bypass. Cki is passed directly through to CKo0-3.
Cki MULT = Cki is passed through clock multiplier to CKo0-3.

Clock Source Refers to which clock samples STi and which clock outputs STo; STi applies when STio is input; STo applies when STio is output.

Table 7 - ZL50020 Operating Modes

11.1 Divided Clock Mode Operation

When the device is in Divided Clock mode, STio0 - 31 are driven by CKi. In this mode, the output streams and clocks have the same amount of jitter as the input clock (CKi), but the output data rate cannot exceed the input data rate defined by CKi. For example, if CKi is 4.096 MHz, the input and output data rate cannot be higher than 2.048 Mbps, and the generated output clock rates cannot exceed 4.096 MHz.

11.2 Multiplied Clock Mode Operation

When the device is in Multiplied Clock mode, device hardware is used to multiply CKi internally. STio0 - are driven by this internally generated clock. In this mode, the output clocks and data can run at any of the specified rates, but they may have different jitter characteristics from the input clock (CKi). The input data rates are still limited by the CKi rate (as per Table 1), as input data are always sampled directly by CKi.

11.3 Output Clock Frequencies

The device can generate a limited number of clock and frame pulse output signals. All signals are synchronous to each other and are locked to the input CKi and FPi. The device can provide outputs with the following frequencies, with the exception that when in Divided Clock mode, the output clock rate cannot exceed the input CKi rate.

CKo0	4.096 MHz
CKo1	8.192 MHz
CKo2	16.384 MHz
CKo3	4.096 MHz, 8.192 MHz, 16.384 MHz or 32.768 MHz
FPo0	8 kHz (244 ns wide pulse)
FPo1	8 kHz (122 ns wide pulse)
FPo2	8 kHz (61 ns wide pulse)
FPo3	8 kHz (244 ns, 122 ns, 61 ns or 30 ns wide pulse)

Table 8 - Generated Output Frequencies

12.0 Microprocessor Port

The device provides access to the internal registers, connection memories and data memories via the microprocessor port. The microprocessor port is capable of supporting both Motorola and Intel non-multiplexed microprocessors. The microprocessor port consists of a 16-bit parallel data bus (D15 - 0), 14 bit address bus (A13 - 0) and six control signals (MOT_INTEL, $\overline{CS}$, $\overline{DS}$_$\overline{RD}$, R/$\overline{W}$_$\overline{WR}$ and $\overline{DTA}$_RDY).

The data memory can only be read from the microprocessor port. For a data memory read operation, D7 - 0 will be used and D15 - 8 will output zeros.

For a CM_L read or write operation, all bits (D15 - 0) of the data bus will be used. For a CM_H write operation, D4 - 0 of the data bus must be configured and D15 - 5 are ignored. D15 - 5 must be driven either high or low. For a CM_H read operation, D4 - 0 will be used and D15 - 5 will output zeros.

Refer to Figure 20 on page 63, Figure 21 on page 64, Figure 22 on page 65 and Figure 23 on page 66 for the microprocessor timing.

13.0 Device Reset and Initialization

The $\overline{RESET}$ pin is used to reset the ZL50020. When this pin is low, the following functions are performed:

- synchronously puts the microprocessor port in a reset state
- tristates the STio0 - 31 outputs
- drives the STOHZ0 - 15 outputs to high
- preloads all internal registers with their default values (refer to the individual registers for default values)
- clears all internal counters

13.1 Power-up Sequence

The recommended power-up sequence is for the V_{DD_IO} supply (normally +3.3 V) to be established before the power-up of the V_{DD_CORE} supply (normally +1.8 V). The V_{DD_CORE} supply may be powered up at the same time as V_{DD_IO}, but should not “lead” the V_{DD_IO} supply by more than 0.3 V.

13.2 Device Initialization on Reset

Upon power up, the ZL50020 should be initialized as follows:

- Set the ODE pin to low to disable the STio0 - 31 outputs and to drive STOHZ0 - 15 to high
- Set the $\overline{TRST}$ pin to low to disable the JTAG TAP controller
- Reset the device by pulsing the $\overline{RESET}$ pin to zero for longer than 1 μs
- After releasing the $\overline{RESET}$ pin from low to high, wait for a certain period of time (see Note below) for the device to stabilize from the power down state before the first microprocessor port access can occur
- Program CKIN1 - 0 (bit 6 -5) in the Control Register (CR) to define the frequency of the CKi and FPi inputs
- Wait at least 500 μs prior to the next microport access (see Note below)
- Use the block programming mode to initialize the connection memory
- Release the ODE pin from low to high after the connection memory is programmed

Note: If CKi is 16.384 MHz, the waiting time is 500 μs; if CKi is 8.192 MHz, the waiting time is 1 ms; if CKi is 4.096 MHz, the waiting time is 2 ms.

13.3 Software Reset

In addition to the hardware reset from the $\overline{\text{RESET}}$ pin, the device can also be reset by using software reset SRSTSW (bit 1) in the Software Reset Register (SRR).

14.0 Pseudo Random Bit Generation and Error Detection

The ZL50020 has one Bit Error Rate (BER) transmitter and one BER receiver for each pair of input and output streams, resulting in 32 transmitters connected to the output streams and 32 receivers associated with the input streams. Each transmitter can generate a BER sequence with a pattern of 2^{15}-1 pseudorandom code (ITU O.151). Each transmitter can start at any location on the stream and will last for a minimum of 1 channel to a maximum of 1 frame time (125 μs). The BER receivers and transmitters are enabled by programming the RBEREN (bit 5) and TBEREN (bit 4) in the IMS register. In order to save power, the 32 transmitters and/or receivers can be disabled. (This is the default state.)

Multiple connection memory locations can be programmed for BER tests such that the BER patterns can be transmitted for multiple consecutive output channels. If consecutive input channels are not selected, the BER receiver will not compare the bit patterns correctly. The number of output channels which the BER pattern occupies has to be the same as the number of channels defined in the BER Length Register (BRLR) which defines how many BER channels are to be monitored by the BER receiver.

For each input stream, there is a set of registers for the BER test. The registers are as follows:

- BER Receiver Control Register (**BRCR**) - ST[n]CBER (bit 1) is used to clear the Bit Receiver Error Register (BRER). ST[n]SBER (bit 0) is used to enable the per-stream BER receiver.
- BER Receiver Start Register (**BRSR**) - ST[n]BRS7 - 0 (bit 7 - 0) defines the input channel from which the BER sequence will start to be compared.
- BER Receiver Length Register (**BRLR**) - ST[n]BL8 - 0 (bit 8 - 0) define how many channels the sequence will last. Depending on the data rate being used, the BER test can last for a maximum of 32, 64, 128 or 256channels at the data rates of 2.048, 4.096, 8.192or 16.384Mbps, respectively. The minimum length of the BER test is a single channel. The user must take care to program the correct channel length for the BER test so that the channel length does not exceed the total number of channels available in the stream.
- BER Receiver Error Register (**BRER**) - This read-only register contains the number of counted errors. When the error count reaches 0xFFFF, the BER counter will stop updating so that it will not overflow. ST[n]CBER (bit 1) in the BER Receiver Control Register is used to reset the BRER register.

For normal BER operation, CMM (bit 0) must be 1 in the Connection Memory Low (CM_L). PCC1 - 0 (bits 2 - 1) in the Connection Memory Low must be programmed to “10” to enable the per-stream based BER transmitters. For each stream, the length (or total number of channels) of BER testing can be as long as one whole frame, but the channels MUST be consecutive. Upon completion of programming the connection memory, the corresponding BER receiver can be started by setting ST[n]SBER (bit 0) in the BRCR to high. There must be at least 2 frames (250 μs) between completion of connection memory programming and starting the BER receiver before the BER receiver can correctly identify BER errors. A 16 bit BER counter is used to count the number of bit errors.

15.0 PCM A-law/μ-law Translation

The ZL50020 provides per-channel code translation to be used to adapt pulse code modulation (PCM) voice or data traffic between networks which use different encoding laws. Code translation is valid in both Connection Mode and Message Mode.

In order to use this feature, the Connection Memory High (CM_H) entry for the output channel must be programmed. $\overline{V}$/D (bit 4) defines if the traffic in the channel is voice or data. Setting ICL1 - 0 (bits 3 - 2) programs the input coding law and OCL1 - 0 (bits 1- 0) programs the output coding law as shown in Table 9.

The different code options are:

Input Coding (ICL1- 0)	Output Coding (OCL1 - 0)	Voice Coding ($\overline{V}$/D bit = 0)	Data Coding ($\overline{V}$/D bit = 1)
00	00	ITU-T G.711 A-law	No code
01	01	ITU-T G.711 μ-law	Alternate Bit Inversion (ABI)
10	10	A-law without Alternate Bit Inversion (ABI)	Inverted Alternate Bit Inversion (ABI)
11	11	μ-law without Magnitude Inversion (MI)	All bits inverted

Table 9 - Input and Output Voice and Data Coding

For voice coding options, the ITU-T G.711 A-law and ITU-T G.711 μ-law are the standard rules for encoding. A-law without Alternate Bit Inversion (ABI) is an alternative code that does not invert the even bits (6, 4, 2, 0). μ-law without Magnitude Inversion (MI) is an alternative code that does not perform inversion of magnitude bits (6, 5, 4, 3, 2, 1, 0).

When transferring data code, the option “no code” does not invert the bits. The Alternate Bit Inversion (ABI) option inverts the even bits (6, 4, 2, 0) while the Inverted Alternate Bit Inversion (ABI) inverts the odd bits (7, 5, 3, 1). When the “All bits inverted” option is selected, all of the bits (7, 6, 5, 4, 3, 2, 1, 0) are inverted.

The input channel and output channel encoding law are configured independently. If the output channel coding is set to be different from the input channel, the ZL50020 performs translation between the two standards. If the input and output encoding laws are set to the same standard, no translation occurs. As the $\overline{V}$/D (bit 4) of the Connection Memory High (CM_H) must be set on a per-channel basis, it is not possible to translate between voice and data encoding laws.

16.0 Quadrant Frame Programming

By programming the Stream Input Quadrant Frame Registers (SIQFR0 - 31), users can divide one frame of input data into four quadrant frames and can force the LSB or MSB of every input channel in these quadrants to one or zero for robbed-bit signaling. The four quadrant frames are defined as follows:

Data Rate	Quadrant 0	Quadrant 1	Quadrant 2	Quadrant 3
2.048 Mbps	Channel 0 - 7	Channel 8 - 15	Channel 16 - 23	Channel 24 - 31
4.096 Mbps	Channel 0 - 15	Channel 16 - 31	Channel 32 - 47	Channel 48 - 63
8.192 Mbps	Channel 0 - 31	Channel 32 - 63	Channel 64 - 95	Channel 96 - 127
16.384 Mbps	Channel 0 - 63	Channel 64 - 127	Channel 128 - 191	Channel 192 - 255

Table 10 - Definition of the Four Quadrant Frames

When the quadrant frame control bits, STIN[n]Q3C2 - 0 (bit 11 - 9), STIN[n]Q2C2 - 0 (bit 8 - 6), STIN[n]Q1C2 - 0 (bit 5 - 3) or STIN[n]Q1C2 - 0 (bit 2 - 0), are set, the LSB or MSB of every input channel in the quadrant is forced to “1” or “0” as shown by the following table:

STIN[n]Q[y]C[2:0]	Action
0xx	Normal Operation
100	Replaces LSB of every channel in Quadrant y with ‘0’
101	Replaces LSB of every channel in Quadrant y with ‘1’
110	Replaces MSB of every channel in Quadrant y with ‘0’
111	Replaces MSB of every channel in Quadrant y with ‘1’
Note: y = 0, 1, 2, 3	

Table 11 - Quadrant Frame Bit Replacement

Note that Quadrant Frame Programming and BER reception cannot be used simultaneously on the same input stream.

17.0 JTAG Port

The JTAG test port is implemented to meet the mandatory requirements of the IEEE-1149.1 (JTAG) standard. The operation of the boundary-scan circuitry is controlled by an external Test Access Port (TAP) Controller.

17.1 Test Access Port (TAP)

The Test Access Port (TAP) accesses the ZL50020 test functions. It consists of three input pins and one output pin as follows:

- **Test Clock Input (TCK)** - TCK provides the clock for the test logic. TCK does not interfere with any on-chip clock and thus remains independent in the functional mode. TCK permits shifting of test data into or out of the Boundary-Scan register cells concurrently with the operation of the device and without interfering with the on-chip logic.
- **Test Mode Selection Inputs (TMS)** - The TAP Controller uses the logic signals received at the TMS input to control test operations. The TMS signals are sampled at the rising edge of the TCK pulse. This pin is internally pulled to high when it is not driven from an external source.
- **Test Data Input (TDi)** - Serial input data applied to this port is fed either into the instruction register or into a test data register, depending on the sequence previously applied to the TMS input. The registers are described in a subsequent section. The received input data is sampled at the rising edge of the TCK pulse. This pin is internally pulled to high when it is not driven from an external source.
- **Test Data Output (TDo)** - Depending on the sequence previously applied to the TMS input, the contents of either the instruction register or test data register are serially shifted out towards TDo. The data from TDo is clocked on the falling edge of the TCK pulses. When no data is shifted through the boundary scan cells, the TDo driver is set to a high impedance state.
- **Test Reset ($\overline{\text{TRST}}$)** - Resets the JTAG scan structure. This pin is internally pulled to high when it is not driven from an external source.

17.2 Instruction Register

The ZL50020 uses the public instructions defined in the IEEE-1149.1 standard. The JTAG interface contains a four-bit instruction register. Instructions are serially loaded into the instruction register from the TDi when the TAP Controller is in its shifted-OR state. These instructions are subsequently decoded to achieve two basic functions: to select the test data register that may operate while the instruction is current and to define the serial test data register path that is used to shift data between TDi and TDo during data register scanning.

17.3 Test Data Registers

As specified in the IEEE-1149.1 standard, the ZL50020 JTAG interface contains three test data registers:

- **The Boundary-Scan Register** - The Boundary-Scan register consists of a series of boundary-scan cells arranged to form a scan path around the boundary of the ZL50020 core logic.
- **The Bypass Register** - The Bypass register is a single stage shift register that provides a one-bit path from TDi to TDo.
- **The Device Identification Register** - The JTAG device ID for the ZL50020 is $0C36414B_H$

Version	<31:28>	0000
Part Number	<27:12>	1100 0011 0110 0100
Manufacturer ID	<11:1>	0001 0100 101
LSB	<0>	1

17.4 BSDL

A Boundary Scan Description Language (BSDL) file is available from Zarlink Semiconductor to aid in the use of the IEEE-1149.1 test interface.

18.0 Register Address Mapping

Address A13 - A0	CPU Access	Register Name	Abbreviation	Reset By
0000_H	R/W	Control Register	CR	Switch/Hardware
0001_H	R/W	Internal Mode Selection Register	IMS	Switch/Hardware
0002_H	R/W	Software Reset Register	SRR	Hardware Only
0003_H	R/W	Output Clock and Frame Pulse Control Register	OCFCR	Hardware
0004_H	R/W	Output Clock and Frame Pulse Selection Register	OCFSR	Hardware
0005_H	R/W	FPo_OFF0 Register	FPOFF0	Hardware
0006_H	R/W	FPo_OFF1 Register	FPOFF1	Hardware
0007_H	R/W	FPo_OFF2 Register	FPOFF2	Hardware
0010_H	R Only	Internal Flag Register	IFR	Switch/Hardware
0011_H	R Only	BER Error Flag Register 0	BERFR0	Switch/Hardware
0012_H	R Only	BER Error Flag Register 1	BERFR1	Switch/Hardware
0013_H	R Only	BER Receiver Lock Register 0	BERLR0	Switch/Hardware
0014_H	R Only	BER Receiver Lock Register 1	BERLR1	Switch/Hardware
0100_H - $011F_H$	R/W	Stream Input Control Registers 0 - 31	SICR0 - 31	Switch/Hardware
0120_H - $013F_H$	R/W	Stream Input Quadrant Frame Registers 0 - 31	SIQFR0 - 31	Switch/Hardware
0200_H - $021F_H$	R/W	Stream Output Control Registers 0 - 31	SOCR0 - 31	Switch/Hardware
0300_H - $031F_H$	R/W	BER Receiver Start Registers 0 - 31	BRSR0 - 31	Switch/Hardware
0320_H - $033F_H$	R/W	BER Receiver Length Registers 0 - 31	BRLR0 - 31	Switch/Hardware
0340_H - $035F_H$	R/W	BER Receiver Control Registers 0 - 31	BRCR0 - 31	Switch/Hardware
0360_H - $037F_H$	R Only	BER Receiver Error Registers 0 - 31	BRER0 - 31	Switch/Hardware

Table 12 - Address Map for Registers (A13 = 0)

19.0 Detailed Register Description

External Read/Write Address: 0000_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	OPM	0	FPIN POS	CKINP	FPINP	CKIN 1	CKIN 0	VAR EN	MBPE	OSB	MS1	MS0

Bit	Name	Description
15 - 12	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
11	OPM	**Operation Mode.** This bit is used to set the device in Master/Slave operation. Refer to Table 7, “ZL50020 Operating Modes” on page 32 for more details.
10	Unused	**Reserved.** In normal functional mode, this bits **MUST** be set to zero.
9	FPINPOS	**Input Frame Pulse (FPi) Position** When this bit is low, FPi straddles frame boundary (as defined by ST-BUS). When this bit is high, FPi starts from frame boundary (as defined by GCI-Bus)
8	CKINP	**Clock Input (CKi) Polarity** When this bit is low, the CKi falling edge aligns with the frame boundary. When this bit is high, the CKi rising edge aligns with the frame boundary.
7	FPINP	**Frame Pulse Input (FPi) Polarity** When this bit is low, the input frame pulse FPi has the negative frame pulse format. When this bit is high, the input frame pulse FPi has the positive frame pulse format.
6 - 5	CKIN1 - 0	**Input Clock (CKi) and Frame Pulse (FPi) Selection** CKIN1 - 0 / FPi Active Period / CKi 00 / 61 ns / 16.384 MHz 01 / 122 ns / 8.192 MHz 10 / 244 ns / 4.096 MHz 11 / Reserved The MODE_4M0 and MODE_4M1 pins, as described in “Pin Description” on page 10, should also be set to define the input clock mode.
4	VAREN	**Variable Delay Mode Enable** When this bit is low, the variable delay mode is disabled on a device-wide basis. When this bit is high, the variable delay mode is enabled on a device-wide basis.
3	MBPE	**Memory Block Programming Enable** When this bit is high, the connection memory block programming mode is enabled to program the connection memory. When it is low, the memory block programming mode is disabled.

Table 13 - Control Register (CR) Bits

External Read/Write Address: 0000_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	OPM	0	FPIN POS	CKINP	FPINP	CKIN 1	CKIN 0	VAR EN	MBPE	OSB	MS1	MS0

Bit	Name	Description
2	OSB	**Output Stand By Bit:** This bit enables the STio0 - 31 and the STOHZ0 -15 serial outputs. The following table describes the HiZ control of the serial data outputs: $\overline{\text{RESET}}$ Pin / SRSTSW (in SRR) / ODE Pin / OSB Bit / STio0 - 31 / STOHZ0 - 15 0 / X / X / X / HiZ / Driven High 1 / 1 / X / X / HiZ / Driven High 1 / 0 / 0 / X / HiZ / Driven High 1 / 0 / 1 / 0 / HiZ / Driven High 1 / 0 / 1 / 1 / Active (Controlled by CM) / Active (Controlled by CM) Note: Unused output streams are tristated (STio = HiZ, STOHZ = Driven High). Refer to SOCR0 - 31 (bit2 - 0).
1 - 0	MS1 - 0	**Memory Select Bits** These two bits are used to select connection memory low, connection high or data memory for access by CPU: MS1 - 0 / Memory Selection 00 / Connection Memory Low Read/Write 01 / Connection Memory High Read/Write 10 / Data Memory Read 11 / Reserved

Table 13 - Control Register (CR) Bits (continued)

External Read/Write Address: 0001_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	STIO_ PD_EN	BDH	BDL	RBER EN	TBER EN	BPD 2	BPD 1	BPD 0	MBPS

Bit	Name	Description
15 - 9	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
8	STIO_PD_ EN	**STio Pull-down Enable** When this bit is low, the pull-down resistors on all STio pads will be disabled. When this bit is high, the pull-down resistors on all STio pads will be enabled.
7	BDH	**Bi-directional Control for Streams 16-31** **BDH** — **STio16 - 31 Operation** 0 — normal operation: STi16-31 are inputs, STio16-31 are outputs 1 — bi-directional operation: STi16-31 tied low internally, STio16-31 are bi-directional
6	BDL	**Bi-directional Control for Streams 0-15** **BDL** — **STio0 - 15 Operation** 0 — normal operation: STi0-15 are inputs, STio0-15 are outputs 1 — bi-directional operation: STi0-15 tied low internally, STio0-15 are bi-directional
5	RBEREN	**PRBS Receiver Enable** When this bit is low, all the BER receivers are disabled. To enable any BER receivers, this bit **MUST** be high.
4	TBEREN	**PRBS Transmitter Enable** When this bit is low, all the BER transmitters are disabled. To enable any BER transmitters, this bit **MUST** be high.

Table 14 - Internal Mode Selection Register (IMS) Bits

External Read/Write Address: 0001_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	STIO_ PD_EN	BDH	BDL	RBER EN	TBER EN	BPD 2	BPD 1	BPD 0	MBPS

Bit	Name	Description
3 - 1	BPD2 - 0	**Block Programming Data** These bits refer to the value to be loaded into the connection memory, whenever the memory block programming feature is activated. After the MBPE bit in the Control Register is set to high and the MBPS bit in this register is set to high, the contents of the bits BPD2 - 0 are loaded into bits 2 - 0 of the Connection Memory Low. Bits 15 - 3 of the Connection Memory Low and bits 15 - 0 of Connection Memory High are zeroed.
0	MBPS	**Memory Block Programming Start:** A zero to one transition of this bit starts the memory block programming function. The MBPS and BPD2 - 0 bits in this register must be defined in the same write operation. Once the MBPE bit in the Control Register is set to high, the device requires two frames to complete the block programming. After the programming function has finished, the MBPS bit returns to low, indicating the operation is completed. When MBPS is high, MBPS or MBPE can be set to low to abort the programming operation. Whenever the microprocessor writes a one to the MBPS bit, the block programming function is started. As long as this bit is high, the user must maintain the same logical value to the other bits in this register to avoid any change in the device setting.

Table 14 - Internal Mode Selection Register (IMS) Bits (continued)

External Read/Write Address: 0002_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	SRST SW	0

Bit	Name	Description
15 - 2	Unused	**Reserved** In normal functional mode, these bits **MUST** be set to zero.
1	SRSTSW	**Software Reset Bit for Switch** When this bit is low, switching blocks are in normal operation. When this bit is high, switching blocks are in software reset state. Refer to Table 12, “Address Map for Registers (A13 = 0)” on page 32 for details regarding which registers are affected.
0	Unused	**Reserved** In normal functional mode, these bits **MUST** be set to zero.

Table 15 - Software Reset Register (SRR) Bits

External Read/Write Address: 0003_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	FPOF2 EN	FPOF1 EN	FPOF0 EN	0	0	CKO FPO3 EN	CKO FPO2 EN	CKO FPO1 EN	CKO FPO0 EN

Bit	Name	Description
15 - 9	Unused	**Reserved** In normal functional mode, these bits **MUST** be set to zero.
8	FPOF2EN	**FPo_OFF2 Enable** When this bit is high, output frame pulse FPo_OFF2 When this bit is low, output frame pulse FPo_OFF2.
7	FPOF1EN	**FPo_OFF1 Enable** When this bit is high, output frame pulse FPo_OFF1 is enabled. When this bit is low, output frame pulse FPo_OFF1 is in high impedance state.
6	FPOF0EN	**FPo_OFF0 Enable** When this bit is high, output frame pulse FPo_OFF0 is enabled. When this bit is low, output frame pulse FPo_OFF0 is in high impedance state.
5	Unused	**Reserved** In normal functional mode, these bits **MUST** be set to zero.
4	Unused	**Reserved** In normal functional mode, these bits **MUST** be set to zero.
3	CKOFPO3 EN	**CKo3 and FPo3 Enable** When this bit is high, output clock CKo3 and output frame pulse FPo3 are enabled. When this bit is low, CKo3 and FPo3 are in high impedance state.
2	CKOFPO2 EN	**CKo2 and FPo2 Enable** When this bit is high, output clock CKo2 and output frame pulse FPo2 are enabled. When this bit is low, CKo2 and FPo2 are in high impedance state.
1	CKOFPO1 EN	**CKo1 and FPo1 Enable** When this bit is high, output clock CKo1 and output frame pulse FPo1 are enabled. When this bit is low, CKo1 and FPo1 are in high impedance state.
0	CKOFPO0 EN	**CKo0 and FPo0 Enable** When this bit is high, output clock CKo0 and output frame pulse FPo0 are enabled. When this bit is low, CKo0 and FPo0 are in high impedance state.

Table 16 - Output Clock and Frame Pulse Control Register (OCFCR) Bits

External Read/Write Address: 0004_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	CKO FPO3 SEL1	CKO FPO3 SEL0	CKO3 P	FPO3 P	FPO3 POS	CKO2 P	FPO2 P	FPO2 POS	CKO1 P	FPO1 P	FPO1 POS	CKO0 P	FPO0 P	FPO0 POS

Bit	Name	Description
15 - 14	Unused	**Reserved** In normal functional mode, these bits **MUST** be set to zero.
13 - 12	CKOFPO3 SEL1 - 0	**Output Clock (CKo3) Frequency and Output Frame Pulse (FPo3) Pulse Cycle Selection** CKOFPO3 SEL1 - 0 / FPo3 / CKo3 00 / 244 ns / 4.096 MHz 01 / 122 ns / 8.192 MHz 10 / 61 ns / 16.384 MHz 11 / 30 ns / 32.768 MHz
11	CKO3P	**Output Clock (CKo3) Polarity Selection** When this bit is low, the output clock CKo3 falling edge aligns with the frame boundary. When this bit is high, the output clock CKo3 rising edge aligns with the frame boundary.
10	FPO3P	**Output Frame Pulse (FPo3) Polarity Selection** When this bit is low, the output frame pulse FPo3 has the negative frame pulse format. When this bit is high, the output frame pulse FPo3 has the positive frame pulse format.
9	FPO3POS	**Output Frame Pulse (FPo3) Position** When this bit is low, FPo3 straddles frame boundary (as defined by ST-BUS). When this bit is high, FPo3 starts from frame boundary (as defined by GCI-Bus).
8	CKO2P	**Output Clock (CKo2) Polarity Selection** When this bit is low, the output clock CKo2 falling edge aligns with the frame boundary. When this bit is high, the output clock CKo2 rising edge aligns with the frame boundary.
7	FPO2P	**Output Frame Pulse (FPo2) Polarity Selection** When this bit is low, the output frame pulse FPo2 has the negative frame pulse format. When this bit is high, the output frame pulse FPo2 has the positive frame pulse format.
6	FPO2POS	**Output Frame Pulse (FPo2) Position** When this bit is low, FPo2 straddles frame boundary (as defined by ST-BUS). When this bit is high, FPo2 starts from frame boundary (as defined by GCI-Bus).

Table 17 - Output Clock and Frame Pulse Selection Register (OCFSR) Bits

External Read/Write Address: 0004_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	CKO FPO3 SEL1	CKO FPO3 SEL0	CKO3 P	FPO3 P	FPO3 POS	CKO2 P	FPO2 P	FPO2 POS	CKO1 P	FPO1 P	FPO1 POS	CKO0 P	FPO0 P	FPO0 POS

Bit	Name	Description
5	CKO1P	**Output Clock (CKo1) Polarity Selection** When this bit is low, the output clock CKo1 falling edge aligns with the frame boundary. When this bit is high, the output clock CKo1 rising edge aligns with the frame boundary.
4	FPO1P	**Output Frame Pulse (FPo1) Polarity Selection** When this bit is low, the output frame pulse FPo1 has the negative frame pulse format. When this bit is high, the output frame pulse FPo1 has the positive frame pulse format.
3	FPO1POS	**Output Frame Pulse (FPo1) Position** When this bit is low, FPo1 straddles frame boundary (as defined by ST-BUS). When this bit is high, FPo1 starts from frame boundary (as defined by GCI-Bus).
2	CKO0P	**Output Clock (CKo0) Polarity Selection** When this bit is low, the output clock CKo0 falling edge aligns with the frame boundary. When this bit is high, the output clock CKo0 rising edge aligns with the frame boundary.
1	FPO0P	**Output Frame Pulse (FPo0) Polarity Selection** When this bit is low, the output frame pulse FPo0 has the negative frame pulse format. When this bit is high, the output frame pulse FPo0 has the positive frame pulse format.
0	FPO0POS	**Output Frame Pulse (FPo0) Position** When this bit is low, FPo0 straddles frame boundary (as defined by ST-BUS). When this bit is high, FPo0 starts from frame boundary (as defined by GCI-Bus).

Note: In Divided Clock modes, CKo3 - 1 cannot exceed frequency of CKi.

Table 17 - Output Clock and Frame Pulse Selection Register (OCFSR) Bits (continued)

External Read/Write Address: 0005_H - 0007_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	FOF[n] OFF7	FOF[n] OFF6	FOF[n] OFF5	FOF[n] OFF4	FOF[n] OFF3	FOF[n] OFF2	FOF[n] OFF1	FOF[n] OFF0	FOF[n] C1	FOF[n] C0

Bit	Name	Description
15 - 10	Unused	**Reserved.** In normal functional mode, these bits **MUST** be set to zero.
9 - 2	FOF[n]OFF7 - 0	**FPo_OFF[n] Channel Offset** The binary value of these bits refers to the channel offset from original frame boundary. Permitted channel offset values depend on bits 1-0 of this register.
1 - 0	FOF[n]C1 - 0	**FPo_OFF[n] Control bits**

FOF[n]C 1-0	Data Rate (Mbps)	FPo_OFF[n] Pulse Cycle Width	FOF[n]OFF7 - 0 Permitted Channel Offset	Polarity Control	Position Control
00	2.048	one 4.096 MHz clock	0 - 31	FPO0P	FPO0POS
01	4.096	one 8.192 MHz clock	0 - 63	FPO1P	FPO1POS
10	8.192	one 16.384 MHz clock	0 - 127	FPO2P	FPO2POS
11	16.384	one 16.384 MHz clock	0 - 255	FPO2P	FPO2POS

Note: [n] denotes output offset frame pulse from 0 to 2.

Table 18 - FPo_OFF[n] Register (FPo_OFF[n]) Bits

External Read Address: 0010_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	OUT ERR	IN ERR

Bit	Name	Description
15 - 2	Unused	**Reserved** In normal functional mode, these bits are zero.
1	OUTERR	**Output Error (Read Only)** This bit is set high when the total number of output channels is programmed to be more than the maximum capacity of 2048, in which case the output channels beyond the maximum capacity should be disabled. This bit will be cleared automatically after programming is corrected.
0	INERR	**Input Error (Read Only)** This bit is set high when the total number of input channels is programmed to be more than the maximum capacity of 2048, in which case the input channels beyond the maximum capacity should be disabled.This bit will be cleared automatically after programming is corrected.

Table 19 - Internal Flag Register (IFR) Bits - Read Only

External Read Address: 00011_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BER F15	BER F14	BER F13	BER F12	BER F11	BER F10	BER F9	BER F8	BER F7	BER F6	BER F5	BER F4	BER F3	BER F2	BER F1	BER F0

Bit	Name	Description
15 - 0	BERF[n]	**BER Error Flag[n]:** If BERF[n] is high, it indicates that BER Receiver Error Register [n] (BRER[n]) is not zero. If BERF[n] is low, it indicates that BER Receiver Error Register [n] (BRER[n]) is zero.

Note: [n] denotes input stream from 0 - 15.

Table 20 - BER Error Flag Register 0 (BERFR0) BIts - Read Only

External Read/Write Address: 00012_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BER F31	BER F30	BER F29	BER F28	BER F27	BER F26	BER F25	BER F24	BER F23	BER F22	BER F21	BER F20	BER F19	BER F18	BER F17	BER F16

Bit	Name	Description
15 - 0	BERF[n]	**BER Error Flag[n]:** If BERF[n] is high, it indicates that BER Receiver Error Register [n] (BRER[n]) is not zero. If BERF[n] is low, it indicates that BER Receiver Error Register [n] (BRER[n]) is zero.
Note: [n] denotes input stream from 16 - 31.		

Table 21 - BER Error Flag Register 1 (BERFR1) Bits - Read Only

External Read Address: 00013_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BER L15	BER L14	BER L13	BER L12	BER L11	BER L10	BER L9	BER L8	BER L7	BER L6	BER L5	BER L4	BER L3	BER L2	BER L1	BER L0

Bit	Name	Description
15 - 0	BERL[n]	**BER Receiver Lock[n]** If BERL[n] is high, it indicates that BER Receiver of STi[n] is locked. If BERL[n] is low, it indicates that BER Receiver of STi[n] is not locked.
Note: [n] denotes input stream from 0 - 15.		

Table 22 - BER Receiver Lock Register 0 (BERLR0) Bits - Read Only

External Read Address: 00014_H
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BER L31	BER L30	BER L29	BER L28	BER L27	BER L26	BER L25	BER L24	BER L23	BER L22	BER L21	BER L20	BER L19	BER L18	BER L17	BER L16

Bit	Name	Description
15 - 0	BERL[n]	**BER Receiver Lock[n]:** If BERL[n] is high, it indicates that BER Receiver of STi[n] is locked. If BERL[n] is low, it indicates that BER Receiver of STi[n] is not locked.
Note: [n] denotes input stream from 16 - 31.		

Table 23 - BER Receiver Lock Register 1 (BERLR1) Bits - Read Only

External Read/Write Address: 0100_H - $011F_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	STIN[n] BD2	STIN[n] BD1	STIN[n] BD0	STIN[n] SMP1	STIN[n] SMP0	STIN[n] DR3	STIN[n] DR2	STIN[n] DR1	STIN[n] DR0

Bit	Name	Description
15 - 9	Unused	**Reserved** In normal functional mode, these bits **MUST** be set to zero.
8 - 6	STIN[n]BD2 - 0	**Input Stream[n] Bit Delay Bits.** The binary value of these bits refers to the number of bits that the input stream will be delayed relative to FPi. The maximum value is 7. Zero means no delay.
5 - 4	STIN[n]SMP1 - 0	**Input Data Sampling Point Selection Bits**

STIN[n]SMP1-0	Sampling Point (2.048 Mbps, 4.096 Mbps, 8.192 Mbps streams)	Sampling Point (16.384 Mbps streams)
00	3/4 point	2/4 point
01	1/4 point	
10	2/4 point	4/4 point
11	4/4 point	

Table 24 - Stream Input Control Register 0 - 31 (SICR0 - 31) Bits

External Read/Write Address: 0100_H - $011F_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	STIN[n] BD2	STIN[n] BD1	STIN[n] BD0	STIN[n] SMP1	STIN[n] SMP0	STIN[n] DR3	STIN[n] DR2	STIN[n] DR1	STIN[n] DR0

Bit	Name	Description
3 - 0	STIN[n]DR3 - 0	**Input Data Rate Selection Bits:**

STIN[n]DR3-0	Data Rate
0000	Stream Unused
0001	2.048 Mbps
0010	4.096 Mbps
0011	8.192 Mbps
0100	16.384 Mbps
0101 - 1111	Reserved

Note: [n] denotes input stream from 0 - 31.

Table 24 - Stream Input Control Register 0 - 31 (SICR0 - 31) Bits (continued)

External Read/Write Address: 0120_H - $013F_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	STIN[n] Q3C2	STIN[n] Q3C1	STIN[n] Q3C0	STIN[n] Q2C2	STIN[n] Q2C1	STIN[n] Q2C0	STIN[n] Q1C2	STIN[n] Q1C1	STIN[n] Q1C0	STIN[n] Q0C2	STIN[n] Q0C1	STIN[n] Q0C0

Bit	Name	Description
15 - 12	Unused	**Reserved** In normal functional mode, these bits **MUST** be set to zero.
11 - 9	STIN[n]Q3C2 - 0	**Quadrant Frame 3 Control Bits** These three bits are used to control STi[n]'s quadrant frame 3, which is defined as Ch24 to 31, Ch48 to 63, Ch96 to 127 and Ch192 to 255 for the 2.048 Mbps, 4.096 Mbps, 8.192 Mbps, and 16.384 Mbps modes respectively. STIN[n]Q3C 2-0 — Operation 0xx — normal operation 100 — LSB of each channel is replaced by "0" 101 — LSB of each channel is replaced by "1" 110 — MSB of each channel is replaced by "0" 111 — MSB of each channel is replaced by "1"
8 - 6	STIN[n]Q2C2 - 0	**Quadrant Frame 2 Control Bits** These three bits are used to control STi[n]'s quadrant frame 2, which is defined as Ch16 to 23, Ch32 to 47, Ch64 to 95 and Ch128 to 191 for the 2.048 Mbps, 4.096 Mbps 8.192 Mbps, and 16.384 Mbps modes respectively. STIN[n]Q2C 2-0 — Operation 0xx — normal operation 100 — LSB of each channel is replaced by "0" 101 — LSB of each channel is replaced by "1" 110 — MSB of each channel is replaced by "0" 111 — MSB of each channel is replaced by "1"

Table 25 - Stream Input Quadrant Frame Register 0 - 31 (SIQFR0 - 31) Bits

External Read/Write Address: 0120_H - $013F_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	STIN[n] Q3C2	STIN[n] Q3C1	STIN[n] Q3C0	STIN[n] Q2C2	STIN[n] Q2C1	STIN[n] Q2C0	STIN[n] Q1C2	STIN[n] Q1C1	STIN[n] Q1C0	STIN[n] Q0C2	STIN[n] Q0C1	STIN[n] Q0C0

Bit	Name	Description
5 - 3	STIN[n]Q1C2 - 0	**Quadrant Frame 1 Control Bits** these three bits are used to control STi[n]'s quadrant frame 1, which is defined as Ch8 to 15, Ch16 to 31, Ch32 to 63 and Ch64 to 127 for the 2.048 Mbps, 4.096 Mbps, 8.192 Mbps, and 16.384 Mbps modes respectively. STIN[n]Q1C 2-0 / Operation 0xx: normal operation 100: LSB of each channel is replaced by "0" 101: LSB of each channel is replaced by "1" 110: MSB of each channel is replaced by "0" 111: MSB of each channel is replaced by "1"
2 - 0	STIN[n]Q0C2 - 0	**Quadrant Frame 0 Control Bits** These three bits are used to control STi[n]'s quadrant frame 0, which is defined as Ch0 to 7, Ch0 to 15, Ch0 to 31 and Ch0 to 63 for the 2.048 Mbps, 4.096 Mbps, 8.192 Mbps, and 16.384 Mbps modes respectively. STIN[n]Q0C2-0 / Operation 0xx: normal operation 100: LSB of each channel is replaced by "0" 101: LSB of each channel is replaced by "1" 110: MSB of each channel is replaced by "0" 111: MSB of each channel is replaced by "1"

Note: [n] denotes input stream from 0 - 31.

Table 25 - Stream Input Quadrant Frame Register 0 - 31 (SIQFR0 - 31) Bits (continued)

External Read/Write Address: 0200_H - $021F_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	STOHZ [n]A2	STOHZ [n]A1	STOHZ [n]A0	STO[n] FA1	STO[n] FA0	STO[n] AD2	STO[n] AD1	STO[n] AD0	STO[n] DR3	STO[n] DR2	STO[n] DR1	STO[n] DR0

Bit	Name	Description
15 - 12	Unused	**Reserved** In normal functional mode, these bits **MUST** be set to zero.
11 - 9	STOHZ[n]A2 - 0 (Valid only for STio0-15)	**STOHZ Additional Advancement Bits**

STOHZ[n]A2-0	Additional Advancement (2.048 Mbps, 4.096 Mbps, 8.192 Mbps)	Additional Advancement (16.384 Mbps streams)
000	0 bit	0 bit
001	1/4 bit	2/4 bit
010	2/4 bit	4/4 bit
011	3/4 bit	Reserved
100	4/4 bit	
101-111	Reserved	

Bit	Name	Description
8 - 7	STO[n]FA1 - 0	**Output Stream[n] Fractional Advancement Bits**

STO[n]FA1-0	Advancement (2.048 Mbps, 4.096 Mbps, 8.192 Mbps streams)	Advancement (16.384 Mbps streams)
00	0	0
01	1/4 bit	2/4
10	2/4 bit	Reserved
11	3/4 bit	

Bit	Name	Description
6 - 4	STO[n]AD2 - 0	**Output Stream[n] Bit Advancement Selection Bits** The binary value of these bits refers to the number of bits that the output stream is to be advanced relative to FPo. The maximum value is 7. Zero means no advancement.
3 - 0	STO[n]DR3 - 0	**Output Data Rate Selection Bits**

STIN[n]DR3 - 0	Data Rate
0000	disabled: STio HiZ (STOHZ driven high)
0001	2.048 Mbps
0010	4.096 Mbps
0011	8.192 Mbps
0100	16.384 Mbps
0101 - 1111	Reserved

Note: [n] denotes output stream from 0 - 31.

Table 26 - Stream Output Control Register 0 - 31 (SOCR0 - 31) Bits

External Read/Write Address: 0300_H - $031F_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	ST[n] BRS7	ST[n] BRS6	ST[n] BRS5	ST[n] BRS4	ST[n] BRS3	ST[n] BRS2	ST[n] BRS1	ST[n] BRS0

Bit	Name	Description
15 - 8	Unused	**Reserved** In normal functional mode, these bits **MUST** be set to zero.
7 - 0	ST[n] BRS7 - 0	**Stream[n] BER Receive Start Bits** The binary value of these bits refers to the input channel in which the BER data starts to be compared.

Note: [n] denotes input stream from 0 - 31.

Table 27 - BER Receiver Start Register [n] (BRSR[n]) Bits

External Read/Write Address: 0320_H - $03F_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	ST[n] BL8	ST[n] BL7	ST[n] BL6	ST[n] BL5	ST[n] BL4	ST[n] BL3	ST[n] BL2	ST[n] BL1	ST[n] BL0

Bit	Name	Description
15 - 9	Unused	**Reserved** In normal functional mode, these bits **MUST** be set to zero.
8 - 0	ST[n] BL8 - 0	**Stream[n] BER Length Bits** The binary value of these bits refers to the number of consecutive channels expected to receive the BER pattern. The maximum number of BER channels is 32, 64, 128 and 256 for the data rates of 2.048 Mbps, 4.096 Mbps, 8.192 Mbps and 16.384 Mbps respectively. The minimum number of BER channels is 1. If these bits are set to zero, no BER test will be performed.

Note: [n] denotes input stream from 0 - 31.

Table 28 - BER Receiver Length Register [n] (BRLR[n]) Bits

External Read/Write Address: 0340_H - $035F_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	ST[n] CBER	ST[n] SBER

Bit	Name	Description
15 - 2	Unused	**Reserved** In normal functional mode, these bits **MUST** be set to zero.
1	ST[n] CBER	**Stream[n] Bit Error Rate Counter Clear** When this bit is high, it resets the internal bit error counter and the stream BER Receiver Error Register to zero.
0	ST[n] SBER	**Stream[n] Bit Error Rate Test Start** When this bit is high, it enables the BER receiver; starts the bit error rate test. The bit error test result is kept in the BER Receiver Error (BRER[n]) register. Upon the completion of the BER test, set this bit to zero. Note that the RBEREB bit must be set in the IMS Register first.

Note: [n] denotes input stream from 0 - 31

Table 29 - BER Receiver Control Register [n] (BRCR[n]) Bits

External Read Address: 0360_H - $037F_H$
Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ST[n] BC15	ST[n] BC14	ST[n] BC13	ST[n] BC12	ST[n] BC11	ST[n] BC10	ST[n] BC9	ST[n] BC8	ST[n] BC7	ST[n] BC6	ST[n] BC5	ST[n] BC4	ST[n] BC3	ST[n] BC2	ST[n] BC1	ST[n] BC0

Bit	Name	Description
15 - 0	ST[n] BC15 - 0	**Stream[n] BER Count Bits (Read Only)** The binary value of these bits refers to the bit error counts. When it reaches its maximum value of 0xFFFF, the value will be held and will not rollover.

Note: [n] denotes input stream from 0 - 31

Table 30 - BER Receiver Error Register [n] (BRER[n]) Bits - Read Only

20.0 Memory

20.1 Memory Address Mappings

When A13 is high, the data or connection memory can be accessed by the microprocessor port. Bit 1 - 0 in the Control Register determine the access to the data or connection memory (CM_L or CM_H).

MSB (Note 1)	Stream Address (St0 - 31)						Channel Address (Ch0 - 255)								
A13	**A12**	**A11**	**A10**	**A9**	**A8**	**Stream [n]**	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**Channel [n]**
1	0	0	0	0	0	Stream 0	0	0	0	0	0	0	0	0	Ch 0
1	0	0	0	0	1	Stream 1	0	0	0	0	0	0	0	1	Ch 1
1	0	0	0	1	0	Stream 2	.	.	.	.	.	.	.	.	.
1	0	0	0	1	1	Stream 3	.	.	.	.	.	.	.	.	.
1	0	0	1	0	0	Stream 4	0	0	0	1	1	1	1	0	Ch 30
1	0	0	1	0	1	Stream 5	0	0	0	1	1	1	1	1	Ch 31 (Note 2)
1	0	0	1	1	0	Stream 6	0	0	1	0	0	0	0	0	Ch 32
1	0	0	1	1	1	Stream 7	0	0	1	0	0	0	0	1	Ch 33
1	0	1	0	0	0	Stream 8	.	.	.		.	.		.	.
.	.	.	.	.	.	.	.	.	.		.			.	.
.	.	.	.	.	.	.	0	0	1	1	1	1	1	0	Ch 62
.	.	.	.	.	.	.	0	0	1	1	1	1	1	1	Ch 63 (Note 3)
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
1	0	1	1	1	0	Stream 14	.	.	.	.	.	.	.	.	.
1	0	1	1	1	1	Stream 15	.	.	.	.	.	.	.	.	.
.	.	.	.	.		.	0	1	1	1	1	1	1	0	Ch126
.	.	.	.	.		.	0	1	1	1	1	1	1	1	Ch 127 (Note 4)
.	.	.	.	.		.	.	.	.	.	.	.	.	.	.
.	.	.	.	.		.	.	.	.	.	.	.	.	.	.
1	1	1	1	1		Stream 30	.	.	.	.	.	.	.	.	.
1	1	1	1	1		Stream 31	.	.	.	.	.	.	.	.	.
							1	1	1	1	1	1	1	0	Ch 254
							1	1	1	1	1	1	1	1	Ch 255 (Note 5)

Notes:
1. A13 must be high for access to data and connection memory positions. A13 must be low to access internal registers.
2. Channels 0 to 31 are used when serial stream is at 2.048 Mbps.
3. Channels 0 to 63 are used when serial stream is at 4.096 Mbps.
4. Channels 0 to 127 are used when serial stream is at 8.192 Mbps.
5. Channels 0 to 255 are used when serial stream is at 16.384 Mbps.

Table 31 - Address Map for Memory Locations (A13 = 1)

20.2 Connection Memory Low (CM_L) Bit Assignment

When the CMM bit (bit 0) in the connection memory low is zero, the per-channel transmission is set to the normal channel-switching. The connection memory low bit assignment for the channel transmission mode is shown in Table 32 on page 57.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UA EN	V/$\overline{C}$	SSA 4	SSA 3	SSA 2	SSA 1	SSA 0	SCA 7	SCA 6	SCA 5	SCA 4	SCA 3	SCA 2	SCA 1	SCA 0	**CMM =0**

Bit	Name	Description
15	UAEN	**Conversion between μ-law and A-law Enable** When this bit is low, normal switch without μ-law/A-law conversion. Connection memory high will be ignored. When this bit is high, switch with μ-law/A-law conversion, and connection memory high controls the conversion method.

Table 32 - Connection Memory Low (CM_L) Bit Assignment when CMM = 0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UA EN	V/$\overline{C}$	SSA 4	SSA 3	SSA 2	SSA 1	SSA 0	SCA 7	SCA 6	SCA 5	SCA 4	SCA 3	SCA 2	SCA 1	SCA 0	**CMM =0**

Bit	Name	Description
14	V/$\overline{C}$	**Variable/Constant Delay Control** When this bit is low, the output data for this channel will be taken from constant delay memory. When this bit is set to high, the output data for this channel will be taken from variable delay memory. Note that VAREN must be set in Control Register first.
13 - 9	SSA4 - 0	**Source Stream Address** The binary value of these 5 bits represents the input stream number.
8 - 1	SCA7 - 0	**Source Channel Address** The binary value of these 8 bits represents the input channel number.
0	CMM = 0	**Connection Memory Mode = 0** If this is low, the connection memory is in the normal switching mode. Bit13 - 1 are the source stream number and channel number.
Note: For proper μ-law/A-law conversion, the CM_H bits should be set before Bit 15 (UAEN bit) is set to high.		

Table 32 - Connection Memory Low (CM_L) Bit Assignment when CMM = 0

When CMM is one, the device is programmed to perform one of the special per-channel transmission modes. Bits PCC0 and PCC1 from connection memory are used to select the per-channel tristate, message or BER test mode as shown in Table 33 on page 58.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UA EN	0	0	0	0	MSG 7	MSG 6	MSG 5	MSG 4	MSG 3	MSG 2	MSG 1	MSG 0	PCC 1	PCC 0	**CMM =1**

Bit	Name	Description
15	UAEN	**Conversion between μ-law and A-law Enable (Message mode only)** When this bit is low, message mode has no μ-law/A-law conversion. Connection memory high will be ignored. When this bit is high, message mode has μ-law/A-law conversion, and connection memory high controls the conversion method.
14 - 11	Unused	**Reserved** In normal functional mode, these bits **MUST** be set to zero.
10 - 3	MSG7 - 0	**Message Data Bits** 8-bit data for the message mode. Not used in the per-channel tristate and BER test modes.

Table 33 - Connection Memory Low (CM_L) Bit Assignment when CMM = 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UA EN	0	0	0	0	MSG 7	MSG 6	MSG 5	MSG 4	MSG 3	MSG 2	MSG 1	MSG 0	PCC 1	PCC 0	**CMM =1**

Bit	Name	Description
2 - 1	PCC1 - 0	**Per-Channel Control Bits** These two bits control the corresponding entry's value on the STio stream**.** PCC1 / PCC0 / Channel Output Mode 0 / 0 / Per Channel Tristate 0 / 1 / Message Mode 1 / 0 / BER Test Mode 1 / 1 / Reserved
0	CMM = 1	**Connection Memory Mode = 1** If this is high, the connection memory is in the per-channel control mode which is per-channel tristate, per-channel message mode or per-channel BER mode.

Note: For proper μ-law/A-law conversion, the CM_H bits should be set before Bit 15 (UAEN bit) is set to high.

Table 33 - Connection Memory Low (CM_L) Bit Assignment when CMM = 1

20.3 Connection Memory High (CM_H) Bit Assignment

Connection memory high provides the detailed information required for μ-law and A-law conversion. ICL and OCL bits describe the Input Coding Law and the Output Coding Law, respectively. They are used to select the expected PCM coding laws for the connection, on the TDM inputs, and on the TDM outputs. The $\overline{V}$/D bit is used to select the class of coding law. If the $\overline{V}$/D bit is cleared (to select a voice connection), the ICL and OCL bits select between A-law and μ-law specifications related to G.711 voice coding. If the $\overline{V}$/D bit is set (to select a data connection), the ICL and OCL bits select between various bit inverting protocols. These coding laws are illustrated in the following table. If the ICL is different than the OCL, all data bytes passing through the switch on that particular connection are translated between the indicated laws. If the ICL and the OCL are the same, no coding law translation is performed. The ICL, the OCL bits and $\overline{V}$/D bit only have an effect on PCM code translations for constant delay connections, variable delay connections and per-channel message mode.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	$\overline{V}$/D	ICL 1	ICL 0	OCL 1	OCL 0

Bit	Name	Description
15 - 5	Unused	**Reserved** In normal functional mode, these bits **MUST** be set to zero.

Table 34 - Connection Memory High (CM_H) Bit Assignment

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	$\overline{V}$/D	ICL 1	ICL 0	OCL 1	OCL 0

Bit	Name	Description
4	$\overline{V}$/D	**Voice/Data Control** When this bit is low, the corresponding channel is for voice. When this bit is high, the corresponding channel is for data.
3 - 2	ICL1 - 0	**Input Coding Law.**

ICL1-0	Input Coding Law	
	For Voice ($\overline{V}$/D bit = 0)	For Data ($\overline{V}$/D bit = 1)
00	CCITT.ITU A-law	No code
01	CCITT.ITU μ-law	ABI
10	A-law w/o ABI	Inverted ABI
11	μ-law w/o Magnitude Inversion	All Bits Inverted

1 - 0	OCL1 - 0	**Output Coding Law**

OCL1-0	Output Coding Law	
	For Voice ($\overline{V}$/D bit = 0)	For Data ($\overline{V}$/D bit = 1)
00	CCITT.ITU A-law	No code
01	CCITT.ITU μ-law	ABI
10	A-law w/o ABI	Inverted ABI
11	μ-law w/o Magnitude Inversion	All Bits Inverted

Note 1: For proper μ-law/A-law conversion, the CM_H bits should be set before Bit 15 of CM_L is set to high.

Note 2: Refer to G.711 standard for detail information of different laws.

Table 34 - Connection Memory High (CM_H) Bit Assignment

21.0 DC Parameters

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	I/O Supply Voltage	V_{DD_IO}	-0.5	5.0	V
2	Core Supply Voltage	V_{DD_CORE}	-0.5	2.5	V
3	Input Voltage	V_{I_3V}	-0.5	V_{DD} + 0.5	V
4	Input Voltage (5 V-tolerant inputs)	V_{I_5V}	-0.5	7.0	V
5	Continuous Current at Digital Outputs	I_o		15	mA
6	Package Power Dissipation	P_D		1.5	W
7	Storage Temperature	T_S	- 55	+125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units
1	Operating Temperature	T_{OP}	-40	25	+85	°C
2	Positive Supply	V_{DD_IO}	3.0	3.3	3.6	V
3	Positive Supply	V_{DD_CORE}	1.71	1.8	1.89	V
4	Input Voltage	V_I	0	3.3	V_{DD_IO}	V
5	Input Voltage on 5 V-Tolerant Inputs	V_{I_5V}	0	5.0	5.5	V

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Supply Current - V_{DD_CORE}	I_{DD_CORE}			120	mA	
2	Supply Current - V_{DD_IO}	I_{DD_IO}			70	mA	C_L=30pF
3	Input High Voltage	V_{IH}	2.0			V	
4	Input Low Voltage	V_{IL}			0.8	V	
5	Input Leakage (input pins) Input Leakage (bi-directional pins)	I_{IL} I_{BL}			5 5	µA µA	$0 \le < V_{IN} \le V_{DD_IO}$ See Note 1
6	Weak Pullup Current	I_{PU}		-33		µA	Input at 0V
7	Weak Pulldown Current	I_{PD}		33		µA	Input at V_{DD_IO}
8	Input Pin Capacitance	C_I		3		pF	
9	Output High Voltage	V_{OH}	2.4			V	I_{OH} = 8 mA
10	Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
11	Output High Impedance Leakage	I_{OZ}			5	µA	$0 < V < V_{DD}$
12	Output Pin Capacitance	C_O		5	10	pF	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

Note 1: Maximum leakage on pins (output or I/O pins in high impedance state) is over an applied voltage (V_{IN}).

22.0 AC Parameters

AC Electrical Characteristics† - Timing Parameter Measurement Voltage Levels

	Characteristics	Sym.	Level	Units	Conditions
1	CMOS Threshold	V_{CT}	0.5 V_{DD_IO}	V	
2	Rise/Fall Threshold Voltage High	V_{HM}	0.7 V_{DD_IO}	V	
3	Rise/Fall Threshold Voltage Low	V_{LM}	0.3 V_{DD_IO}	V	

† Characteristics are over recommended operating conditions unless otherwise stated.

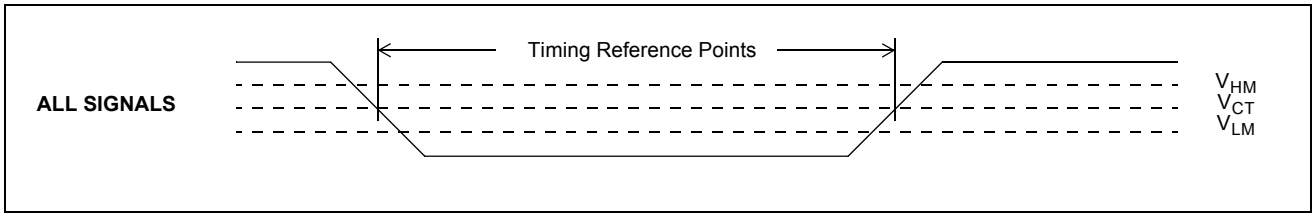


Figure 19 - Timing Parameter Measurement Voltage Levels

AC Electrical Characteristics† - Motorola Non-Multiplexed Bus Mode - Read Access

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions[2]
1	$\overline{CS}$ de-asserted time	t_{CSD}	15			ns	
2	$\overline{DS}$ de-asserted time	t_{DSD}	15			ns	
3	$\overline{CS}$ setup to $\overline{DS}$ falling	t_{CSS}	0			ns	
4	R/$\overline{W}$ setup to $\overline{DS}$ falling	t_{RWS}	10			ns	
5	Address setup to $\overline{DS}$ falling	t_{AS}	5			ns	
6	$\overline{CS}$ hold after $\overline{DS}$ rising	t_{CSH}	0			ns	
7	R/$\overline{W}$ hold after $\overline{DS}$ rising	t_{RWH}	0			ns	
8	Address hold after $\overline{DS}$ rising	t_{AH}	0			ns	
9	Data setup to $\overline{DTA}$ Low	t_{DS}	8			ns	C_L = 50 pF
10	Data hold after $\overline{DS}$ rising	t_{DHZ}	7			ns	C_L = 50 pF, R_L = 1 K (Note 1)
11	Acknowledgement delay time. From $\overline{DS}$ low to $\overline{DTA}$ low: Registers Memory	t_{AKD}			 75 185	 ns ns	 C_L = 50 pF C_L = 50 pF
12	Acknowledgement hold time. From $\overline{DS}$ high to $\overline{DTA}$ high	t_{AKH}	4		12	ns	C_L = 50 pF, R_L = 1 K (Note 1)
13	$\overline{DTA}$ drive high to HiZ	t_{AKZ}			8	ns	

Note 1: High impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

Note 2: A delay of 500 µs to 2 ms (see Section 13.2 on page 33) must be applied before the first microprocessor access is performed after the $\overline{RESET}$ pin is set high.

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

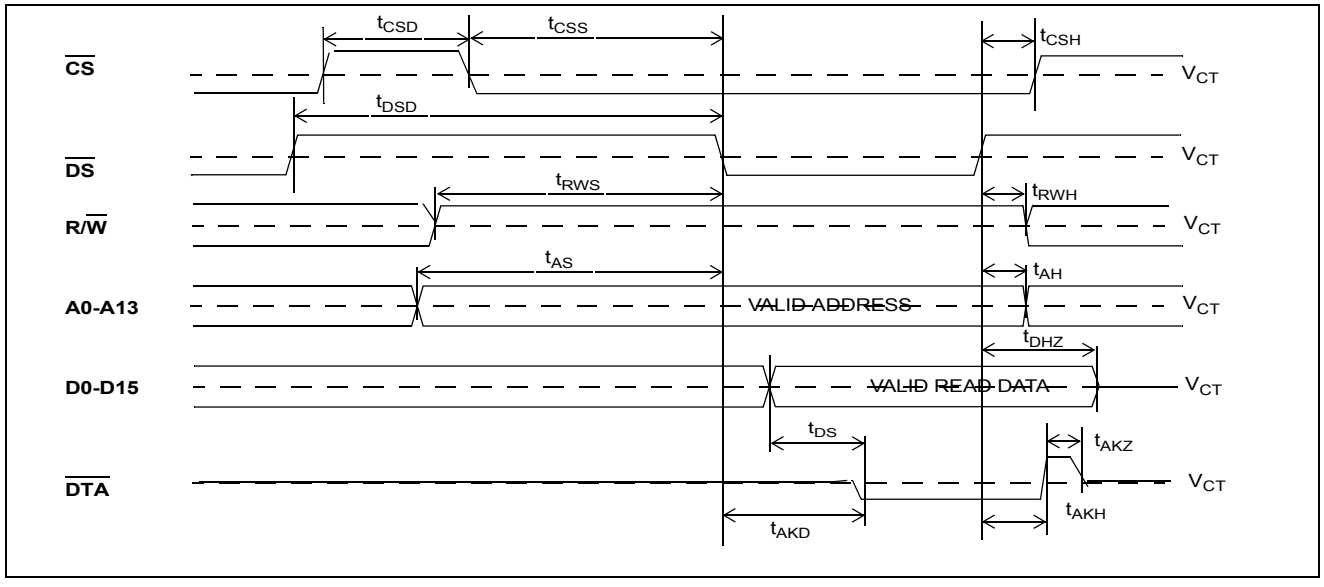


Figure 20 - Motorola Non-Multiplexed Bus Timing - Read Access

AC Electrical Characteristics† - Motorola Non-Multiplexed Bus Mode - Write Access

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions[2]
1	$\overline{CS}$ de-asserted time	t_{CSD}	15			ns	
2	$\overline{DS}$ de-asserted time	t_{DSD}	15			ns	
3	$\overline{CS}$ setup to $\overline{DS}$ falling	t_{CSS}	0			ns	
4	R/$\overline{W}$ setup to $\overline{DS}$ falling	t_{RWS}	10			ns	
5	Address setup to $\overline{DS}$ falling	t_{AS}	5			ns	
6	Data setup to $\overline{DS}$ falling	t_{DS}	0			ns	C_L = 50 pF
7	$\overline{CS}$ hold after $\overline{DS}$ rising	t_{CSH}	0			ns	
8	R/$\overline{W}$ hold after $\overline{DS}$ rising	t_{RWH}	0			ns	
9	Address hold after $\overline{DS}$ rising	t_{AH}	0			ns	
10	Data hold from $\overline{DS}$ rising	t_{DH}	5			ns	C_L = 50 pF, R_L = 1 K (Note 1)
11	Acknowledgement delay time. From $\overline{DS}$ low to $\overline{DTA}$ low: Registers Memory	t_{AKD}			 55 150	 ns ns	 C_L = 50 pF C_L = 50 pF
12	Acknowledgement hold time. From $\overline{DS}$ high to $\overline{DTA}$ high	t_{AKH}	4		12	ns	C_L = 50 pF, R_L = 1 K (Note 1)
13	$\overline{DTA}$ drive high to HiZ	t_{AKZ}			8	ns	

Note 1: High impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

Note 2: A delay of 500 µs to 2 ms (see Section 13.2 on page 33) must be applied before the first microprocessor access is performed after the $\overline{RESET}$ pin is set high.

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

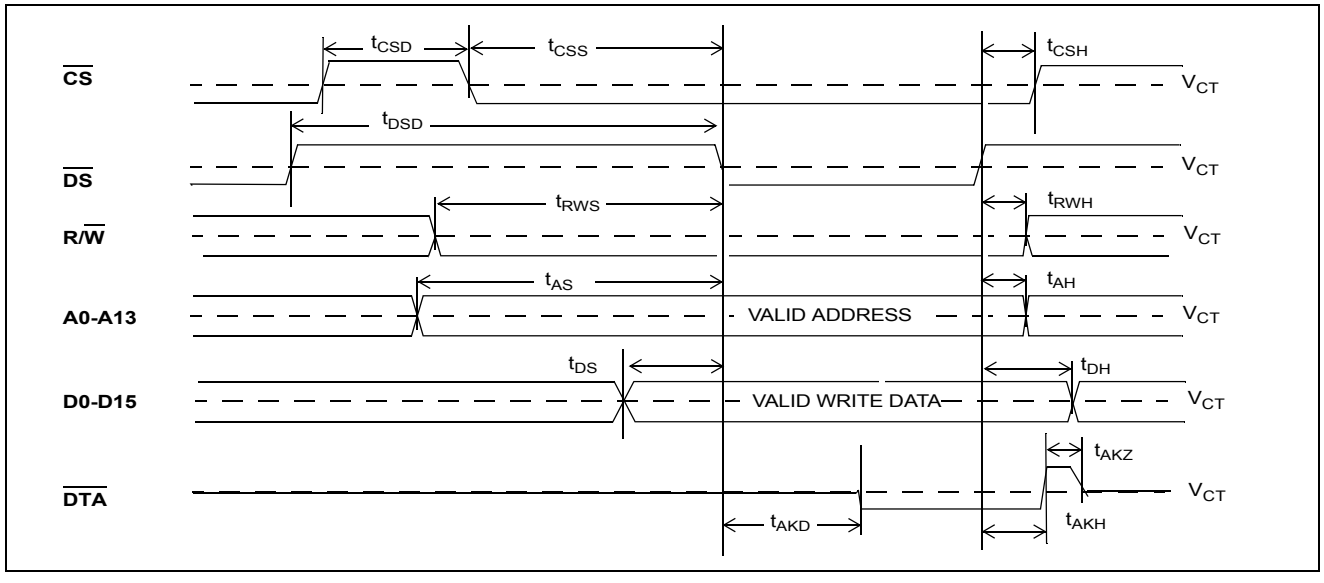


Figure 21 - Motorola Non-Multiplexed Bus Timing - Write Access

AC Electrical Characteristics† - Intel Non-Multiplexed Bus Mode - Read Access

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions[2]
1	$\overline{CS}$ de-asserted time	t_{CSD}	15			ns	
2	$\overline{RD}$ setup to $\overline{CS}$ falling	t_{RS}	10			ns	
3	$\overline{WR}$ setup to $\overline{CS}$ falling	t_{WS}	10			ns	
4	Address setup to $\overline{CS}$ falling	t_{AS}	5			ns	
5	$\overline{RD}$ hold after $\overline{CS}$ rising	t_{RH}	0			ns	
6	$\overline{WR}$ hold after $\overline{CS}$ rising	t_{WH}	0			ns	
7	Address hold after $\overline{CS}$ rising	t_{AH}	0			ns	
8	Data setup to RDY high	t_{DS}	8			ns	C_L = 50 pF
9	Data hold after $\overline{CS}$ rising	t_{CSZ}	7			ns	C_L = 50 pF, R_L = 1 K (Note 1)
10	Acknowledgement delay time. From $\overline{CS}$ low to RDY high: Registers Memory	t_{AKD}			 175 185	 ns ns	 C_L = 50 pF C_L = 50 pF
11	Acknowledgement hold time. From $\overline{CS}$ high to RDY low	t_{AKH}	4		12	ns	C_L = 50 pF, R_L = 1 K (Note 1)
12	RDY drive low to HiZ	t_{AKZ}			8	ns	

Note 1: High impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

Note 2: A delay of 500 µs to 2 ms (see Section 13.2 on page 33) must be applied before the first microprocessor access is performed after the $\overline{RESET}$ pin is set high.

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

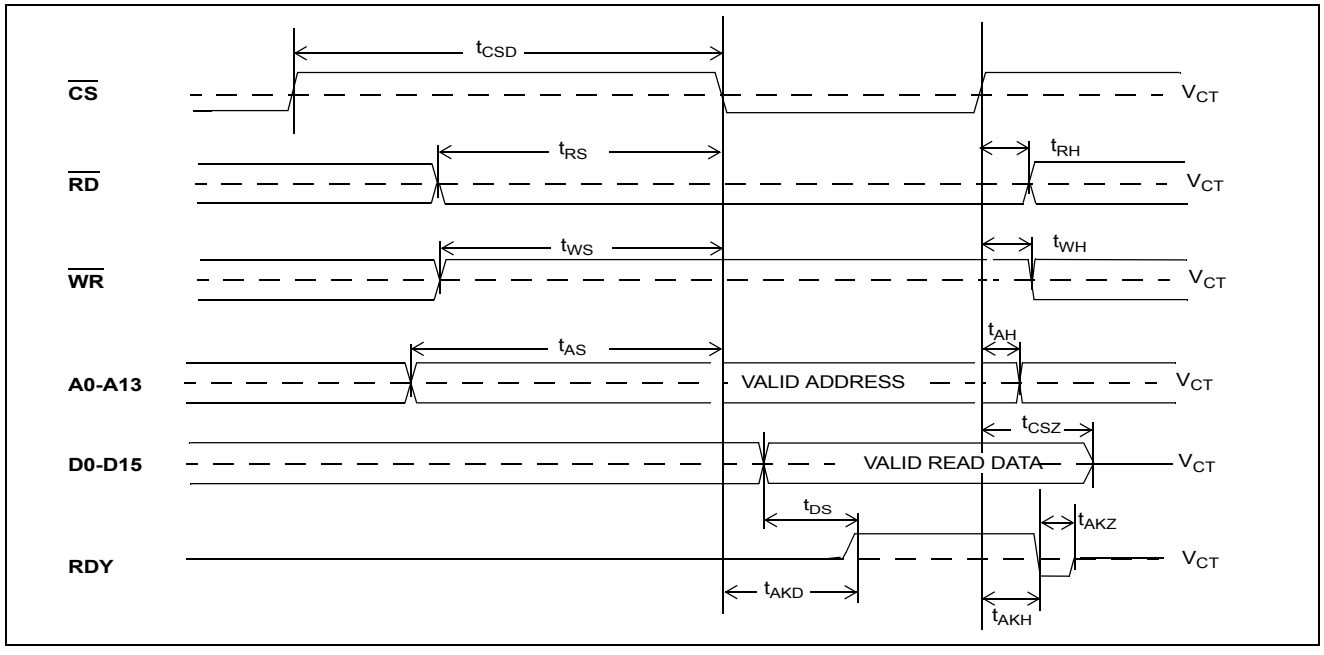


Figure 22 - Intel Non-Multiplexed Bus Timing - Read Access

AC Electrical Characteristics† - Intel Non-Multiplexed Bus Mode - Write Access

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions[2]
1	$\overline{CS}$ de-asserted time	t_{CSD}	15			ns	
2	$\overline{WR}$ setup to $\overline{CS}$ falling	t_{WS}	10			ns	
3	$\overline{RD}$ setup to $\overline{CS}$ falling	t_{RS}	10			ns	
4	Address setup to $\overline{CS}$ falling	t_{AS}	5			ns	
5	Data setup to $\overline{CS}$ falling	t_{DS}	0			ns	C_L = 50 pF
6	$\overline{WR}$ hold after $\overline{CS}$ rising	t_{WH}	0			ns	
7	$\overline{RD}$ hold after $\overline{CS}$ rising	t_{RH}	0			ns	
8	Address hold after $\overline{CS}$ rising	t_{AH}	10			ns	
9	Data hold after $\overline{CS}$ rising	t_{DH}	5			ns	C_L = 50 pF, R_L = 1 K (Note 1)
10	Acknowledgement delay time. From $\overline{CS}$ low to RDY high: Registers Memory	t_{AKD}			 55 150	 ns ns	 C_L = 50 pF C_L = 50 pF
11	Acknowledgement hold time. From $\overline{CS}$ high to RDY low	t_{AKH}	4		12	ns	C_L = 50 pF, R_L = 1 K (Note 1)
12	RDY drive low to HiZ	t_{AKZ}			8	ns	

Note 1: High impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

Note 2: A delay of 500 µs to 2 ms (Section 13.2 on page 33) must be applied before the first microprocessor access is performed after the $\overline{RESET}$ pin is set high.

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

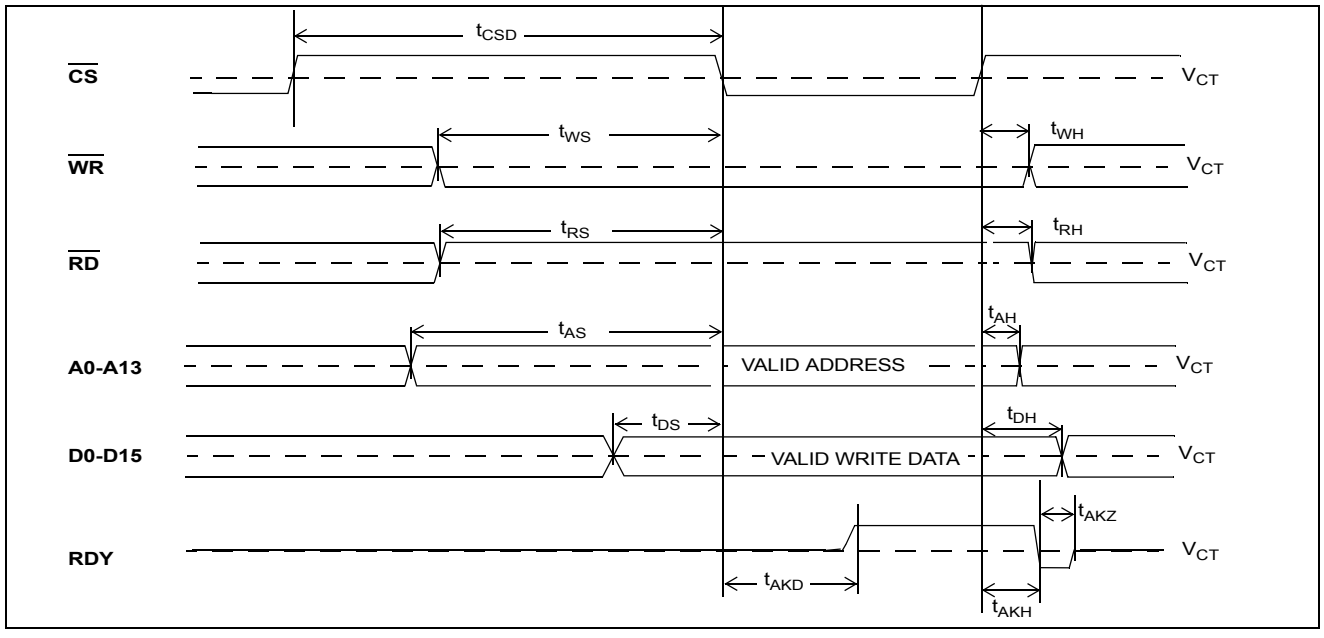


Figure 23 - Intel Non-Multiplexed Bus Timing - Write Access

AC Electrical Characteristics† - JTAG Test Port Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	TCK Clock Period	t_{TCKP}	100			ns	
2	TCK Clock Pulse Width High	t_{TCKH}	20			ns	
3	TCK Clock Pulse Width Low	t_{TCKL}	20			ns	
4	TMS Set-up Time	t_{TMSS}	10			ns	
5	TMS Hold Time	t_{TMSH}	10			ns	
6	TDi Input Set-up Time	t_{TDIS}	20			ns	
7	TDi Input Hold Time	t_{TDIH}	60			ns	
8	TDo Output Delay	t_{TDOD}			30	ns	C_L = 30 pF
9	$\overline{TRST}$ pulse width	t_{TRSTW}	200			ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

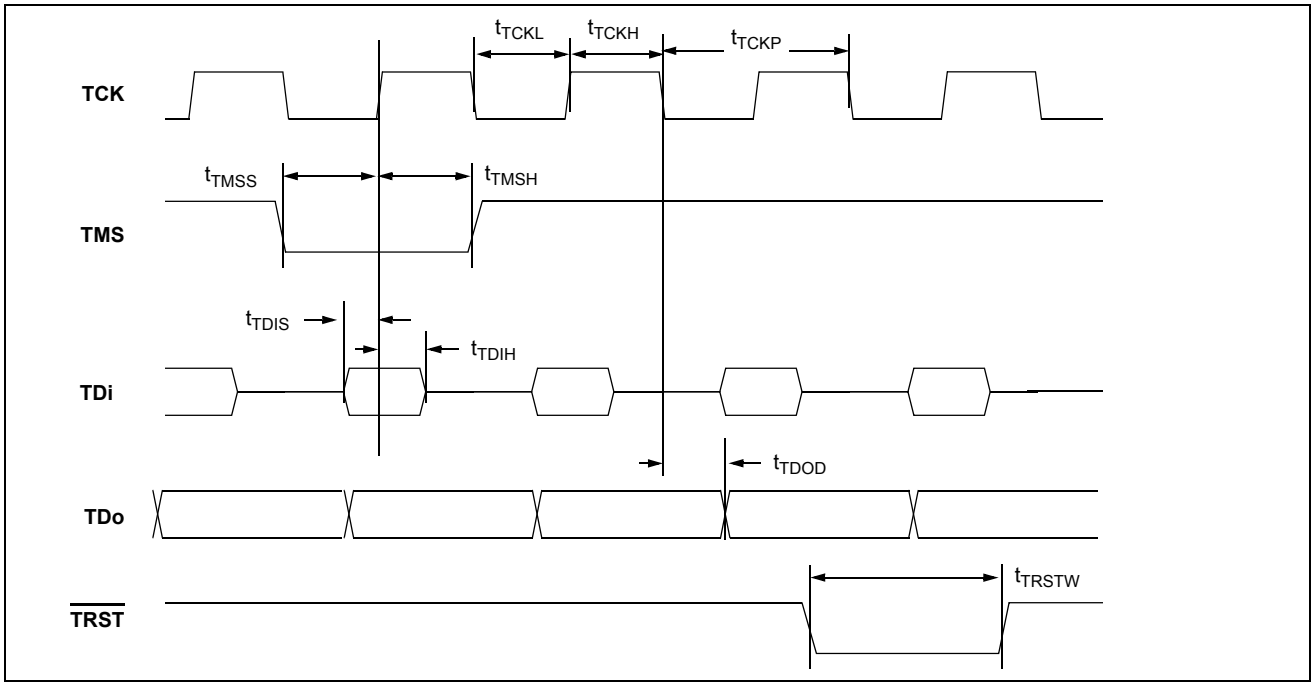


Figure 24 - JTAG Test Port Timing Diagram

AC Electrical Characteristics† - FPi and CKi Timing when CKIN1-0 bits = 00 (16.384 MHz)

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	FPi Input Frame Pulse Width	t_{FPIW}	40	61	115	ns	
2	FPi Input Frame Pulse Setup Time	t_{FPIS}	20			ns	
3	FPi Input Frame Pulse Hold Time	t_{FPIH}	20			ns	
4	CKi Input Clock Period	t_{CKIP}	55	61	67	ns	
5	CKi Input Clock High Time	t_{CKIH}	27		34	ns	
6	CKi Input Clock Low Time	t_{CKIL}	27		34	ns	
7	CKi Input Clock Rise/Fall Time	t_rCKi, t_fCKi			3	ns	
8	CKi Input Clock Cycle to Cycle Variation	t_{CVC}	0		20	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - FPi and CKi Timing when CKIN1-0 bits = 01 (8.192 MHz)

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	FPi Input Frame Pulse Width	t_{FPIW}	90	122	220	ns	
2	FPi Input Frame Pulse Setup Time	t_{FPIS}	45			ns	
3	FPi Input Frame Pulse Hold Time	t_{FPIH}	45			ns	
4	CKi Input Clock Period	t_{CKIP}	110	122	135	ns	
5	CKi Input Clock High Time	t_{CKIH}	55		69	ns	
6	CKi Input Clock Low Time	t_{CKIL}	55		69	ns	
7	CKi Input Clock Rise/Fall Time	t_rCKi, t_fCKi			3	ns	
8	CKi Input Clock Cycle to Cycle Variation	t_{CVC}	0		20	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - FPi and CKi Timing when CKIN1-0 bits = 10 (4.096 MHz)

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	FPi Input Frame Pulse Width	t_{FPIW}	90	244	420	ns	
2	FPi Input Frame Pulse Setup Time	t_{FPIS}	110			ns	
3	FPi Input Frame Pulse Hold Time	t_{FPIH}	110			ns	
4	CKi Input Clock Period	t_{CKIP}	220	244	270	ns	
5	CKi Input Clock High Time	t_{CKIH}	110		135	ns	
6	CKi Input Clock Low Time	t_{CKIL}	110		135	ns	
7	CKi Input Clock Rise/Fall Time	t_rCKi, t_fCKi			3	ns	
8	CKi Input Clock Cycle to Cycle Variation	t_{CVC}	0		20	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

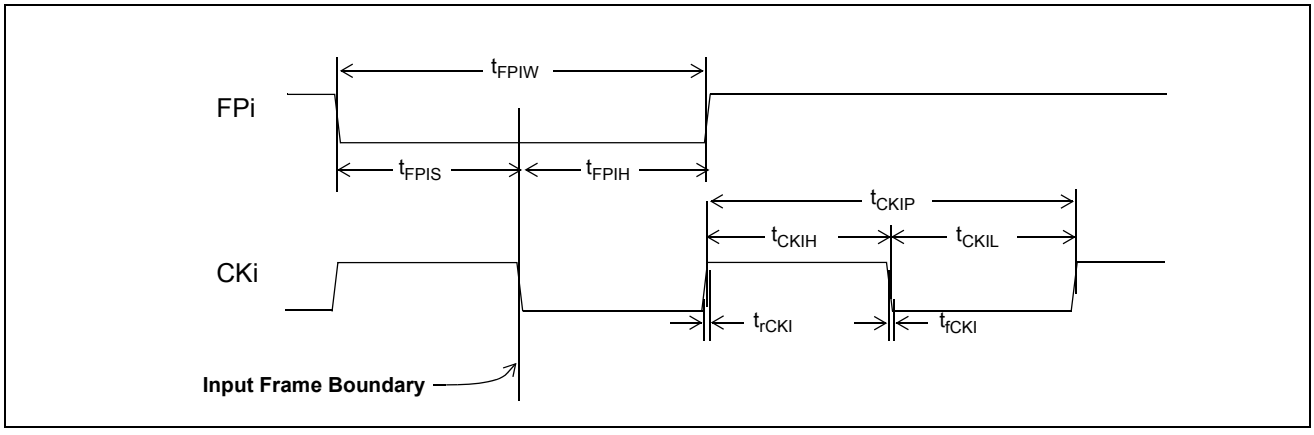


Figure 25 - Frame Pulse Input and Clock Input Timing Diagram (ST-BUS)

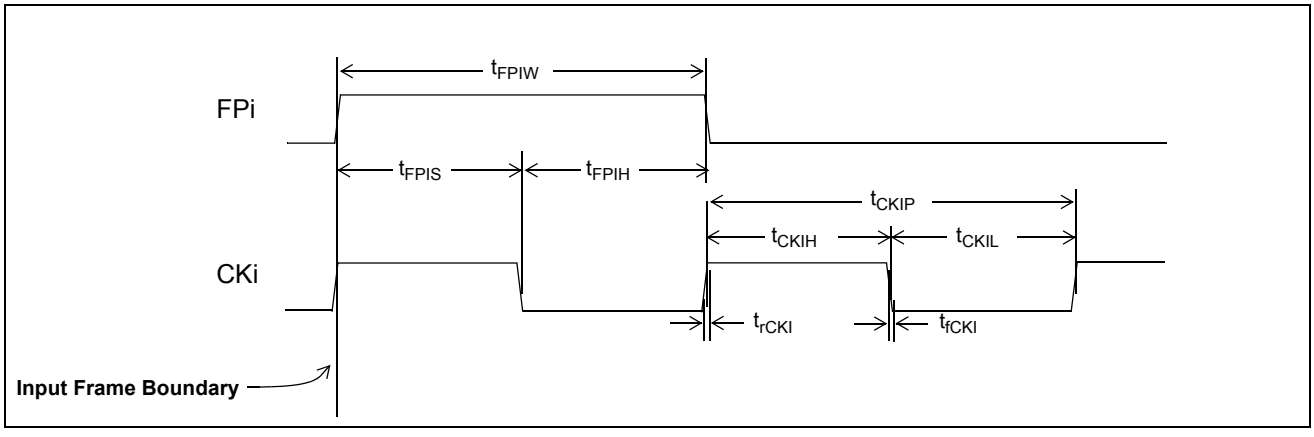


Figure 26 - Frame Pulse Input and Clock Input Timing Diagram (GCI-Bus)

AC Electrical Characteristics† - ST-BUS/GCI-Bus Input Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	STi Setup Time						
	2.048 Mbps	t_{SIS2}	5			ns	
	4.096 Mbps	t_{SIS4}	5			ns	
	8.192 Mbps	t_{SIS8}	5			ns	
	16.384 Mbps	t_{SIS16}	5			ns	
2	STi Hold Time						
	2.048 Mbps	t_{SIH2}	8			ns	
	4.096 Mbps	t_{SIH4}	8			ns	
	8.192 Mbps	t_{SIH8}	8			ns	
	16.384 Mbps	t_{SIH16}	8			ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

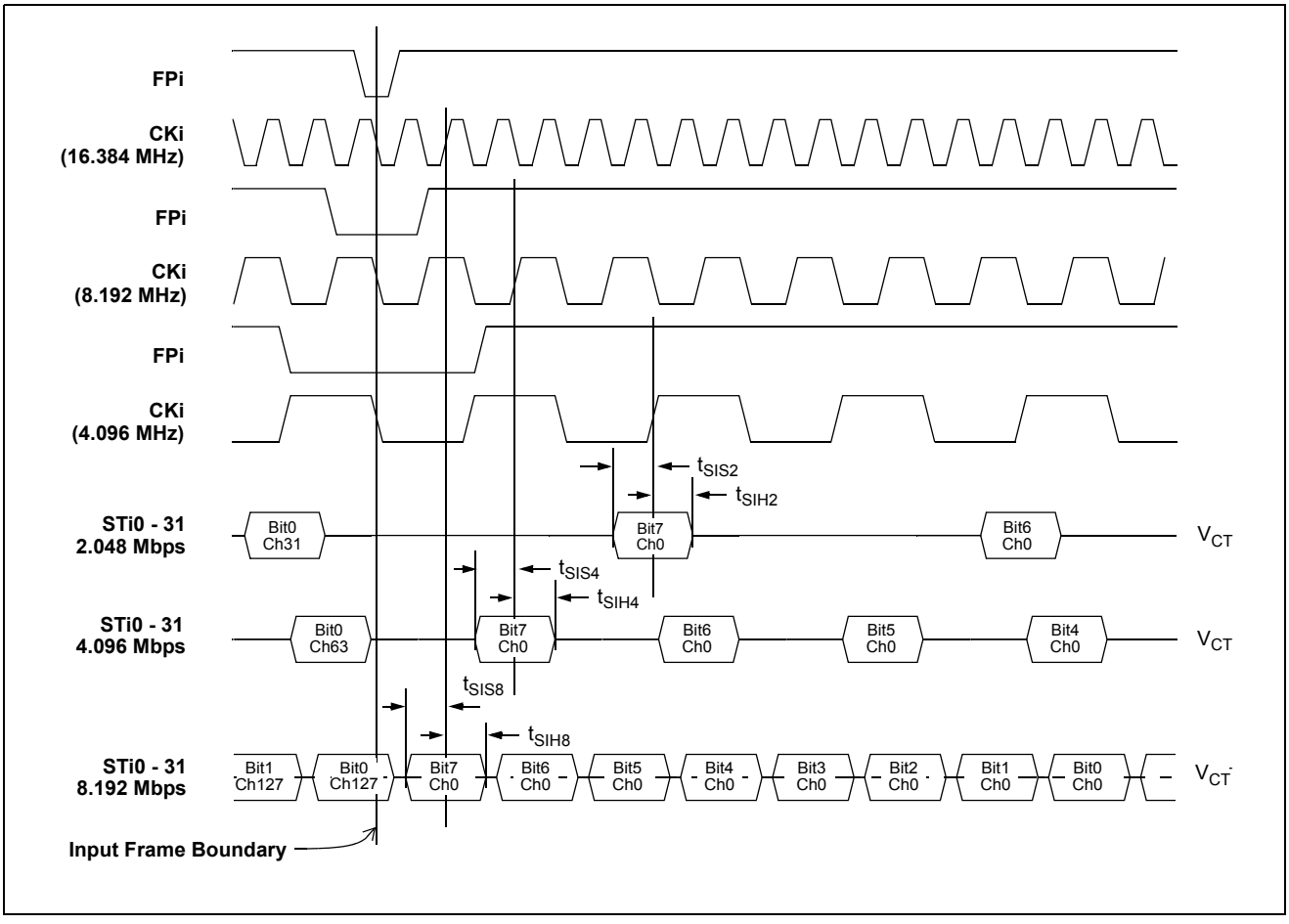


Figure 27 - ST-BUS Input Timing Diagram when Operated at 2, 4, 8 Mbps

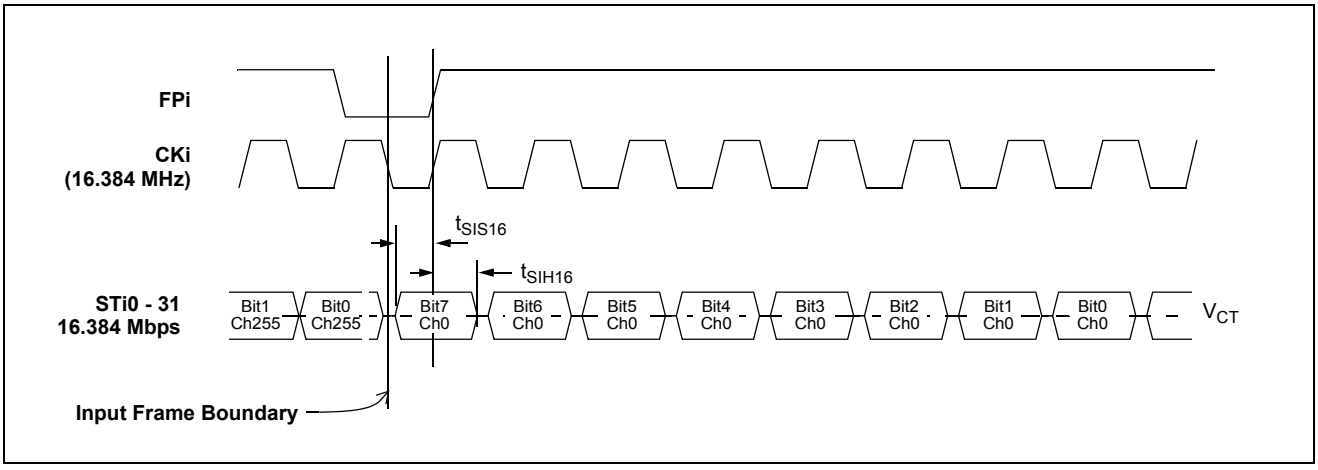


Figure 28 - ST-BUS Input Timing Diagram when Operated at 16 Mbps

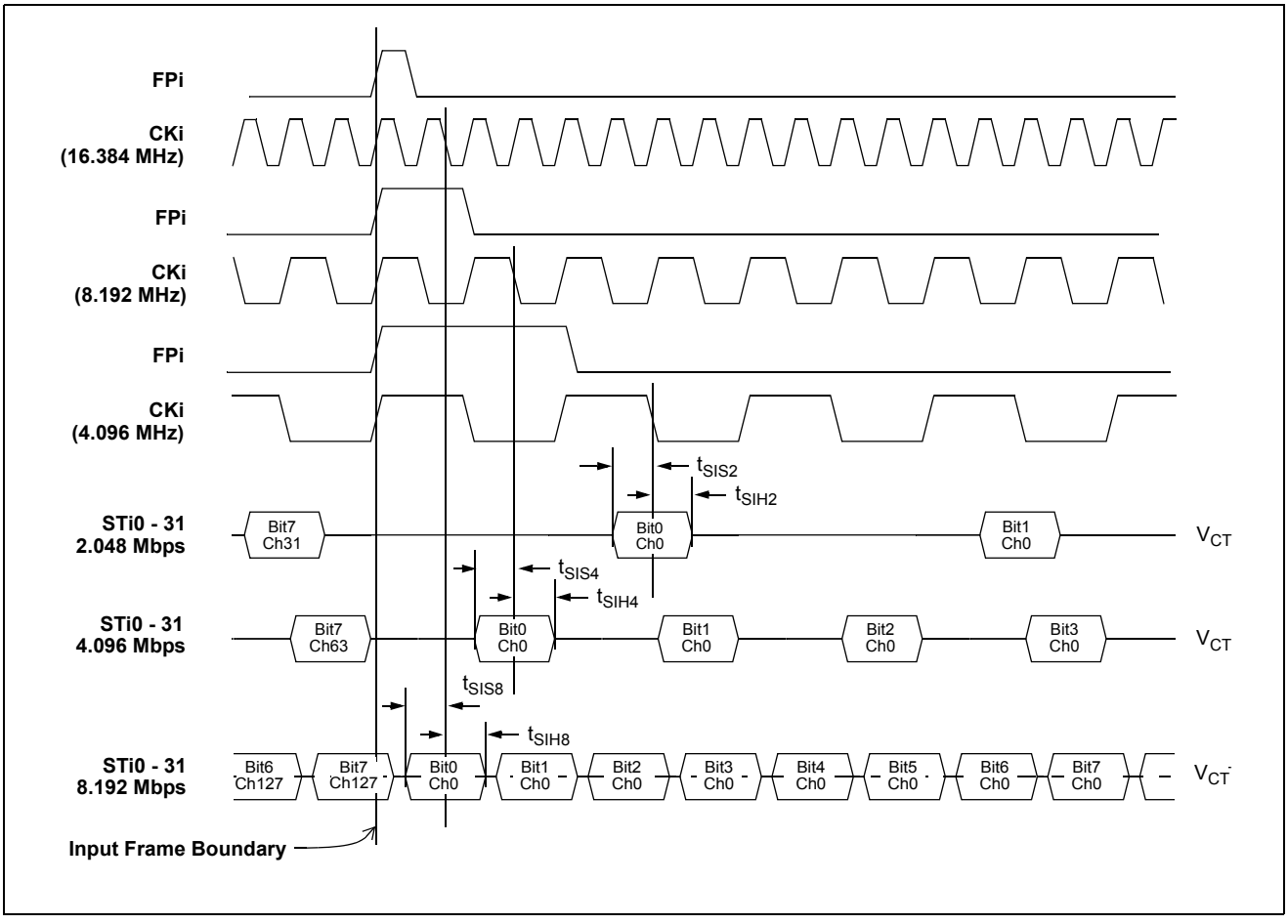


Figure 29 - GCI-Bus Input Timing Diagram when Operated at 2, 4, 8 Mbps

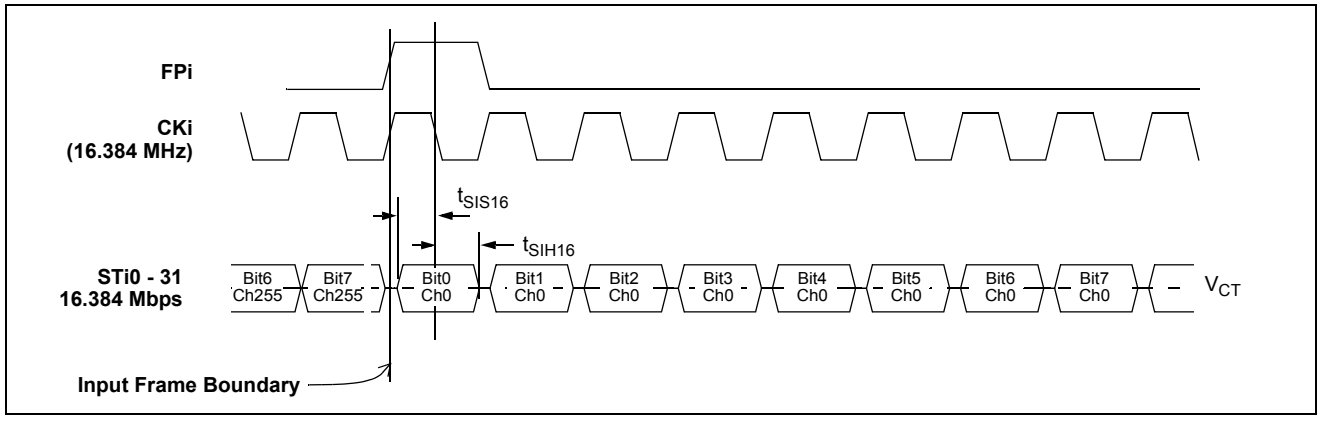


Figure 30 - GCI-Bus Input Timing Diagram when Operated at 16 Mbps

AC Electrical Characteristics† - ST-BUS/GCI-Bus Output Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	STio Delay - Active to Active						C_L = 30 pF
	@2.048 Mbps	t_{SOD2}	0		6	ns	Multiplied Clock Mode
	@4.096 Mbps	t_{SOD4}	0		6	ns	
	@8.192 Mbps	t_{SOD8}	0		6	ns	
	@16.384 Mbps	t_{SOD16}	0		6	ns	
	@2.048 Mbps	t_{SOD2}	-6		0	ns	Divided Clock Mode
	@4.096 Mbps	t_{SOD4}	-6		0	ns	
	@8.192 Mbps	t_{SOD8}	-6		0	ns	
	@16.384 Mbps	t_{SOD16}	-6		0	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

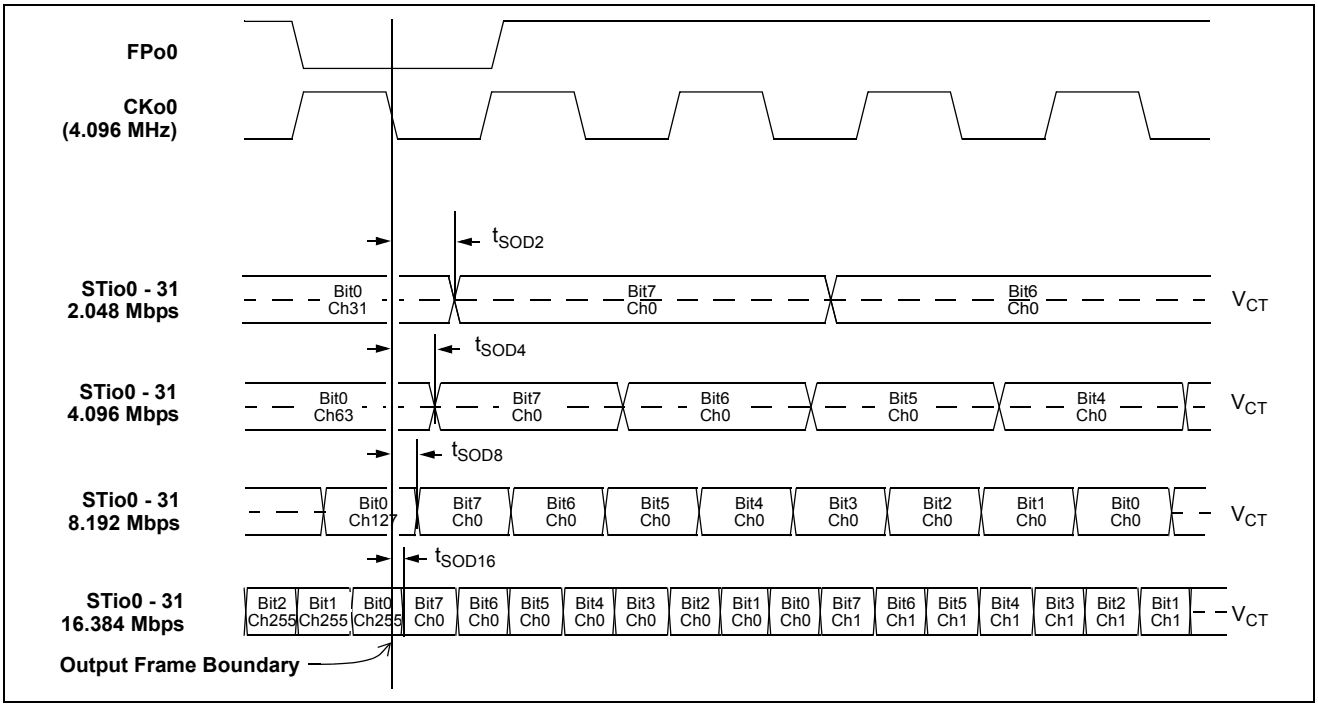


Figure 31 - ST-BUS Output Timing Diagram when Operated at 2, 4, 8 or 16 Mbps

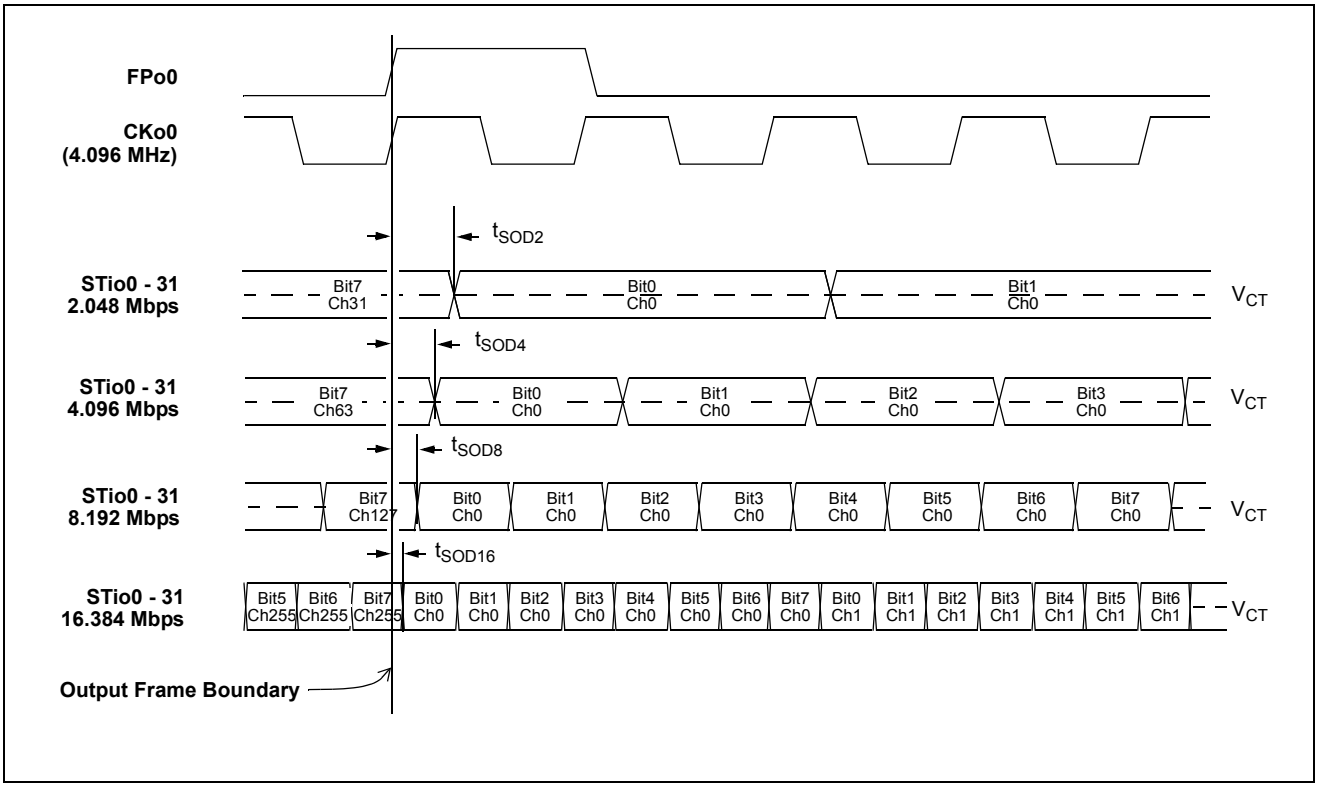


Figure 32 - GCI-Bus Output Timing Diagram when Operated at 2, 4, 8 or 16 Mbps

AC Electrical Characteristics† - ST-BUS/GCI-Bus Output Tristate Timing

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions*
1	STio Delay - Active to High-Z	t_{DZ}	-3 -8		7 0	ns ns	Multiplied Clock Mode Divided Clock Mode
2	STio Delay - High-Z to Active	t_{ZD}	-3 -8		7 0	ns ns	Multiplied Clock Mode Divided Clock Mode
3	Output Drive Enable (ODE) Delay - High-Z to Active CKi @ 4.096 MHz CKi @ 8.192 MHz CKi @ 16.384 MHz	t_{ZD_ODE}			77 260 138 77	ns ns ns ns	Multiplied Clock Mode Divided Clock Mode

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

Note 1: High impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel the time taken to discharge C_L.

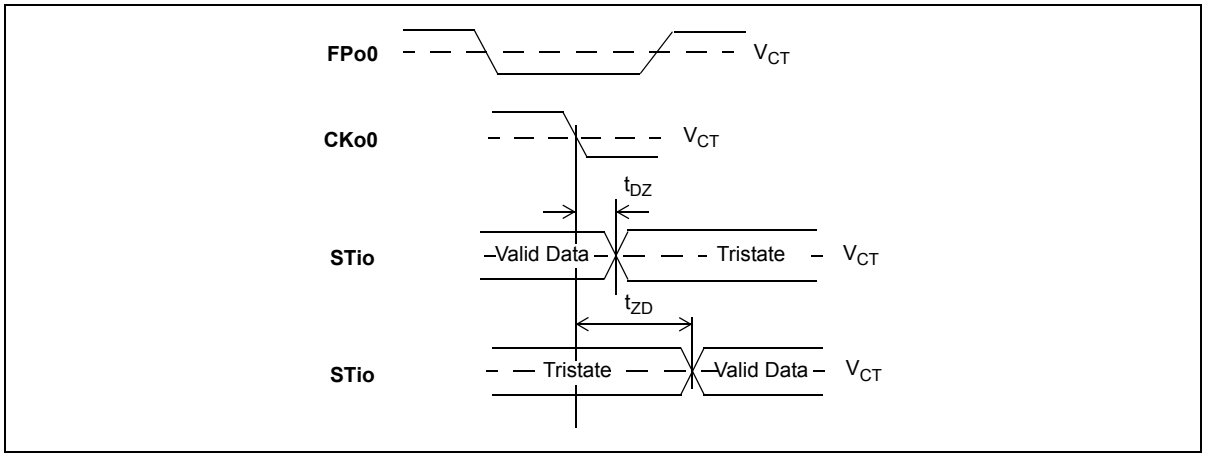


Figure 33 - Serial Output and External Control

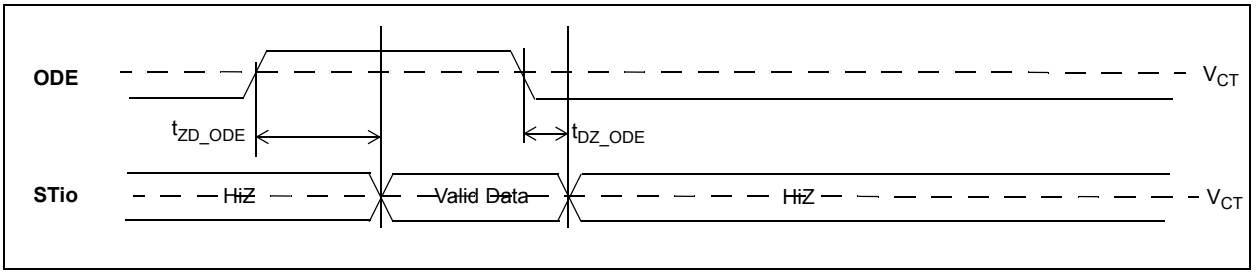


Figure 34 - Output Drive Enable (ODE)

AC Electrical Characteristics† - Clock Mode Input/Output Frame Boundary Alignment

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Input and Output Frame Offset in Divided Clock Mode	t_{FBOS}	5		13	ns	
2	Input and Output Frame Offset in Multiplied Clock Mode	t_{FBOS}	2		10	ns	Input reference jitter is equal to zero.

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

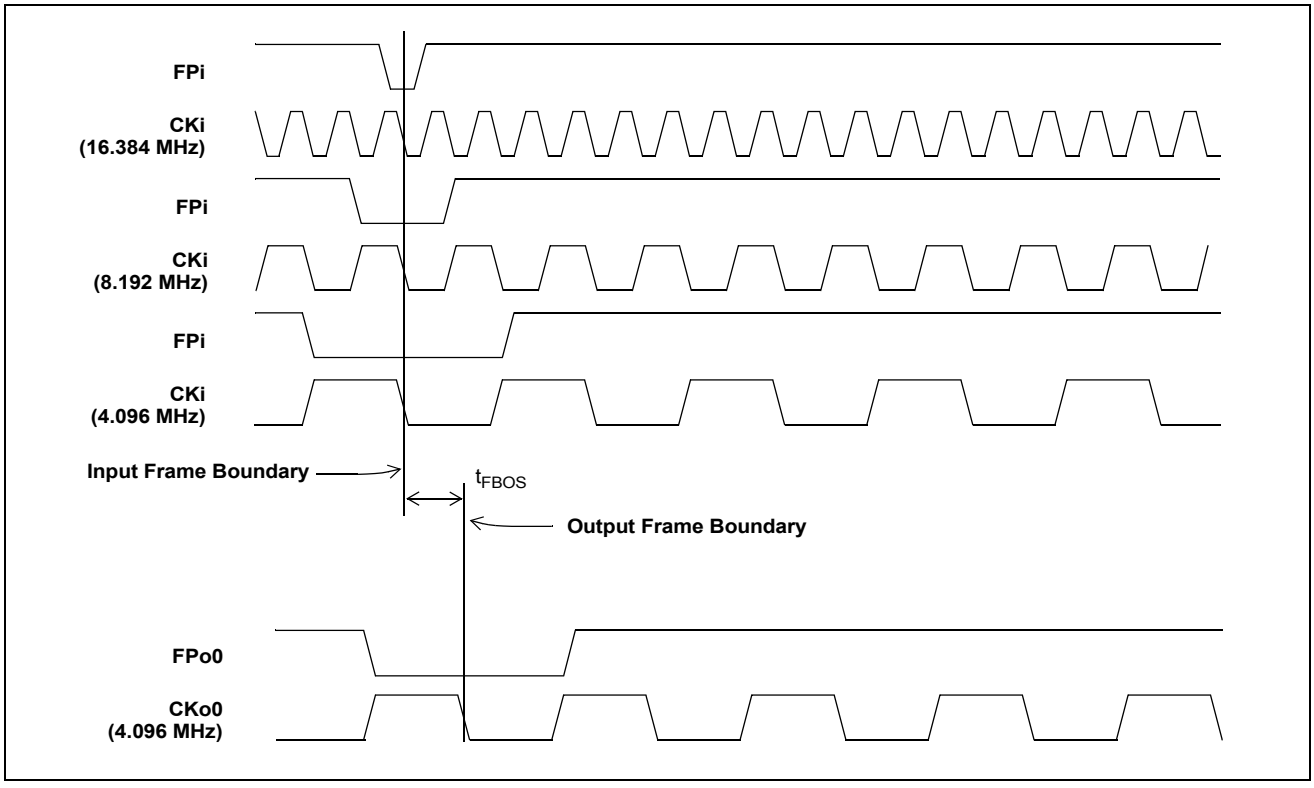


Figure 35 - Input and Output Frame Boundary Offset

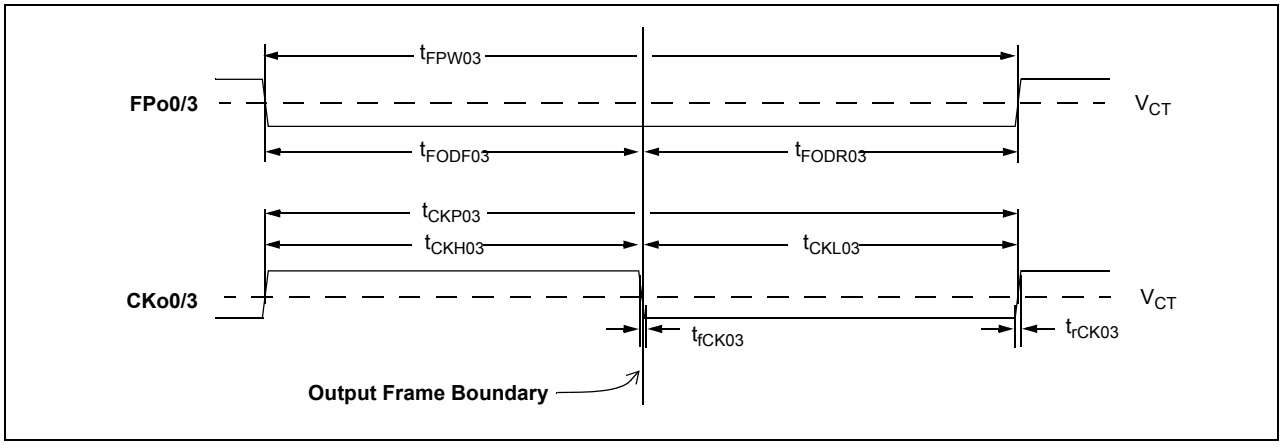


Figure 36 - FPo0 and CKo0 Timing Diagram

AC Electrical Characteristics† - FPo0/CKo0 and FPo3/CKo3 (4.096 MHz) Timing for Divided Clock Mode and Multiplied Clock Mode with Less than 10 ns of Input Cycle to Cycle Variation

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	FPo0 Output Pulse Width	t_{FPW03}	239	244	249	ns	C_L = 30 pF
2	FPo0 Output Delay from the FPo0 falling edge to the output frame boundary	t_{FODF03}	117		127	ns	
3	FPo0 Output Delay from the output frame boundary to the FPo0 rising edge	t_{FODR03}	117		127	ns	
4	CKo0 Output Clock Period	t_{CKP03}	239	244	249	ns	C_L = 30 pF
5	CKo0 Output High Time	t_{CKH03}	117		127	ns	
6	CKo0 Output Low Time	t_{CKL03}	117		127	ns	
7	CKo0 Output Rise/Fall Time	t_{rCK03}, t_{fCK03}			5	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - FPo0/CKo0 and FPo3/CKo3 (4.096 MHz) Timing for Multiplied Clock Mode with More than 10 ns of Cycle to Cycle Variation on CKi

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	FPo0 Output Pulse Width	t_{FPW03}	218	244	270	ns	C_L = 30 pF
2	FPo0 Output Delay from the FPo0 falling edge to the output frame boundary	t_{FODF03}	117		127	ns	
3	FPo0 Output Delay from the output frame boundary to the FPo0 rising edge	t_{FODR03}	97		146	ns	
4	CKo0 Output Clock Period	t_{CKP03}	218	244	270	ns	C_L = 30 pF
5	CKo0 Output High Time	t_{CKH03}	117		127	ns	
6	CKo0 Output Low Time	t_{CKL03}	97		146	ns	
7	CKo0 Output Rise/Fall Time	t_{rCK03}, t_{fCK03}			5	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

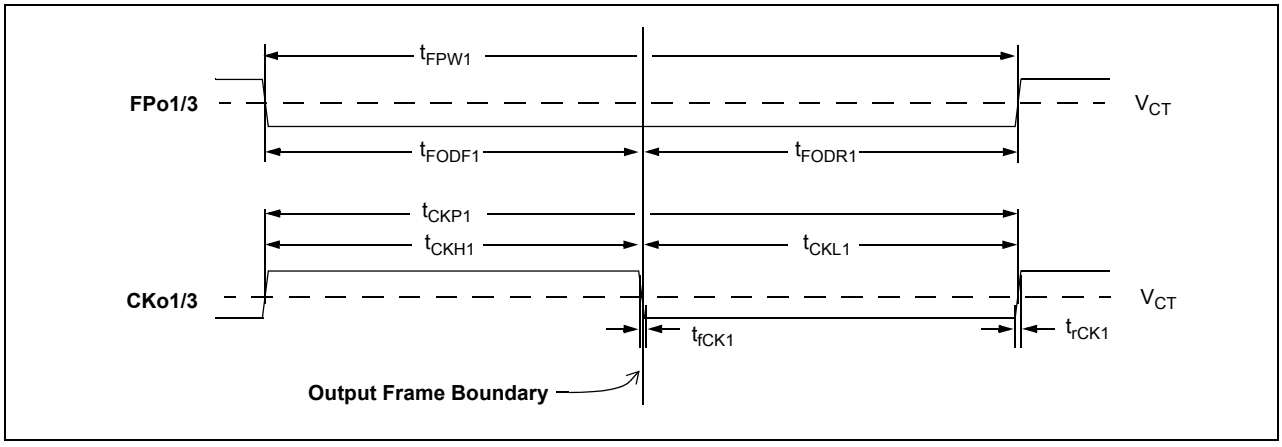


Figure 37 - FPo1 and CKo1 Timing Diagram

AC Electrical Characteristics† - FPo1/CKo1 and FPo3/CKo3 (8.192 MHz) Timing for Divided Clock Mode and Multiplied Clock Mode with Less than 10 ns of Input Cycle to Cycle Variation

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	FPo1 Output Pulse Width	t_{FPW13}	117	122	127	ns	C_L = 30 pF
2	FPo1 Output Delay from the FPo1 falling edge to the output frame boundary	t_{FODF13}	56		66	ns	
3	FPo1 Output Delay from the output frame boundary to the FPo1 rising edge	t_{FODR13}	56		66	ns	
4	CKo1 Output Clock Period	t_{CKP13}	117	122	127	ns	C_L = 30 pF
5	CKo1 Output High Time	t_{CKH13}	56		66	ns	
6	CKo1 Output Low Time	t_{CKL13}	56		66	ns	
7	CKo1 Output Rise/Fall Time	t_{rCK13}, t_{fCK13}			5	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - FPo1/CKo1 and FPo3/CKo3 (8.192 MHz) Timing for Multiplied Clock Mode with More than 10 ns of Cycle to Cycle Variation on CKi

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	FPo1 Output Pulse Width	t_{FPW13}	106	122	127	ns	C_L = 30 pF
2	FPo1 Output Delay from the FPo1 falling edge to the output frame boundary	t_{FODF13}	56		66	ns	
3	FPo1 Output Delay from the output frame boundary to the FPo1 rising edge	t_{FODR13}	46		66	ns	
4	CKo1 Output Clock Period	t_{CKP13}	106	122	148	ns	C_L = 30 pF
5	CKo1 Output High Time	t_{CKH13}	46		87	ns	
6	CKo1 Output Low Time	t_{CKL13}	46		66	ns	
7	CKo1 Output Rise/Fall Time	t_{rCK13}, t_{fCK13}			5	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

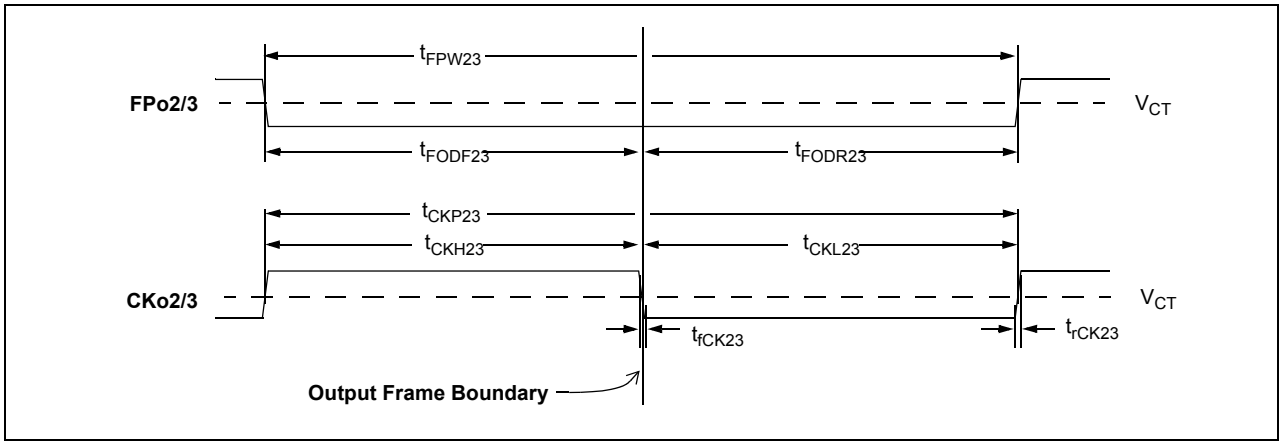


Figure 38 - FPo2 and CKo2 Timing Diagram

AC Electrical Characteristics† - FPo2/CKo2 and FPo3/CKo3 (16.384 MHz) Timing for Divided Clock Mode and Multiplied Clock Mode with Less than 10 ns of Cycle to Cycle Variation on CKi

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	FPo2 Output Pulse Width	t_{FPW23}	56	61	66	ns	C_L = 30 pF
2	FPo2 Output Delay from the FPo2 falling edge to the output frame boundary	t_{FODF23}	25		36	ns	
3	FPo2 Output Delay from the output frame boundary to the FPo1 rising edge	t_{FODR23}	25		36	ns	
4	CKo2 Output Clock Period	t_{CKP23}	56	61	66	ns	C_L = 30 pF
5	CKo2 Output High Time	t_{CKH23}	25		36	ns	
6	CKo2 Output Low Time	t_{CKL23}	25		36	ns	
7	CKo2 Output Rise/Fall Time	t_{rCK23}, t_{fCK23}			5	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - FPo2/CKo2 and FPo3/CKo3 (16.384 MHz) Timing for Multiplied Clock Mode with More than 10 ns of Cycle to Cycle Variation on CKi

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	FPo2 Output Pulse Width	t_{FPW23}	56	61	66	ns	C_L = 30 pF
2	FPo2 Output Delay from the FPo2 falling edge to the output frame boundary	t_{FODF23}	25		36	ns	
3	FPo2 Output Delay from the output frame boundary to the FPo2 rising edge	t_{FODR23}	25		36	ns	
4	CKo2 Output Clock Period	t_{CKP2}	47	61	76	ns	C_L = 30 pF
5	CKo2 Output High Time	t_{CKH23}	17		43	ns	
6	CKo2 Output Low Time	t_{CKL23}	17		43	ns	
7	CKo2 Output Rise/Fall Time	t_{rCK23}, t_{fCK23}			5	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

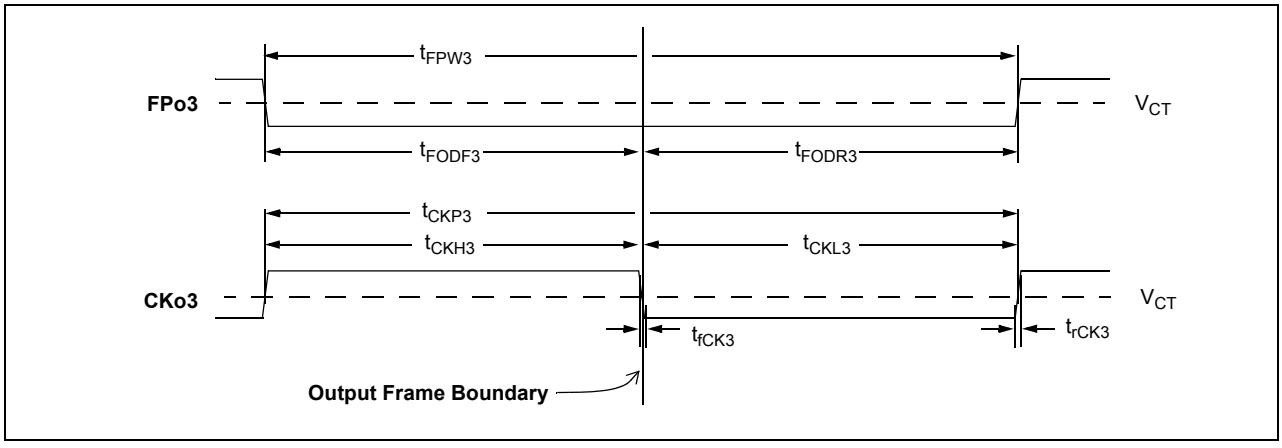


Figure 39 - FPo3 and CKo3 Timing Diagram

AC Electrical Characteristics† - FPo3/CKo3 (32.768 MHz) Timing for Divided Clock Mode and Multiplied Clock Mode with Less than 10 ns of Cycle to Cycle Variation on CKi

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	FPo3 Output Pulse Width	t_{FPW3}	27	30.5	34	ns	C_L = 30 pF
2	FPo3 Output Delay from the FPo3 falling edge to the output frame boundary	t_{FODF3}	10		18	ns	
3	FPo3 Output Delay from the output frame boundary to the FPo3 rising edge	t_{FODR3}	12		21	ns	
4	CKo3 Output Clock Period	t_{CKP3}	27	30.5	34	ns	C_L = 30 pF
5	CKo3 Output High Time	t_{CKH3}	12		19	ns	
6	CKo3 Output Low Time	t_{CKL3}	12		19	ns	
7	CKo3 Output Rise/Fall Time	t_{rCK3}, t_{fCK3}			5	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - FPo3/CKo3 (32.768 MHz) Timing for Multiplied Clock Mode with More than 10 ns of Cycle to Cycle Variation on CKi

	Characteristic	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	FPo3 Output Pulse Width	t_{FPW3}	27	30.5	34	ns	C_L = 30 pF
2	FPo3 Output Delay from the FPo3 falling edge to the output frame boundary	t_{FODF3}	12		19	ns	
3	FPo3 Output Delay from the output frame boundary to the FPo3 rising edge	t_{FODR3}	12		19	ns	
4	CKo3 Output Clock Period	t_{CKP3}	17	30.5	44	ns	C_L = 30 pF
5	CKo3 Output High Time	t_{CKH3}	5		29	ns	
6	CKo3 Output Low Time	t_{CKL3}	12		18	ns	
7	CKo3 Output Rise/Fall Time	t_{rCK3}, t_{fCK3}			5	ns	

† Characteristics are over recommended operating conditions unless otherwise stated.

‡ Typical figures are at 25°C, VDD_CORE at 1.8 V and VDD_IO at 3.3 V and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Divided Clock Mode Output Timing

	Characteristic	Sym.	Min.	Max.	Units
1	CKo0 to CKo1 (8.192 MHz) delay	t_{C1D}	-1	2	ns
2	CKo0 to CKo2 (16.384 MHz) delay	t_{C2D}	-1	3	ns
3	CKo0 to CKo3 (16.384 MHz/8.192 MHz/4.096 MHz) delay	t_{C3D}	-2	2	ns

† Characteristics are over recommended operating conditions unless otherwise stated.

AC Electrical Characteristics† - Multiplied Clock Mode Output Timing

	Characteristic	Sym.	Min.	Max.	Units
1	CKo0 to CKo1 (8.192 MHz) delay	t_{C1D}	-1	2	ns
2	CKo0 to CKo2 (16.384 MHz) delay	t_{C2D}	-1	3	ns
3	CKo0 to CKo3 (32.768 MHz/16.384 MHz/8.192 MHz/4.096 MHz) delay	t_{C3D}	-1	3	ns

† Characteristics are over recommended operating conditions unless otherwise stated.

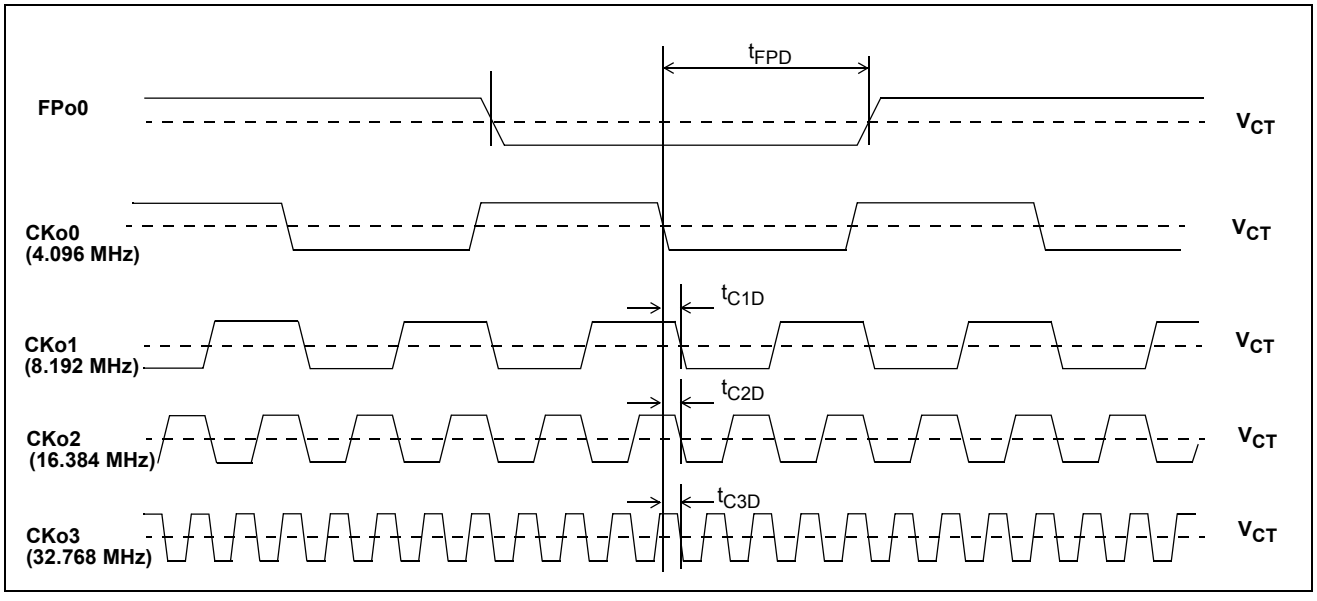
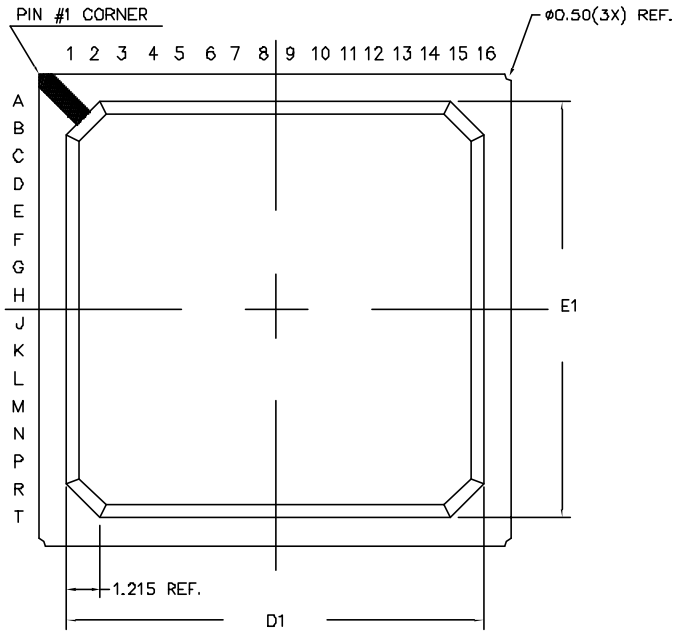
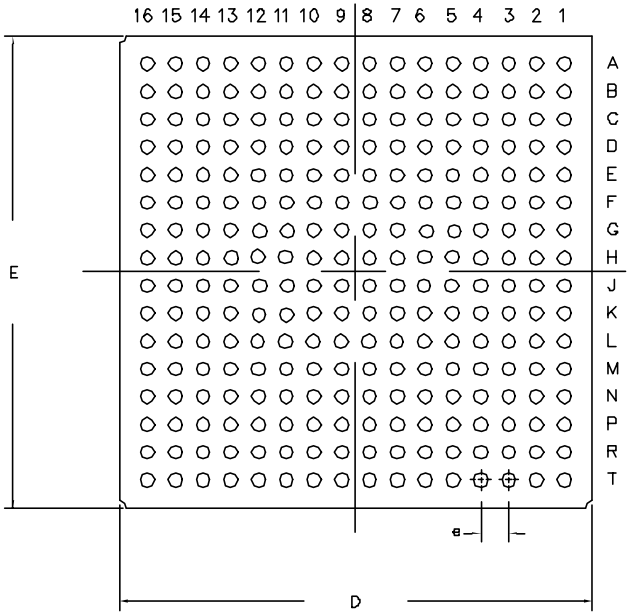


Figure 40 - Output Timing (ST-BUS Format)

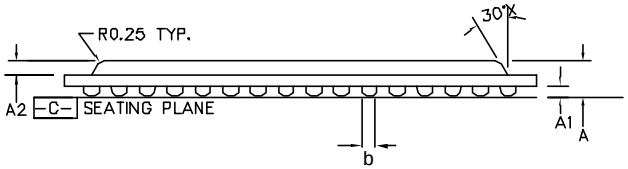
TOP VIEW



BOTTOM VIEW



DIMENSION	MIN	MAX
A	1.42	1.80
A1	0.30	0.50
A2	0.85 REF	
D	16.80	17.20
D1	14.80	15.20
E	16.80	17.20
E1	14.80	15.20
b	0.40	0.60
e	1.00	
N	256	
Conforms to JEDEC MS-034		



SIDE VIEW

NOTES: –
1. Controlling dimensions are in MM.
2. Seating plane is defined by the spherical crown of the solder balls.
3. Not to scale.
4. N is the number of solder balls
5. Substrate thickness is 0.36 MM.

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ISSUE	1			
ACN	214440			
DATE	26June03			
APPRD.				

ZARLINK SEMICONDUCTOR

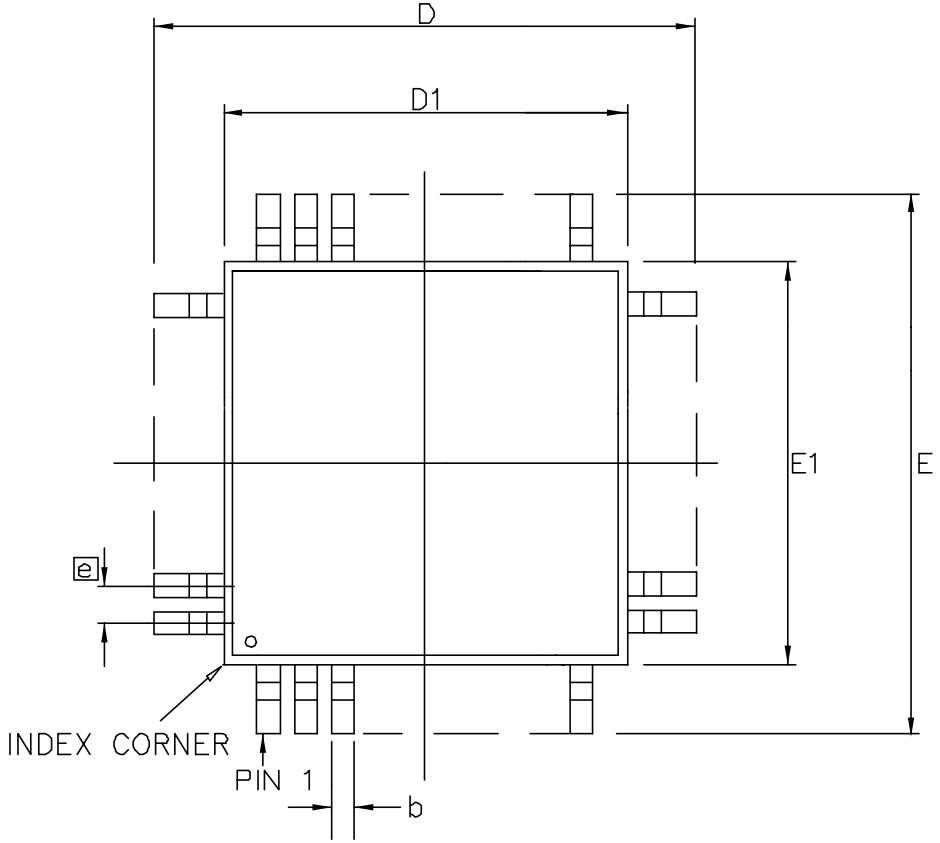
Previous package codes

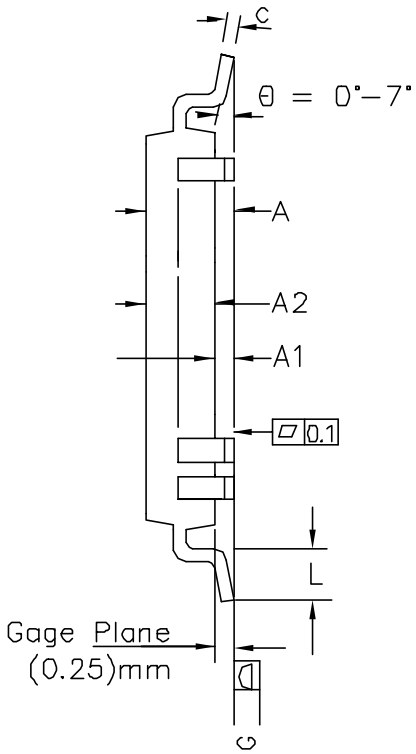
BP/G

Package Code GA

Package Outline for 256ball BGA 17x17x1.61mm

GPD00842





Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	—	1.60		—	0.063
A1	0.05	0.15		0.002	0.006
A2	1.35	1.45		0.053	0.057
D	30.00 BSC			1.181 BSC	
D1	28.00 BSC			1.102 BSC	
E	30.00 BSC			1.181 BSC	
E1	28.00 BSC			1.102 BSC	
L	0.45	0.75		0.018	0.029
e	0.40 BSC			0.016 BSC	
b	0.13	0.23		0.005	0.009
c	0.09	0.20		0.003	0.008
	Pin features				
N	256				
ND	64				
NE	64				
NOTE	SQUARE				

Conforms to JEDEC MS–026 BJC Iss. D

Notes:

1. Pin 1 indicator may be a corner chamfer, dot or both, located within a zone of dimension E1/4 x D1/4 from the index corner
2. All dimensioning and tolerancing conform to ANSI Y14.5–1982.
3. Dimensions D1 and E1 do not include mold protrusion – allowable mold protrusion is 0.254 mm on D1 and E1 dimensions.
4. "N" is the total number of terminals
5. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package
6. Dimension b does not include Dambar protrusion.
7. Controlling Dimensions are in Millimeter
8. A1 is defined as the distance from the seating plane to the lowest point of the package body

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ZARLINK SEMICONDUCTOR

Previous package codes

GP

Package Code QC

Package Outline for 256 lead LQFP (28 x 28 x 1.4mm) 2.0mm Footprint

GPD00837

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