Panasonic

AN32150B

http://www.semicon.panasonic.co.jp/en/

LED Driver LSI with Step-up Charge Pump Control Circuit

FEATURES

- 7 x 7 LED Matrix Driver
  (Total LED that can be driven = 49)
- Step-up charge pump DC/DC converter : 300 mA
- LDO : 2-ch.
- GPIO : 3-ch.
- GPO : 6-ch. (They are in common with LED driver terminals.)
- SPI interface / I²C interface selectable
- LED drivers (for backlight : 7-ch., for RGB : 3-ch., matrix LED driver : 7 × 7-ch.)
- LED brightness control function with an external illumination sensor
- 55pin Wafer Level Chip Size Package (WLCSP)

DESCRIPTION

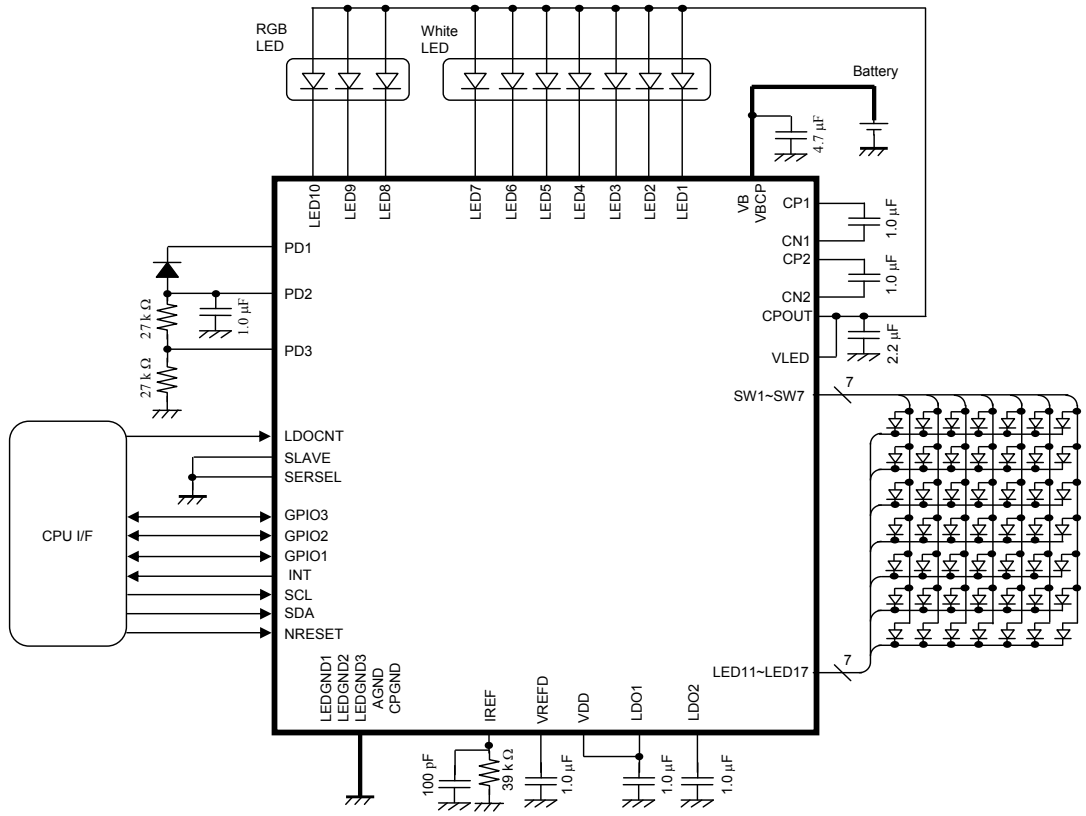
AN32150B is a LED driver and a light intensity controller. It can drive up to 7 channels of LCD backlight, 3 channels of RGB LEDs and 7 channels of LED matrix.

Voltage is supplied by a step-up charge pump DC/DC converter.

APPLICATIONS

- Mobile Phone
- Smart Phone
- PCs
- Game Consoles
- Home Appliances etc.

TYPICAL APPLICATION



Note)
The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Supply voltage	VB_{MAX}	6.0	V	*1
	$VLED_{MAX}$	6.5	V	*1
	VDD_{MAX}	4.3	V	*1
Operating ambience temperature	T_{opr}	– 30 to + 85	°C	*2
Operating junction temperature	T_j	– 30 to + 125	°C	*2
Storage temperature	T_{stg}	– 55 to + 125	°C	*2
Input Voltage Range	GPIO1, GPIO2, GPIO3, PD2, PD3, SERSEL, SLAVE, SCL, SDA	– 0.3 to 4.3	V	—
	NRESET, LDOCNT	– 0.3 to 6.0	V	—
Output Voltage Range	PD1	– 0.3 to 4.3	V	—
	LDO1, LDO2, INT	– 0.3 to 6.0	V	—
	SW1, SW2, SW3, SW4, SW5, SW6, SW7, LED1, LED2, LED3, LED4, LED5, LED6, LED7, LED8, LED9, LED10, LED11, LED12, LED13, LED14, LED15, LED16, LED17	– 0.3 to 6.5	V	—
ESD	HBM	1.0 to 1.5	kV	—

Note) This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

*1: VB_{MAX} = VBCP = VB, VDD_{MAX} = VDD , $VLED_{MAX}$ = VLED
The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.

POWER DISSIPATION RATING

PACKAGE	θ_{JA}	P_D (Ta=25 °C)	P_D (Ta=85 °C)
55 pin Wafer Level Chip Size Package (WLCSP)	120.02 °C /W	0.833 W	0.333 W

Note) For the actual usage, please refer to the P_D-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

CAUTION

Although this LSI has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage range	VB	3.1	3.6	4.6	V	*1
	VLED	3.1	4.5	5.8	V	*1
	VDD	1.7	1.85	3.2	V	*1
Input Voltage Range	GPIO1, GPIO2, GPIO3, PD2, PD3, SERSEL, SLAVE, SCL, SDA	– 0.3	—	VDD + 0.3	V	*2
	NRESET, LDOCNT	– 0.3	—	VB + 0.3	V	*2
Output Voltage Range	PD1	– 0.3	—	VDD + 0.3	V	*2
	LDO1, LDO2, INT	– 0.3	—	VB + 0.3	V	*2
	SW1, SW2, SW3, SW4, SW5, SW6, SW7, LED1, LED2, LED3, LED4, LED5, LED6, LED7, LED8, LED9, LED10, LED11, LED12, LED13, LED14, LED15, LED16, LED17	– 0.3	—	VLED + 0.3	V	*2

Note) *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
Do not apply external currents and voltages to any pin not specifically mentioned.
Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for AGND, CPGND, LEDGND1, LEDGND2 and LEDGND3.
VDD is voltage for VDD. VB is voltage for VB and VBCP. VLED is voltage for VLED.
*2: (VDD + 0.3) V must not exceed 4.3 V. (VB + 0.3) V must not exceed 6 V.
(VLED + 0.3) V must not exceed 6.5 V.

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ELECTRICAL CHARACTERISTICS

VB = VBCP = 3.6 V, VLED = 4.5 V, VDD = 1.85 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current consumption							
Current consumption (1) at OFF mode	ICC1	VB = 4.6 V LDOCNT = Low	—	0	1	μA	—
Current consumption (2) at LDO1 and LDO2 normal mode	ICC2	LDO1 to 2PS = [0] (LDO1, 2 normal mode) LDO1ON = [1] (LDO1 ON) VB = 4.6 V LDOCNT = High	—	130	300	μA	—
Current consumption (3) at LDO1 OFF mode, LDO2 power save mode	ICC3	LDO2 PS = [1] (LDO2 power save mode) LDO1ON = [0] (LDO1 OFF) VB = 4.6 V LDOCNT = High	—	10	25	μA	—
Current consumption (4) at VB through mode, LDO1 OFF mode, LDO2 power save mode	ICC4	LDO2 PS = [1] (LDO2 power save mode) LDO1ON = [0] (LDO1 OFF) VB = 4.6 V LDOCNT = High VB through mode I_{CPOUT} = 0 mA LED10ON = [1] (Current 0)	—	1.0	3.0	mA	—
Current consumption (5) at charge pump 1.5× (600 kHz operating) mode, LDO1 OFF mode, LDO2 power save mode	ICC5	LDO2 PS = [1] (LDO2 power save mode) LDO1ON = [0] (LDO1 OFF) VB = 3.1 V LDOCNT = High LED10ON = [1] (current 0) Charge Pump ON, 1.5×, 600 kHz operating mode I_{CPOUT} = 0 mA	—	2.0	5.0	mA	—

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ELECTRICAL CHARACTERISTICS (continued)

VB = VBCP = 3.6 V, VLED = 4.5 V, VDD = 1.85 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current consumption							
Current consumption (6) at charge pump 1.5× (1.2 MHz operating) mode, LDO1 OFF mode, LDO2 power save mode	ICC6	LDO2 PS = [1] (LDO2 power save mode) LDO1ON = [0] (LDO1 OFF) VB = 3.1 V LDOCNT = High LED10ON = [1] (current 0) Charge Pump ON, 1.5×, 1.2 MHz operating mode I_{CPOUT} = 0 mA	—	5.0	9.0	mA	—
Reference voltage							
Output voltage	VREF	VB = 3.1 V to 4.6 V	1.21	1.24	1.27	V	—
Voltage regulator (LDO1) normal mode Ioutmax = –100 mA							
Output voltage (1) 1.85 V mode	VL11	VB = 3.1 V to 4.6 V I_{LDO1} = –10 µA to –100 mA	1.79	1.85	1.91	V	—
Output voltage (2) 2.85 V mode	VL12	VB = 3.1 V to 4.6 V I_{LDO1} = –10 µA to –100 mA	2.76	2.85	2.94	V	—
Short circuit protection current (1) 1.85 V mode	IPT11	LDOCNT = High V_{LDO1} = 0 V	20	50	150	mA	—
Short circuit protection current (2) 2.85 V mode	IPT12	LDOCNT = High V_{LDO1} = 0 V	20	50	150	mA	—
Ripple rejection (1) 1.85 V mode	PSL11	VB = 3.6 V + 0.2 V[p-p] f = 1 kHz I_{LDO1} = –50 mA PSL11 = 20 log(acV_{LDO1} / 0.2)	—	–70	–60	dB	—
Ripple rejection (2) 1.85 V mode	PSL12	VB = 3.6 V + 0.2 V[p-p] f = 10 kHz I_{LDO1} = –50 mA PSL12 = 20 log(acV_{LDO1} / 0.2)	—	–60	–50	dB	—
Ripple rejection (3) 2.85 V mode	PSL13	VB = 3.6 V + 0.2 V[p-p] f = 1 kHz I_{LDO1} = –50 mA PSL13 = 20 log(acV_{LDO1} / 0.2)	—	–70	–60	dB	—
Ripple rejection (4) 2.85 V mode	PSL14	VB = 3.6 V + 0.2 V[p-p] f = 10 kHz I_{LDO1} = –50 mA PSL14 = 20 log(acV_{LDO1} / 0.2)	—	–60	–50	dB	—

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ELECTRICAL CHARACTERISTICS (continued)

VB = VBCP = 3.6 V, VLED = 4.5 V, VDD = 1.85 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Voltage regulator (LDO1) power save mode : Ioutmax = – 15 mA (Ioutmax = – 5 mA at 2.85 V setting)							
Output voltage (1)	VLPS11	VB = 3.1 V to 4.6 V I_{LDO1} = – 10 µA to – 15 mA	1.79	1.85	1.91	V	—
Output voltage (2)	VLPS12	VB = 3.1 V to 4.6 V I_{LDO1} = – 10 µA to – 5 mA	2.76	2.85	2.94	V	—
Voltage regulator (LDO2) normal mode Ioutmax = – 100 mA							
Output voltage	VL2	VB = 3.1 V to 4.6 V I_{LDO2} = – 10 µA to – 100 mA	2.76	2.85	2.94	V	—
Short circuit protection current	IPT2	LDOCNT = High V_{LDO2} = 0 V	20	50	150	mA	—
Ripple rejection (1)	PSL21	VB = 3.6 V + 0.2 V[p-p] f = 1 kHz I_{LDO2} = – 50 mA PSL21 = 20 log(acV_{LDO2} / 0.2)	—	– 70	– 60	dB	—
Ripple rejection (2)	PSL22	VB = 3.6 V +0.2 V[p-p] f = 10 kHz I_{LDO2} = – 50 mA PSL22 = 20 log(acV_{LDO2} / 0.2)	—	– 60	– 50	dB	—
Voltage regulator (LDO2) power save mode Ioutmax = – 5 mA							
Output voltage	VLPS2	VB = 3.1 V to 4.6 V I_{LDO2} = – 10 µA to – 5 mA	2.76	2.85	2.94	V	—

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ELECTRICAL CHARACTERISTICS (continued)

VB = VBCP = 3.6 V, VLED = 4.5 V, VDD = 1.85 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Charge pump DC/DC converter							
Oscillator frequency	FDC1	VB = 3.1 V to 4.6 V	1.92	2.40	2.88	MHz	—
VB through switch							
Resistance at switch ON	RVBS	VB = 4.5 V I_{CPOUT} = – 30 mA RVBS = (V_{VBCP} – V_{CPOUT}) / 30 mA	—	0.6	1	Ω	—
SCAN switch							
Resistance at switch ON	RSCAN	VLED = 4.5 V I_{SW1} to I_{SW7} = 20 mA RSCAN = V_{SW1} to V_{SW7} / 20 mA	—	1	2	Ω	—
Current regulator (LED1 to 7)							
Output current (1)	IBL1	At 31.750 mA setting V_{LED1} to V_{LED7} = 1 V IBL1 = I_{LED1} to I_{LED7}	30.132	31.718	33.304	mA	*1
Output current (2)	IBL2	At 1 mA setting V_{LED1} to V_{LED7} = 1 V IBL2 = I_{LED1} to I_{LED7}	0.948	0.998	1.048	mA	*1
Current step	IBSTEP	Minimum current step	0	125	250	μA	—
Off leak current	IBLOFF	OFF setting V_{LED1} to V_{LED7} = 4.5 V IBLOFF = I_{LED1} to I_{LED7}	—	—	1	μA	—
Error between channels	IBLCH	At 16 mA setting Current error between each channel and the median of LED1 to LED7	– 5	—	5	%	—

Note) *1 : Allowable value at the time when the recommended parts (ERJ2RHD393X) is connected to IREF.

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ELECTRICAL CHARACTERISTICS (continued)

VB = VBCP = 3.6 V, VLED = 4.5 V, VDD = 1.85 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current regulator (LED8 to 10)							
Output current (1)	IRGB1	At 31.750 mA setting V_{LED8} to V_{LED10} = 1 V IRGB1 = I_{LED8} to I_{LED10}	30.087	31.671	33.254	mA	*1
Output current (2)	IRGB2	At 1 mA setting V_{LED8} to V_{LED10} = 1 V IRGB2 = I_{LED8} to I_{LED10}	0.946	0.996	1.046	mA	*1
Current step	IRGBSTEP	Minimum current step	0	125	250	µA	—
Off leak current	IRGBOFF	OFF setting V_{LED8} to V_{LED10} = 4.5 V IRGBOFF = I_{LED8} to I_{LED10}	—	—	1	µA	—
Error between channels	IRGBCH	At 16 mA setting Current error between each channel and the median of LED8 to LED10	–5	—	5	%	—
Current regulator (LED11 to 17)							
Output current (1)	IMX1	At 1 mA setting V_{LED11} to V_{LED17} = 1 V IMX1 = I_{LED11} to I_{LED17}	0.943	0.993	1.043	mA	*1
Output current (2)	IMX2	At 2 mA setting V_{LED11} to V_{LED17} = 1 V IMX2 = I_{LED11} to I_{LED17}	1.891	1.990	2.090	mA	*1
Output current (3)	IMX3	At 4 mA setting V_{LED11} to V_{LED17} = 1 V IMX3 = I_{LED11} to I_{LED17}	3.768	3.966	4.164	mA	*1
Output current (4)	IMX4	At 8 mA setting V_{LED11} to V_{LED17} = 1 V IMX4 = = I_{LED11} to I_{LED17}	7.558	7.956	8.354	mA	*1
Output current (5)	IMX5	At 15 mA setting V_{LED11} to V_{LED17} = 1 V IMX5 = = I_{LED11} to I_{LED17}	14.172	14.918	15.663	mA	*1
Off leak current	IMXOFF	OFF setting V_{LED11} to V_{LED17} = 4.5 V IMXOFF = I_{LED11} to I_{LED17}	—	—	1	µA	—
Error between channels	IMXCH	At 15 mA setting Current error between each channel and the median of LED11 to LED17	– 5	—	5	%	—

Note) *1 : Allowable value at the time when the recommended parts (ERJ2RHD393X) is connected to IREF.

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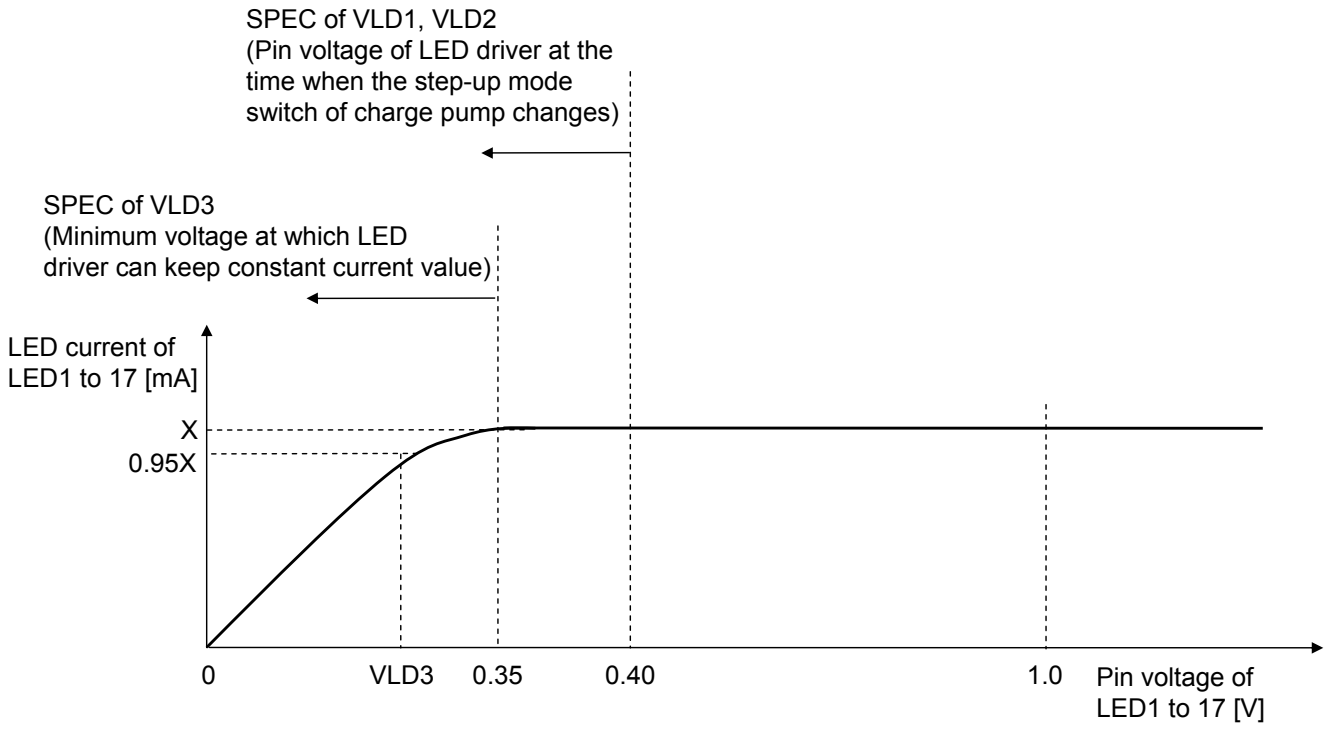
ELECTRICAL CHARACTERISTICS (continued)

VB = VBCP = 3.6 V, VLED = 4.5 V, VDD = 1.85 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Overvoltage detection							
Detection voltage	VOV	Charge pump DC/DC overvoltage detection	5.3	5.5	5.7	V	—
Step-up mode switch of charge pump							
Detection voltage (1)	VLD1	LED1 to LED7 pin voltage at the time when the step-up mode switch of charge pump changes	—	0.35	0.40	V	—
Detection voltage (2)	VLD2	LED8, 9 and 10 pin voltage at the time when the step-up mode switch of charge pump changes	—	0.35	0.40	V	—
Minimum voltage at which LED driver can keep constant current value							
Minimum voltage at which LED driver can keep constant current value	VLD3	95% LED current value at the time when LED1 to LED17 pin voltage is set to 1 V. Minimum value of LED1 to LED17 pin voltage	—	0.20	0.35	V	—



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ELECTRICAL CHARACTERISTICS (continued)

VB = VBCP = 3.6 V, VLED = 4.5 V, VDD = 1.85 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
GPIO I/F							
High-level input voltage range (1) at 1.85 V mode operation	VIH1	High-level recognition voltage of GPIO1 to 3. IOVSEL1 to 3 = [1] (Output voltage LDO1 level setting) LDO1VSEL = [0]	1.5	—	LDO1 + 0.3	V	—
Low-level input voltage range (1) at 1.85 V mode operation	VIL1	Low-level recognition voltage of GPIO1 to 3. IOVSEL1 to 3 = [1] (Output voltage LDO1 level setting) LDO1VSEL = [0]	– 0.3	—	0.4	V	—
High-level input voltage range (2) at 2.85 V mode operation	VIH2	High-level recognition voltage of GPIO1 to 3. LDO1VSEL = [1]	2.3	—	LDO1 + 0.3	V	—
Low-level input voltage range (2) at 2.85 V mode operation	VIL2	Low-level recognition voltage of GPIO1 to 3. LDO1VSEL = [1]	– 0.3	—	0.6	V	—
High-level input current	IIH1	V_{GPIO1} to V_{GPIO3} = 2.85 V IIH1 = I_{GPIO1} to I_{GPIO3}	—	0	1	µA	—
Low-level input current	IIL1	V_{GPIO1} to V_{GPIO3} = 0 V IIL1 = I_{GPIO1} to I_{GPIO3}	—	0	1	µA	—
High-level output voltage (1)	VOH1	V_{GPIO1} to V_{GPIO3} = – 2 mA IOVSEL1 to 3 = [0] (Output voltage LDO2 level setting)	LDO2 × 0.8	—	—	V	—
Low-level output voltage (1)	VOL1	I_{GPIO1} to I_{GPIO3} = 2 mA IOVSEL1 to 3 = [0] (Output voltage LDO2 level setting)	—	—	LDO2 × 0.2	V	—
High-level output voltage (2)	VOH2	I_{GPIO1} to I_{GPIO3} = – 2 mA IOVSEL1 to 3 = [1] (Output voltage LDO1 level setting)	LDO1 × 0.8	—	—	V	—
Low-level output voltage (2)	VOL2	I_{GPIO1} to I_{GPIO3} = 2 mA IOVSEL1 ~ 3 = [1] (Output voltage LDO1 level setting)	—	—	LDO1 × 0.2	V	—
Pull-down resistance	RPD	I_{GPIO1} to I_{GPIO3} = 5 µA RPD = V_{GPIO1} to V_{GPIO3} / 5 µA	60	110	210	kΩ	—

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ELECTRICAL CHARACTERISTICS (continued)

VB = VBCP = 3.6 V, VLED = 4.5 V, VDD = 1.85 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
LDOCNT							
High-level input voltage range	VIH3	High-level recognition voltage	1.6	—	VB + 0.3	V	—
Low-level input voltage range	VIL3	Low-level recognition voltage	– 0.3	—	0.4	V	—
High-level input current	IIH2	V_{LDOCNT} = 3.6 V	—	0	1	μA	—
Low-level input current	IIL2	V_{LDOCNT} = 0 V	—	0	1	μA	—
NRESET							
High-level input voltage range	VIH4	High-level recognition voltage	1.5	—	VB + 0.3	V	—
Low-level input voltage range	VIL4	Low-level recognition voltage	– 0.3	—	0.6	V	—
High-level input current	IIH3	V_{NRESET} = 3.6 V	—	0	1	μA	—
Low-level input current	IIL3	V_{NRESET} = 0 V	—	0	1	μA	—
INT							
ON resistance	RINTON	I_{INT} = 5 mA RINTON = V_{INT} / 5 mA	—	—	50	Ω	—

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ELECTRICAL CHARACTERISTICS (continued)

VB = VBCP = 3.6 V, VLED = 4.5 V, VDD = 1.85 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
I²C I/F							
High-level input voltage	VIH5	High-level recognition voltage of SDA, SCL	0.7 × VDD	—	VDD + 0.5, 3.2	V	*2
Low-level input voltage	VIL5	Low-level recognition voltage of SDA, SCL	– 0.5	—	0.3 × VDD	V	—
Low-level output voltage 1	VOL3	VDD > 2 V I_{SDA} = 3 mA	0	—	0.4	V	—
Low-level output voltage 2	VOL4	VDD < 2 V I_{SDA} = 3 mA	0	—	0.2 × VDD	V	—
Input current each I/O pin	Ii	V_{SDA}, V_{SCL} = 0.1 V to 2.88 V	– 10	0	10	μA	—
SCL clock frequency	f_{SCL}	—	0	—	400	kHz	—
Light Intensity Control							
PD1 pin ON resistance	RPD1ON	—	—	—	100	Ω	—
PD3 pin ON resistance	RPD3ON	—	—	—	50	Ω	—
A/D converted value (1)	AD1	V_{PD2} = VLPS2 / 256 Read value of the register, ADC_DATA[9:2]	—	1	5	LSB	—
A/D converted value (2)	AD2	V_{PD2} = VLPS2 × 128 / 256 Read value of the register, ADC_DATA[9:2]	124	128	132	LSB	—
A/D converted value (3)	AD3	V_{PD2} = VLPS2 × 255 / 256 Read value of the register, ADC_DATA[9:2]	251	255	—	LSB	—

Note) *2 : Maximum value of High-level input voltage range is the lower one of (VDD + 0.5 V) and 3.2 V.

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ELECTRICAL CHARACTERISTICS (continued)

VB = VBCP = 3.6 V, VLED = 4.5 V, VDD = 1.85 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current consumption							
Current consumption (1) at OFF mode	ICC1	VB = 3.1 V to 4.6 V LDOCNT = Low	—	0	—	μA	*3
Current consumption (2) at LDO1 and LDO2 normal mode	ICC2	LDO1 to 2PS = [0] (LDO1, 2 normal mode) LDO1ON = [1] (LDO1 ON) VB = 3.1 V to 4.6 V LDOCNT = High	—	130	—	μA	*3
Current consumption (3) at LDO1 OFF mode, LDO2 power save mode	ICC3	LDO2 PS = [1] (LDO2 power save mode) LDO1ON = [0] (LDO1 OFF) VB = 3.1 V to 4.6 V LDOCNT = High	—	10	—	μA	*3
Current consumption (4) at VB through mode, LDO1 OFF mode, LDO2 power save mode	ICC4	LDO2 PS = [1] (LDO2 power save mode) LDO1ON = [0] (LDO1 OFF) VB = 3.1 V to 4.6 V LDOCNT = High VB through mode I_{CPOUT} = 0 mA LED10ON = [1] (Current 0)	—	1.0	—	mA	*3

Note) *3 : Typical Design Value

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ELECTRICAL CHARACTERISTICS (continued)

VB = VBCP = 3.6 V, VLED = 4.5 V, VDD = 1.85 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Voltage regulator (LDO1) power save mode loutmax = – 15 mA (loutmax = – 5 mA at 2.85 V setting)							
Ripple rejection (1) at power save mode	PSL11	1.85 V mode VB = 3.6 V + 0.2 V[p-p] f = 1 kHz I_{LDO1} = – 7.5 mA PSL11 = 20 log(acV_{LDO1} / 0.2)	—	– 40	—	dB	*3
Ripple rejection (2) at power save mode	PSL12	1.85 V mode VB = 3.6 V + 0.2 V[p-p] f = 10 kHz I_{LDO1} = – 7.5 mA PSL12 = 20 log(acV_{LDO1} / 0.2)	—	– 30	—	dB	*3
Voltage regulator (LDO2) power save mode loutmax = – 5 mA							
Ripple rejection (1) at power save mode	PSL21	VB = 3.6 V + 0.2 V[p-p] f = 1 kHz I_{LDO2} = – 2.5 mA PSL21 = 20 log(acV_{LDO2} / 0.2)	—	– 40	—	dB	*3
Ripple rejection (2) at power save mode	PSL22	VB = 3.6 V + 0.2 V[p-p] f = 10 kHz I_{LDO2} = – 2.5 mA PSL22 = 20 log(acV_{LDO2} / 0.2)	—	– 30	—	dB	*3

Note) *3 : Typical Design Value

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ELECTRICAL CHARACTERISTICS (continued)

VB = VBCP = 3.6 V, VLED = 4.5 V, VDD = 1.85 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
I²C I/F							
Hysteresis of Schmitt trigger input 1	Vhys1	V_{DD} > 2 V, Hysteresis voltage of SDA, SCL	0.05 × VDD	—	—	V	*4 *5
Hysteresis of Schmitt trigger input 2	Vhys2	V_{DD} < 2 V, Hysteresis voltage of SDA, SCL	0.1 × VDD	—	—	V	*4 *5
Output fall time from V_{IHmin} to V_{ILmax}	Tof	Bus capacitance : 10 pF to 400 pF $I_P \leq 6$ mA (V_{OLmax} = 0.6 V) I_P : Max. sink current	20 + 0.1 × C_b	—	250	ns	*4 *5
Pulse width of spikes which must be suppressed by the input filter	Tsp	—	0	—	50	ns	*4 *5
Capacitance for each I/O pin	Ci	—	—	—	10	pF	*4 *5

Note) *4 : The timing of Fast-mode Plus devices in I²C-bus is specified in Page.19. All values referred to V_{IHMIN} and V_{ILMAX} level.
*5 : These are values checked by design but not production tested.

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ELECTRICAL CHARACTERISTICS (continued)

VB = VBCP = 3.6 V, VLED = 4.5 V, VDD = 1.85 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
I²C I/F (continued)							
Hold time (repeated)	$t_{HD:STA}$	The first clock pulse is generated after $t_{HD:STA}$	0.6	—	—	µs	*4 *5
Low period of the SCL clock	t_{LOW}	—	1.3	—	—	µs	*4 *5
High period of the SCL clock	t_{HIGH}	—	0.6	—	—	µs	*4 *5
Set-up time for a repeat START condition	$t_{SU:STA}$	—	0.6	—	—	µs	*4 *5
Data hold time	$t_{HD:DAT}$	—	0	—	0.9	µs	*4 *5
Data set-up time	$t_{SU:DAT}$	—	100	—	—	ns	*4 *5
Rise time of both SDA and SCL signals	tr	—	20 + 0.1 × C_b	—	300	ns	*4 *5
Fall time of both SDA and SCL signals	t_f	—	20 + 0.1 × C_b	—	300	ns	*4 *5
Set-up time of STOP condition	$t_{SU:STO}$	—	0.6	—	—	µs	*4 *5
Bus free time between a STOP and START condition	t_{BUF}	—	1.3	—	—	µs	*4 *5
Capacitive load for each bus line	C_b	—	—	—	400	pF	*4 *5
Noise margin at the Low-level for each connected device	V_{aL}	—	0.1 × VDD	—	—	V	*4 *5
Noise margin at the High-level for each connected device	V_{aH}	—	0.2 × VDD	—	—	V	*4 *5

Note) *4 : The timing of Fast-mode Plus devices in I²C-bus is specified in Page.19. All values referred to V_{IHMIN} and V_{ILMAX} level.
*5 : These are values checked by design but not production tested.

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ELECTRICAL CHARACTERISTICS (continued)

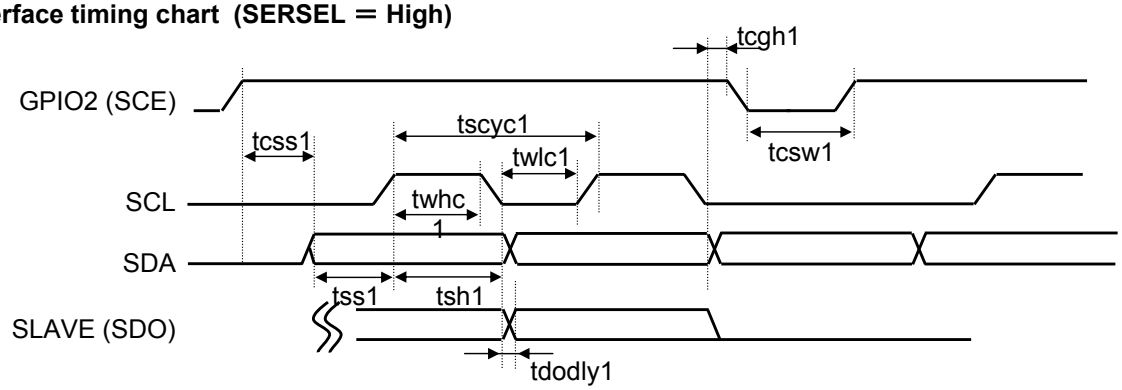
VB = VBCP = 3.6 V, VLED = 4.5 V, VDD = 1.85 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SPI interface characteristics (VDD = 1.85 V ± 3%) Reception timing							
SCL cycle time	tscyc1	—	—	152	—	ns	*3
SCL cycle time High period	twhc1	—	—	70	—	ns	*3
SCL cycle time Low period	twlc1	—	—	70	—	ns	*3
Serial data setup time	tss1	—	—	62	—	ns	*3
Serial data hold time	tsh1	—	—	62	—	ns	*3
Transmitting and receiving interval	tcsw1	—	—	62	—	ns	*3
Chip enable setup time	tcss1	—	—	5	—	ns	*3
Chip enable hold time	tcgh1	—	—	5	—	ns	*3
SPI interface characteristics (VDD = 1.85 V ± 3%) Transmission timing							
SCL cycle time	tscyc1	—	—	152	—	ns	*3
SCL cycle time High period	twhc1	—	—	70	—	ns	*3
SCL cycle time Low period	twlc1	—	—	70	—	ns	*3
Serial data setup time	tss1	—	—	62	—	ns	*3
Serial data hold time	tsh1	—	—	62	—	ns	*3
Transmitting and receiving interval	tcsw1	—	—	62	—	ns	*3
Chip enable setup time	tcss1	—	—	5	—	ns	*3
Chip enable hold time	tcgh1	—	—	5	—	ns	*3
DC delay time	tdodly1	Only read mode	—	30	—	ns	*3

Note) *3 : Typical Design Value

SPI interface timing chart (SERSEL = High)



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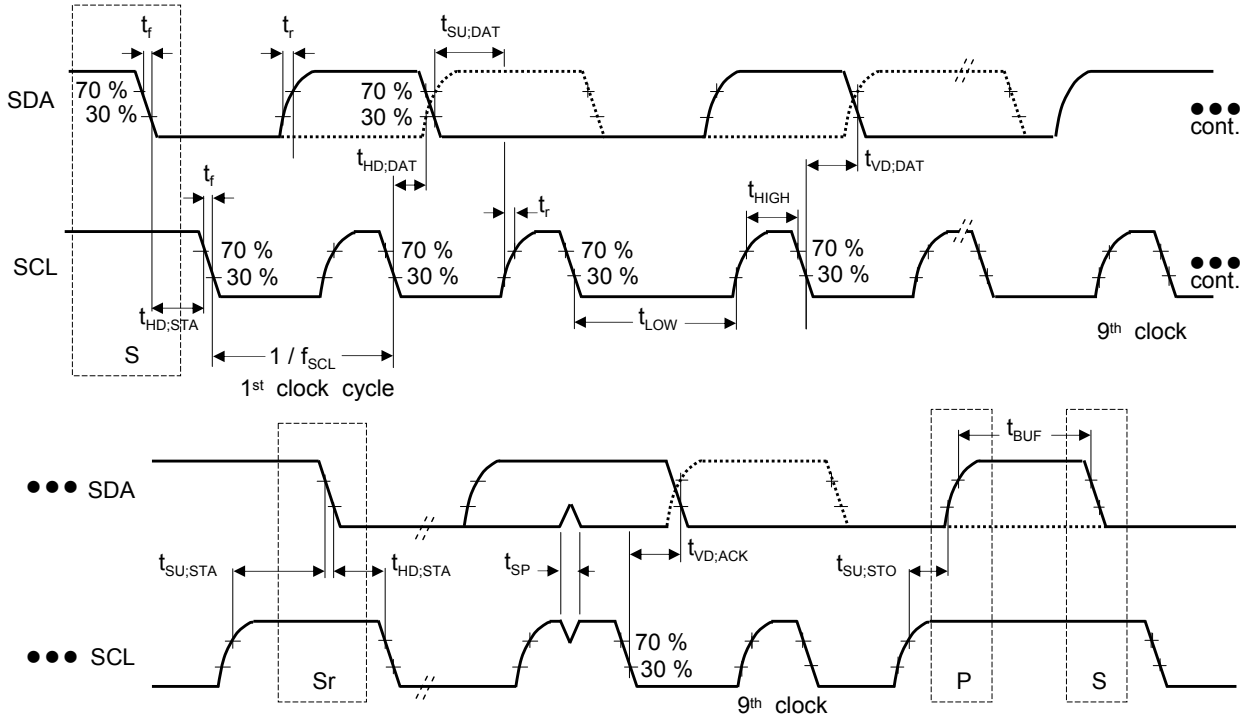
ELECTRICAL CHARACTERISTICS (continued)

VB = VBCP = 3.6 V, VLED = 4.5 V, VDD = 1.85 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified



V_{ILMAX} = 0.3 V_{DD}

V_{IHMIN} = 0.7 V_{DD}

S : START condition

Sr : Repeat START condition

P : STOP condition

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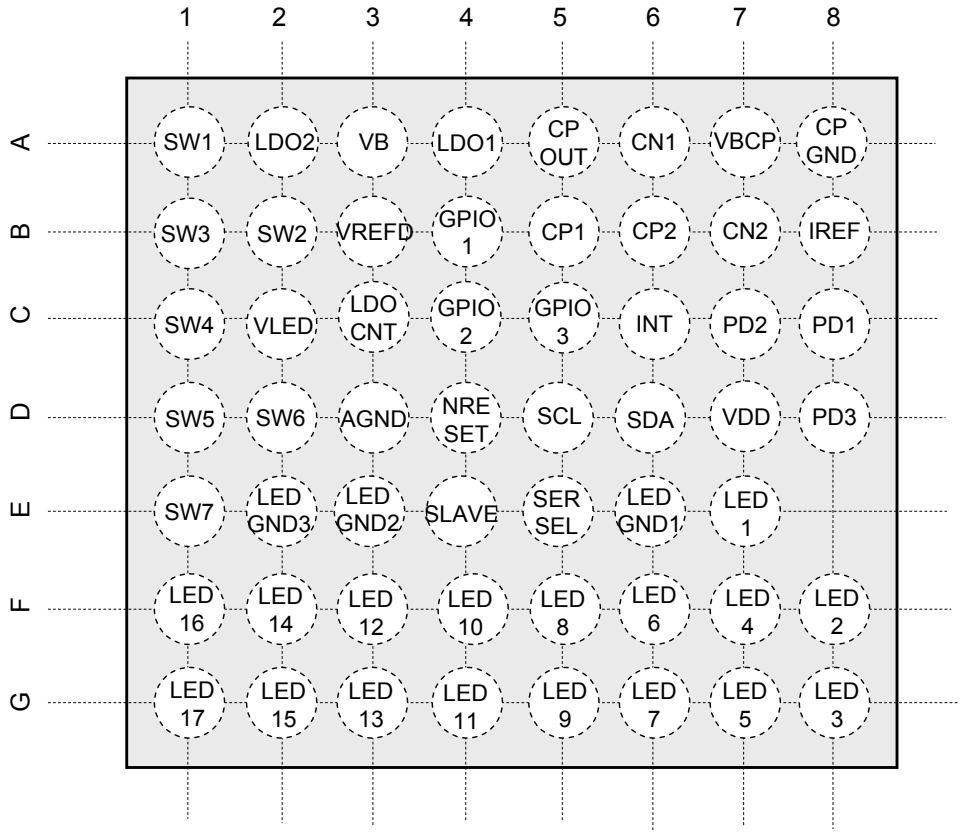
PIN CONFIGURATION

TOP VIEW



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PIN FUNCTIONS

Pin No.	Pin name	Type	Description	Pin processing at unused
A1	SW1	Output	Control switch pin for matrix driver Connected to A column of matrix LED.	Open
A2	LDO2	Output	LDO2 (2.85 V) output pin	(Required pin)
A3	VB	Power supply	Power supply connection pin for BGR and LDO circuits	(Required pin)
A4	LDO1	Output	LDO1 (1.85 V / 2.85 V) output pin (Default : 1.85 V output)	(Required pin)
A5	CPOUT	Output	Charge pump output pin (Output pin for VB through SW)	Open
A6	CN1	Output	Capacitor connection pin for charge pump DC/DC converter	Open
A7	VBCP	Power supply	Power supply connection pin for charge pump DC/DC converter and for through switch	(Required pin)
A8	CPGND	Ground	GND for charge pump DC/DC converter	Connect to GND
B1	SW3	Output	Control switch pin for matrix driver Connected to C column of matrix LED.	Open
B2	SW2	Output	Control switch pin for matrix driver Connected to B column of matrix LED.	Open
B3	VREFD	Output	Capacitor connection pin for BGR circuit	(Required pin)
B4	GPIO1	Input / Output	GPIO input / output port pin (Default input mode with pull-down)	Recommended to connect to GND
B5	CP1	Output	Capacitor connection pin for charge pump DC/DC converter	Open
B6	CP2	Output	Capacitor connection pin for charge pump DC/DC converter	Open
B7	CN2	Output	Capacitor connection pin for charge pump DC/DC converter	Open
B8	IREF	Output	Resistor connection pin for constant current setup	(Required pin)
C1	SW4	Output	Control switch pin for matrix driver Connected to D column of matrix LED.	Open
C2	VLED	Power supply	Power supply for matrix driver Connected to the output of battery or step-up charge pump DC/DC converter.	Connect to VBAT or CPOUT (Open disabled)
C3	LDOCNT	Input	BGR circuit, ON/OFF control pin of LDO1 and LDO2	(Required pin)
C4	GPIO2	Input / Output	GPIO input / output port pin (Default input mode with pull-down) At SERSEL pin = High (SPI mode) : SCE pin	Recommended to connect to GND
C5	GPIO3	Input / Output	GPIO input / output port pin (Default input mode with pull-down)	Recommended to connect to GND
C6	INT	Output	Interrupt output pin	Open
C7	PD2	Input	Photo diode connection pin	Connect to GND
C8	PD1	Output	Photo diode connection pin	Open
D1	SW5	Output	Control switch pin for matrix driver Connected to E column of matrix LED.	Open
D2	SW6	Output	Control switch pin for matrix driver Connected to F column of matrix LED.	Open
D3	AGND	Ground	GND for analog block	Connect to GND
D4	NRESET	Input	Reset input pin	(Required pin)
D5	SCL	Input	SPI / I^2C interface common clock input pin	(Required pin)

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PIN FUNCTIONS (continued)

Pin No.	Pin name	Type	Description	Pin processing at unused
D6	SDA	Input / Output	Data input / output pin for I²C interface At SERSEL pin = High (SPI mode) : Data input pin	(Required pin)
D7	VDD	Power supply	Power supply for I²C interface	(Required pin)
D8	PD3	Input	Detection resistor connection pin for photo diode adjustment	Open
E1	SW7	Output	Control switch pin for matrix driver Connected to G column of matrix LED.	Open
E2 E3	LEDGND3 LEDGND2	Ground	GND for matrix LED	Connect to GND
E4	SLAVE	Input / Output	Slave address selection pin for I²C interface At SERSEL pin = High (SPI mode) : SDO pin	(Required pin)
E5	SERSEL	Input	I²C / SPI interface selection pin	Connect to GND or VDD
E6	LEDGND1	Ground	GND for BL pin	Connect to GND
E7	LED1	Output	Constant current output pin for LED driver	Open
F1	LED16	Output	Constant current circuit, PWM control output pin Connected to the 6th row of matrix LED. And GPO (open drain) output pin	Open
F2	LED14	Output	Constant current circuit, PWM control output pin Connected to the 4th row of matrix LED.	Open
F3	LED12	Output	Constant current circuit, PWM control output pin Connected to the 2nd row of matrix LED.	Open
F4	LED10	Output	Constant current output pin for LED driver, and GPO (open drain) output pin	Open
F5	LED8	Output	Constant current output pin for LED driver, and GPO (open drain) output pin	Open
F6	LED6	Output	Constant current output pin for LED driver	Open
F7	LED4	Output	Constant current output pin for LED driver	Open
F8	LED2	Output	Constant current output pin for LED driver	Open
G1	LED17	Output	Constant current circuit, PWM control output pin Connected to the 7th row of matrix LED. And GPO (open drain) output pin	Open
G2	LED15	Output	Constant current circuit, PWM control output pin Connected to the 5th row of matrix LED. And GPO (open drain) output pin	Open
G3	LED13	Output	Constant current circuit, PWM control output pin Connected to the 3rd row of matrix LED.	Open
G4	LED11	Output	Constant current circuit, PWM control output pin Connected to the 1st row of matrix LED.	Open
G5	LED9	Output	Constant current output pin for LED driver, and GPO (open drain) output pin	Open
G6	LED7	Output	Constant current output pin for LED driver	Open
G7	LED5	Output	Constant current output pin for LED driver	Open
G8	LED3	Output	Constant current output pin for LED driver	Open

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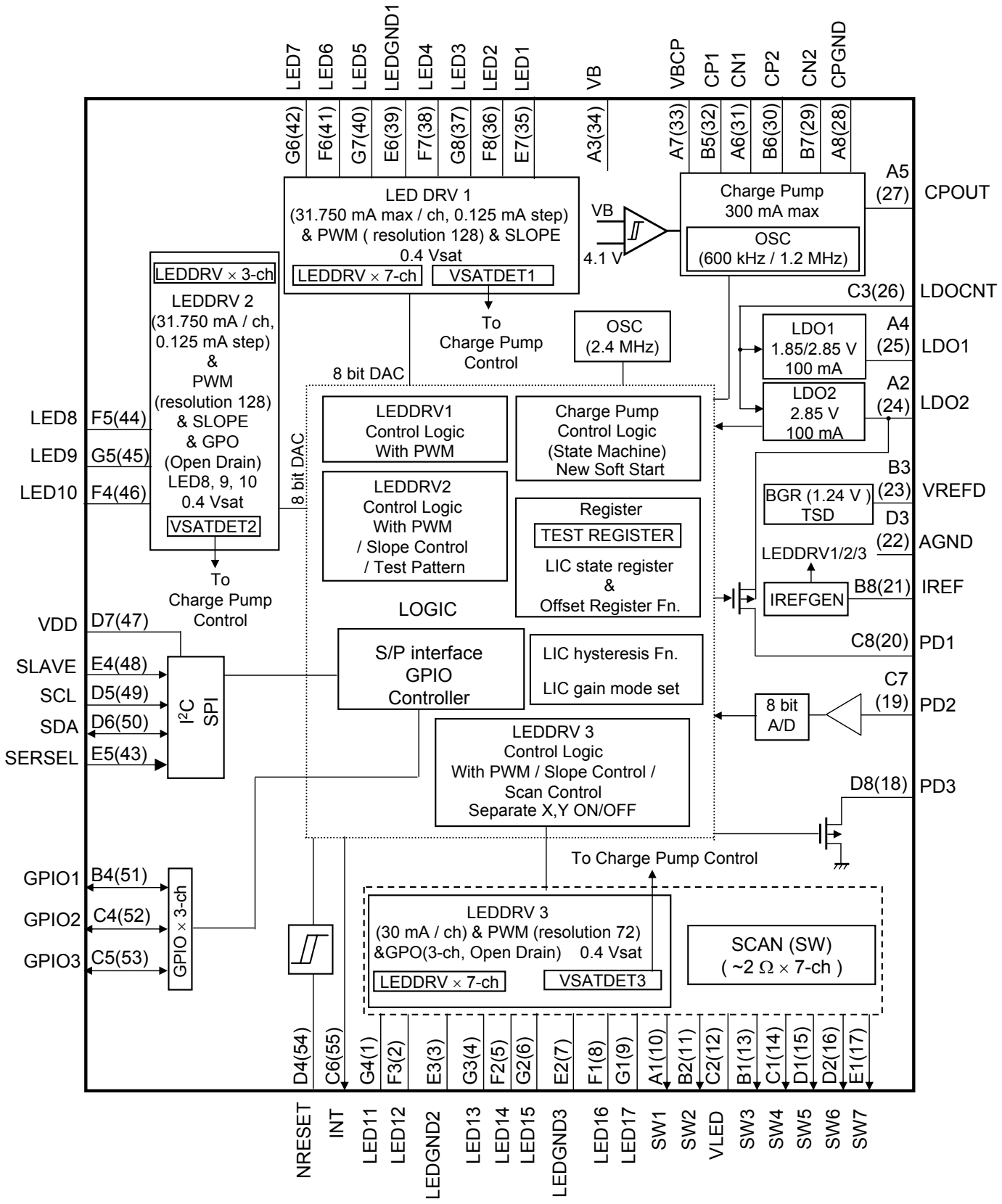
FUNCTIONAL BLOCK DIAGRAM



Note) This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

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OPERATION

1. Power-on / Power-off sequence

Description of each mode

Mode	LDOCNT	LDO1ON	LDO2STB	LDO1PS	LDO2PS	Notes
OFF	Low	0	0	0	0	• The serial signal is not received at LDOCNT = Low. It is necessary to set LDOCNT to High for the return from OFF mode.
OFF ↓ Power save	Low ↓ High	1	0	1	1	• The serial signal can be received after 5 ms from LDOCNT = High. • The setting of registers is initialized after this LSI return from OFF mode. Then LDO1 and LDO2 operate in power save mode respectively.
Normal	High	0/1	0	0	0	• When NRESET is set to Low, the setting of registers is initialized. Then LDO1 and LDO2 operate in power save mode respectively. • The serial signal is turned LDO1 on or off. • LDO2 turns on at LDOCNT = High. • The serial signal is not received at NRESET = Low. • Low period of one or more internal clocks is required during NRESET = Low. • NRESET prohibits the input signal of those other than a rectangle wave. • When NRESET is set to Low, all the registers are set to the default value.
Normal / power save ↓ OFF	High ↓ Low	0	0	0/1 ↓ 0	0/1 ↓ 0	• The setting order to change into OFF mode is as follows. LDOCNT = Low → NRESET = Low, or NRESET = Low → LDOCNT = Low
Normal ↓ Power save	High	0/1	0	0/1	0/1	• LDO1, 2 can be individually shifted to power save mode by the serial signal. • It is possible to return from power save mode to normal mode with serial signal.
Power save ↓ Normal						
Normal / power save ↓ OFF(LDO1 only)	High ↓ Low	1	1	0/1	0/1	• When LDO1 output is used as power supply for I²C I/F and LDO1 is turned OFF by LDO1ON via serial interface, LDO1 cannot return to ON mode via serial interface. • When LDO1 output is used as power supply fro I²C I/F, write [1] in LDO2STB first. After that, LDOCNT changes from High to Low, and LDO1 only shifts to OFF mode.
OFF(LDO1 only) ↓ Normal / power save	Low ↓ High					• If LDOCNT is set to High from Low, this LSI can shift from standby to normal mode.

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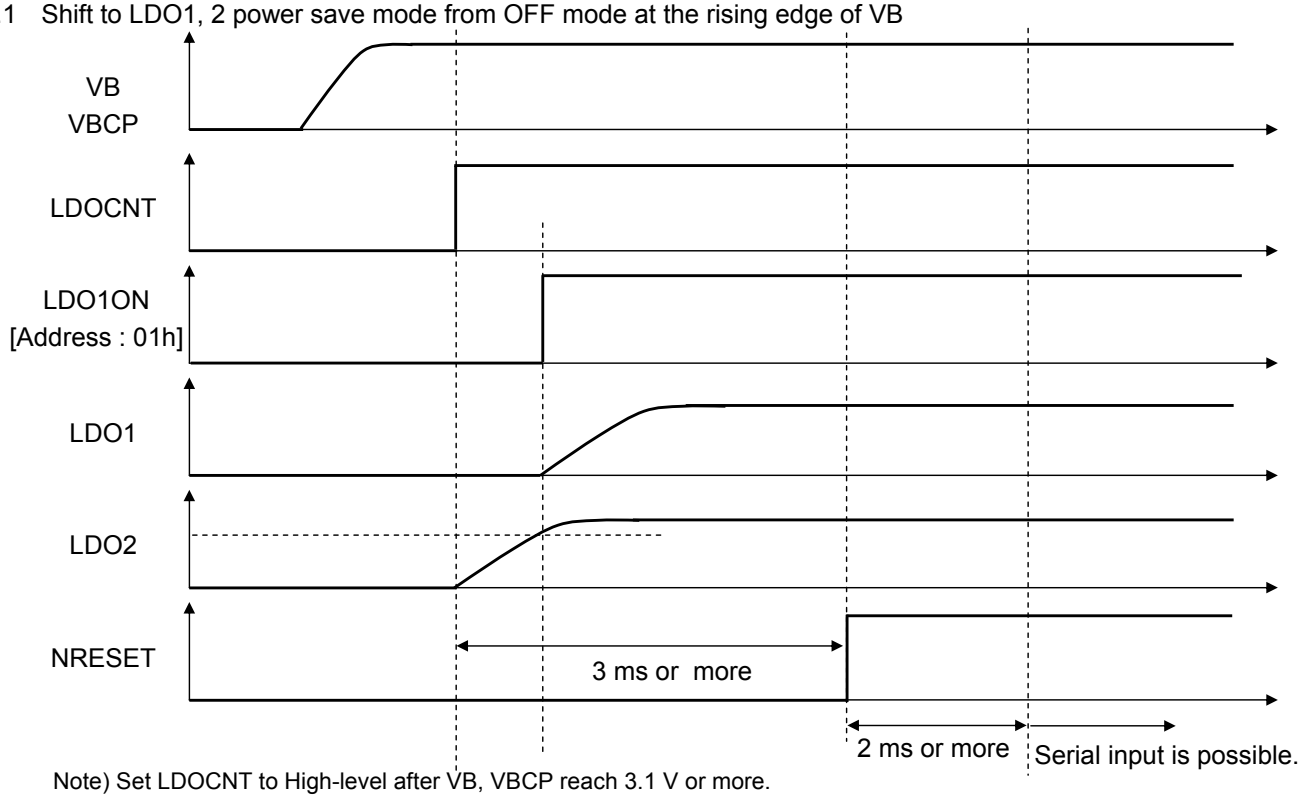
OPERATION (continued)

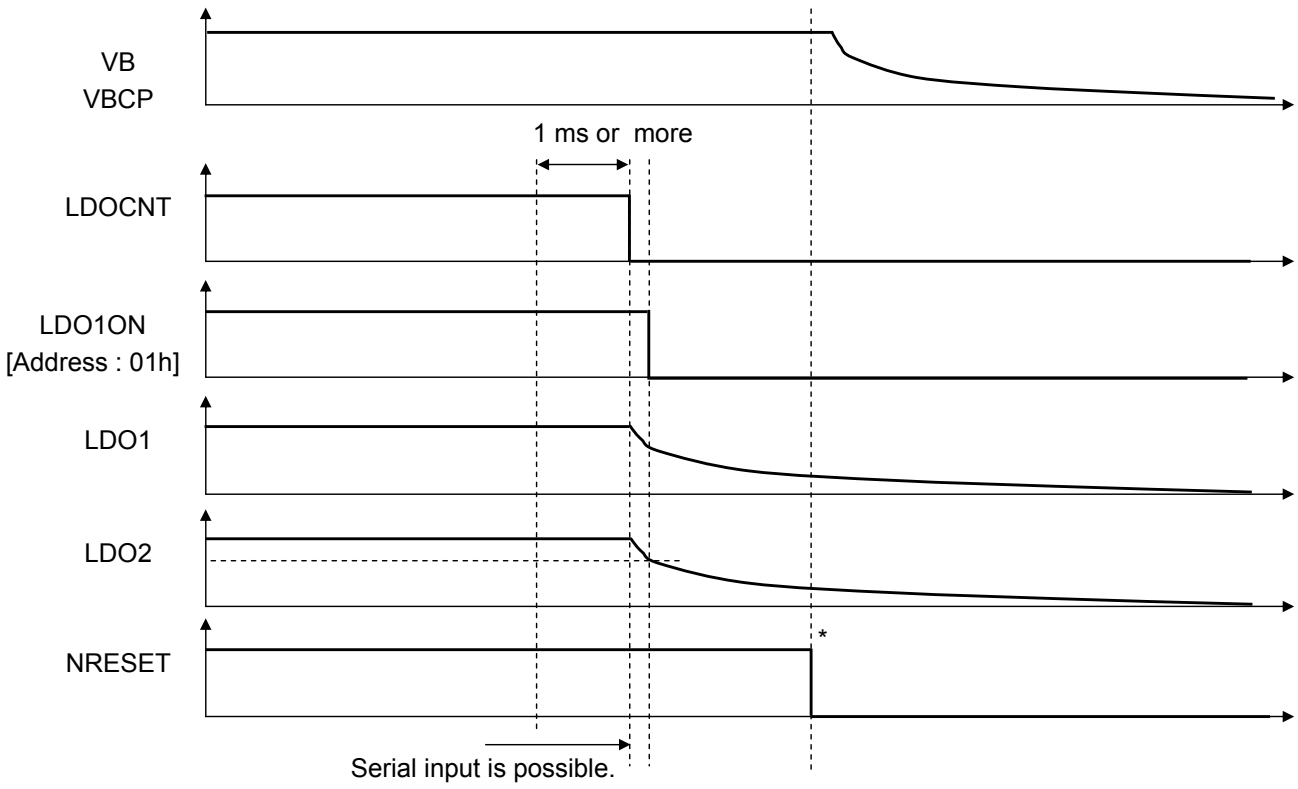
1. Power-on / Power-off sequence (continued)

1.1 Shift to LDO1, 2 power save mode from OFF mode at the rising edge of VB



Note) Set LDOCNT to High-level after VB, VBCP reach 3.1 V or more.
LDO1, LDO2 operate at power save mode after they just rise.

1.2 Shift to OFF mode from LDO1, 2 normal / power save mode



Note) * : There is no problem if NRESET falling timing is before or after LDOCNT falls.

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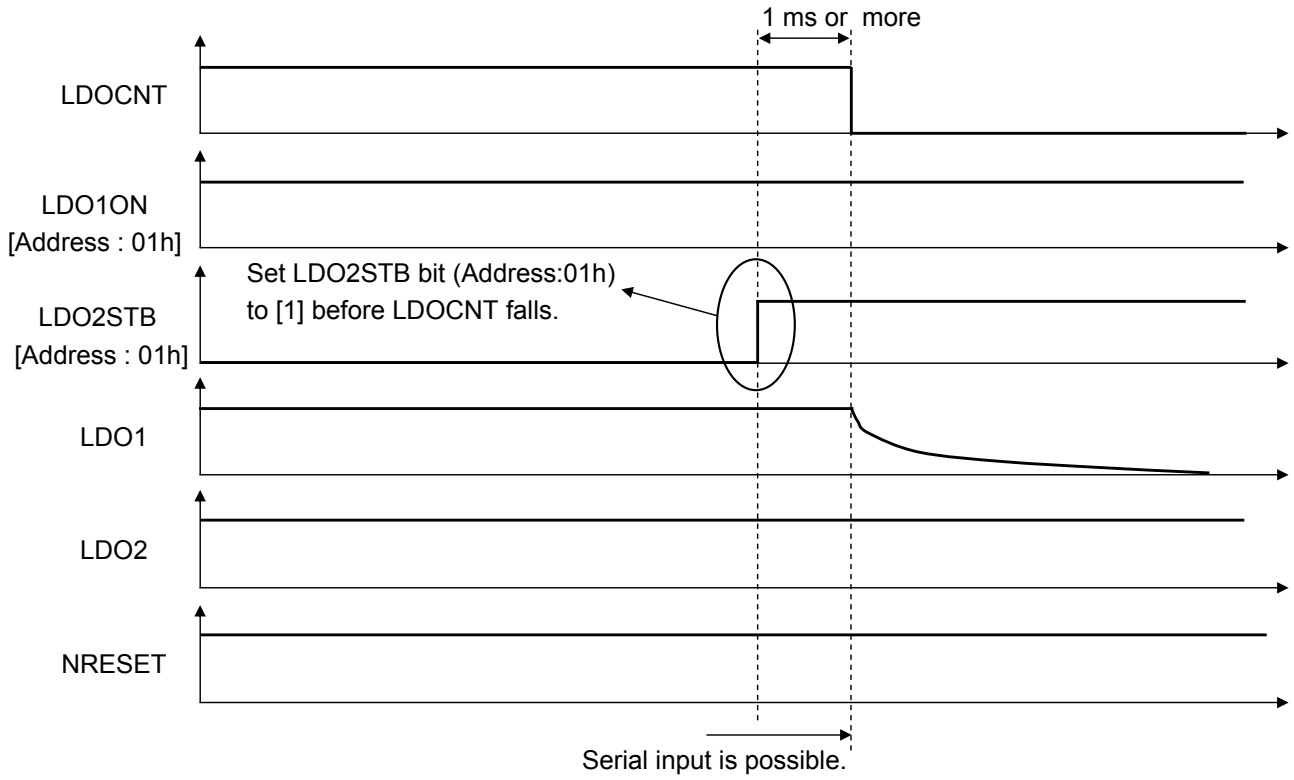
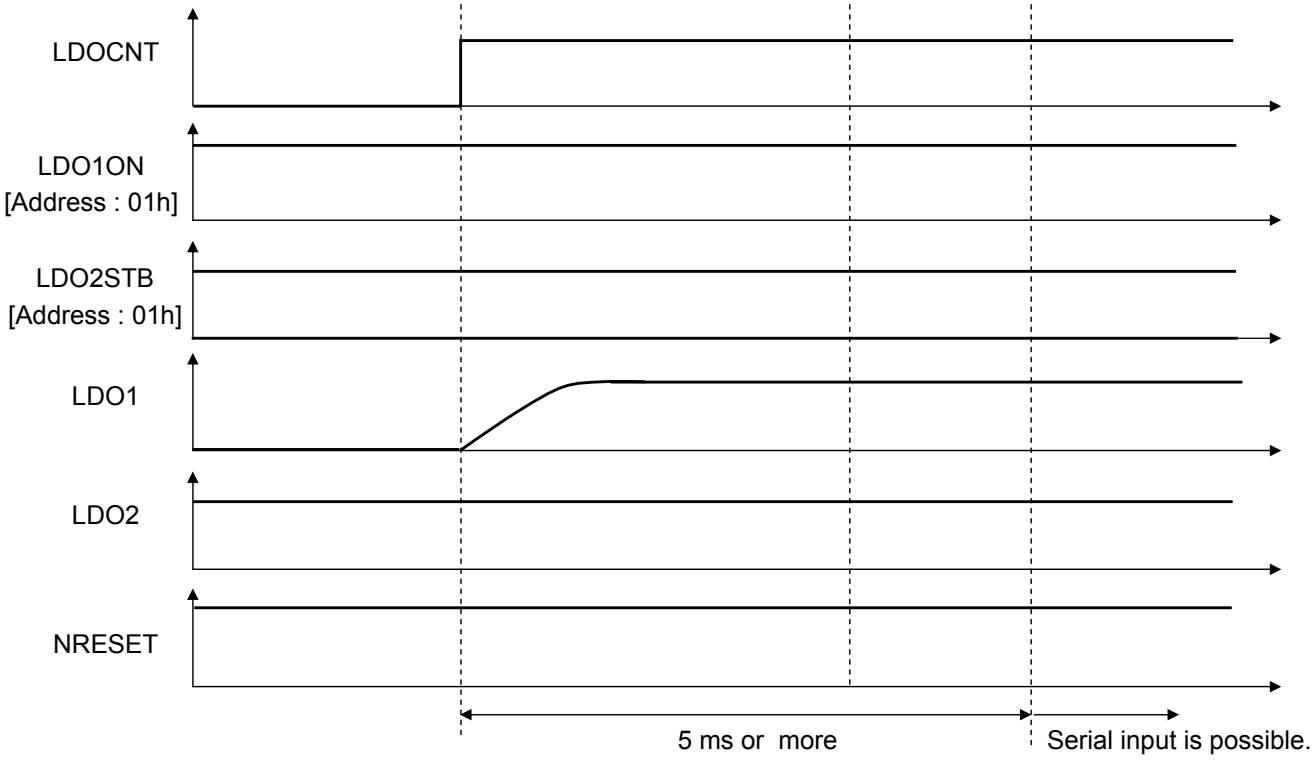
OPERATION (continued)

1. Power-on / Power-off sequence (continued)

1.3 Shift to LDO OFF mode with LDOCNT from normal mode



1.4 Shift to normal mode from LDO OFF mode with LDOCNT



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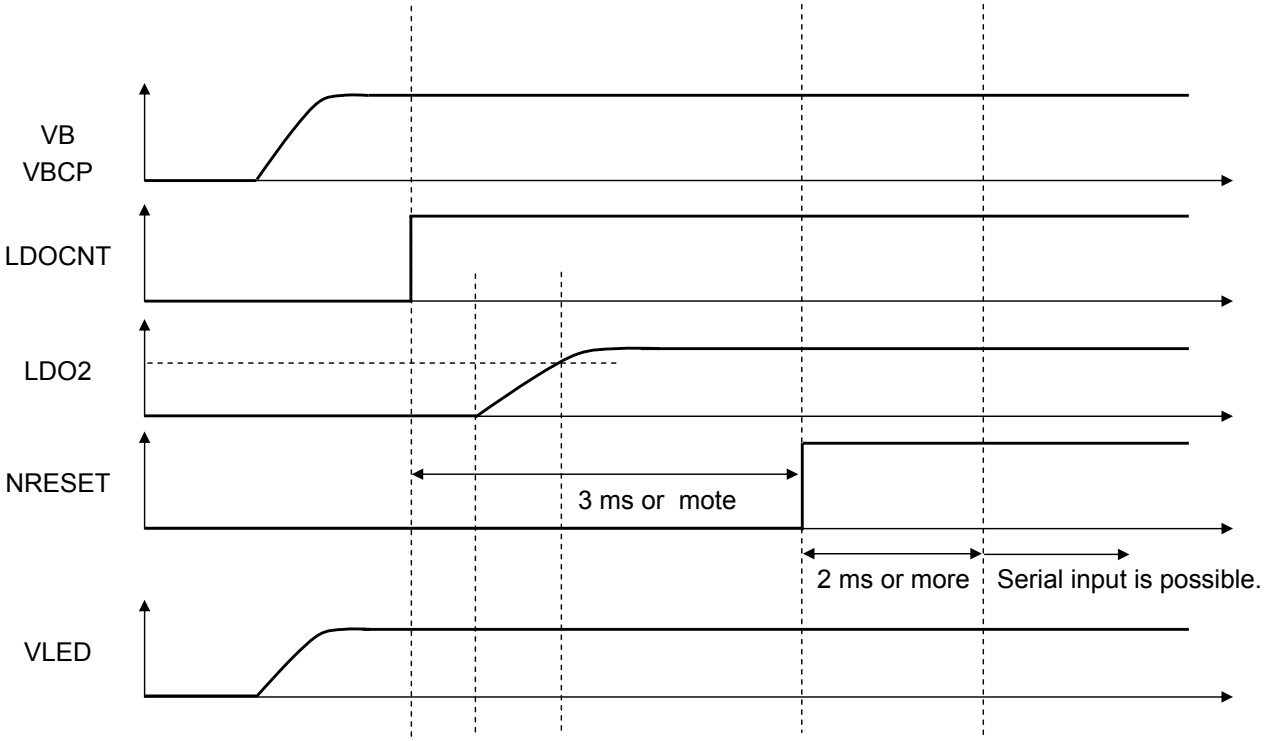
OPERATION (continued)

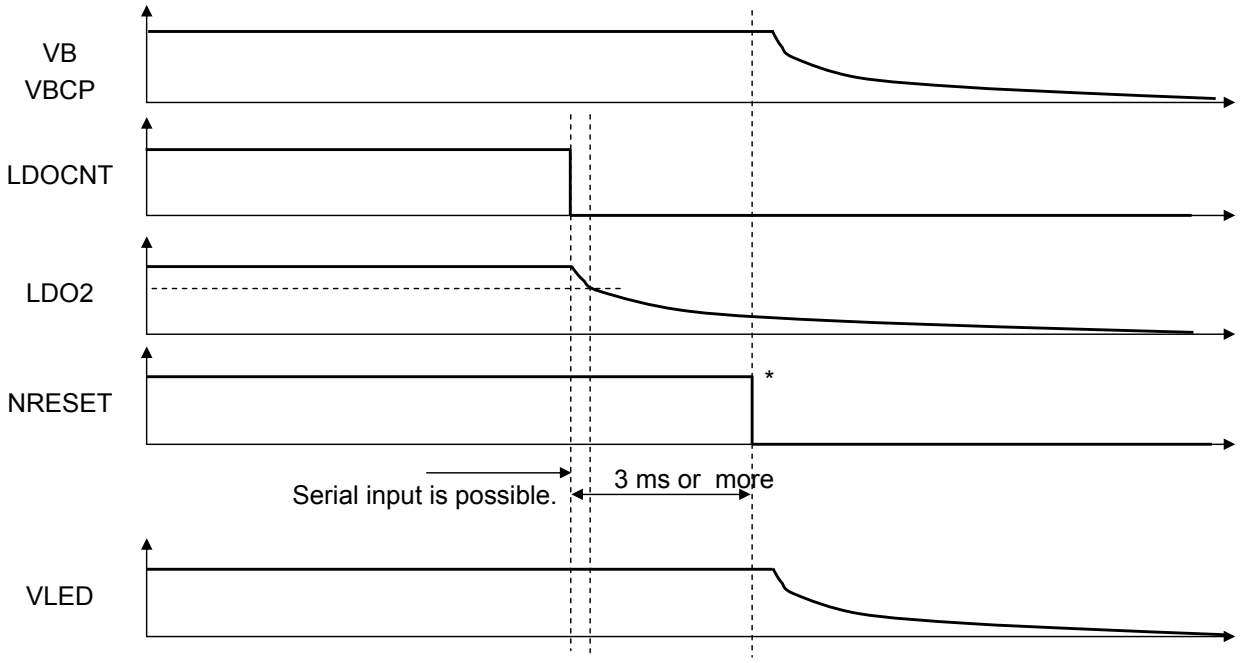
1. Power-on / Power-off sequence (continued)

1.5 Power-on sequence when an external power supply is used as LED power supply (VLED) (at non-connected between CPOUT and VLED)



Note) Rise VLED at the same time as VB,VBCP rise or after VB, VBCP rise.

1.6 Power-off sequence when an external power supply is used as LED power supply (VLED) (at non-connected between CPOUT and VLED)



Note) Fall VLED at the same time as VB falls or before VB falls.

∗ : There is no problem if NRESET falling timing is before or after LDOCNT falls.

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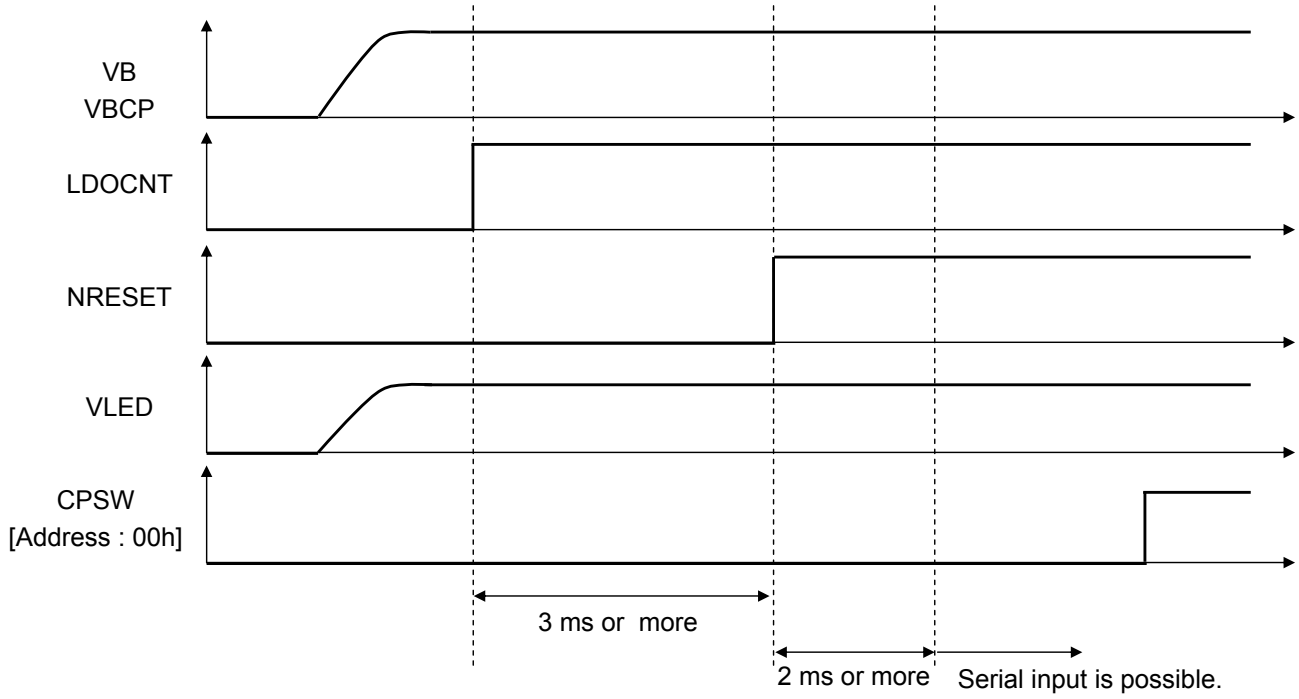
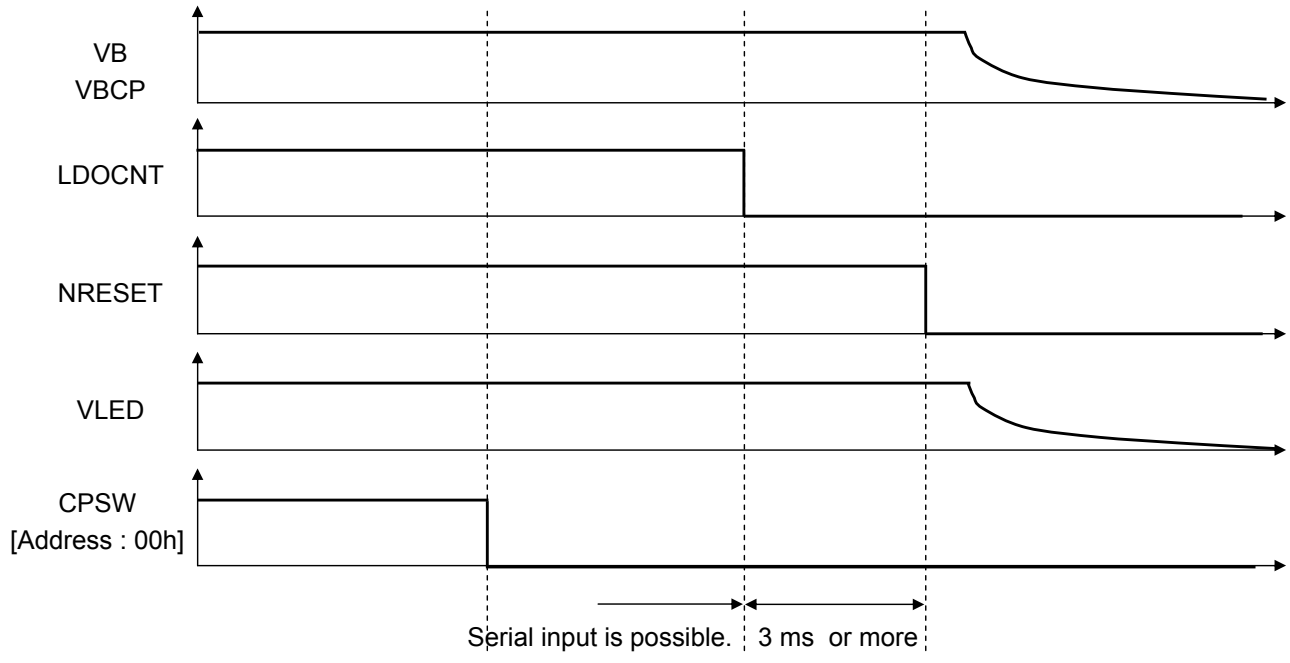
OPERATION (continued)

1. Power-on / Power-off sequence (continued)

1.7 Power-on sequence of charge pump setting



1.8 Power-off sequence of charge pump setting



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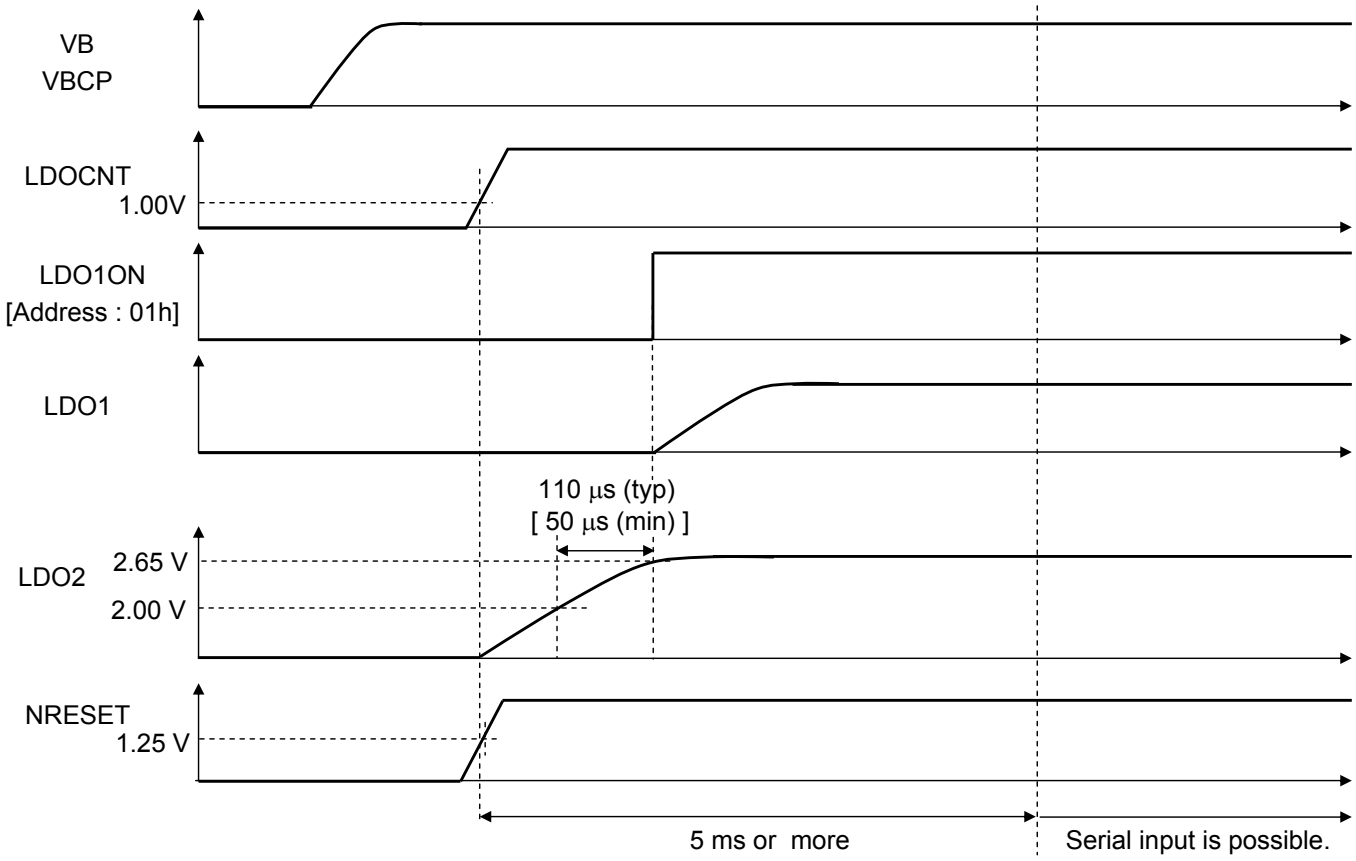
OPERATION (continued)

1. Power-on / Power-off sequence (continued)

1.9 Start-up sequence when terminal NRESET is not used



Note) When the period of time that LDO2 pin voltage rises from 2.0 V to 2.65 V is 50 ms or more, this LSI operates normally even if LDOCNT pin and NRESET pin are connected together.

Supplement) Electrical characteristics of LDO2 pin rising time : 110 µs (typ), 50 µs (min)

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OPERATION (continued)

1. Power-on / Power-off sequence (continued)

1.10 Mode of VBAT / LDOCNT

VBAT	LDOCNT	LDO2STB (Address : 01h)	LDO1ON (Address : 01h)	LDO1PS (Address : 01h)	LDO2PS (Address : 01h)	MODE (LDO1)	MODE (LDO2)
Low	Low	"0"	"0"	"0"	"0"	OFF	OFF
Low	High	"0"	"0"	"0"	"0"	Prohibited	
High	Low	"0"	"0"	"0"	"0"	OFF	OFF
High	High	"X"	"0"	"X"	"0"	OFF	ON
High	High	"X"	"0"	"X"	"1"	OFF	Power save
High	High	"X"	"1"	"0"	"0"	ON	ON
High	High	"X"	"1"	"0"	"1"	ON	Power save
High	High	"X"	"1"	"1"	"0"	Power save	ON
High	High	"X"	"1"	"1"	"1"	Power save	Power save
High	Low	"1"	"X"	"X"	"0"	OFF	ON
High	Low	"1"	"X"	"X"	"1"	OFF	Power save

Note) As for VBAT and LDOCNT,
Low : 0 V, High : 3.1 V to 4.6 V (operating supply voltage range)

1.11 Power-on sequence of VDD

It is possible to turn on/off VDD at any timing regardless of ON/OFF of other power supplies.
But when SLAVE is connected to VDD level outside the LSI, it is impossible to turn on VDD with VB falling.

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OPERATION (continued)

2. Register map

2.1 Address 00h to 1Fh

Sub Address	R/W	Register Name	Default	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
00h	R/W	POWERCNT	00h	—	—	—	CPRETMODE	CPCLKSEL20	CPCLKSEL15	OSCEN	CPSW
01h	R/W	LDOCNT	0Eh	—	—	—	LDO2STB	LDO1PS	LDO2PS	LDO1ON	LDO1VSEL
02h	R	STATECHANGE	01h	—	—	—	CPERR	CP20	CP15	VB	CPOFF
03h	R/W	STATEFORCE	00h	RETURNVB	ERRMSK	ERRCLR	ERRSTOP	FCP20	FCP15	FVB	FCPOFF
04h *1	—	—	—	—	—	—	—	—	—	—	—
05h	R/W	CLKSEL	00h	—	—	—	—	—	—	CLKOUT	EXTCLKSEL
06h	R/W	GPOEN	00h	—	—	GPO6EN	GPO5EN	GPO4EN	GPO3EN	GPO2EN	GPO1EN
07h	R/W	OOUT	00h	—	—	OOUT6	OOUT5	OOUT4	OOUT3	OOUT2	OOUT1
08h	R/W	IOSEL	00h	—	—	—	—	—	IOSEL3	IOSEL2	IOSEL1
09h	R/W	IOOUT	00h	—	—	—	—	—	IOOUT3	IOOUT2	IOOUT1
0Ah	R/W	VOUTSEL	00h	—	—	—	—	—	IOVSEL3	IOVSEL2	IOVSEL1
0Bh	R	INT1	00h	SDET	VBDET	IOSTA3	IOSTA2	IOSTA1	IOFAC3	IOFAC2	IOFAC1
0Ch	W	INTCLR1	00h	—	VBDETCLR	—	—	—	IOFAC3CLR	IOFAC2CLR	IOFAC1CLR
0Dh	R/W	INTMSK1	00h	SDETMSK	VBDETMSK	—	—	—	IOFAC3MSK	IOFAC2MSK	IOFAC1MSK
0Eh	R/W	IOPLD	00h	—	—	—	—	—	IOPLD3	IOPLD2	IOPLD1
0Fh	R/W	IODET	00h	—	—	—	—	—	IODET3	IODET2	IODET1

Note) Read value of " — "(the blanks) is [0] in the register map.
*1: Address 04h is register for the LSI test. Use them with the default value [0].

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Revised : 2013-04-16

OPERATION (continued)

2. Register map (continued)

2.1 Address 00h to 1Fh (continued)

Sub Address	R/W	Register Name	Default	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
10h	R/W	LED CNT1	00h	LEDCNT 1EN	LED1 ACT	LED1 GRP1	LED1 GRP2	LEDCNT1 LED10	LEDCNT1 LED9	LEDCNT1 LED8	LED1 MTX
11h	R/W	LED CNT2	00h	LEDCNT 2EN	LED2 ACT	LED2 GRP1	LED2 GRP2	LEDCNT2 LED10	LEDCNT2 LED9	LEDCNT2 LED8	LED2 MTX
12h	R/W	VDETLED CNT1	00h	VDETLED 8EN	VDETLED 7EN	VDETLED 6EN	VDETLED 5EN	VDETLED 4EN	VDETLED 3EN	VDETLED 2EN	VDETLED 1EN
13h	R/W	VDETLED CNT2	00h	—	—	—	—	—	—	VDETLED 10EN	VDETLED 9EN
14h	R/W	VDETLED CNT3	00h	VDETLED 17EN	VDETLED 16EN	VDETLED 15EN	VDETLED 14EN	VDETLED 13EN	VDETLED 12EN	VDETLED 11EN	VDET MTX
15h	R	INT2	00h	—	INTLED G1	INTLUT	ADCINT	LICGAIN INT	LICDRV2 INT	FRMINT	SLPMAT
16h	W	INTCLR2	00h	—	INTLED G1CLR	INTLUT CLR	ADCINT CLR	LICGAIN INTCLR	LICDRV2 CLR	FRMINT CLR	SLPMAT CLR
17h	R/W	INTMSK2	00h	—	INTLED G1MSK	INTLUT MSK	ADCINT MSK	LICGAIN MSK	LICDRV2 MSK	FRMINT MSK	SLPMAT MSK
18h	R	ADCRD1	00h	ADCGD (NPOWD)	GAINST	LIC_DATA[3:0]				ADC_DATA[1:0]	
19h	R	ADCRD2	00h	ADC_DATA[9:2]							
1Ah	R/W	GAINTH	08h	—	—	—	RSTGAIN	GAINTH[3:0]			
1Bh	R/W	GSWTHH	FAh	GSWTHH[7:0]							
1Ch	R/W	GSWTHL	07h	GSWTHL[7:0]							
1Dh	R/W	INTSEL	00h	—	RSTCNT	INTSEL[5:0]					
1Eh	R/W	LICAD WAIT	0Ch	—	—	—	ADWAIT[4:0]				
1Fh	R/W	REGSEL	00h	—	—	—	—	—	—	REGSEL[1:0] *2	

Note) Read value of " — "(the blanks) is [0] in the register map.

*2 : It is possible to change the register map of Address 20h to 6Fh by setting REGSEL[1: 0]. There are four choices in it.

REGSEL[1:0] = [00] ..... CPU can access the register related to from LED1 to LED10.

REGSEL[1:0] = [01] ..... CPU can access the register related to the modulated LED light.

REGSEL[1:0] = [10] ..... CPU can access RAM1 and the register related to the matrix LED.

REGSEL[1:0] = [11] ..... CPU can access RAM2 and the register related to the matrix LED.

Established : 2011-05-30
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OPERATION (continued)

2. Register map (continued)

2.2 Address 20h to 6Fh

1) At REGSEL[1:0] = [00]

Sub Address	R/W	Register Name	Default	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
20h	R/W	GROUP ASSIGN1	55h	LED4[1:0]		LED3[1:0]		LED2[1:0]		LED1[1:0]	
21h	R/W	GROUP ASSIGN2	28h	—	—	LED7[1:0]		LED6[1:0]		LED5[1:0]	
22h	R/W	GRP1CNT	00h	GRP1LEDSET[7:0]							
23h	R/W	GRP2CNT	00h	GRP2LEDSET[7:0]							
24h	R/W	LEDDRV2 CNT	00h	—	—	—	—	—	LED10ON	LED9ON	LED8ON
25h	R/W	CNT8	28h	ILED8SET[7:0]							
26h	R/W	CNT9	28h	ILED9SET[7:0]							
27h	R/W	CNT10	28h	ILED10SET[7:0]							
28h	R/W	GRP1PWM CNT	00h	GRP1PWMEN	GRP1PWMSET[6:0]						
29h	R/W	PWM8 CNT	00h	PWM8EN	PWM8SET[6:0]						
2Ah	R/W	PWM9 CNT	00h	PWM9EN	PWM9SET[6:0]						
2Bh	R/W	PWM10 CNT	00h	PWM10EN	PWM10SET[6:0]						
2Ch	R/W	HOTARU CNT	88h	HOTATT2[3:0]				HOTATT1[3:0]			
2Dh	R/W	HOTARU ASSIGN	00h	—	—	—	—	—	HOTA10EN	HOTA9EN	HOTA8EN
2Eh	—	—	—	—	—	—	—	—	—	—	—
2Fh	R/W	SLOPE GRP1	00h	SLPGRP1R[3:0]				SLPGRP1F[3:0]			
30h	R/W	SLOPE LED8	00h	SLPLED8R[3:0]				SLPLED8F[3:0]			
31h	R/W	SLOPE LED9	00h	SLPLED9R[3:0]				SLPLED9F[3:0]			
32h	R/W	SLOPE LED10	00h	SLPLED10R[3:0]				SLPLED10F[3:0]			

Note) Read value of " — "(the blanks) is [0] in the register map.

Established : 2011-05-30
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OPERATION (continued)

2. Register map (continued)

2.2 Address 20h to 6Fh (continued)

1) At REGSEL[1:0] = [00] (continued)

Sub Address	R/W	Register Name	Default	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
33h	R/W	HOTARU8CNT1	F8h	DUTYMAX8[3:0]				DUTYMID8[3:0]			
34h	R/W	HOTARU8CNT2	00h	—	—	—	—	DUTYMIN8[3:0]			
35h	R/W	HOTARU8CNT3	88h	HOTA8DT2[3:0]				HOTA8DT1[3:0]			
36h	R/W	HOTARU8CNT4	88h	HOTA8DT4[3:0]				HOTA8DT3[3:0]			
37h	R/W	HOTARU9CNT1	F8h	DUTYMAX9[3:0]				DUTYMID9[3:0]			
38h	R/W	HOTARU9CNT2	00h	—	—	—	—	DUTYMIN9[3:0]			
39h	R/W	HOTARU9CNT3	88h	HOTA9DT2[3:0]				HOTA9DT1[3:0]			
3Ah	R/W	HOTARU9CNT4	88h	HOTA9DT4[3:0]				HOTA9DT3[3:0]			
3Bh	R/W	HOTARU10CNT1	F8h	DUTYMAX10[3:0]				DUTYMID10[3:0]			
3Ch	R/W	HOTARU10CNT2	00h	—	—	—	—	DUTYMIN10[3:0]			
3Dh	R/W	HOTARU10CNT3	88h	HOTA10DT2[3:0]				HOTA10DT1[3:0]			
3Eh	R/W	HOTARU10CNT4	88h	HOTA10DT4[3:0]				HOTA10DT3[3:0]			
45h	R/W	STROBE1	AAh	STBLED 17	STBLED 16	STBLED 15	STBLED 14	STBLED 13	STBLED 12	STBLED 11	STBLED 10
46h	R/W	STROBE2	02h	—	—	—	—	—	STBEN	STBLED 8	STBLED 9

Note) Read value of " — "(the blanks) is [0] in the register map.

Established : 2011-05-30
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OPERATION (continued)

2. Register map (continued)

2.2 Address 20h to 6Fh (continued)

2) At REGSEL[1:0] = [01]

Sub Address	R/W	Register Name	Default	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
20h	R/W	LICEN	28h	—	GAINCNT	ADCAVERA	LICTIME[2:0]			ADCSTART	LICEN
21h	R/W	LICTIME	B4h	GCHGMOD	HYSMODESEL	LICHYSGL	LICHYSGH	LICTH0D[3:0]			
22h	R/W	LICSLP	44h	SLPRATEF[3:0]				SLPRATER[3:0]			
23h	R/W	LICTH0	0Ah	LICTH0[7:0]							
24h	R/W	LICTH1	2Ah	LICTH1[7:0]							
25h	R/W	LICTH2	4Ah	LICTH2[7:0]							
26h	R/W	LICTH3	6Ah	LICTH3[7:0]							
27h	R/W	LICTH4	8Ah	LICTH4[7:0]							
28h	R/W	LICTH5	AAh	LICTH5[7:0]							
29h	R/W	LICTH6	CAh	LICTH6[7:0]							
2Ah	R/W	LICTH7	FAh	LICTH7[7:0]							
2Bh	R/W	LICTH8	10h	LICTH8[7:0]							
2Ch	R/W	LICTH9	30h	LICTH9[7:0]							
2Dh	R/W	LICTH10	60h	LICTH10[7:0]							
2Eh	R/W	LICTH11	90h	LICTH11[7:0]							
2Fh	R/W	LICTH12	B0h	LICTH12[7:0]							
30h	R/W	LICTH13	D0h	LICTH13[7:0]							
31h	R/W	LICTH14	F0h	LICTH14[7:0]							

Note) Read value of " — "(the blanks) is [0] in the register map.

Established : 2011-05-30
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OPERATION (continued)

2. Register map (continued)

2.2 Address 20h to 6Fh (continued)

2) At REGSEL[1:0] = [01] (continued)

Sub Address	R/W	Register Name	Default	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
32h	R/W	LICLUT0	08h	LICLUT0[7:0]							
33h	R/W	LICLUT1	10h	LICLUT1[7:0]							
34h	R/W	LICLUT2	18h	LICLUT2[7:0]							
35h	R/W	LICLUT3	20h	LICLUT3[7:0]							
36h	R/W	LICLUT4	28h	LICLUT4[7:0]							
37h	R/W	LICLUT5	30h	LICLUT5[7:0]							
38h	R/W	LICLUT6	38h	LICLUT6[7:0]							
39h	R/W	LICLUT7	40h	LICLUT7[7:0]							
3Ah	R/W	LICLUT8	48h	LICLUT8[7:0]							
3Bh	R/W	LICLUT9	50h	LICLUT9[7:0]							
3Ch	R/W	LICLUT10	60h	LICLUT10[7:0]							
3Dh	R/W	LICLUT11	70h	LICLUT11[7:0]							
3Eh	R/W	LICLUT12	80h	LICLUT12[7:0]							
3Fh	R/W	LICLUT13	90h	LICLUT13[7:0]							
40h	R/W	LICLUT14	A0h	LICLUT14[7:0]							
41h	R/W	LICLUT15	B0h	LICLUT15[7:0]							
42h	R/W	LICAPPED	01h	—	—	—	LICLED10	LICLED9	LICLED8	LICGRP2	LICGRP1
43h	R/W	LIC INVERT	1Ch	—	—	—	LICINVLED10	LICINV LED9	LICINV LED8	LICINV GRP2	LICINV GRP1
44h	R/W	LIC LEDSET	32h	—	—	LICDEFGP2	LICDEFGP1	LICD2TH[3:0]			
45h	R/W	ADAJH	00h	ADAJH[7:0]							
46h	R/W	ADAJL	00h	ADAJL[7:0]							

Note) Read value of " — "(the blanks) is [0] in the register map.

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OPERATION (continued)

2. Register map (continued)

2.2 Address 20h to 6Fh (continued)

3) At REGSEL[1:0] = [10] or [11]

Sub Address	R/W	Register Name	Default	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
20h	R/W	MTXON	00h	—	—	—	MTXON DETTM	MTXON CPMD	MTXTIME[1:0]		MTXON
21h	R/W	MTXDATA	00h	—	—	—	—	—	—	MTXDATA[1:0]	
22h	R/W	RAMRST	00h	—	—	—	—	—	—	RAM1	RAM2
23h	R/W	SCROLL	00h	—	—	—	—	—	—	—	SCLON
24h	R/W	SCLTIME	00h	—	—	—	—	—	—	SCLTIME[1:0]	
25h	R/W	XCONST	00h	—	X11 CONST	X12 CONST	X13 CONST	X14 CONST	X15 CONST	X16 CONST	X17 CONST
26h	R/W	YCONST	00h	—	SW1 CONST	SW2 CONST	SW3 CONST	SW4 CONST	SW5 CONST	SW6 CONST	SW7 CONST

Note) Read value of " — "(the blanks) is [0] in the register map.

Established : 2011-05-30
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OPERATION (continued)

2. Register map (continued)

2.2 Address 20h to 6Fh (continued)

3) At REGSEL[1:0] = [10] or [11] (continued)

Address 3Fh to 6Fh access RAM1 at REGSEL[1:0] = [10].

Address 3Fh to 6Fh access RAM2 at REGSEL[1:0] = [11].

Sub Address	R/W	Register Name	Default	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
3Fh	R/W	A1	00h	BLA1[3:0]				FRA1[1:0]		DLA1[1:0]	
40h	R/W	A2	00h	BLA2[3:0]				FRA2[1:0]		DLA2[1:0]	
41h	R/W	A3	00h	BLA3[3:0]				FRA3[1:0]		DLA3[1:0]	
42h	R/W	A4	00h	BLA4[3:0]				FRA4[1:0]		DLA4[1:0]	
43h	R/W	A5	00h	BLA5[3:0]				FRA5[1:0]		DLA5[1:0]	
44h	R/W	A6	00h	BLA6[3:0]				FRA6[1:0]		DLA6[1:0]	
45h	R/W	A7	00h	BLA7[3:0]				FRA7[1:0]		DLA7[1:0]	
46h	R/W	B1	00h	BLB1[3:0]				FRB1[1:0]		DLB1[1:0]	
47h	R/W	B2	00h	BLB2[3:0]				FRB2[1:0]		DLB2[1:0]	
48h	R/W	B3	00h	BLB3[3:0]				FRB3[1:0]		DLB3[1:0]	
49h	R/W	B4	00h	BLB4[3:0]				FRB4[1:0]		DLB4[1:0]	
4Ah	R/W	B5	00h	BLB5[3:0]				FRB5[1:0]		DLB5[1:0]	
4Bh	R/W	B6	00h	BLB6[3:0]				FRB6[1:0]		DLB6[1:0]	
4Ch	R/W	B7	00h	BLB7[3:0]				FRB7[1:0]		DLB7[1:0]	
4Dh	R/W	C1	00h	BLC1[3:0]				FRC1[1:0]		DLC1[1:0]	
4Eh	R/W	C2	00h	BLC2[3:0]				FRC2[1:0]		DLC2[1:0]	
4Fh	R/W	C3	00h	BLC3[3:0]				FRC3[1:0]		DLC3[1:0]	
50h	R/W	C4	00h	BLC4[3:0]				FRC4[1:0]		DLC4[1:0]	
51h	R/W	C5	00h	BLC5[3:0]				FRC5[1:0]		DLC5[1:0]	
52h	R/W	C6	00h	BLC6[3:0]				FRC6[1:0]		DLC6[1:0]	
53h	R/W	C7	00h	BLC7[3:0]				FRC7[1:0]		DLC7[1:0]	
54h	R/W	D1	00h	BLD1[3:0]				FRD1[1:0]		DLD1[1:0]	
55h	R/W	D2	00h	BLD2[3:0]				FRD2[1:0]		DLD2[1:0]	
56h	R/W	D3	00h	BLD3[3:0]				FRD3[1:0]		DLD3[1:0]	
57h	R/W	D4	00h	BLD4[3:0]				FRD4[1:0]		DLD4[1:0]	
58h	R/W	D5	00h	BLD5[3:0]				FRD5[1:0]		DLD5[1:0]	
59h	R/W	D6	00h	BLD6[3:0]				FRD6[1:0]		DLD6[1:0]	
5Ah	R/W	D7	00h	BLD7[3:0]				FRD7[1:0]		DLD7[1:0]	

Note) Read value of " — "(the blanks) is [0] in the register map.

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OPERATION (continued)

2. Register map (continued)

2.2 Address 20h to 6Fh (continued)

3) At REGSEL[1:0] = [10] or [11] (continued)

Address 3Fh to 6Fh access RAM1 at REGSEL[1:0] = [10].

Address 3Fh to 6Fh access RAM2 at REGSEL[1:0] = [11].

Sub Address	R/W	Register Name	Default	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
5Bh	R/W	E1	00h	BLE1[3:0]				FRE1[1:0]		DLE1[1:0]	
5Ch	R/W	E2	00h	BLE2[3:0]				FRE2[1:0]		DLE2[1:0]	
5Dh	R/W	E3	00h	BLE3[3:0]				FRE3[1:0]		DLE3[1:0]	
5Eh	R/W	E4	00h	BLE4[3:0]				FRE4[1:0]		DLE4[1:0]	
5Fh	R/W	E5	00h	BLE5[3:0]				FRE5[1:0]		DLE5[1:0]	
60h	R/W	E6	00h	BLE6[3:0]				FRE6[1:0]		DLE6[1:0]	
61h	R/W	E7	00h	BLE7[3:0]				FRE7[1:0]		DLE7[1:0]	
62h	R/W	F1	00h	BLF1[3:0]				FRF1[1:0]		DLF1[1:0]	
63h	R/W	F2	00h	BLF2[3:0]				FRF2[1:0]		DLF2[1:0]	
64h	R/W	F3	00h	BLF3[3:0]				FRF3[1:0]		DLF3[1:0]	
65h	R/W	F4	00h	BLF4[3:0]				FRF4[1:0]		DLF4[1:0]	
66h	R/W	F5	00h	BLF5[3:0]				FRF5[1:0]		DLF5[1:0]	
67h	R/W	F6	00h	BLF6[3:0]				FRF6[1:0]		DLF6[1:0]	
68h	R/W	F7	00h	BLF7[3:0]				FRF7[1:0]		DLF7[1:0]	
69h	R/W	G1	00h	BLG1[3:0]				FRG1[1:0]		DLG1[1:0]	
6Ah	R/W	G2	00h	BLG2[3:0]				FRG2[1:0]		DLG2[1:0]	
6Bh	R/W	G3	00h	BLG3[3:0]				FRG3[1:0]		DLG3[1:0]	
6Ch	R/W	G4	00h	BLG4[3:0]				FRG4[1:0]		DLG4[1:0]	
6Dh	R/W	G5	00h	BLG5[3:0]				FRG5[1:0]		DLG5[1:0]	
6Eh	R/W	G6	00h	BLG6[3:0]				FRG6[1:0]		DLG6[1:0]	
6Fh	R/W	G7	00h	BLG7[3:0]				FRG7[1:0]		DLG7[1:0]	

Note) Read value of " — "(the blanks) is [0] in the register map.

Established : 2011-05-30
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OPERATION (continued)

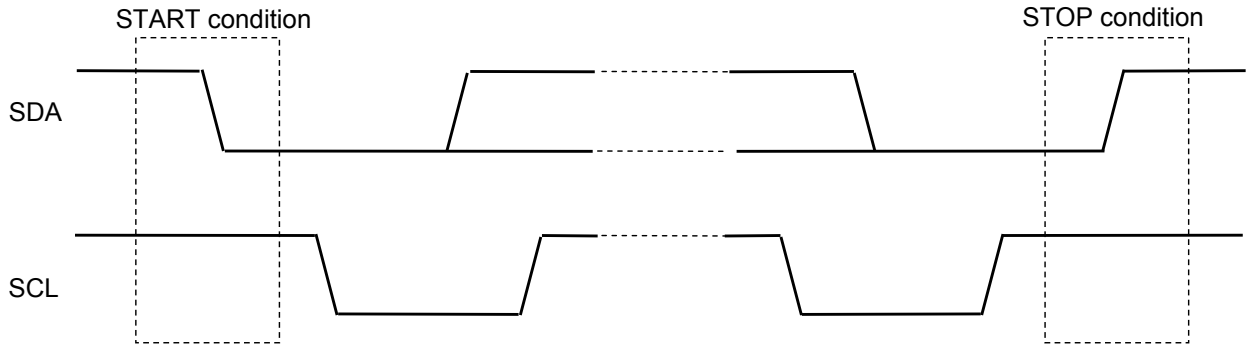
3. I²C-bus interface

3.1 Basic Rules

- This LSI, I²C-bus, is designed to correspond to the Standard-mode (100 kbps) and Fast-mode(400 kbps) devices in the version 2.1 of NXP's specification. However, it does not correspond to the H_S-mode (to 3.4 Mbps).
- This LSI will operate as a slave device in the I²C-bus system. This LSI will not operate as a master device.
- The program operation check of this LSI has not been conducted on the multi-master bus system and the mix-speed bus system, yet. The connected confirmation of this LSI to the CBUS receiver also has not been checked. Please confirm with our company if it will be used in these mode systems.
- The I²C is the brand of NXP.

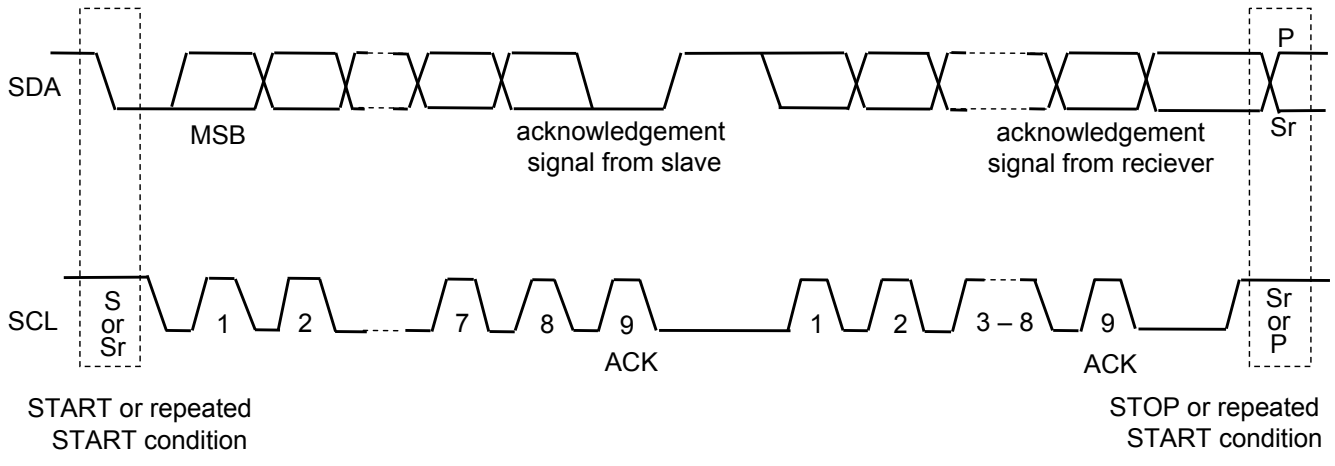
3.2 START and STOP conditions

A High to Low transition on the SDA line while SCL is High is one such unique case. This situation indicates a START condition. A Low to High transition on the SDA line while SCL is High defines a STOP condition. START and STOP conditions are always generated by the master. The bus is considered to be free again a certain time after the STOP condition.



3.3 Transferring Data

Every byte put on the SDA line must be 8-bit long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.



Established : 2011-05-30
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OPERATION (continued)

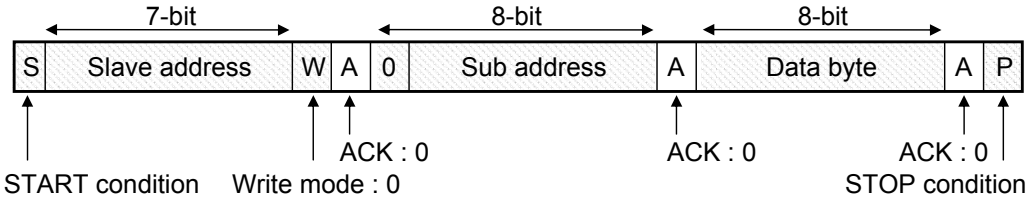
3. I²C-bus interface (continued)

3.4 DATA format

When LSI format is used in this LSI, SERSEL pin should be fixed to Low-level.
Slave address of this LSI is 70h under the condition of SLAVE pin = Low, and is 71h under the condition of SLAVE pin = High.

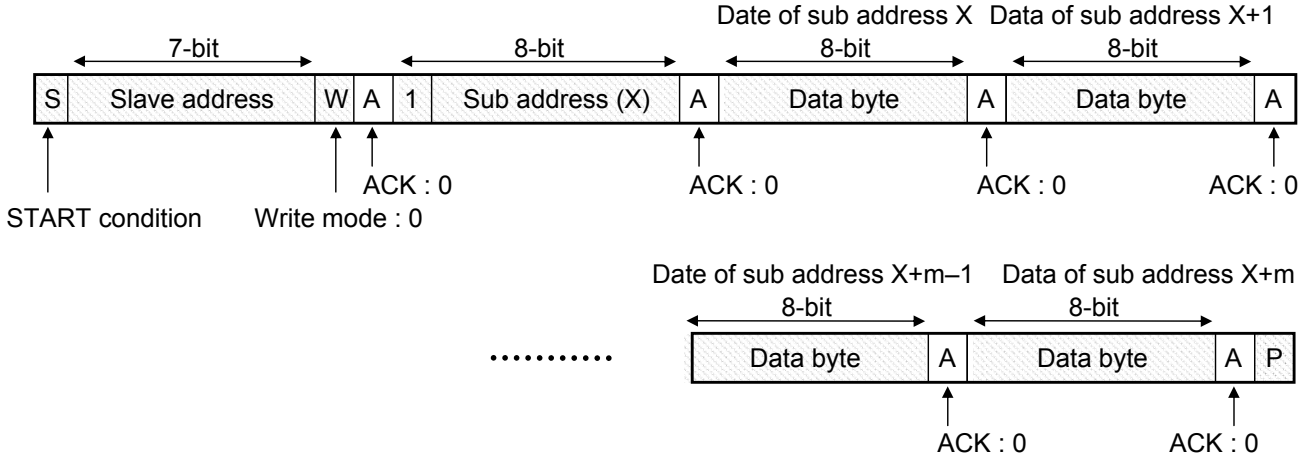
Write mode

When MSB of sub address (8-bit) is "0", the sub address is not incremented automatically.
By transmitting data bytes continuously, the next data bytes are written into the same sub address. by transmitting data byte continuously



Write mode (Auto increment mode)

When MSB of sub address (8-bit) is "1", auto increment mode is defined.
By transmitting data bytes continuously, the data bytes are written into continuous sub address.
The sub address is incremented automatically.



: Data transmission from Master

: Data transmission from Slave

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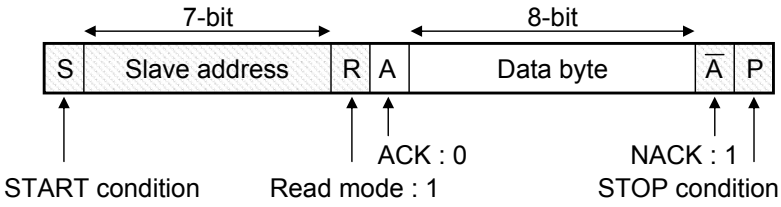
OPERATION (continued)

3. I²C-bus interface (continued)

3.4 DATA format (continued)

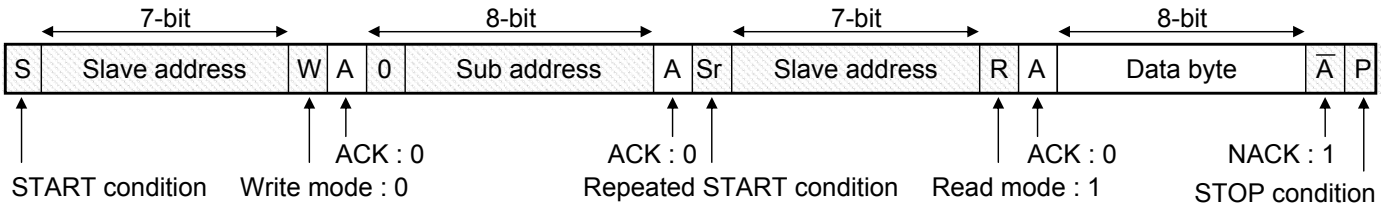
Read mode (In case sub address is not specified)

When data is read without assigning the sub address (8-bit), the data of the sub address assigned in the Write mode immediately before is read.



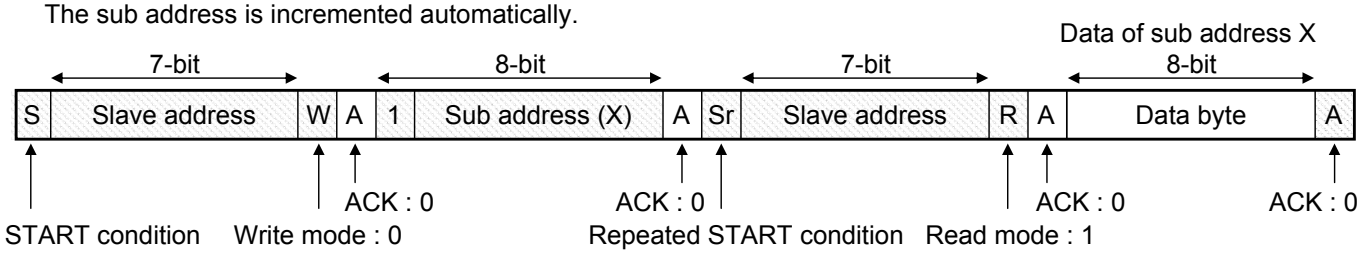
Read mode (In case sub address is specified)

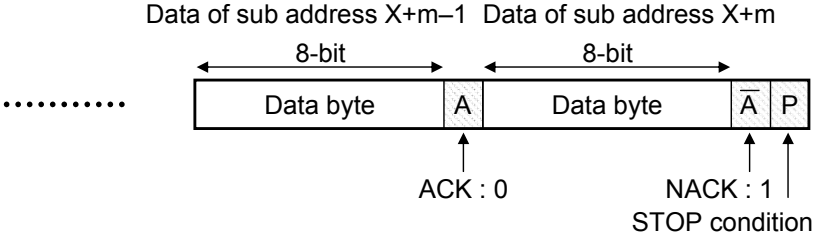
When MSB of sub address (8-bit) is "0", sub address is incremented automatically.
Data byte of specified sub address is read repeatedly continuously until STOP condition is received.



Read mode (Auto increment mode in case sub address is specified)

When MSB of sub address (8-bit) is "1", auto increment mode is specified.
Until STOP condition is received, data byte of sub address incremented automatically by specified sub address can be read continuously
The sub address is incremented automatically.





: Data transmission from Master

: Data transmission from Slave

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OPERATION (continued)

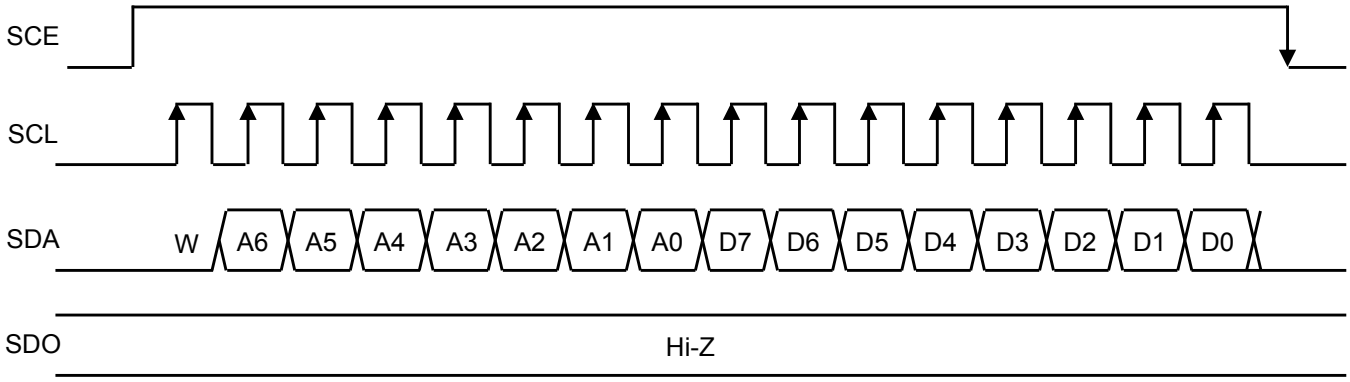
4. SPI interface

The interface with microcomputer consists of 16-bit serial register (8-bit of command, 8-bit of address), address recorder, and transmission register (8-bit).
Serial interface consists of 4 pins, which are a serial clock pin (SCL), a serial data input pin (SDA), a serial data output pin (SDO [=SLAVE]) and a chip enable input pin (SCE [=GPIO2]).
When SPI interface is used in this LSI, SERSEL pin should be fixed to High-level.

4.1 Reception operation

At MSB first, when SDA is Low at 1st CLK of SCL, Write is recognized.
Data is taken into an internal shift register at the rising edge of SCL.
(It is possible to use a maximum frequency of 13 MHz as SCL frequency.)
In High interval of SCE, reception of data becomes ENABLE. (active : High)
Data is transmitted at MSB first in order of control register address (8-bit) and control command (8-bit).

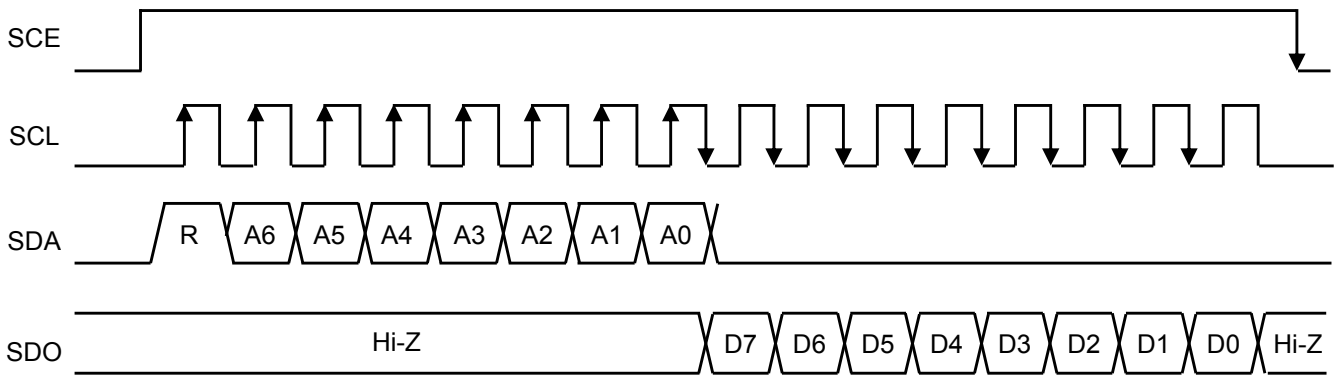
Timing of reception



4.2 Transmission operation

At MSB first, when SDA is High at 1st CLK of SCL, Read is recognized.
Data is taken into an internal sift register at the rising edge of SCL.
(It is possible to use a maximum frequency of 13 MHz as SC frequency.)
In High interval of SCE, transmission of data becomes ENEBLE. (active : High)
Data is transmitted at MSB first in order of control register address (8-bit) and control command (max. 8-bit).
RAM is not read.

Timing of transmission



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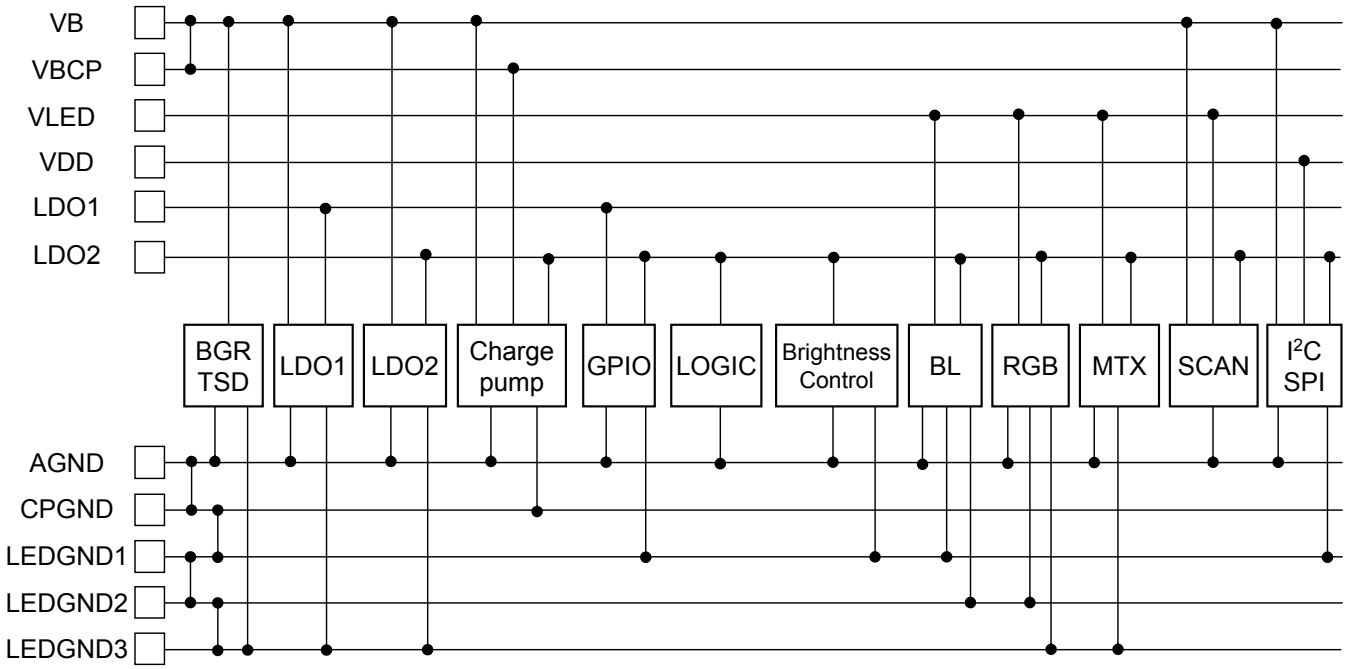
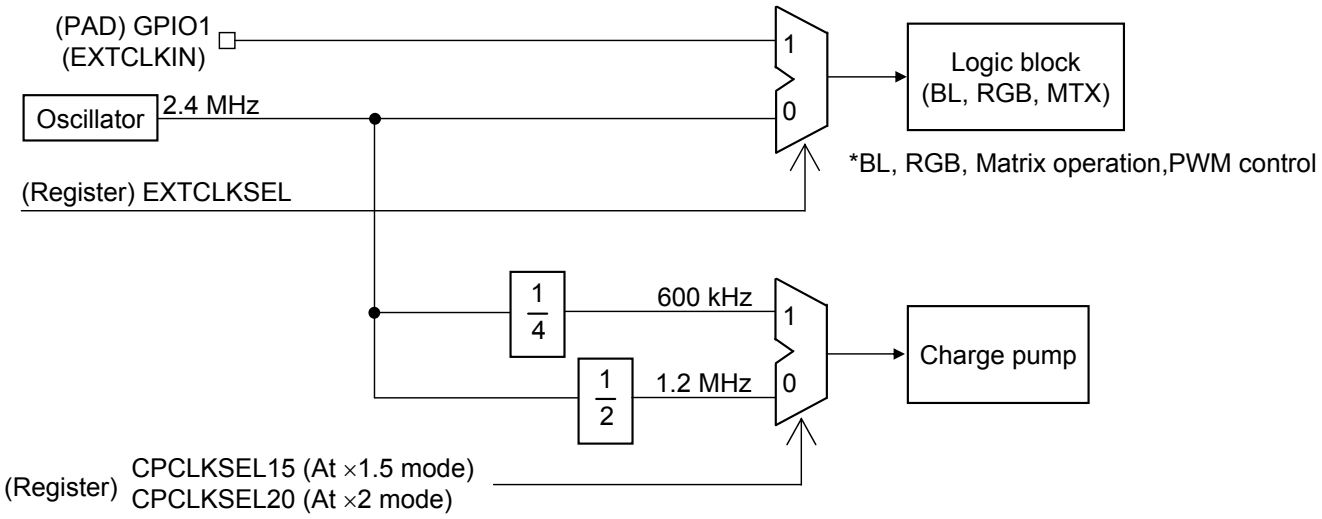
OPERATION (continued)

5. Signal distribution diagram

Distribution diagram of power supply system



Distribution diagram of control / clock system



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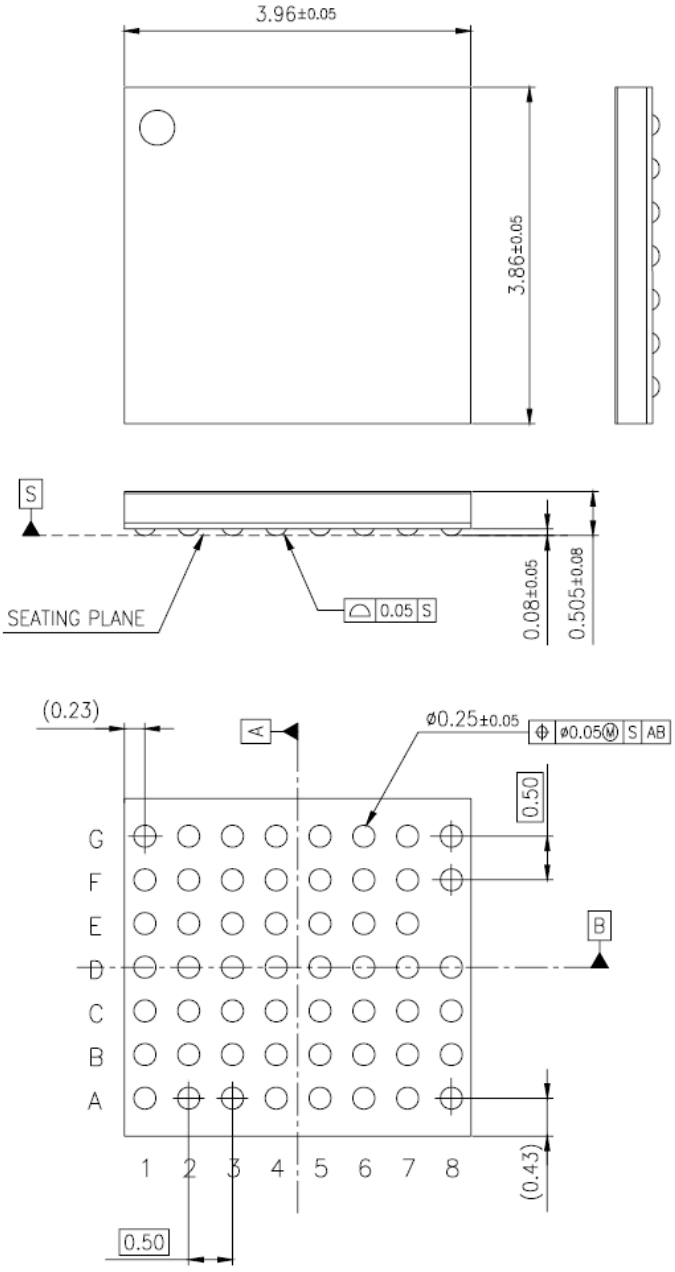
PACKAGE INFORMATION (Reference Data)

Package Code : ULGA055-W-3940AKL

Unit:mm



Body Materia l	: Br/Sb Free Epoxy resin
Reroute Material	: Cu
Bump	: SnAgCu

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IMPORTANT NOTICE

1. When using the LSI for new models, verify the safety including the long-term reliability for each product.
2. When the application system is designed by using this LSI, please confirm the notes in this book.
   Please read the notes to descriptions and the usage notes in the book.
3. This LSI is intended to be used for general electronic equipment.
   Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this LSI may directly jeopardize life or harm the human body.
   Any applications other than the standard applications intended.
   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for automobile, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required
   Our company shall not be held responsible for any damage incurred as a result of or in connection with the LSI being used for any special application, unless our company agrees to the use of such special application.
4. This LSI is neither designed nor intended for use in automotive applications or environments unless the specific product is designated by our company as compliant with the ISO/TS 16949 requirements.
   Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the LSI being used in automotive application, unless our company agrees to such application in this book.
5. Please use this product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our LSI being used by our customers, not complying with the applicable laws and regulations.
6. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might emit smoke or ignite.
7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the semiconductor device. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.
9. Take notice in the use of this product that it might be damaged or occasionally emit smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply..
10. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
    Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.
11. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
12. Verify the risks which might be caused by the malfunctions of external components.
13. Due to the unshielded structure of this LSI, functions and characteristics of the product cannot be guaranteed under the exposure of light. During normal operation or even under testing condition, please ensure that the LSI is not exposed to light.
14. Please ensure that your design does not have metal shield parts touching the chip surface as the surface potential is GND voltage.
15. Pay attention to the breakdown voltage of this LSI when using.
    More than + 1100 V or less than – 1100 V electrostatic discharge to all the pins might damage this product.

Established : 2011-05-30
Revised : 2013-04-16

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Consult our sales staff in advance for information on the following applications:
- Special applications (such as for airplanes, aerospace, automotive equipment, traffic signaling equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.

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(4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

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