
1 GBPS TO 4.25 GBPS MULTI-RATE VCSEL DRIVER

FEATURES

- Multi-Rate Operation from 1 Gbps Up To 4.25 Gbps
- 2-Wire Digital Interface
- Digitally Selectable Modulation Current
- Digitally Selectable Bias Current
- Automatic Power Control (APC) Loop
- Supports Transceiver Management System (TMS)
- Includes Laser Safety Features
- Analog Temperature Sensor Output
- Single 3.3-V Supply

- Operating Temperature –40°C to 85°C
- Small Footprint Surface Mount 4 mm × 4 mm, 20-Pin QFN Package

APPLICATIONS

- Multirate SFP/SFF Modules
- 1.0625 Gbps, 2.125 Gbps, and 4.25 Gbps Fibre Channel Transmitters
- Gigabit Ethernet Transmitters

DESCRIPTION

The ONET4291VA is a versatile high-speed multi-rate VCSEL driver for fiber optic applications with data rates up to 4.25 Gbps.

The device provides a 2-wire interface which allows digital control of the modulation and bias currents, eliminating the need for external components.

The ONET4291VA includes an integrated automatic power control loop as well as circuitry to support laser safety and transceiver management systems.

The part is available in a small footprint 4 mm × 4 mm 20-pin QFN package and it requires a single 3.3-V supply.

This power efficient multi-rate VCSEL driver is characterized for operation from –40°C to 85°C ambient temperature.

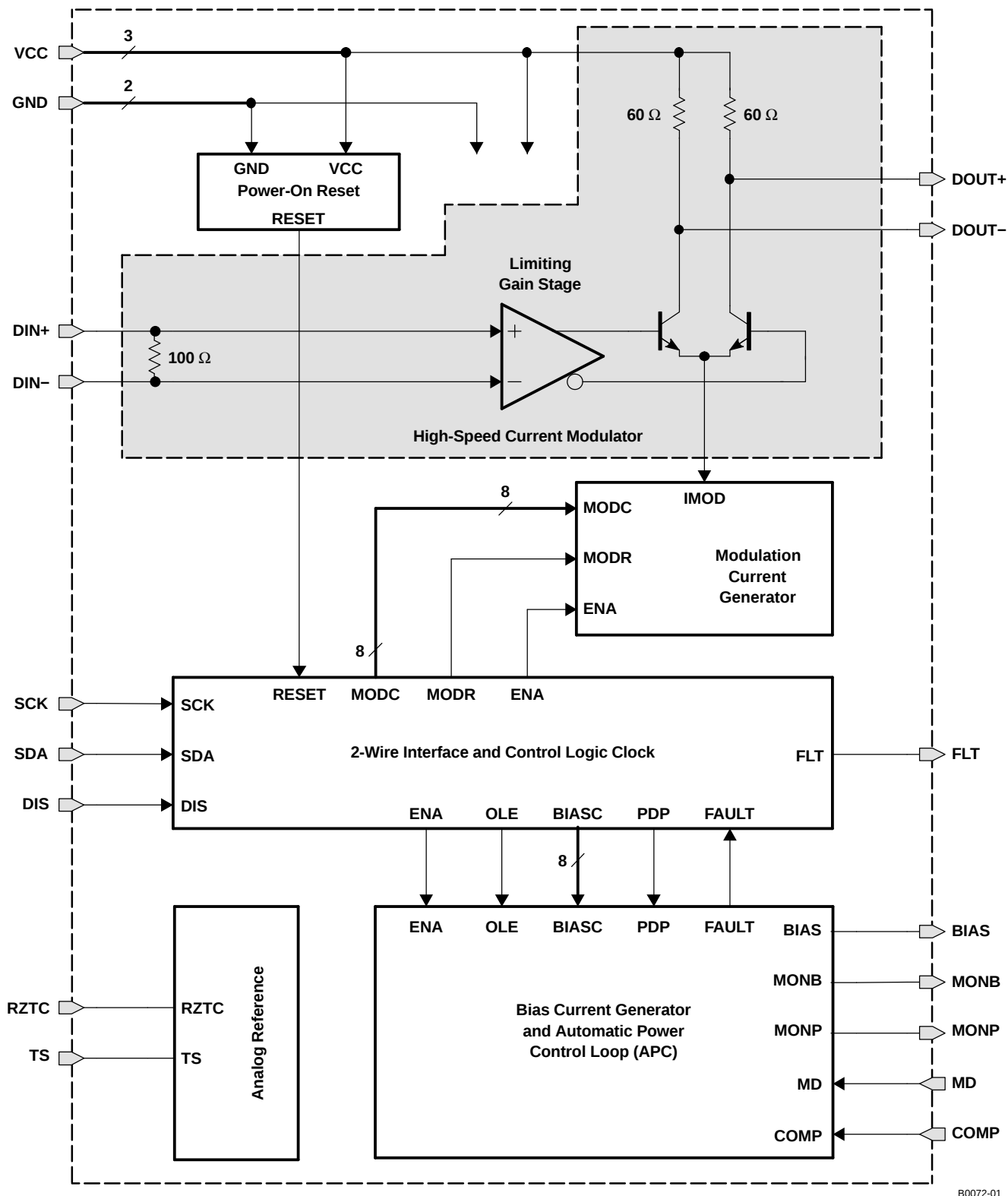
BLOCK DIAGRAM

A simplified block diagram of the ONET4291VA is shown in [Figure 1](#).

This compact, low power 1-Gbps to 4.25-Gbps multi-rate VCSEL driver consists of a high-speed current modulator, a modulation current generator, power-on reset circuitry, a 2-wire interface and control logic block, a bias current generator and automatic power control loop, and an analog reference block.



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B0072-01

Figure 1. Simplified Block Diagram of the ONET4291VA

HIGH-SPEED CURRENT MODULATOR

The data signal is applied to the high-speed current modulator by means of the input signal pins DIN+/DIN–, which provide on-chip differential 100-Ω line-termination. The succeeding limiting gain stage ensures sufficient drive amplitude and edge-speed for driving the current modulator differential pair.

The modulation current is sunk from the common emitter node of the differential pair by means of a modulation current generator, which is digitally controlled by the 2-wire interface and control logic block.

The collector nodes of the differential pair are connected to the output pins DOUT+/DOUT–, which include on-chip $2 \times 60\text{-}\Omega$ back-termination to VCC. The 60-Ω back-termination helps to sufficiently suppress signal distortion caused by double reflections for VCSEL diodes with impedances ranging from 50 Ω through 75 Ω.

MODULATION CURRENT GENERATOR

The modulation current generator provides the current for the current modulator described above. The circuit is digitally controlled by the 2-wire interface and control logic block.

An 8-bit wide control bus, MODC, is used to set the desired modulation current.

Furthermore, two modulation current ranges are selected by means of the MODR signal.

The ENA signal enables or disables the modulation current generator.

The modulation current can be disabled by setting the DIS input pin to a high level. The modulation current is also disabled in a fault condition if the fault detection enable register flag FLTEN is set.

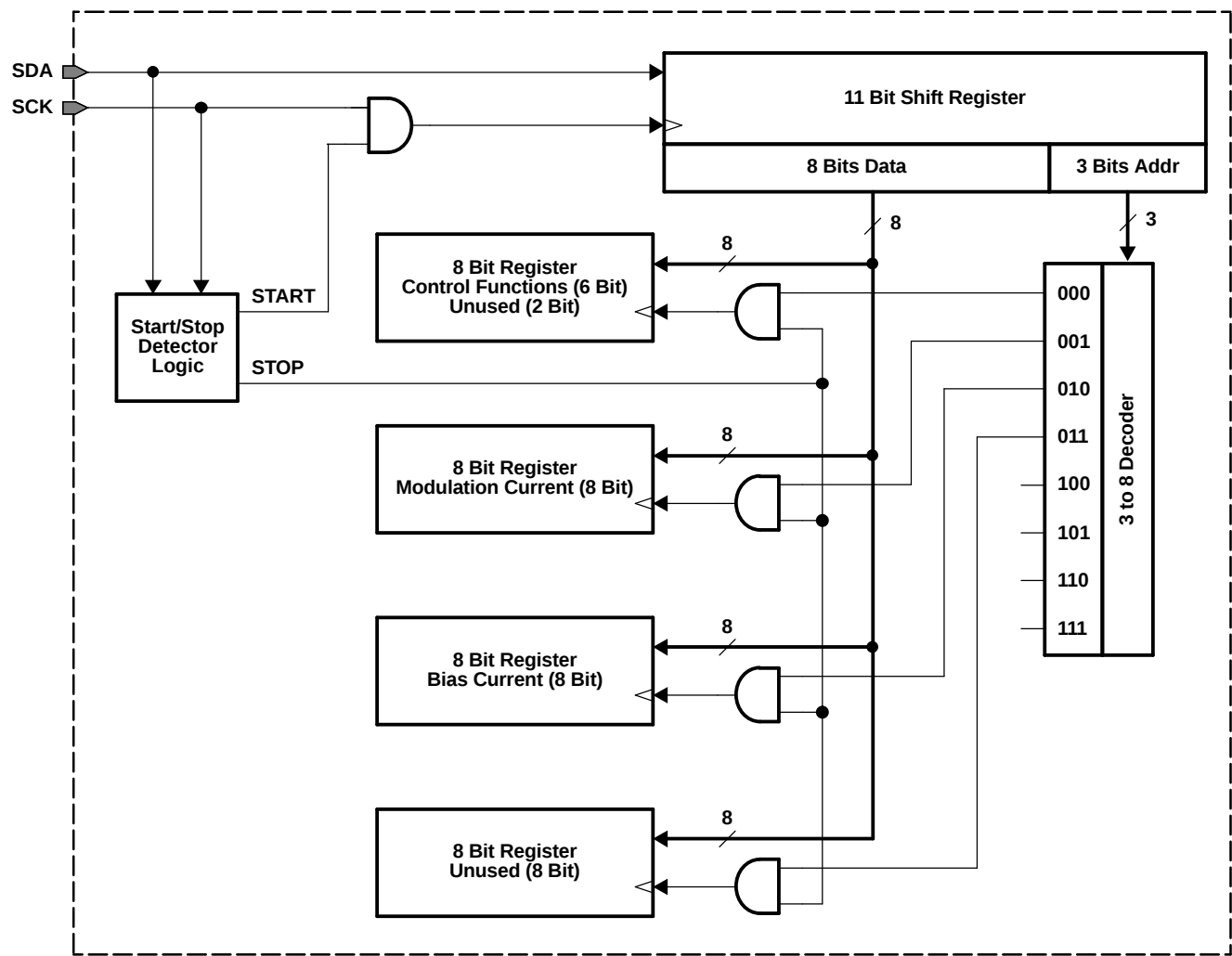
For more information about the register functionality, see the register mapping description.

2-WIRE SERIAL INTERFACE AND CONTROL LOGIC

The ONET4291VA uses a 2-wire serial interface for digital control. A simplified block diagram of this interface is shown in [Figure 2](#).

The two circuit inputs, SDA and SCK, are driven, respectively, by the serial data and serial clock from a microprocessor, for example. Both inputs include 100-kΩ pullup resistors to VCC. For driving these inputs, an open drain output is recommended.

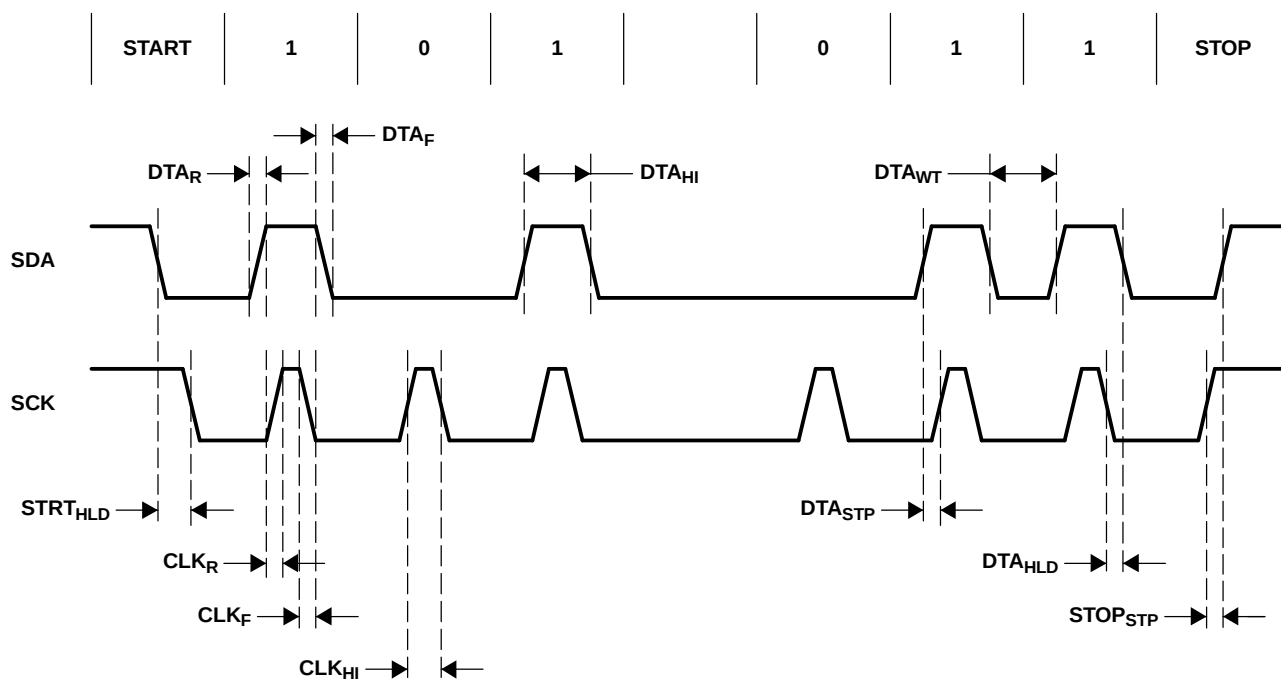
A write cycle consists of a START command, three address bits with MSB first, eight data bits with MSB first, and a STOP command. In idle mode, both SDA and SCK lines are at a high level.



B0068-02

Figure 2. Simplified 2-Wire Interface Block Diagram

The timing definition for the serial data signal SDA and the serial clock signal SCK is shown in [Figure 3](#). The corresponding timing requirements are listed in [Table 1](#).



T0077-01

Figure 3. 2-Wire Interface Timing Diagram

Table 1. 2-Wire Interface Timing

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
STRT _{HLD}	START hold time	Time required from data falling edge to clock falling edge at START	10	ns
CLK _R , DTA _R	Clock and data rise time		10	ns
CLK _F , DTA _F	Clock and data fall time		10	ns
CLK _{HI}	Clock high time	Minimum clock high period	50	ns
DTA _{HI}	Data high time	Minimum data high period	100	ns
DTA _{STP}	Data setup time	Minimum time from data rising edge to clock rising edge	10	ns
DTA _{WT}	Data wait time	Minimum time from data falling edge to data rising edge	50	ns
DTA _{HLD}	Data hold time	Minimum time from clock falling edge to data falling edge	10	ns
STOP _{STP}	STOP setup time	Minimum time from clock rising edge to data rising edge at STOP	10	ns

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Table 3. Register 1 (001b) Mapping

address 1 (001b)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
MODC7	MODC6	MODC5	MODC4	MODC3	MODC2	MODC1	MODC0

Table 4. Register 2 (010b) Mapping

address 2 (010b)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BIASC7	BIASC6	BIASC5	BIASC4	BIASC3	BIASC2	BIASC1	BIASC0

Table 5. Register 3 (011b) Mapping

address 3 (011b)							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

Table 6. Register Functionality

Symbol	Register	Function
ENA	Enable	Enables chip when set to 1. Can be toggled to reset a fault condition.
PDP	Photodiode polarity	Photodiode polarity bit: 1 = common anode 0 = common cathode

BIAS CURRENT GENERATION AND APC LOOP

The bias current generation and APC loop are controlled by means of the 2-wire interface.

In open loop operation, selected by setting OLE = 1 (bit 4 of register 0), the bias current is set directly by the 8-bit wide control word BIASC[0..7] (register 2).

In automatic power control mode, selected by setting OLE = 0, the bias current depends on the register settings BIASC[0..7] and the coupling ratio (CR) between the VCSEL bias current and the photodiode current.

$$CR = I_{\text{BIAS-VCSEL}} / I_{\text{PD}}$$

Two photodiode current ranges can be selected by means of the PDR register (bit 5 of register 0). The photodiode range should be chosen to keep the laser bias control DAC close to the center of its range. This keeps the laser bias current setpoint resolution high and the loop settling time constant within specification.

For details regarding the bias current setting in open loop as well as in closed loop mode, see [Table 6](#).

In closed loop mode, the photodiode polarity bit, PDP, must be set for common anode or common cathode configuration to ensure proper operation. In open loop mode if a photodiode is still present, the photodiode polarity bit must be set to the opposite setting.

ANALOG REFERENCE

The ONET4291VA is supplied by a single 3.3-V $\pm 10\%$ supply voltage connected to the VCC pins. This voltage is referenced to ground (GND).

On-chip bandgap voltage circuitry generates a reference voltage, independent of the supply voltage, from which all other internally required voltages and bias currents are derived.

An external zero temperature coefficient resistor must be connected from the RZTC pin of the device to ground (GND). This resistor is used to generate a precise zero TC current which is used as a reference current for the on-chip DACs.

In order to minimize the module component count, the ONET

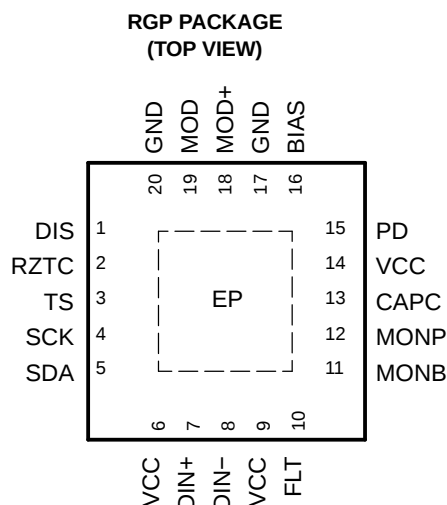
2. Setting the modulation current to zero.
3. Asserting and latching the FLT pin.

Fault recovery is performed by the following procedure:

1. The disable pin DIS and/or the enable control bit ENA are toggled for at least the fault latch reset time T_{RESET} .
2. The FLT pin de-asserts while the disable pin DIS is asserted or the enable bit ENA is de-asserted.
3. If the fault condition is no longer present, the part will return to normal operation with its prior output settings after the disable negate time T_{ON} .
4. If the fault condition is still present, FLT re-asserts once DIS is set to low level and the part will not return to normal operation.

PACKAGE

For the ONET4291VA, a small footprint 4 mm × 4 mm 20-pin QFN package with a lead pitch of 0,5 mm is used. The pin out is shown in [Figure 4](#).



P0031-01

Figure 4. Pinout of ONET4291VA in a 4 mm × 4 mm 20-Pin QFN Package

TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NO.	NAME		
1	DIS	CMOS-in	Dis

TERMINAL FUNCTIONS (continued)

TERMINAL		TYPE	DESCRIPTION
NO.	NAME		
12	MONP	Analog-out	Photodiode current monitor. Sources a 50% replica of the photodiode current. Connect an external resistor to ground (GND).
13	CAPC	Analog	Compensation pin used to control the bandwidth of the APC loop. Connect a 0.01-μF capacitor to ground.
15	PD	Analog	Monitor photodiode input. The pin can source or sink current dependent on PDP register setting. Pin supplies >1.5-V reverse bias.
16	BIAS	Analog	VCSEL diode bias current source. Connect to laser anode through inductor. Murata BLM15HG102SN1 is recommended.
17, 20, EP	GND	Supply	Circuit ground. The exposed die pad (EP) must be grounded.
18	MOD+	CML-out	Non-inverted modulation current output. AC coupled to anode of common cathode VCSEL. On-chip 60-Ω back-terminated to VCC.
19	MOD–	CML-out	Inverted modulation current output. AC coupled through VCSEL matching resistor to ground (GND). On-chip 60-Ω back-terminated to VCC.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		VALUE / UNIT
V _{CC}	Supply voltage	–0.3 V to 4 V
V _{DIS} , V _{RZTC} , V _{TS} , V _{SCK} , V _{SDA} , V _{DIN+} , V _{DIN–} , V _{FLT} , V _{MONB} , V _{MONP} , V _{CAPC} , V _{PD} , V _{BIAS} , V _{MOD+} , V _{MOD–}	Voltage at DIS, RZTC, TS	

DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions, all values are for open loop operation, $I_{MOD} = 6$ mA, $I_{BIAS} = 5$ mA, and $R_{RZTC} = 30$ k Ω , unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} Supply voltage		2.9	3.3	3.6	V
I_{VCC} Supply current	$I_{MOD} = 6$ mA, $I_{BIAS} = 5$ mA, including I_{MOD} and I_{BIAS}		40	45	mA
	Disabled, DIS = high and/or control bit ENA = low		22		
R_{IN} Data input/output resistance	Differential between DIN+/DIN–	85	100	115	Ω
R_{OUT} Data output/output resistance	Single-ended to VCC	50	60	70	Ω
CMOS input current	SCK, SDA, 100-k Ω pullup to VCC	–50		10	μ A
CMOS input current	DIS	–10		10	μ A
V_{OH} CMOS output high voltage	FLT, $I_{SINK} = 1$ mA	2.5			V
V_{OL} CMOS output low voltage	FLT, $I_{SOURCE} = 1$ mA			0.5	V
$I_{BIAS-DIS}$ Bias current during disable				100	μ A
$I_{BIAS-MIN}$ Minimum bias current	See (1)			0.2	mA
$I_{BIAS-MAX}$ Maximum bias current	DAC set to maximum, closed loop	8.5			mA
	DAC				

AC ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions with 50-Ω output load, open loop operation, $I_{MOD} = 6 \text{ mA}$, $I_{BIAS} = 5 \text{ mA}$, and $R_{RZTC} = 30 \text{ k}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
τ_{APC}	APC time constant	$C_{APC} = 0.01 \mu\text{F}$, $I_{PD} = 100 \mu\text{A}$, PD coupling ratio $CR = 1/40$ ⁽²⁾		200		μs
T_{OFF}	Transmitter disable time	Rising edge of DIS to $I_{BIAS} \leq 0.1 \times I_{BIAS-NOMINAL}$ ⁽²⁾		2.4	5	μs
T_{ON}	Disable negate time	Falling edge of DIS to $I_{BIAS} \geq 0.9 \times I_{BIAS-NOMINAL}$ ⁽²⁾			1	ms
T_{INIT1}	Power-on to initialize	Power-on to registers ready to be loaded		20	250	ms
T_{INIT2}	Initialize to transmit	Register load STOP command to part ready to transmit valid data ⁽²⁾			2	ms
T_{RESET}	DIS pulse width	Time DIS must held high to reset part ⁽²⁾	100			ns
T_{FAULT}	Fault assert time	Time from fault condition to FLT high ⁽²⁾			50	μs

(2) Assured by simulation over process, supply, and temperature variation.

TYPICAL CHARACTERISTICS

Typical operating condition is at $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

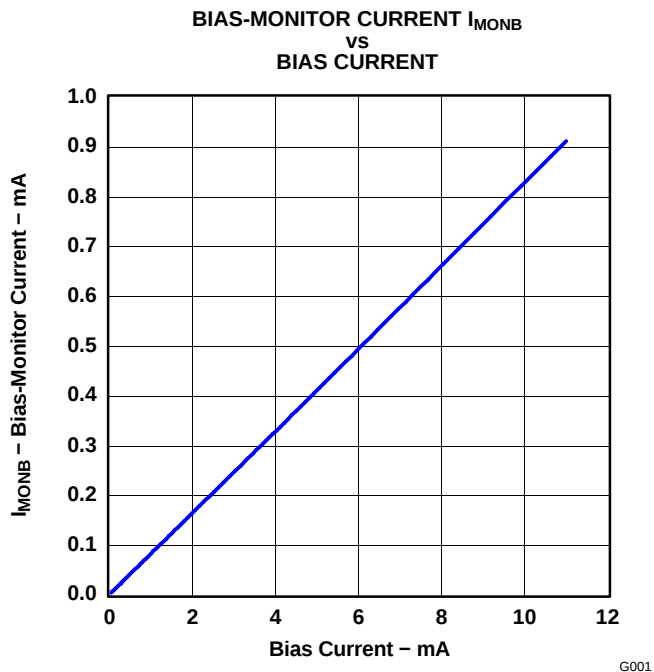
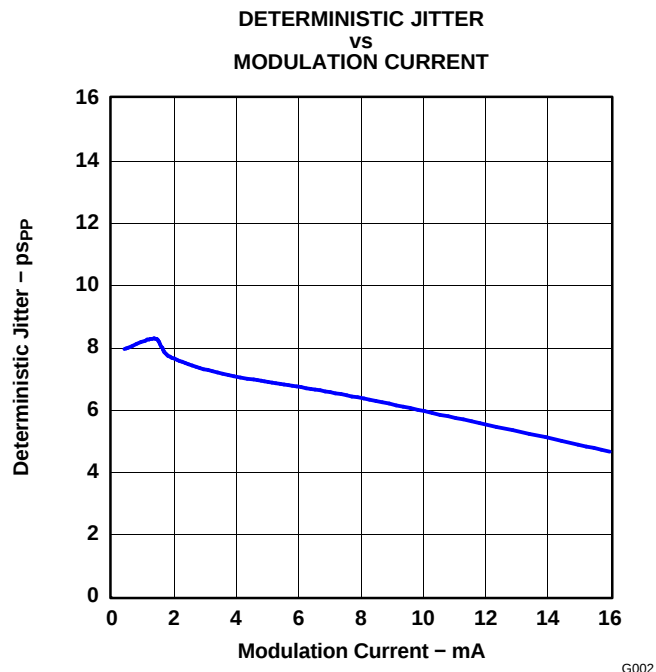


Figure 5.



TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

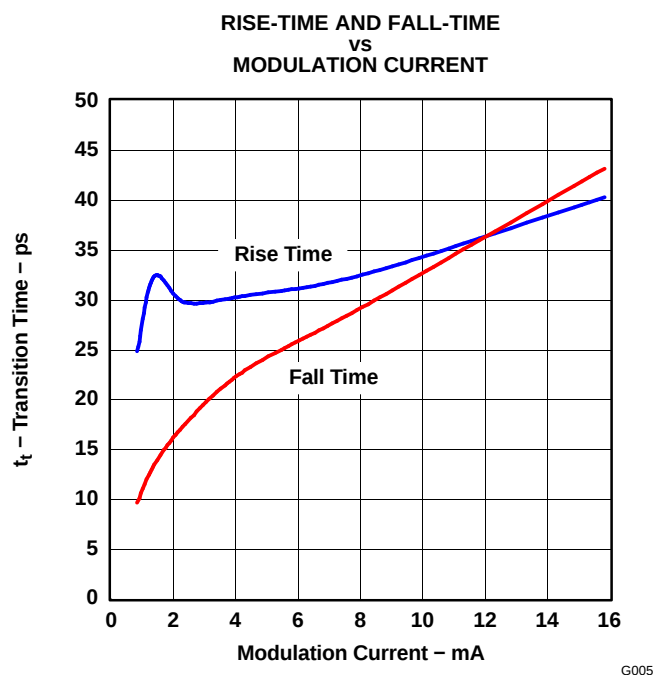


Figure 9.

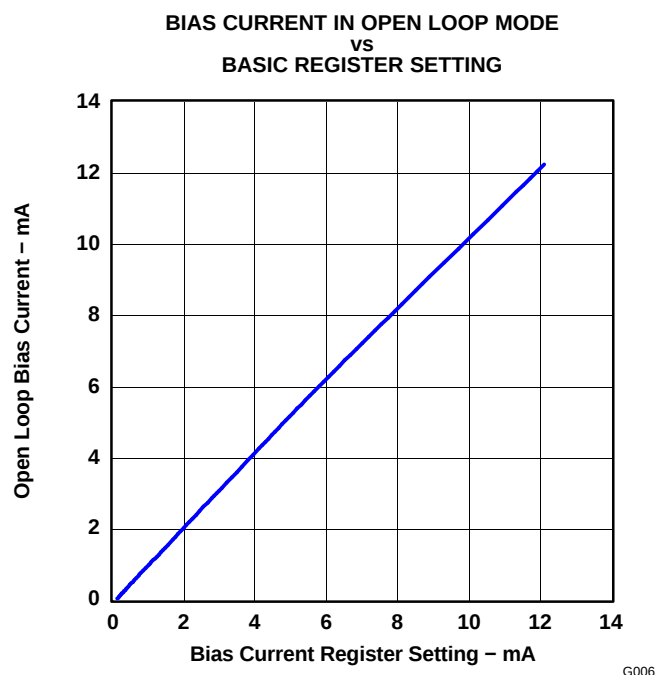


Figure 10.

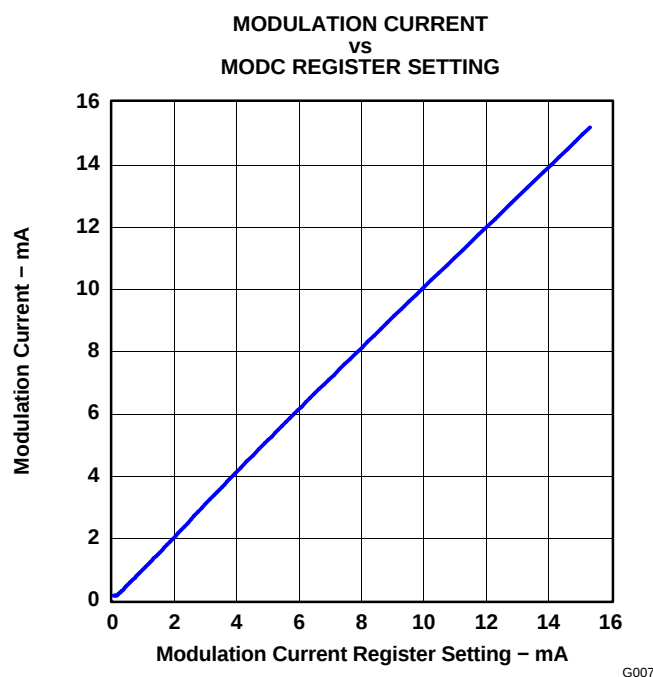
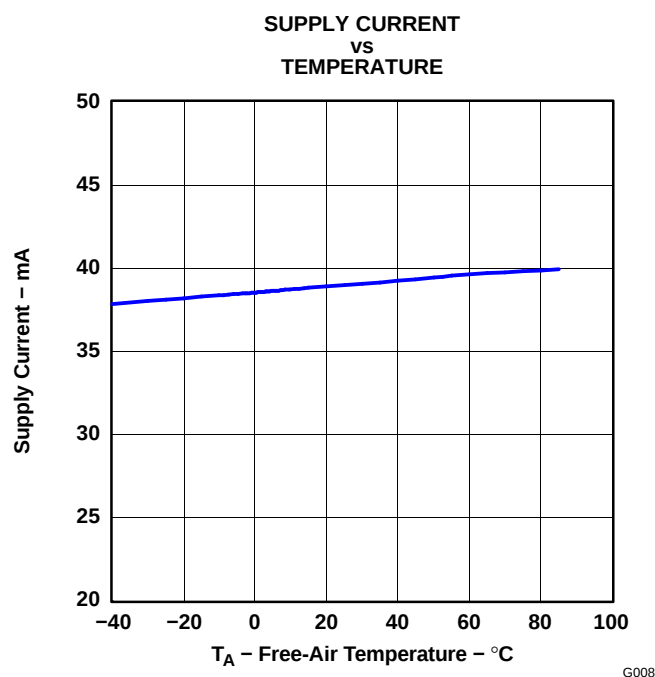


Figure 11.



TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

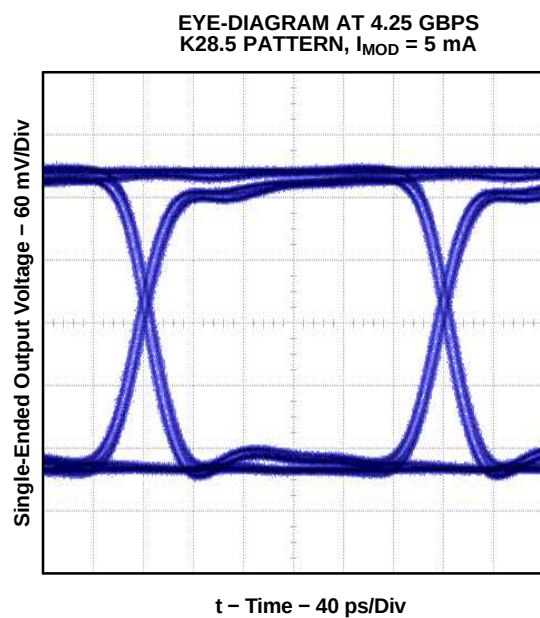


Figure 13.

G009

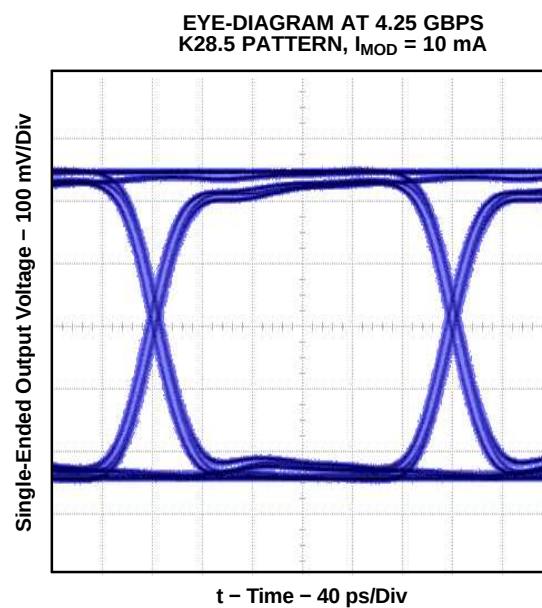


Figure 14.

G010

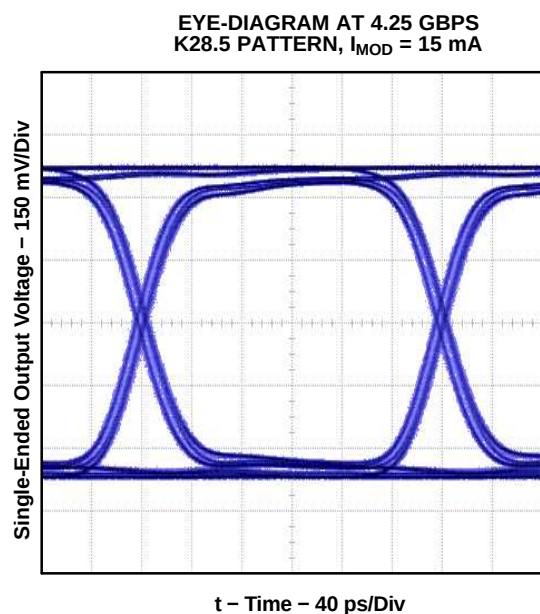
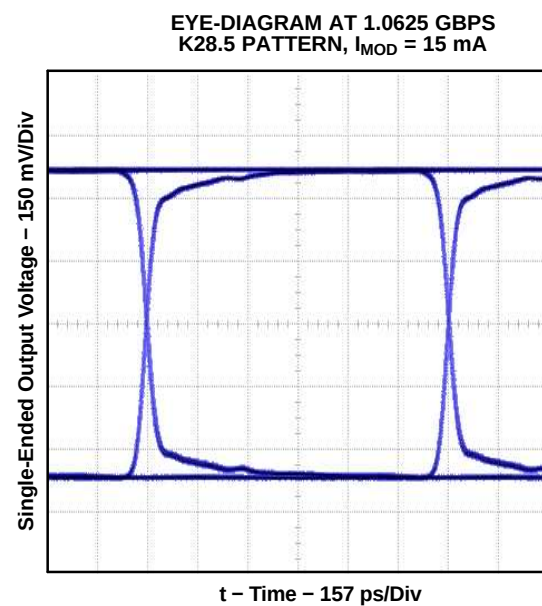


Figure 15.

G011



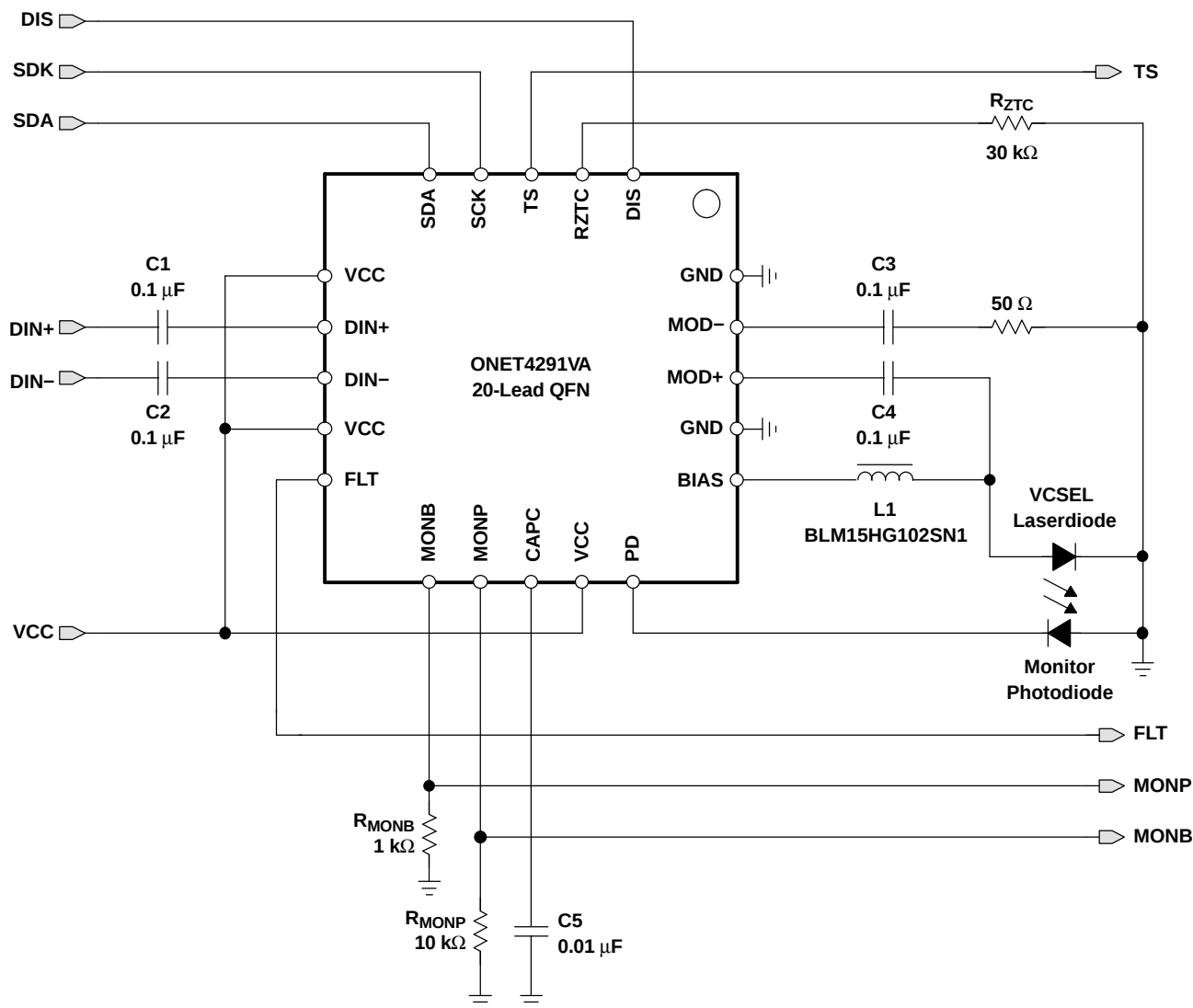
APPLICATION INFORMATION

Figure 17 shows a typical application circuit using the ONET4291VA with a common cathode VCSEL connected to ground.

The VCSEL driver is controlled via the 2-wire interface SDA/SCK by a microprocessor.

In a typical application, the FLT, MONB, MONP, and TS outputs are connected to the microcontroller for transceiver management purposes.

The component values in Figure 17 are typical examples and may be varied according to the intended application.



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
ONET4291VARGPR	ACTIVE	QFN	RGP	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	ONET 4291V	Samples
ONET4291VARGPRG4	ACTIVE	QFN	RGP	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	ONET 4291V	Samples
ONET4291VARGPT	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	ONET 4291V	Samples
ONET4291VARGPTG4	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	ONET 4291V	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ONET4291VARGPR	QFN	RGP	20	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ONET4291VARGPT	QFN	RGP	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

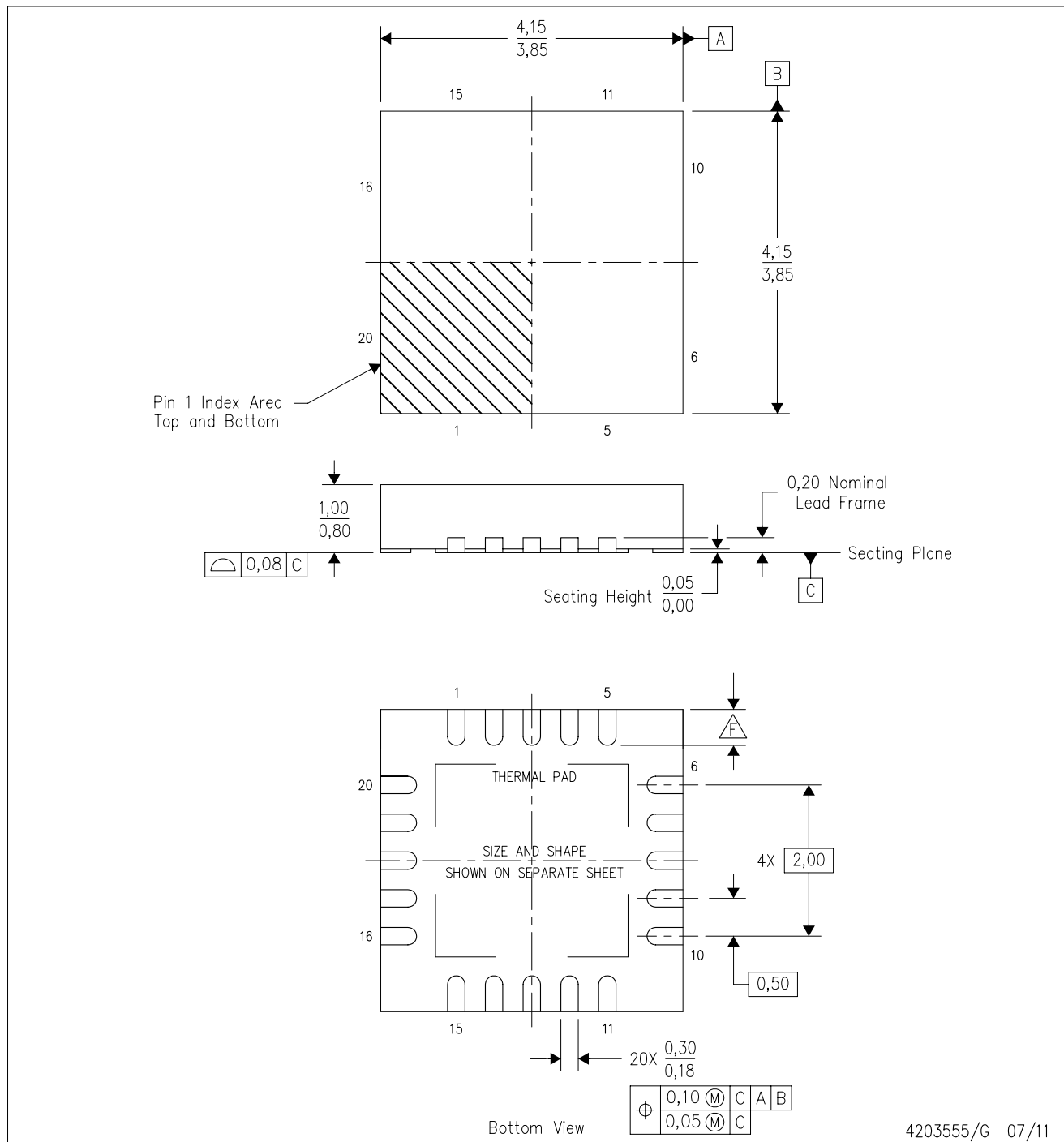


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ONET4291VARGPR	QFN	RGP	20	2500	367.0	367.0	35.0
ONET4291VARGPT	QFN	RGP	20	250	210.0	185.0	35.0

RGP (S-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



4203555/G 07/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

RGP (S-PVQFN-N20)

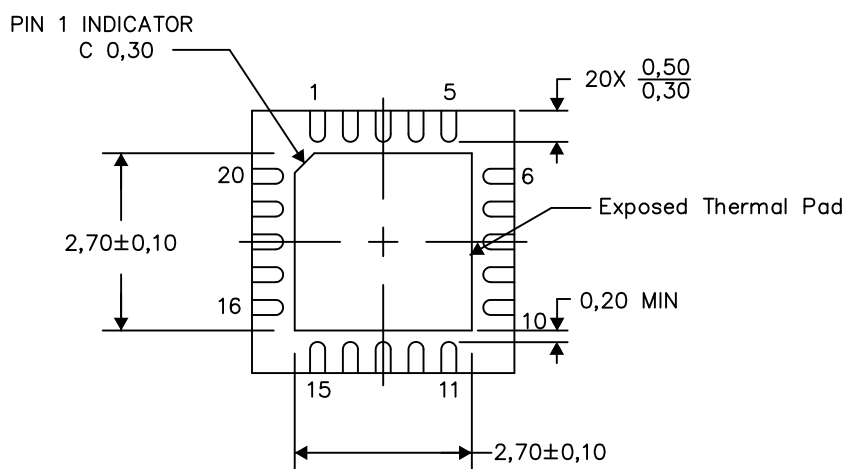
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



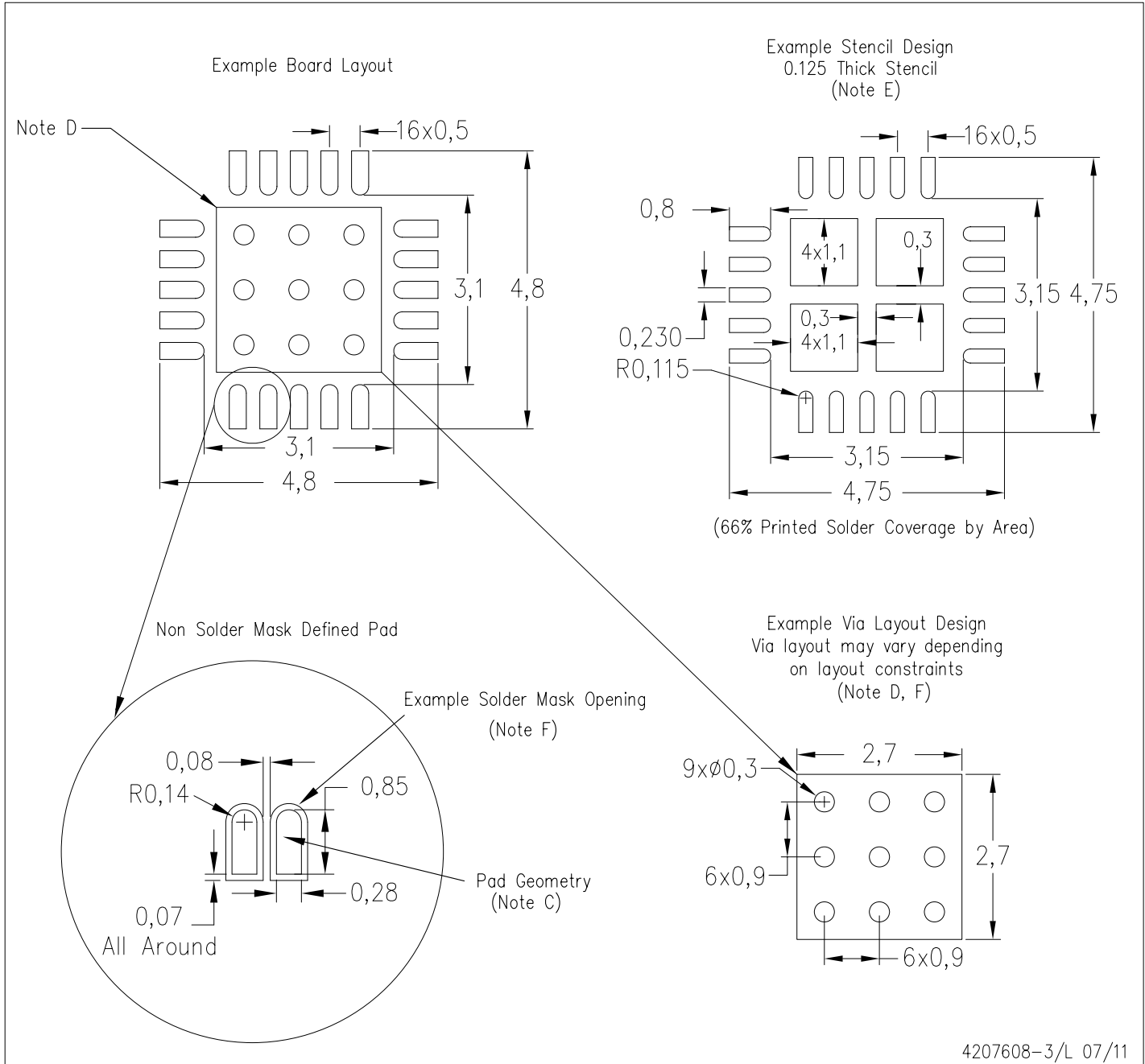
Exposed Thermal Pad Dimensions

4206346-3/Y 12/12

NOTES: A. All linear dimensions are in millimeters

RGP (S-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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Электрон
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Телефон: +7 812 627 14 35

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Адрес: 198099, Санкт-Петербург,
Промышленная ул, дом № 19, литера Н,
помещение 100-Н Офис 331