3STL2540

Low voltage high performance PNP power transistor

Datasheet — production data

Features

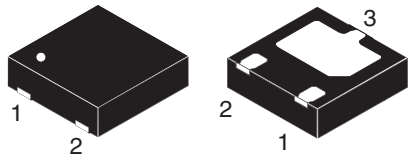
- Very low collector-emitter saturation voltage
- High current gain characteristic
- Small, thin, leadless SMD plastic package with excellent thermal behavior

Applications

- Power management
- DC-DC converters

Description

This device is an PNP transistor manufactured using new low voltage planar technology with double metal process. The result is a transistor which boasts exceptionally high gain performance coupled with very low saturation voltage.



PowerFLAT™ 2 x 2 3L

Figure 1. Internal schematic diagram

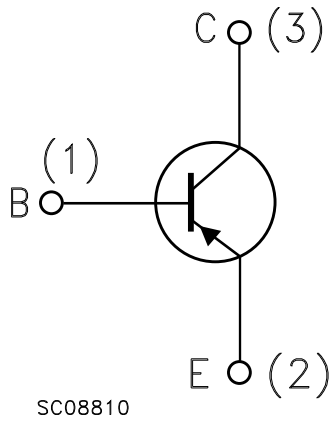


Table 1. Device summary

Order code	Marking	Package	Packaging
3STL2540	L2540	PowerFLAT™ 2 x 2	Tape and reel

1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-base voltage (I_E = 0)	-40	V
V_{CEO}	Collector-emitter voltage (I_B = 0)	-40	V
V_{EBO}	Emitter-base voltage (I_C = 0)	-6	V
I_C	Collector current	-5	A
I_{CM}	Collector peak current (t_P < 5 ms)	-10	A
I_B	Base current	-0.5	A
I_{BM}	Base peak current (t_P < 5 ms)	-1	A
P_{TOT}(1)	Total dissipation at T_A = 25 °C	1.2	W
T_{STG}	Storage temperature	-65 to 150	°C
T_J	Max. operating junction temperature	150	°C

1. Device mounted on a PCB area of 1 cm²

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}(1)	Thermal resistance junction-ambient max	104	°C/W
R_{thJA}(2)	Thermal resistance junction-ambient max	75	°C/W
R_{thJC}	Thermal resistance junction-case max	45	°C/W

1. Device mounted on a PCB area of 1 cm²
2. Device mounted on a PCB area of 6 cm²

2 Electrical characteristics

T_J = 25 °C; unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector cut-off current (I_E = 0)	V_{CB} = - 40 V			-100	nA
I_{EBO}	Emitter cut-off current (I_C = 0)	V_{EB} = - 6 V			-100	nA
$V_{BE(on)}$	Base-emitter on voltage	V_{CE} = - 2 V I_C = - 100 mA		-670		mV
$V_{CE(sat)}$ (1)	Collector-emitter saturation voltage	I_C = - 1 A I_B = - 10 mA I_C = - 2 A I_B = - 100 mA I_C = - 5 A I_B = - 250 mA		 -150 -300	-200	mV
$V_{BE(sat)}$ (1)	Base-emitter saturation voltage	I_C = - 1 A I_B = - 10 mA		800		mV
h_{FE} (1)	DC current gain	V_{CE} = - 2 V I_C = - 0.5 A V_{CE} = - 2 V I_C = - 2 A V_{CE} = - 2 V I_C = - 5 A		280 210 100		
		V_{CE} = -0.2 ÷ - 2 V I_C = - 1 A T_j = -30 °C ÷ 150 °C	100		900	
t_d t_r t_s t_f	Resistive load Delay time Rise time Storage time Fall time	I_C = - 2 A V_{CC} = - 10 V $V_{BE(off)}$ = 5 V, - $I_{B(on)}$ = $I_{B(off)}$ = 200 mA		 25 140 290 60		 ns ns ns ns
f_T	Transition frequency	I_C = - 0.1 A V_{CE} = - 10 V		130		MHz

1. Pulse test: pulse duration ≤300 µs, duty cycle ≤2 %.

2.1 Electrical characteristics (curves)

Figure 2. DC current gain (V_{CE}=-2 V)

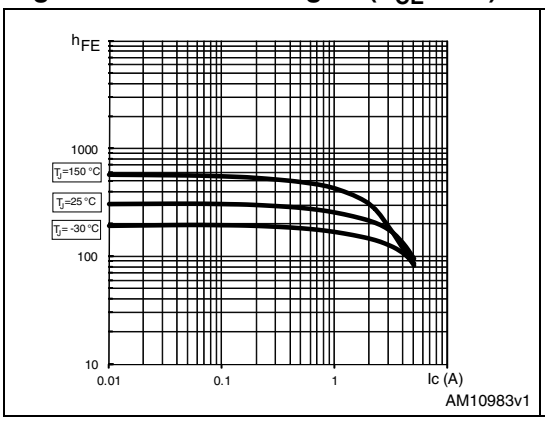


Figure 3. DC current gain (V_{CE}=-5 V)

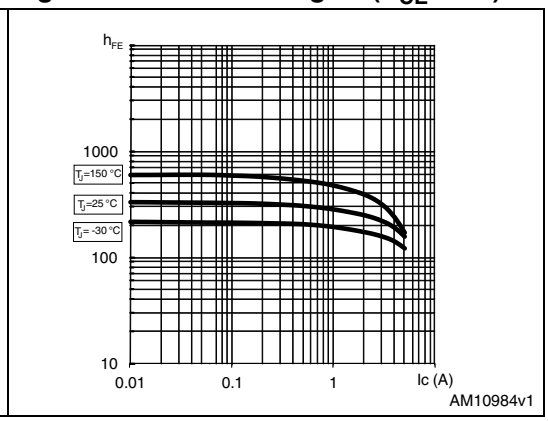


Figure 4. Collector-emitter saturation voltage (V_{CEsat} @ h_{FE}=20)

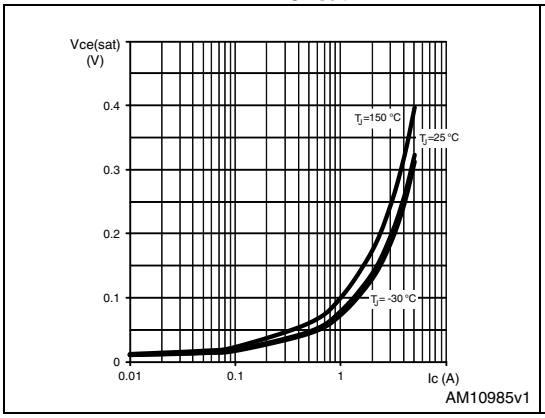


Figure 5. Collector-emitter saturation voltage (V_{CEsat} @ h_{FE}=100)

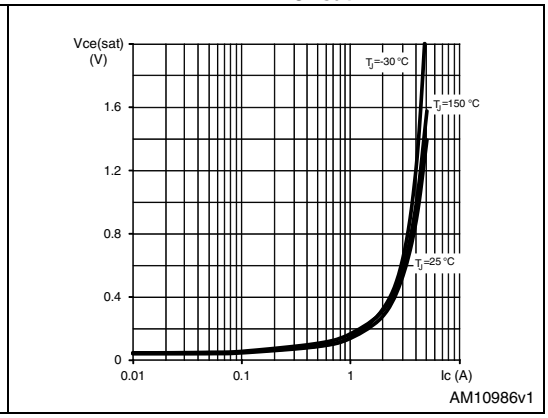


Figure 6. Base-emitter saturation voltage ($V_{be(sat)}$ @ h_{FE}=20)

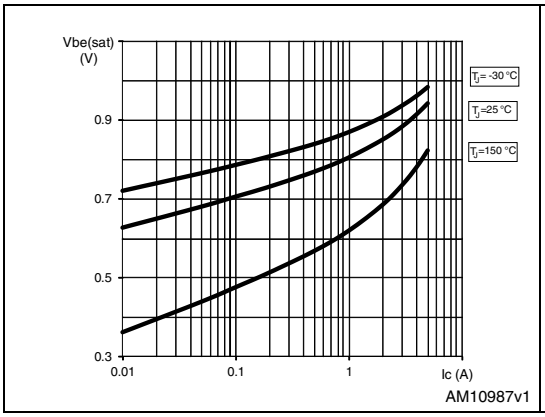


Figure 7. Base-emitter saturation voltage ($V_{be(sat)}$ @ h_{FE}=100)

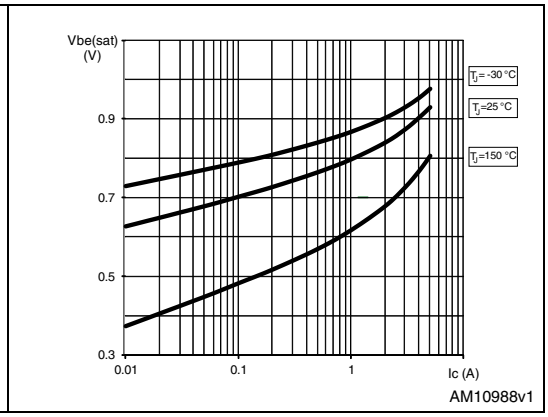


Figure 8. Resistive load switching times

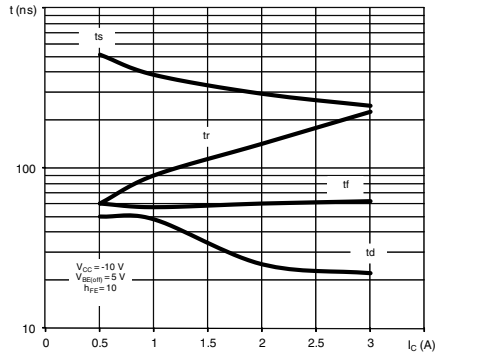
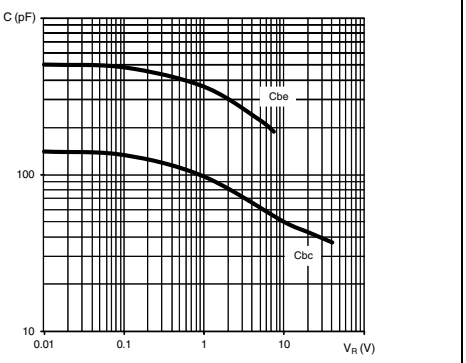


Figure 9. Capacitance curves (f=1 MHz)



3 Package mechanical data

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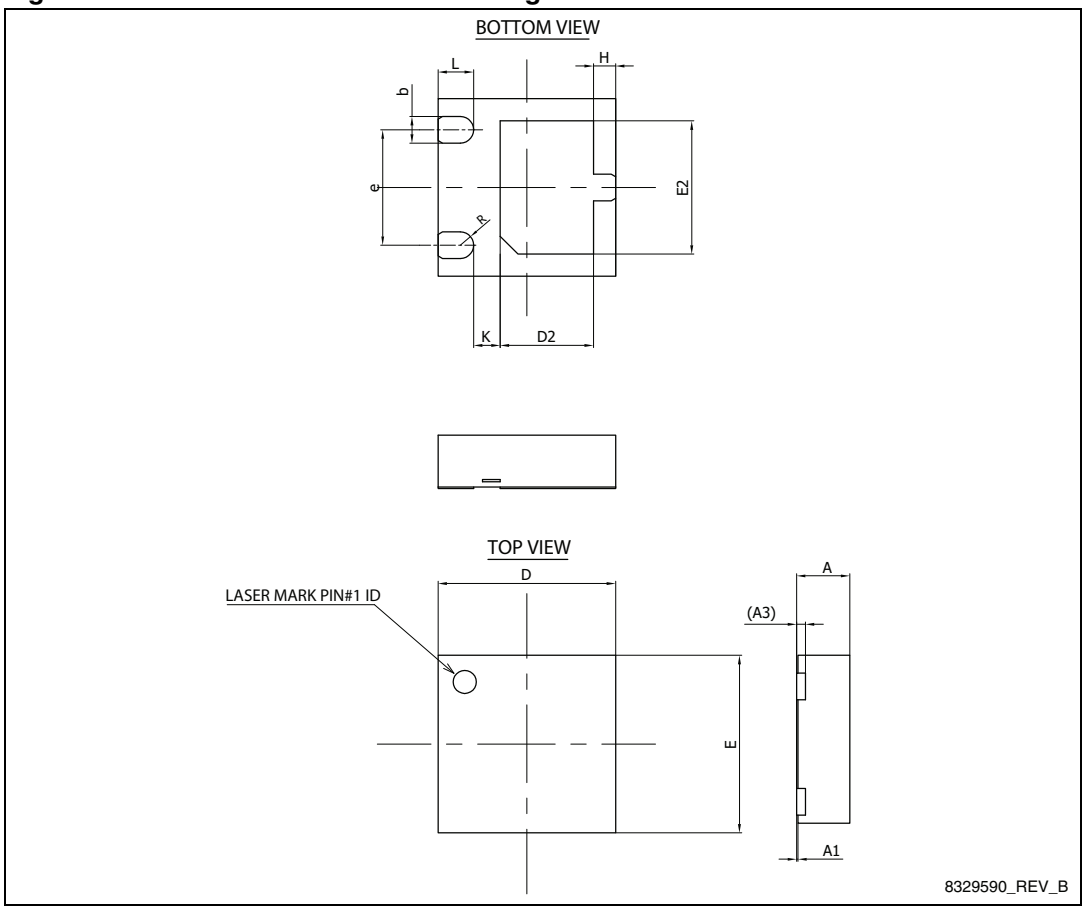
Table 5. PowerFLAT™ 2 x 2 3L mechanical data

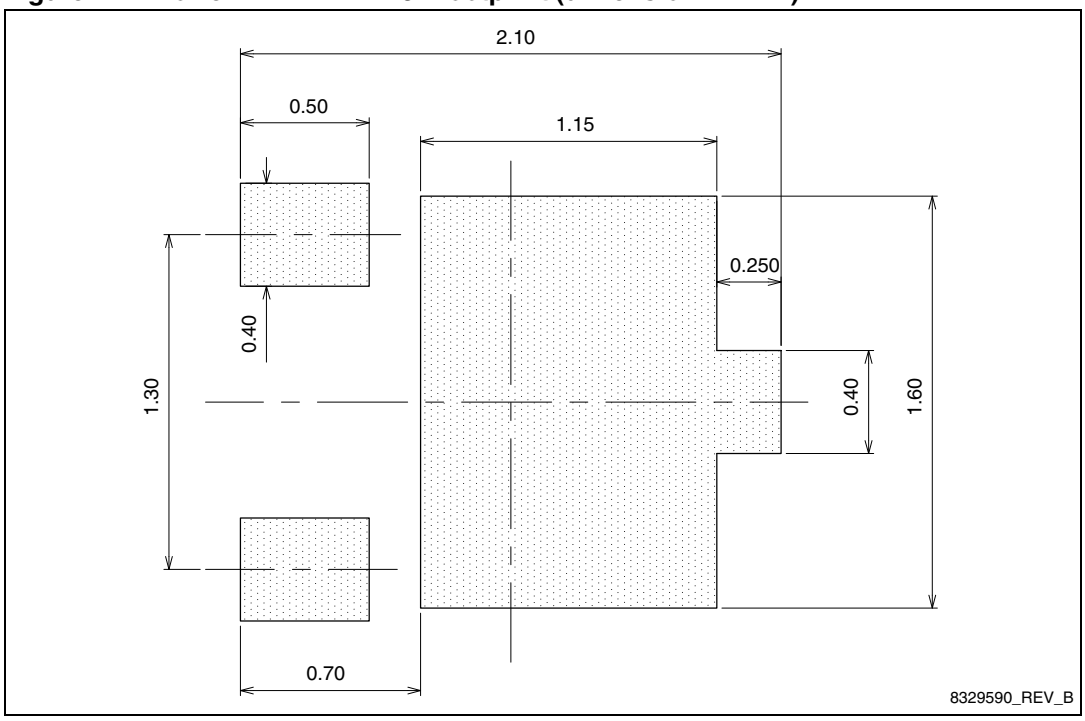
Dim.	mm.		
	Min.	Typ.	Max.
A	0.55	0.60	0.65
A1	0.00	0.02	0.05
A3		0.10	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
E	1.90	2.00	2.10
e	1.20	1.30	1.40
D2	0.95	1.05	1.15
E2	1.40	1.50	1.60
H	0.20	0.25	0.30
K	0.20	0.30	0.40
L	0.35	0.40	0.45
R	0.15		

Figure 10. PowerFLAT™ 2 x 2 3L drawing



4 Packaging mechanical data

Figure 11. PowerFLAT™ 2 x 2 3L footprint (dimension in mm.)



5 Revision history

Table 6. Document revision history

Date	Revision	Changes
07-Dec-2011	1	Initial release
22-May-2012	2	Document status promoted from preliminary data to production data

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