10-Bit, 4× Oversampled SDTV Video Decoder with Deinterlacer

Data Sheet

ADV7280

FEATURES

- Worldwide NTSC/PAL/SECAM color demodulation support
- One 10-bit analog-to-digital converter (ADC), 4× oversampling per channel for CVBS, Y/C, and YPrPb modes
- Analog video input channels with on-chip antialiasing filter
  - ADV7280: up to 4 input channels
  - ADV7280-M: up to 8 input channels
- Video input support for CVBS (composite), Y/C (S-Video), and YPrPb (component)
- NTSC/PAL/SECAM autodetection
- Up to 1.47 V common-mode input range solution
- Excellent common-mode noise rejection capabilities
- 5-line adaptive 2D comb filter and CTI video enhancement
- Adaptive Digital Line Length Tracking (ADLLT), signal processing, and enhanced FIFO management provide mini-time base correction (TBC) functionality
- Integrated automatic gain control (AGC) with adaptive peak white mode
- Fast switching capability
- Integrated interlaced-to-progressive (I2P) video output converter
- Adaptive contrast enhancement (ACE)
- Down dither (8-bit to 6-bit)
- Rovi (Macrovision) copy protection detection
- MIPI CSI-2 output interface (ADV7280-M)
- 8-bit ITU-R BT.656 YCrCb 4:2:2 output and HS, VS, or field synchronization (ADV7280)
- Full featured vertical blanking interval (VBI) data slicer
- Power-down mode available
- 2-wire, I²C-compatible serial interface
- Qualified for automotive applications
- –40°C to +105°C temperature grade
- 32-lead, 5 mm × 5 mm, RoHS-compliant LFCSP

APPLICATIONS

- Smartphone/multimedia handsets
- Automotive infotainment
- DVRs for video security
- Media players

GENERAL DESCRIPTION

The ADV7280/ADV7280-M are versatile one-chip, multiformat video decoders. The ADV7280/ADV7280-M automatically detect standard analog baseband video signals compatible with worldwide NTSC, PAL, and SECAM standards in the form of composite, S-Video, and component video.

The ADV7280 converts the analog video signals into a YCrCb 4:2:2 video data stream that is compatible with the 8-bit ITU-R BT.656 interface standard. The ADV7280-M converts the analog video signals into an 8-bit YCrCb 4:2:2 video data stream that is output over a mobile industry processor interface (MIPI®) CSI-2 interface.

The analog video inputs of the ADV7280/ADV7280-M accept single-ended signals. The ADV7280 provides four analog inputs; the ADV7280-M provides eight analog inputs. The ADV7280 and ADV7280-M support I2P conversion.

The ADV7280/ADV7280-M are programmed via a 2-wire, serial bidirectional port (I²C compatible) and are fabricated in a 1.8 V CMOS process. The LFCSP package option makes these decoders ideal for space-constrained portable applications.

Rev. A
Document Feedback

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2/14—Rev. 0 to Rev. A

Change to Single-Ended CVBS Input Parameter, Analog Supply Current, Table 1 ... 4

8/13—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAMS

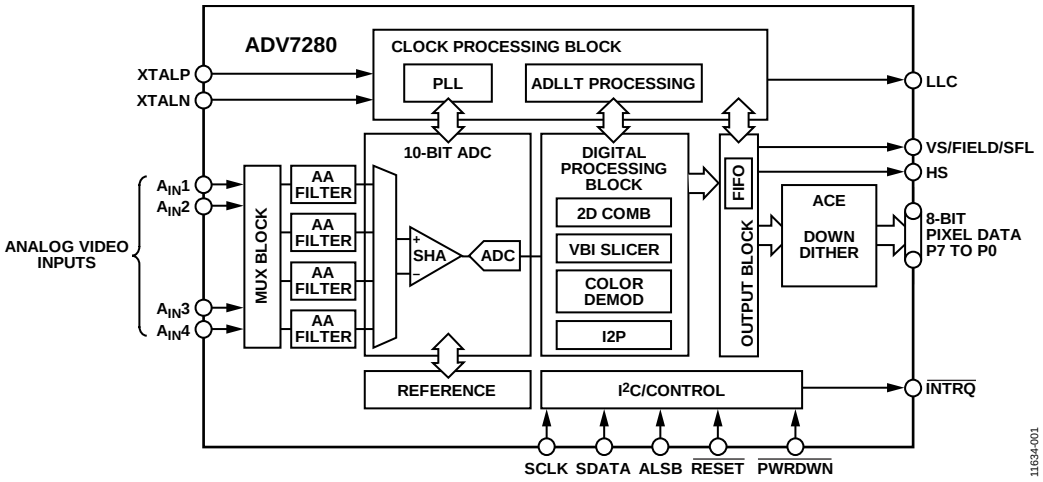

Figure 1. ADV7280 Functional Block Diagram

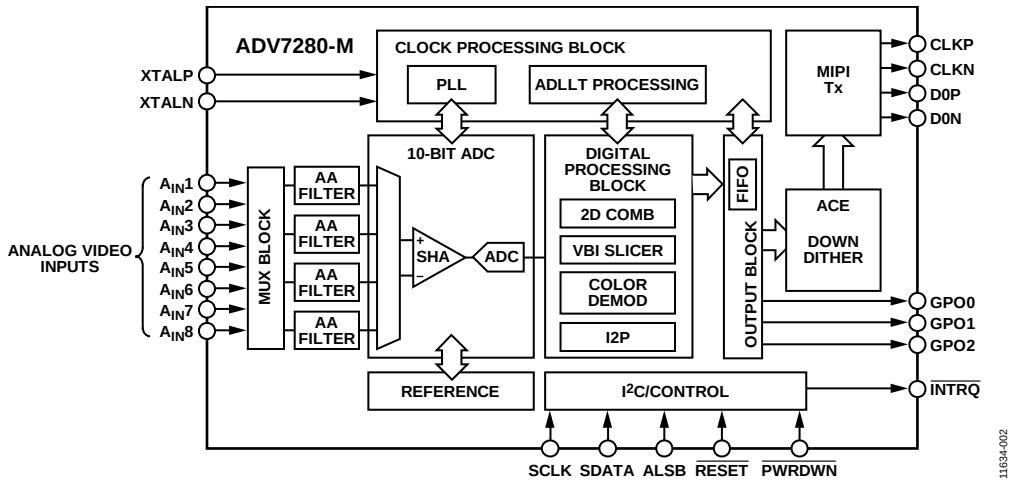

Figure 2. ADV7280-M Functional Block Diagram

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

A_{VDD}, D_{VDD}, P_{VDD}, and M_{VDD} = 1.71 V to 1.89 V, D_{VDDIO} = 2.97 V to 3.63 V, specified at operating temperature range, unless otherwise noted. M_{VDD} applies to the ADV7280-M only.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
STATIC PERFORMANCE						
ADC Resolution	N				10	Bits
Integral Nonlinearity	INL	CVBS mode		2		LSB
Differential Nonlinearity	DNL	CVBS mode		±0.6		LSB
DIGITAL INPUTS						
Input High Voltage	V_{IH}	D_{VDDIO} = 3.3 V	2			V
		D_{VDDIO} = 1.8 V, ADV7280 only	1.2			V
Input Low Voltage	V_{IL}	D_{VDDIO} = 3.3 V			0.8	V
		D_{VDDIO} = 1.8 V, ADV7280 only			0.4	V
Input Leakage Current	I_{IN}	$\overline{\text{RESET}}$ pin	−10		+10	µA
		SDATA, SCLK pins	−10		+15	µA
		$\overline{\text{PWRDWN}}$, ALSB pins	−10		+50	µA
Input Capacitance	C_{IN}				10	pF
CRYSTAL INPUT						
Input High Voltage	V_{IH}	XTALN pin	1.2			V
Input Low Voltage	V_{IL}	XTALN pin			0.4	V
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	D_{VDDIO} = 3.3 V, I_{SOURCE} = 0.4 mA	2.4			V
		D_{VDDIO} = 1.8 V, I_{SOURCE} = 0.4 mA, ADV7280 only	1.4			V
Output Low Voltage	V_{OL}	D_{VDDIO} = 3.3 V, I_{SINK} = 3.2 mA			0.4	V
		D_{VDDIO} = 1.8 V, I_{SINK} = 1.6 mA, ADV7280 only			0.2	V
High Impedance Leakage Current	I_{LEAK}				10	µA
Output Capacitance	C_{OUT}				20	pF
POWER REQUIREMENTS[1, 2, 3]						
Digital I/O Power Supply	D_{VDDIO}	ADV7280-M	2.97	3.3	3.63	V
		ADV7280	1.62	3.3	3.63	V
PLL Power Supply	P_{VDD}		1.71	1.8	1.89	V
Analog Power Supply	A_{VDD}		1.71	1.8	1.89	V
Digital Power Supply	D_{VDD}		1.71	1.8	1.89	V
MIPI Tx Power Supply	M_{VDD}	ADV7280-M only	1.71	1.8	1.89	V
Digital I/O Supply Current	I_{DVDDIO}	ADV7280-M		1.5		mA
		ADV7280		5		mA
PLL Supply Current	I_{PVDD}			12		mA
MIPI Tx Supply Current	I_{MVDD}	ADV7280-M only		14		mA
Analog Supply Current	I_{AVDD}					
Single-Ended CVBS Input				47		mA
Y/C Input				60		mA
YPrPb Input				75		mA
Digital Supply Current	I_{DVDD}					
Single-Ended CVBS Input				70		mA
Y/C Input				70		mA
YPrPb Input				70		mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER-DOWN CURRENTS[1]						
Digital I/O Supply Power-Down Current	I_{DVDDIO_PD}	D_{VDDIO} = 3.3 V, ADV7280-M		73		µA
		D_{VDDIO} = 3.3 V, ADV7280		84		µA
PLL Supply Power-Down Current	I_{PVDD_PD}			46		µA
Analog Supply Power-Down Current	I_{AVDD_PD}			0.2		µA
Digital Supply Power-Down Current	I_{DVDD_PD}			420		µA
MIPI Tx Supply Power-Down Current	I_{MVDD_PD}	ADV7280-M only		4.5		µA
Total Power Dissipation in Power-Down Mode				1		mW

[1] Guaranteed by characterization.
[2] Typical current consumption values are measured with nominal voltage supply levels and an SMPTE bar test pattern.
[3] All specifications apply when the I2P core is activated, unless otherwise stated.

VIDEO SPECIFICATIONS

A_{VDD}, D_{VDD}, P_{VDD}, and M_{VDD} = 1.71 V to 1.89 V, D_{VDDIO} = 2.97 V to 3.63 V, specified at operating temperature range, unless otherwise noted. Specifications guaranteed by characterization. M_{VDD} applies to the ADV7280-M only.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NONLINEAR SPECIFICATIONS[1]						
Differential Phase	DP	CVBS input, modulated 5-step		0.9		Degrees
Differential Gain	DG	CVBS input, modulated 5-step		0.5		%
Luma Nonlinearity	LNL	CVBS input, 5-step		2.0		%
NOISE SPECIFICATIONS						
Signal-to-Noise Ratio, Unweighted	SNR	Luma ramp		57.1		dB
		Luma flat field		58		dB
Analog Front-End Crosstalk				60		dB
Common-Mode Rejection Ratio[2]	CMRR			73		dB
LOCK TIME SPECIFICATIONS						
Horizontal Lock Range			–5		+5	%
Vertical Lock Range			40		70	Hz
f_{SC} Subcarrier Lock Range				±1.3		kHz
Color Lock-In Time				60		Lines
Synchronization Depth Range			20		200	%
Color Burst Range			5		200	%
Vertical Lock Time				2		Fields
Autodetection Switch Speed[3]				100		Lines
Fast Switch Speed[4]				100		ms
LUMA SPECIFICATIONS		CVBS, 1 V input				
Luma Brightness Accuracy				1		%
Luma Contrast Accuracy				1		%

[1] These specifications apply for all CVBS input types (NTSC, PAL, and SECAM).
[2] The CMRR of this circuit design is critically dependent on the external resistor matching on the circuit inputs (see the Input Network section). The CMRR measurement was performed with 0.1% tolerant resistors, a common-mode voltage of 1 V, and a common-mode frequency of 10 kHz.
[3] Autodetection switch speed is the time required for the ADV7280/ADV7280-M to detect which video format is present at its input, for example, PAL I or NTSC M.
[4] Fast switch speed is the time required for the ADV7280/ADV7280-M to switch from one analog input to another, for example, switching from $A_{IN}1$ to $A_{IN}2$.

ANALOG SPECIFICATIONS

A_{VDD}, D_{VDD}, P_{VDD}, and M_{VDD} = 1.71 V to 1.89 V, D_{VDDIO} = 2.97 V to 3.63 V, specified at operating temperature range, unless otherwise noted. Specifications guaranteed by characterization. M_{VDD} applies to the ADV7280-M only.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLAMP CIRCUITRY					
External Clamp Capacitor			0.1		µF
Input Impedance	Clamps switched off		10		MΩ
Large Clamp Source Current			0.4		mA
Large Clamp Sink Current			0.4		mA
Fine Clamp Source Current			10		µA
Fine Clamp Sink Current			10		µA

MIPI VIDEO OUTPUT SPECIFICATIONS (ADV7280-M ONLY)

A_{VDD}, D_{VDD}, P_{VDD}, and M_{VDD} = 1.71 V to 1.89 V, D_{VDDIO} = 2.97 V to 3.63 V, specified at operating temperature range, unless otherwise noted. The CSI-2 clock lane of the ADV7280-M remains in high speed (HS) mode even when the data lane enters low power (LP) mode. For this reason, some measurements on the clock lane that pertain to low power mode are not applicable. Unless otherwise stated, all high speed measurements were performed with the ADV7280-M operating in progressive mode and with a nominal 432 Mbps output data rate. Specifications guaranteed by characterization.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
UNIT INTERVAL	UI					
Interlaced Output				4.63		ns
Progressive Output				2.31		ns
DATA LANE LP TX DC SPECIFICATIONS[1]						
Thevenin Output High Level	V_{OH}		1.1	1.2	1.3	V
Thevenin Output Low Level	V_{OL}		−50	0	+50	mV
DATA LANE LP TX AC SPECIFICATIONS[1]						
Rise Time, 15% to 85%					25	ns
Fall Time, 85% to 15%					25	ns
Rise Time, 30% to 85%					35	ns
Data Lane LP Slew Rate vs. C_{LOAD}						
Maximum Slew Rate over Entire Vertical Edge Region		Rising edge			150	mV/ns
		Falling edge			150	mV/ns
Minimum Slew Rate						
400 mV ≤ V_{OUT} ≤ 930 mV		Falling edge	30			mV/ns
400 mV ≤ V_{OUT} ≤ 700 mV		Rising edge	30			mV/ns
700 mV ≤ V_{OUT} ≤ 930 mV		Rising edge	>0			mV/ns
Pulse Width of LP Exclusive-OR Clock		First clock pulse after stop state or last pulse before stop state	40			ns
		All other clock pulses	20			ns
Period of LP Exclusive-OR Clock			90			ns
CLOCK LANE LP TX DC SPECIFICATIONS[1]						
Thevenin Output High Level	V_{OH}		1.1	1.2	1.3	V
Thevenin Output Low Level	V_{OL}		−50	0	+50	mV
CLOCK LANE LP TX AC SPECIFICATIONS[1]						
Rise Time, 15% to 85%					25	ns
Fall Time, 85% to 15%					25	ns

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Clock Lane LP Slew Rate						
Maximum Slew Rate over Entire Vertical Edge Region		Rising edge			150	mV/ns
		Falling edge			150	mV/ns
Minimum Slew Rate						
400 mV ≤ V_{OUT} ≤ 930 mV		Falling edge	30			mV/ns
400 mV ≤ V_{OUT} ≤ 700 mV		Rising edge	30			mV/ns
700 mV ≤ V_{OUT} ≤ 930 mV		Rising edge	>0			mV/ns
DATA LANE HS TX SIGNALING REQUIREMENTS		See Figure 3				
Low Power to High Speed Transition Stage	t_9	Time that the D0P pin is at V_{OL} and the D0N pin is at V_{OH}	50			ns
	t_{10}	Time that the D0P and D0N pins are at V_{OL}	40 + (4 × UI)		85 + (6 × UI)	ns
	t_{11}	t_{10} plus the HS-zero period	145 + (10 × UI)			ns
High Speed Differential Voltage Swing	$\|V_1\|$		140	200	270	mV p-p
Differential Voltage Mismatch					10	mV
Single-Ended Output High Voltages					360	mV
Static Common-Mode Voltage Level			150	200	250	mV
Static Common-Mode Voltage Mismatch					5	mV
Dynamic Common Level Variations						
50 MHz to 450 MHz					25	mV
Above 450 MHz					15	mV
Rise Time, 20% to 80%			0.15		0.3 × UI	ns
Fall Time, 80% to 20%			0.15		0.3 × UI	ns
High Speed to Low Power Transition Stage	t_{12}	Time that the ADV7280-M drives the flipped last data bit after sending the last payload data bit of an HS transmission burst	60 + (4 × UI)			ns
	t_{13}	Post-end-of-transmission rise time (30% to 85%)			35	ns
	t_{14}	Time from start of t_{12} to start of low power state following an HS transmission burst			105 + (12 × UI)	ns
	t_{15}	Time that a low power state is transmitted after an HS transmission burst			100	ns
CLOCK LANE HS TX SIGNALING REQUIREMENTS		See Figure 3				
Low Power to High Speed Transition Stage[2]	t_9	Time that the CLKP pin is at V_{OL} and the CLKN pin is at V_{OH}	50			ns
		Time that the CLKP and CLKN pins are at V_{OL}	38		95	ns
		Clock HS-zero period	300	500		ns
High Speed Differential Voltage Swing	$\|V_2\|$		140	200	270	mV p-p
Differential Voltage Mismatch					10	mV
Single-Ended Output High Voltages					360	mV
Static Common-Mode Voltage Level			150	200	250	mV
Static Common-Mode Voltage Mismatch					5	mV
Dynamic Common Level Variations						
50 MHz to 450 MHz					25	mV
Above 450 MHz					15	mV
Rise Time, 20% to 80%			0.15		0.3 × UI	ns
Fall Time, 80% to 20%			0.15		0.3 × UI	ns

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
HS TX CLOCK TO DATA LANE TIMING REQUIREMENTS						
Data to Clock Skew			0.35 × UI		0.65 × UI	ns

[1] These measurements were performed with C_{LOAD} = 50 pF.
[2] The clock lane remains in high speed mode throughout normal operation. These results apply only to the ADV7280-M during startup.

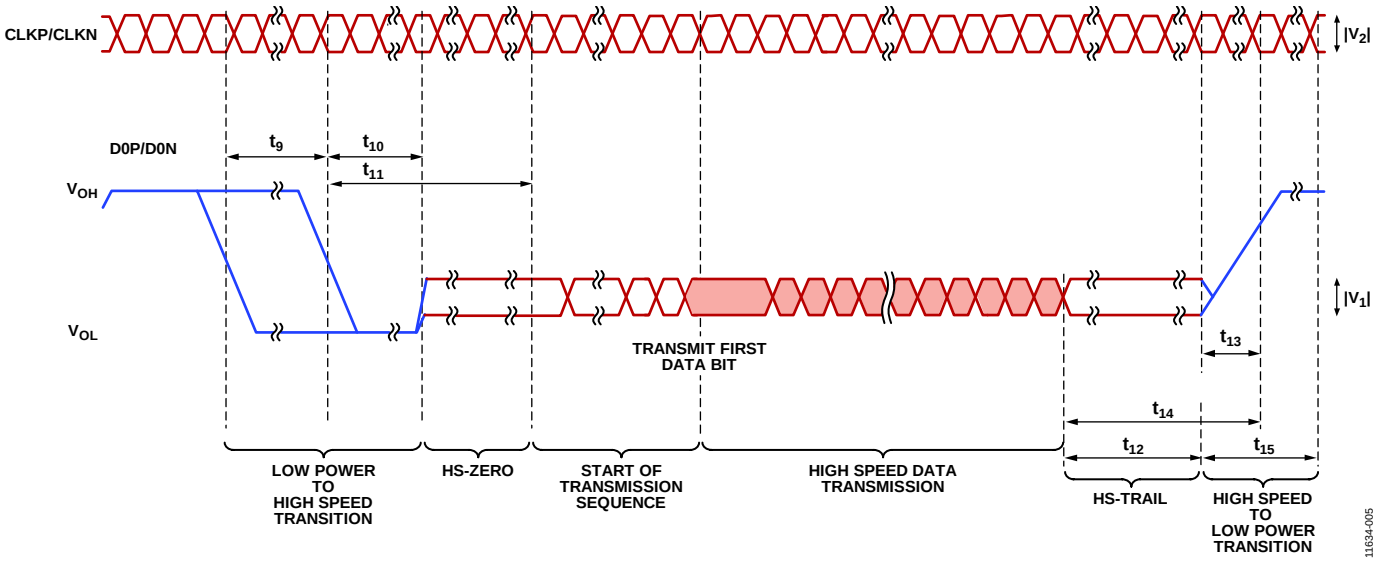

Figure 3. ADV7280-M Output Timing Diagram (Conforms with MIPI CSI-2 Specification)

PIXEL PORT TIMING SPECIFICATIONS (ADV7280 ONLY)

A_{VDD}, D_{VDD}, and P_{VDD} = 1.71 V to 1.89 V, D_{VDDIO} = 1.62 V to 3.63 V, specified at operating temperature range, unless otherwise noted. Specifications guaranteed by characterization.

Table 5.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CLOCK OUTPUTS						
LLC Mark Space Ratio	t_9:t_{10}		45:55		55:45	% duty cycle
DATA AND CONTROL OUTPUTS						
Data Output Transitional Time	t_{11}	Negative clock edge to start of valid data ($t_{SETUP} = t_{10} - t_{11}$)			3.8	ns
	t_{12}	End of valid data to negative clock edge ($t_{HOLD} = t_9 - t_{12}$)			6.9	ns

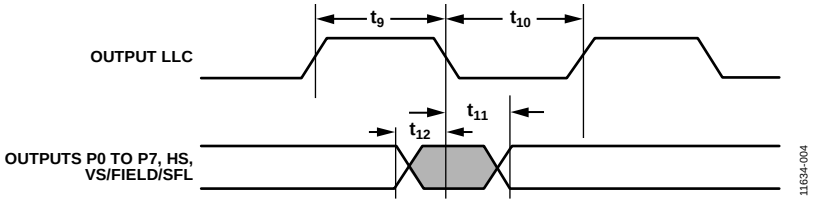

Figure 4. ADV7280 Pixel Port and Control Output Timing Diagram

CLOCK AND I²C TIMING SPECIFICATIONS

A_{VDD}, D_{VDD}, P_{VDD}, and M_{VDD} = 1.71 V to 1.89 V, D_{VDDIO} = 2.97 V to 3.63 V, specified at operating temperature range, unless otherwise noted. Specifications guaranteed by characterization. M_{VDD} applies to the ADV7280-M only.

Table 6.

Parameter	Symbol	Min	Typ	Max	Unit
SYSTEM CLOCK AND CRYSTAL					
Nominal Frequency			28.63636		MHz
Frequency Stability				±50	ppm
I²C PORT					
SCLK Frequency				400	kHz
SCLK Minimum Pulse Width High	t_1	0.6			µs
SCLK Minimum Pulse Width Low	t_2	1.3			µs
Hold Time (Start Condition)	t_3	0.6			µs
Setup Time (Start Condition)	t_4	0.6			µs
SDATA Setup Time	t_5	100			ns
SCLK and SDATA Rise Times	t_6			300	ns
SCLK and SDATA Fall Times	t_7			300	ns
Setup Time (Stop Condition)	t_8		0.6		µs
$\overline{\text{RESET}}$ INPUT					
$\overline{\text{RESET}}$ Pulse Width		5			ms

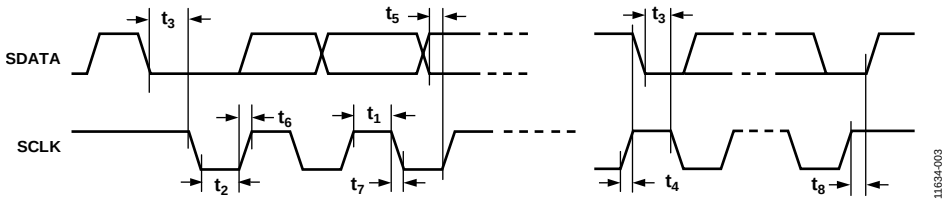

Figure 5. I²C Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
A_{VDD} to DGND	2.2 V
D_{VDD} to DGND	2.2 V
P_{VDD} to DGND	2.2 V
M_{VDD} to DGND[1]	2.2 V
D_{VDDIO} to DGND	4 V
P_{VDD} to D_{VDD}	−0.9 V to +0.9 V
M_{VDD} to D_{VDD}[1]	−0.9 V to +0.9 V
A_{VDD} to D_{VDD}	−0.9 V to +0.9 V
Digital Inputs Voltage	DGND − 0.3 V to D_{VDDIO} + 0.3 V
Digital Outputs Voltage	DGND − 0.3 V to D_{VDDIO} + 0.3 V
Analog Inputs to Ground	Ground − 0.3 V to A_{VDD} + 0.3 V
Maximum Junction Temperature (T_J max)	140°C
Storage Temperature Range	−65°C to +150°C
Infrared Reflow Soldering (20 sec)	260°C

[1] M_{VDD} applies to the ADV7280-M only.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

These devices are high performance integrated circuits with an ESD rating of <2 kV, and they are ESD sensitive. Proper precautions must be taken for handling and assembly.

THERMAL RESISTANCE

The thermal resistance values in Table 8 are specified for the device soldered onto a 4-layer printed circuit board (PCB) with a common ground plane and with the exposed pad of the device connected to DGND. The values in Table 8 are maximum values.

Table 8. Thermal Resistance for the 32-Lead LFCSP

Thermal Characteristic	Symbol	Value	Unit
Junction-to-Ambient Thermal Resistance (Still Air)	θ_{JA}	32.5	°C/W
Junction-to-Case Thermal Resistance	θ_{JC}	2.3	°C/W

REFLOW SOLDER

The ADV7280/ADV7280-M are Pb-free, environmentally friendly products. They are manufactured using the most up-to-date materials and processes. The coating on the leads of each device is 100% pure Sn electroplate. The devices are suitable for Pb-free applications and can withstand surface-mount soldering at up to 255°C (±5°C).

In addition, the ADV7280/ADV7280-M are backward-compatible with conventional SnPb soldering processes. This means that the electroplated Sn coating can be soldered with Sn/Pb solder pastes at conventional reflow temperatures of 220°C to 235°C.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

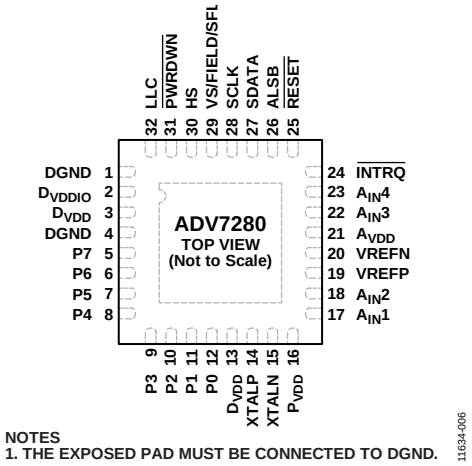

Figure 6. Pin Configuration, ADV7280

Table 9. Pin Function Descriptions, ADV7280

Pin No.	Mnemonic	Type	Description
1, 4	DGND	Ground	Ground for Digital Supply.
2	D_{VDDIO}	Power	Digital I/O Power Supply (1.8 V or 3.3 V).
3, 13	D_{VDD}	Power	Digital Power Supply (1.8 V).
5 to 12	P7 to P0	Output	Video Pixel Output Ports.
14	XTALP	Output	Connect this pin to the external 28.63636 MHz crystal, or leave it unconnected if an external 1.8 V, 28.63636 MHz clock oscillator source is used to clock the ADV7280. The crystal used with the ADV7280 must be a fundamental crystal.
15	XTALN	Input	Input Pin for the External 28.63636 MHz Crystal. The crystal used with the ADV7280 must be a fundamental crystal. If an external 1.8 V, 28.63636 MHz clock oscillator source is used to clock the ADV7280, the output of the oscillator is fed into the XTALN pin.
16	P_{VDD}	Power	PLL Power Supply (1.8 V).
17, 18, 22, 23	$A_{IN}1$ to $A_{IN}4$	Input	Analog Video Input Channels.
19	VREFP	Output	Internal Voltage Reference Output.
20	VREFN	Output	Internal Voltage Reference Output.
21	A_{VDD}	Power	Analog Power Supply (1.8 V).
24	$\overline{\text{INTRQ}}$	Output	Interrupt Request Output. An interrupt occurs when certain signals are detected on the input video.
25	$\overline{\text{RESET}}$	Input	System Reset Input (Active Low). A minimum low reset pulse width of 5 ms is required to reset the ADV7280 circuitry.
26	ALSB	Input	This pin selects the I^2C write address for the ADV7280. When ALSB is set to Logic 0, the write address is 0x40; when ALSB is set to Logic 1, the write address is 0x42.
27	SDATA	Input/output	I^2C Port Serial Data Input/Output.
28	SCLK	Input	I^2C Port Serial Clock Input. The maximum clock rate is 400 kHz.
29	VS/FIELD/SFL	Output	Vertical Synchronization Output Signal/Field Synchronization Output Signal/Subcarrier Frequency Lock. When configured for the SFL function, this pin provides a serial output stream that can be used to lock the subcarrier frequency when the ADV7280 decoder is connected to any Analog Devices, Inc., digital video encoder.
30	HS	Output	Horizontal Synchronization Output Signal.
31	$\overline{\text{PWRDWN}}$	Input	Power-Down Pin. A logic low on this pin places the ADV7280 in power-down mode.
32	LLC	Output	Line-Locked Output Clock for Output Pixel Data. The clock output is nominally 27 MHz, but it increases or decreases according to the video line length.
	EPAD (EP)		Exposed Pad. The exposed pad must be connected to DGND.

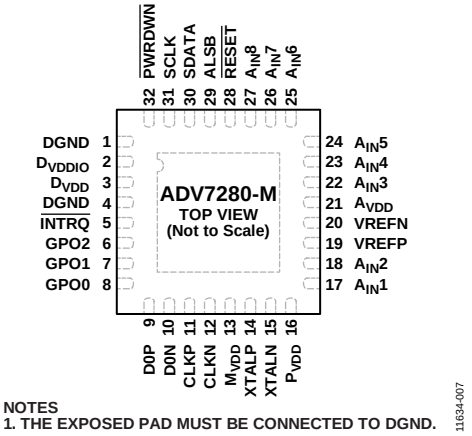

Figure 7. Pin Configuration, ADV7280-M

Table 10. Pin Function Descriptions, ADV7280-M

Pin No.	Mnemonic	Type	Description
1, 4	DGND	Ground	Ground for Digital Supply.
2	D_{VDDIO}	Power	Digital I/O Power Supply (3.3 V).
3	D_{VDD}	Power	Digital Power Supply (1.8 V).
5	$\overline{INTRQ}$	Output	Interrupt Request Output. An interrupt occurs when certain signals are detected on the input video.
6 to 8	GPO2 to GPO0	Output	General-Purpose Outputs. These pins can be configured via I^2C to allow control of external devices.
9	D0P	Output	Positive MIPI Differential Data Output.
10	D0N	Output	Negative MIPI Differential Data Output.
11	CLKP	Output	Positive MIPI Differential Clock Output.
12	CLKN	Output	Negative MIPI Differential Clock Output.
13	M_{VDD}	Power	MIPI Digital Power Supply (1.8 V).
14	XTALP	Output	Connect this pin to the external 28.63636 MHz crystal, or leave it unconnected if an external 1.8 V, 28.63636 MHz clock oscillator source is used to clock the ADV7280-M. The crystal used with the ADV7280-M must be a fundamental crystal.
15	XTALN	Input	Input Pin for the External 28.63636 MHz Crystal. The crystal used with the ADV7280-M must be a fundamental crystal. If an external 1.8 V, 28.63636 MHz clock oscillator source is used to clock the ADV7280-M, the output of the oscillator is fed into the XTALN pin.
16	P_{VDD}	Power	PLL Power Supply (1.8 V).
17, 18, 22, 23, 24, 25, 26, 27	$A_{IN}1$ to $A_{IN}8$	Input	Analog Video Input Channels.
19	VREFP	Output	Internal Voltage Reference Output.
20	VREFN	Output	Internal Voltage Reference Output.
21	A_{VDD}	Power	Analog Power Supply (1.8 V).
28	$\overline{RESET}$	Input	System Reset Input (Active Low). A minimum low reset pulse width of 5 ms is required to reset the ADV7280-M circuitry.
29	ALSB	Input	This pin selects the I^2C write address for the ADV7280-M. When ALSB is set to Logic 0, the write address is 0x40; when ALSB is set to Logic 1, the write address is 0x42.
30	SDATA	Input/output	I^2C Port Serial Data Input/Output.
31	SCLK	Input	I^2C Port Serial Clock Input. The maximum clock rate is 400 kHz.
32	$\overline{PWRDWN}$	Input	Power-Down Pin. A logic low on this pin places the ADV7280-M in power-down mode.
	EPAD (EP)		Exposed Pad. The exposed pad must be connected to DGND.

THEORY OF OPERATION

The ADV7280/ADV7280-M are versatile one-chip, multiformat video decoders. The ADV7280/ADV7280-M automatically detect standard analog baseband video signals compatible with worldwide NTSC, PAL, and SECAM standards in the form of composite, S-Video, and component video.

The ADV7280 converts the analog video signals into an 8-bit YCrCb 4:2:2 component video data stream that is compatible with the ITU-R BT.656 interface standard.

The ADV7280-M converts the analog video signals into an 8-bit YCrCb 4:2:2 video data stream that is output over a MIPI CSI-2 interface. The MIPI CSI-2 output interface connects to a wide range of video processors and FPGAs.

The ADV7280/ADV7280-M accept composite video signals, as well as S-Video and YPbPr video signals, supporting a wide range of consumer and automotive video sources. The accurate 10-bit analog-to-digital conversion provides professional quality video performance for consumer applications with true 8-bit data resolution.

The advanced interlaced-to-progressive (I2P) function allows the ADV7280/ADV7280-M to convert an interlaced video input into a progressive video output. This function is performed without the need for external memory. The ADV7280/ADV7280-M use edge adaptive technology to minimize video defects on low angle lines.

The automatic gain control (AGC) and clamp restore circuitry allows an input video signal peak-to-peak range of 0 V to 1.0 V at the analog video input pins of the ADV7280/ADV7280-M. Alternatively, the AGC and clamp restore circuitry can be bypassed for manual settings.

The ADV7280/ADV7280-M support a number of other functions, including 8-bit to 6-bit down dither mode and adaptive contrast enhancement (ACE).

The ADV7280/ADV7280-M are programmed via a 2-wire, serial bidirectional port (I^2C compatible) and are fabricated in a 1.8 V CMOS process. The monolithic CMOS construction of the ADV7280/ADV7280-M ensures greater functionality with lower power dissipation. The LFCSP package option makes these decoders ideal for space-constrained portable applications.

ANALOG FRONT END (AFE)

The analog front end (AFE) of the ADV7280/ADV7280-M comprises a single high speed, 10-bit ADC that digitizes the analog video signal before applying it to the standard definition processor (SDP).

The AFE also includes an input mux that enables multiple video signals to be applied to the ADV7280/ADV7280-M. The input mux allows up to four composite video signals to be applied to the ADV7280 and up to eight composite video signals to be applied to the ADV7280-M.

Current clamps are positioned in front of the ADC to ensure that the video signal remains within the range of the converter.

A resistor divider network is required before each analog input channel to ensure that the input signal is kept within the range of the ADC (see the Input Network section). Fine clamping of the video signal is performed downstream by digital fine clamping within the ADV7280/ADV7280-M.

Table 11 lists the three ADC clock rates that are determined by the video input format to be processed. These clock rates ensure 4× oversampling per channel for CVBS, Y/C, and YPrPb modes.

Table 11. ADC Clock Rates

Input Format	ADC Clock Rate (MHz)[1]	Oversampling Rate per Channel
CVBS	57.27	4×
Y/C (S-Video)	114	4×
YPrPb	172	4×

[1] Based on a 28.63636 MHz crystal between the XTALP and XTALN pins.

STANDARD DEFINITION PROCESSOR (SDP)

The ADV7280/ADV7280-M are capable of decoding a large selection of baseband video signals in composite, S-Video, and component formats. The video standards supported by the video processor include

- PAL B, PAL D, PAL G, PAL H, PAL I, PAL M, PAL N, PAL Nc, PAL 60
- NTSC J, NTSC M, NTSC 4.43
- SECAM B, SECAM D, SECAM G, SECAM K, SECAM L

Using the standard definition processor (SDP), the ADV7280/ADV7280-M can automatically detect the video standard and process it accordingly.

The ADV7280/ADV7280-M have a five-line adaptive 2D comb filter that provides superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to the video standard and signal quality without user intervention. Video user controls such as brightness, contrast, saturation, and hue are also available with the ADV7280/ADV7280-M.

The ADV7280/ADV7280-M implement the patented Adaptive Digital Line Length Tracking (ADLLT™) algorithm to track varying video line lengths from sources such as VCRs. ADLLT enables the ADV7280/ADV7280-M to track and decode poor quality video sources such as VCRs and noisy sources from tuner outputs and camcorders. The ADV7280/ADV7280-M contain a chroma transient improvement (CTI) processor that sharpens the edge rate of chroma transitions, resulting in sharper vertical transitions.

Adaptive contrast enhancement (ACE) offers improved visual detail using an algorithm that automatically varies contrast levels to enhance picture detail. ACE increases the contrast in dark areas of an image without saturating the bright areas of the image. This feature is particularly useful in automotive applications, where it can be important to discern objects in shaded areas.

Down dithering converts the output of the ADV7280/ADV7280-M from an 8-bit to a 6-bit output, enabling ease of design for standard LCD panels.

The I2P block converts the interlaced video input into a progressive video output without the need for external memory.

The SDP can process a variety of VBI data services, such as closed captioning (CCAP), wide screen signaling (WSS), and copy generation management system (CGMS). VBI data is transmitted as ancillary data packets.

The ADV7280/ADV7280-M are fully Rovi® (Macrovision®) compliant; detection circuitry enables Type I, Type II, and Type III protection levels to be identified and reported to the user. The decoders are also fully robust to all Macrovision signal inputs.

POWER SUPPLY SEQUENCING

OPTIMAL POWER-UP SEQUENCE

The optimal power-up sequence for the ADV7280/ADV7280-M is to first power up the 3.3 V D_{VDDIO} supply, followed by the 1.8 V supplies: D_{VDD}, P_{VDD}, A_{VDD}, and M_{VDD} (for the ADV7280-M).

When powering up the ADV7280/ADV7280-M, follow these steps. During power-up, all supplies must adhere to the specifications listed in the Absolute Maximum Ratings section.

1. Assert the $\overline{\text{PWRDWN}}$ and $\overline{\text{RESET}}$ pins (pull the pins low).
2. Power up the D_{VDDIO} supply.
3. After D_{VDDIO} is fully asserted, power up the 1.8 V supplies.
4. After the 1.8 V supplies are fully asserted, pull the $\overline{\text{PWRDWN}}$ pin high.
5. Wait 5 ms and then pull the $\overline{\text{RESET}}$ pin high.
6. After all power supplies and the $\overline{\text{PWRDWN}}$ and $\overline{\text{RESET}}$ pins are powered up and stable, wait an additional 5 ms before initiating I^2C communication with the ADV7280/ADV7280-M.

SIMPLIFIED POWER-UP SEQUENCE

Alternatively, the ADV7280/ADV7280-M can be powered up by asserting all supplies and the $\overline{\text{PWRDWN}}$ and $\overline{\text{RESET}}$ pins simultaneously. After this operation, perform a software reset, then wait 10 ms before initiating I^2C communication with the ADV7280/ADV7280-M.

While the supplies are being established, care must be taken to ensure that a lower rated supply does not go above a higher rated supply level. During power-up, all supplies must adhere to the specifications listed in the Absolute Maximum Ratings section.

POWER-DOWN SEQUENCE

The ADV7280/ADV7280-M supplies can be deasserted simultaneously as long as D_{VDDIO} does not go below a lower rated supply.

UNIVERSAL POWER SUPPLY (ADV7280 ONLY)

The ADV7280-M model requires a D_{VDDIO} supply at a nominal value of 3.3 V. The ADV7280 model, however, can operate with a D_{VDDIO} supply at a nominal value of 1.8 V. Therefore, it is possible to power up all the supplies for the ADV7280 (D_{VDD}, P_{VDD}, A_{VDD}, and D_{VDDIO}) to 1.8 V.

When D_{VDDIO} is at a nominal value of 1.8 V, power up the ADV7280 as follows:

1. Follow the power-up sequence described in the Optimal Power-Up Sequence section, but power up the D_{VDDIO} supply to 1.8 V instead of 3.3 V. Also, power up the $\overline{\text{PWRDWN}}$ and $\overline{\text{RESET}}$ pins to 1.8 V instead of 3.3 V.
2. Set the drive strengths of the digital outputs of the ADV7280 to their maximum setting.
3. Connect any pull-up resistors connected to pins on the ADV7280 (such as the SCLK and SDATA pins) to 1.8 V instead of 3.3 V.

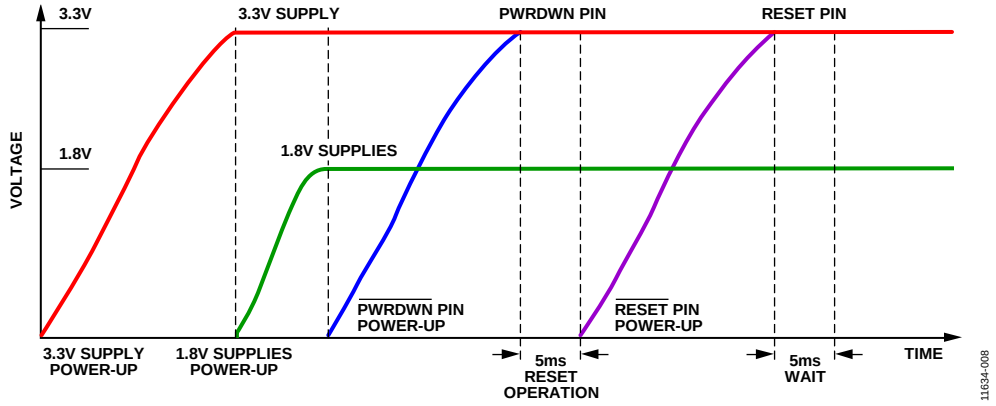

Figure 8. Optimal Power-Up Sequence

INPUT NETWORK

An input network (external resistor and capacitor circuit) is required on the $A_{IN}x$ input pins of the decoder. Figure 9 shows the input network to use on each $A_{IN}x$ input pin of the ADV7280/ADV7280-M when any of the following video input formats is used:

- Single-ended CVBS
- YC (S-Video)
- YPrPb

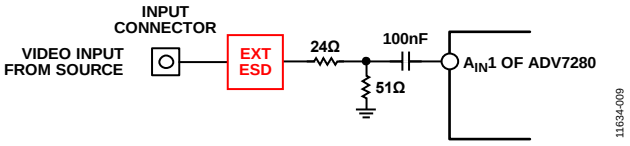

Figure 9. Input Network

The 24 Ω and 51 Ω resistors supply the 75 Ω end termination required for the analog video input. These resistors also create a resistor divider with a gain of 0.68. The resistor divider attenuates the amplitude of the input analog video and scales the input to the ADC range of the ADV7280/ADV7280-M. This allows an input range to the ADV7280/ADV7280-M of up to 1.47 V p-to-p. Note that amplifiers within the ADC restore the amplitude of the input signal so that signal-to-noise ratio (SNR) performance is maintained.

The 100 nF ac coupling capacitor removes the dc bias of the analog input video before it is fed into the $A_{IN}x$ pin of the ADV7280/ADV7280-M. The clamping circuitry within the ADV7280/ADV7280-M restores the dc bias of the input signal to the optimal level before it is fed into the ADC of the ADV7280/ADV7280-M.

INPUT CONFIGURATION

The input format of the ADV7280/ADV7280-M is specified using the INSEL[4:0] bits (see Table 12). These bits also configure the SDP core to process CVBS, Y/C (S-Video), or component (YPrPb) format. The INSEL[4:0] bits are located in the user sub map of the register space at Address 0x00[4:0]. For more information about the registers, see the Register Maps section.

The INSEL[4:0] bits specify predefined analog input routing schemes, eliminating the need for manual mux programming and allowing the user to route the various video signal types to the decoder. For example, if the CVBS input is selected, the remaining channels are powered down.

Table 12. Input Format Specified by the INSEL[4:0] Bits

		Analog Inputs	
INSEL[4:0] Bit Value	**Video Format**	**ADV7280**	**ADV7280-M**
00000	CVBS	CVBS input on $A_{IN}1$	CVBS input on $A_{IN}1$
00001	CVBS	CVBS input on $A_{IN}2$	CVBS input on $A_{IN}2$
00010	CVBS	CVBS input on $A_{IN}3$	CVBS input on $A_{IN}3$
00011	CVBS	CVBS input on $A_{IN}4$	CVBS input on $A_{IN}4$
00100	CVBS	Reserved	CVBS input on $A_{IN}5$
00101	CVBS	Reserved	CVBS input on $A_{IN}6$
00110	CVBS	Reserved	CVBS input on $A_{IN}7$
00111	CVBS	Reserved	CVBS input on $A_{IN}8$
01000	Y/C (S-Video)	Y input on $A_{IN}1$; C input on $A_{IN}2$	Y input on $A_{IN}1$; C input on $A_{IN}2$
01001	Y/C (S-Video)	Y input on $A_{IN}3$; C input on $A_{IN}4$	Y input on $A_{IN}3$; C input on $A_{IN}4$
01010	Y/C (S-Video)	Reserved	Y input on $A_{IN}5$; C input on $A_{IN}6$
01011	Y/C (S-Video)	Reserved	Y input on $A_{IN}7$; C input on $A_{IN}8$
01100	YPrPb	Y input on $A_{IN}1$; Pb input on $A_{IN}2$; Pr input on $A_{IN}3$	Y input on $A_{IN}1$; Pb input on $A_{IN}2$; Pr input on $A_{IN}3$
01101	YPrPb	Reserved	Y input on $A_{IN}4$; Pb input on $A_{IN}5$; Pr input on $A_{IN}6$
01110 to 11111	Reserved	Reserved	Reserved

ADAPTIVE CONTRAST ENHANCEMENT (ACE)

The ADV7280/ADV7280-M can increase the contrast of an image depending on the content of the picture, allowing bright areas to be made brighter and dark areas to be made darker. The optional ACE feature enables the contrast within dark areas to be increased without significantly affecting the bright areas. The ACE feature is particularly useful in automotive applications, where it can be important to discern objects in shaded areas.

The ACE function is disabled by default. To enable the ACE function, execute the register writes shown in Table 13. To disable the ACE function, execute the register writes shown in Table 14.

Table 13. Register Writes to Enable the ACE Function

Register Map	Register Address	Register Write	Description
User Sub Map (0x40 or 0x42)	0x0E	0x40	Enter User Sub Map 2
User Sub Map 2 (0x40 or 0x42)	0x80	0x80	Enable ACE
User Sub Map 2 (0x40 or 0x42)	0x0E	0x00	Reenter user sub map

Table 14. Register Writes to Disable the ACE Function

Register Map	Register Address	Register Write	Description
User Sub Map (0x40 or 0x42)	0x0E	0x40	Enter User Sub Map 2
User Sub Map 2 (0x40 or 0x42)	0x80	0x00	Disable ACE
User Sub Map 2 (0x40 or 0x42)	0x0E	0x00	Reenter user sub map

I2P FUNCTION

The advanced interlaced-to-progressive (I2P) function allows the ADV7280/ADV7280-M to convert an interlaced video input into a progressive video output. This function is performed without the need for external memory. The ADV7280/ADV7280-M use edge adaptive technology to minimize video defects on low angle lines.

The I2P function is disabled by default. To enable the I2P function, use the recommended scripts from Analog Devices.

MIPI CSI-2 OUTPUT (ADV7280-M ONLY)

The decoder in the ADV7280-M outputs an ITU-R BT.656 data stream. The ITU-R BT.656 data stream is connected into a CSI-2 Tx module. Data from the CSI-2 Tx module is fed into a D-PHY physical layer and output serially from the device.

The output of the ADV7280-M consists of a single data channel on the D0P and D0N lanes and a clock channel on the CLKP and CLKN lanes.

Video data is output over the data lanes in high speed mode. The data lanes enter low power mode during the horizontal and vertical blanking periods.

The clock lanes are used to clock the output video. After the ADV7280-M is programmed, the clock lanes exit low power mode and remain in high speed mode until the part is reset or powered down.

The ADV7280-M outputs video data in an 8-bit YCrCb 4:2:2 format. When the I2P core is disabled, the video data is output in an interlaced format at a nominal data rate of 216 Mbps. When the I2P core is enabled, the video data is output in a progressive format at a nominal data rate of 432 Mbps (see the I2P Function section for more information).

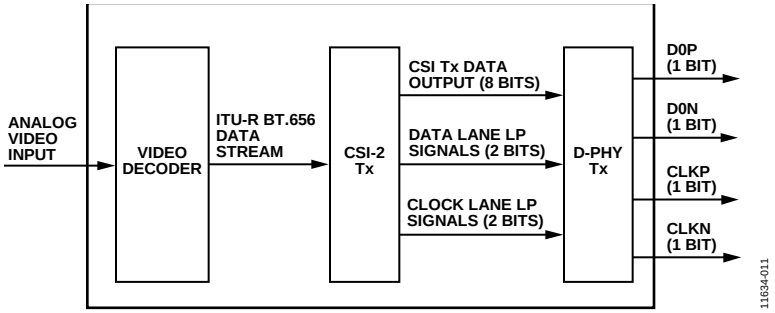

Figure 10. MIPI CSI-2 Output Stage of the ADV7280-M

ITU-R BT.656 Tx CONFIGURATION (ADV7280 ONLY)

The ADV7280 receives analog video and outputs digital video according to the ITU-R BT.656 specification. The ADV7280 outputs the ITU-R BT.656 video data stream over the P0 to P7 data pins and has a line-locked clock (LLC) pin and two synchronization pins (HS and VS/FIELD/SFL).

Video data is output over the P0 to P7 pins in YCrCb 4:2:2 format. Synchronization signals are automatically embedded in the video data signal in accordance with the ITU-R BT.656 specification.

The LLC output is used to clock the output data on the P0 to P7 pins at a nominal frequency of 27 MHz.

The two synchronization pins (HS and VS/FIELD/SFL) output a variety of synchronization signals such as horizontal sync, vertical sync, field sync, and color subcarrier frequency lock (SFL) sync. The majority of these synchronization signals are already embedded in the video data. Therefore, the use of the synchronization pins is optional.

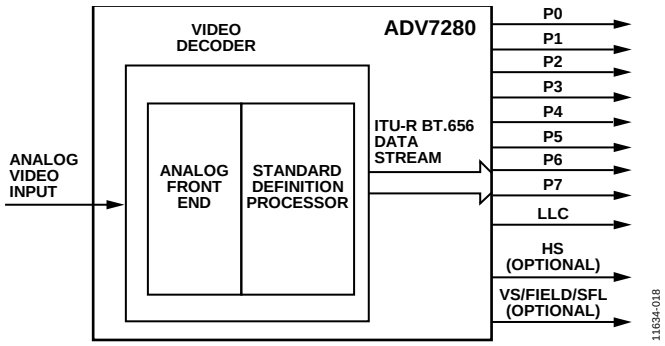

Figure 11. ITU-R BT.656 Output Stage of the ADV7280

I²C PORT DESCRIPTION

The ADV7280/ADV7280-M support a 2-wire, I²C-compatible serial interface. Two inputs, serial data (SDATA) and serial clock (SCLK), carry information between the ADV7280/ADV7280-M and the system I²C master controller. The I²C port of the ADV7280/ADV7280-M allows the user to set up and configure the decoder and to read back captured VBI data.

The ADV7280/ADV7280-M have a number of possible I²C slave addresses and subaddresses (see the Register Maps section). The main map of the ADV7280/ADV7280-M has four possible slave addresses for read and write operations, depending on the logic level of the ALSB pin (see Table 15).

Table 15. Main Map I²C Address for the ADV7280/ADV7280-M

ALSB Pin	R/$\overline{W}$ Bit	Slave Address
0	0	0x40 (write)
0	1	0x41 (read)
1	0	0x42 (write)
1	1	0x43 (read)

The ALSB pin controls Bit 1 of the slave address. By changing the logic level of the ALSB pin, it is possible to control two ADV7280/ADV7280-M devices in an application without using the same I²C slave address. The LSB (Bit 0) specifies either a read or write operation: Logic 1 corresponds to a read operation, and Logic 0 corresponds to a write operation.

To control the device on the bus, a specific protocol is followed.

1. The master initiates a data transfer by establishing a start condition, which is defined as a high to low transition on SDATA while SCLK remains high, and indicates that an address/data stream follows.
2. All peripherals respond to the start condition and shift the next eight bits (the 7-bit address plus the R/$\overline{W}$ bit). The bits are transferred from MSB to LSB.
3. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse; this is known as an acknowledge (ACK) bit.
4. All other devices withdraw from the bus and maintain an idle condition. In the idle condition, the device monitors the SDATA and SCLK lines for the start condition and the correct transmitted address.

The R/$\overline{W}$ bit determines the direction of the data. Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. Logic 1 on the LSB of the first byte means that the master reads information from the peripheral.

The ADV7280/ADV7280-M act as standard I²C slave devices on the bus. The data on the SDATA pin is eight bits long, supporting the 7-bit address plus the R/$\overline{W}$ bit. The device has subaddresses to enable access to the internal registers; therefore, it interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses auto-increment, allowing data to be written to or read from the starting subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register individually without updating all the registers.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. During a given SCLK high period, the user should issue only one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADV7280/ADV7280-M do not issue an acknowledge and return to the idle condition.

If the highest subaddress is exceeded in auto-increment mode, one of the following actions is taken:

- In read mode, the register contents of the highest subaddress continue to be output until the master device issues a no acknowledge, which indicates the end of a read. A no acknowledge condition occurs when the SDATA line is not pulled low on the ninth pulse.
- In write mode, the data for the invalid byte is not loaded into a subaddress register. A no acknowledge is issued by the ADV7280/ADV7280-M, and the part returns to the idle condition.

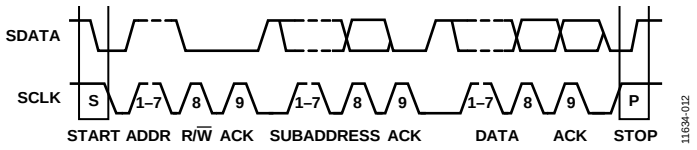

Figure 12. Bus Data Transfer

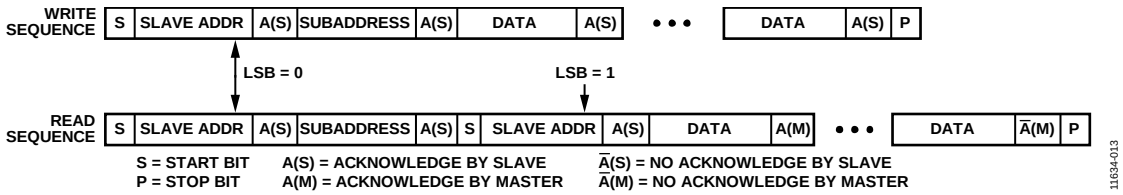

Figure 13. Read and Write Sequence

REGISTER MAPS

The ADV7280/ADV7280-M contain three register maps: the main register map, the VPP register map, and the CSI register map (ADV7280-M only).

Main Map

The I²C slave address of the main map of the ADV7280/ADV7280-M is set by the ALSB pin (see Table 15). The main map allows the user to program the I²C slave addresses of the VPP and CSI maps. The main map contains three sub maps: the user sub map, the interrupt/VDP sub map, and User Sub Map 2. These three sub maps are accessed by writing to the SUB_USR_EN bits (Address 0x0E[6:5]) within the main map (see Figure 14 and Table 16).

User Sub Map

The user sub map contains registers that program the analog front end and digital core of the ADV7280/ADV7280-M. The user sub map has the same I²C slave address as the main map. To access the user sub map, set the SUB_USR_EN bits in the main map (Address 0x0E[6:5]) to 00.

Interrupt/VDP Sub Map

The interrupt/VDP sub map contains registers that can be used to program internal interrupts, control the INTRQ pin, and decode vertical blanking interval (VBI) data.

The interrupt/VDP sub map has the same I²C slave address as the main map. To access the interrupt/VDP sub map, set the SUB_USR_EN bits in the main map (Address 0x0E[6:5]) to 01.

User Sub Map 2

User Sub Map 2 contains registers that control the ACE, down dither, and fast lock functions. It also contains controls that set the acceptable input luma and chroma limits before the ADV7280/ADV7280-M enter free run and color kill modes.

User Sub Map 2 has the same I²C slave address as the main map. To access User Sub Map 2, set the SUB_USR_EN bits in the main map (Address 0x0E[6:5]) to 10.

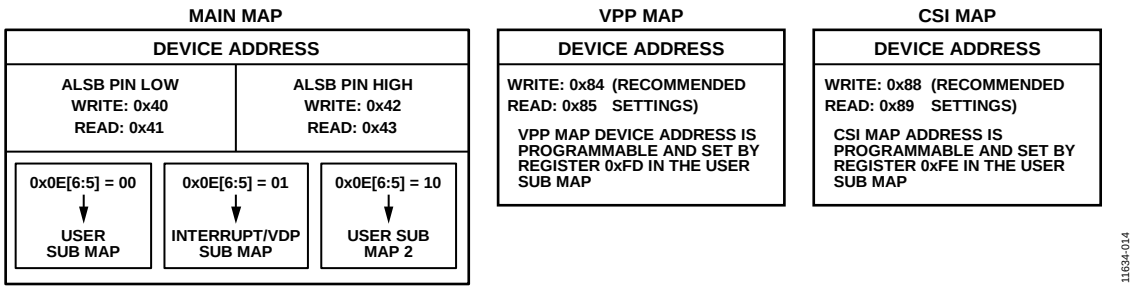

Figure 14. Register Map and Sub Map Access

Table 16. I²C Register Map and Sub Map Addresses

ALSB Pin	R/$\overline{W}$ Bit	Slave Address	SUB_USR_EN Bits (Address 0x0E[6:5])	Register Map or Sub Map
0	0 (write)	0x40	00	User sub map
0	1 (read)	0x41	00	User sub map
0	0 (write)	0x40	01	Interrupt/VDP sub map
0	1 (read)	0x41	01	Interrupt/VDP sub map
0	0 (write)	0x40	10	User Sub Map 2
0	1 (read)	0x41	10	User Sub Map 2
1	0 (write)	0x42	00	User sub map
1	1 (read)	0x43	00	User sub map
1	0 (write)	0x42	01	Interrupt/VDP sub map
1	1 (read)	0x43	01	Interrupt/VDP sub map
1	0 (write)	0x42	10	User Sub Map 2
1	1 (read)	0x43	10	User Sub Map 2
X[1]	0 (write)	0x84	XX[1]	VPP map
X[1]	1 (read)	0x85	XX[1]	VPP map
X[1]	0 (write)	0x88	XX[1]	CSI map (ADV7280-M only)
X[1]	1 (read)	0x89	XX[1]	CSI map (ADV7280-M only)

[1] X and XX mean don't care.

VPP Map

The video postprocessor (VPP) map contains registers that control the I2P core (interlaced-to-progressive converter).

The VPP map has a programmable I²C slave address, which is programmed using Register 0xFD in the user sub map of the main map. The default value for the VPP map address is 0x00; however, the VPP map cannot be accessed until the I²C slave address is reset. The recommended I²C slave address for the VPP map is 0x84.

To reset the I²C slave address of the VPP map, write to the VPP_SLAVE_ADDRESS[7:1] bits in the main register map (Address 0xFD[7:1]). Set these bits to a value of 0x84 (I²C write address; I²C read address is 0x85).

CSI Map (ADV7280-M Only)

The CSI map contains registers that control the MIPI CSI-2 output stream from the ADV7280-M.

The CSI map has a programmable I²C slave address, which is programmed using Register 0xFE in the user sub map of the main map. The default value for the CSI map address is 0x00; however, the CSI map cannot be accessed until the I²C slave address is reset. The recommended I²C slave address for the CSI map is 0x88.

To reset the I²C slave address of the CSI map, write to the CSI_TX_SLAVE_ADDRESS[7:1] bits in the main register map (Address 0xFE[7:1]). Set these bits to a value of 0x88 (I²C write address; I²C read address is 0x89).

SUB_USR_EN Bits, Address 0x0E[6:5]

The ADV7280/ADV7280-M main map contains three sub maps: the user sub map, the interrupt/VDP sub map, and User Sub Map 2 (see Figure 14). The user sub map is available by default. The other two sub maps are accessed using the SUB_USR_EN bits. When programming of the interrupt/VDP map or User Sub Map 2 is completed, it is necessary to write to the SUB_USR_EN bits to return to the user sub map.

PCB LAYOUT RECOMMENDATIONS

The ADV7280/ADV7280-M are high precision, high speed, mixed-signal devices. To achieve maximum performance from the parts, it is important to use a well-designed PCB. This section provides guidelines for designing a PCB for use with the ADV7280/ADV7280-M.

ANALOG INTERFACE INPUTS

When routing the analog interface inputs on the PCB, keep track lengths to a minimum. Use 75 Ω trace impedances when possible; trace impedances other than 75 Ω increase the chance of reflections.

POWER SUPPLY DECOUPLING

It is recommended that each power supply pin be decoupled with 100 nF and 10 nF capacitors. The basic principle is to place a decoupling capacitor within approximately 0.5 cm of each power pin. Avoid placing the decoupling capacitors on the opposite side of the PCB from the ADV7280/ADV7280-M because doing so introduces inductive vias in the path.

Place the decoupling capacitors between the power plane and the power pin. Current should flow from the power plane to the capacitor and then to the power pin. Do not apply the power connection between the capacitor and the power pin. The best approach is to place a via near, or beneath, the decoupling capacitor pads down to the power plane (see Figure 15).

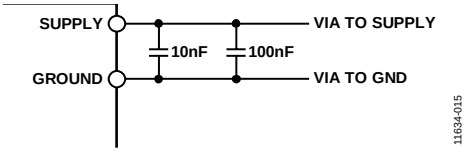

Figure 15. Recommended Power Supply Decoupling

It is especially important to maintain low noise and good stability for the P_{VDD} pin. Careful attention must be paid to regulation, filtering, and decoupling. It is highly desirable to provide separate regulated supplies for each circuit group (A_{VDD}, D_{VDD}, D_{VDDIO}, P_{VDD}, and, for the ADV7280-M, M_{VDD}).

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during horizontal and vertical sync periods). This disparity can result in a measurable change in the voltage supplied to the analog supply regulator, which can, in turn, produce changes in the regulated analog supply voltage. This problem can be mitigated by regulating the analog supply, or at least the P_{VDD} supply, from a different, cleaner power source, for example, from a 12 V supply.

Using a single ground plane for the entire board is also recommended. Experience has shown that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller, and long ground loops can result.

VREFN AND VREFP PINS

Place the circuit associated with the VREFN and VREFP pins as close as possible to the ADV7280/ADV7280-M and on the same side of the PCB as the part.

DIGITAL OUTPUTS ($\overline{\text{INTRQ}}$, GPO0 TO GPO2)

Minimize the trace length that the digital outputs must drive. Longer traces have higher capacitance, requiring more current and, in turn, causing more internal digital noise. Shorter traces reduce the possibility of reflections.

Adding a 30 Ω to 50 Ω series resistor can suppress reflections, reduce EMI, and reduce current spikes inside the ADV7280/ADV7280-M. If series resistors are used, place them as close as possible to the pins of the ADV7280/ADV7280-M. However, try not to add vias or extra length to the output trace in an attempt to place the resistors closer.

If possible, limit the capacitance that each digital output must drive to less than 15 pF. This recommendation can be easily accommodated by keeping traces short and by connecting the outputs to only one device. Loading the outputs with excessive capacitance increases the current transients inside the ADV7280/ADV7280-M, creating more digital noise on the power supplies.

EXPOSED METAL PAD

The ADV7280/ADV7280-M have an exposed metal pad on the bottom of the package. This pad must be soldered to ground. The exposed pad is used for proper heat dissipation, noise suppression, and mechanical strength.

DIGITAL INPUTS

The digital inputs of the ADV7280/ADV7280-M are designed to work with 1.8 V signals (3.3 V for D_{VDDIO}) and are not tolerant of 5 V signals. Extra components are required if 5 V logic signals must be applied to the decoder.

MIPI OUTPUTS FOR THE ADV7280-M (D0P, D0N, CLKP, CLKN)

It is recommended that the MIPI output traces be kept as short as possible and on the same side of the PCB as the ADV7280-M device. It is also recommended that a solid plane (preferably a ground plane) be placed on the layer adjacent to the MIPI traces to provide a solid reference plane.

MIPI transmission operates in both differential and single-ended modes. During high speed transmission, the pair of outputs operates in differential mode; in low power mode, the pair operates as two independent single-ended traces. Therefore, it is recommended that each output pair be routed as two loosely coupled 50 Ω single-ended traces to reduce the risk of crosstalk between the two traces in low power mode.

TYPICAL CIRCUIT CONNECTIONS

Figure 16 provides an example of how to connect the ADV7280. For detailed schematics of the ADV7280 evaluation board, contact a local Analog Devices field applications engineer or an Analog Devices distributor.

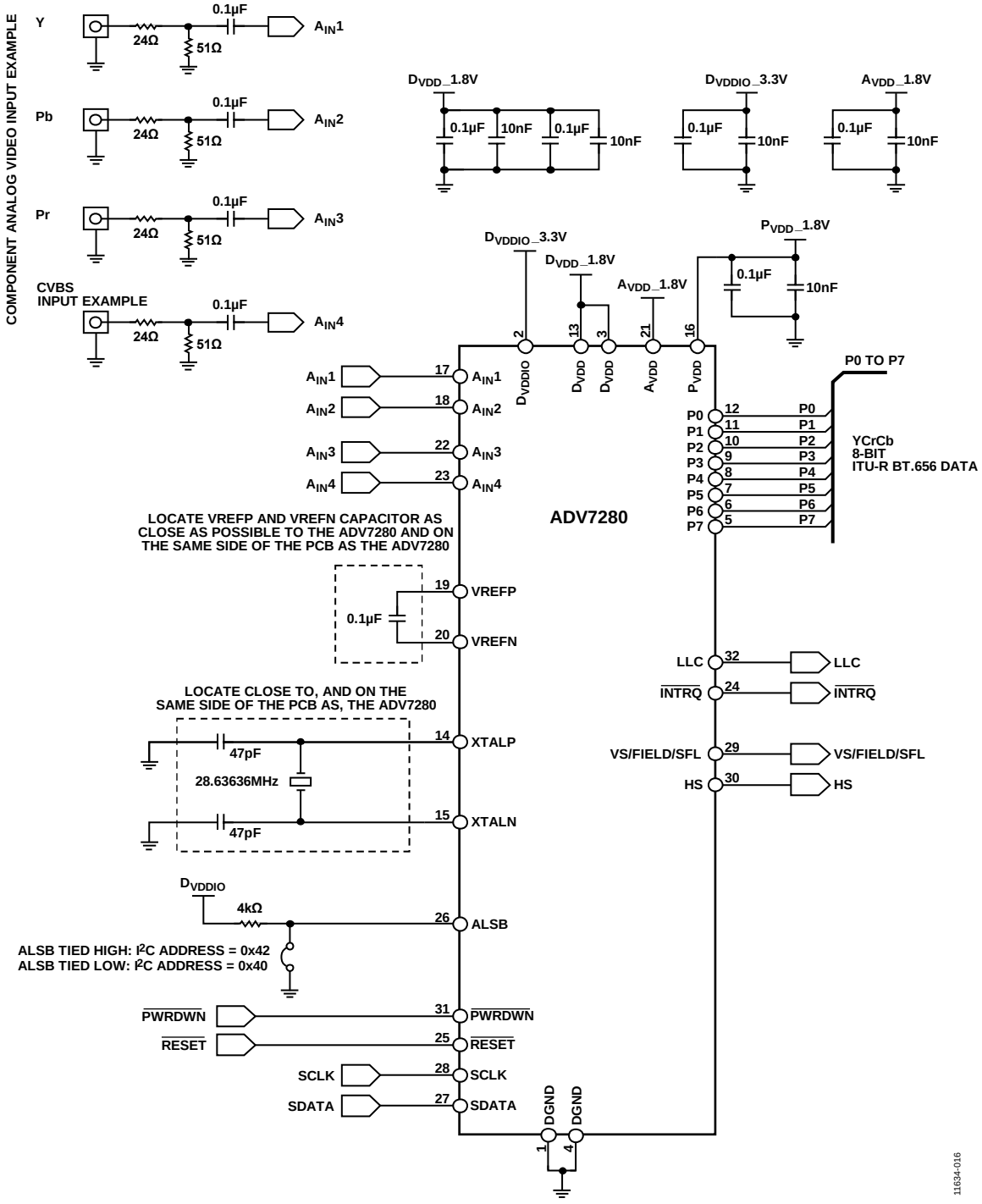

Figure 16. Typical Connection Diagram, ADV7280

Figure 17 provides an example of how to connect the ADV7280-M. For detailed schematics of the ADV7280-M evaluation board, contact a local Analog Devices field applications engineer or an Analog Devices distributor.

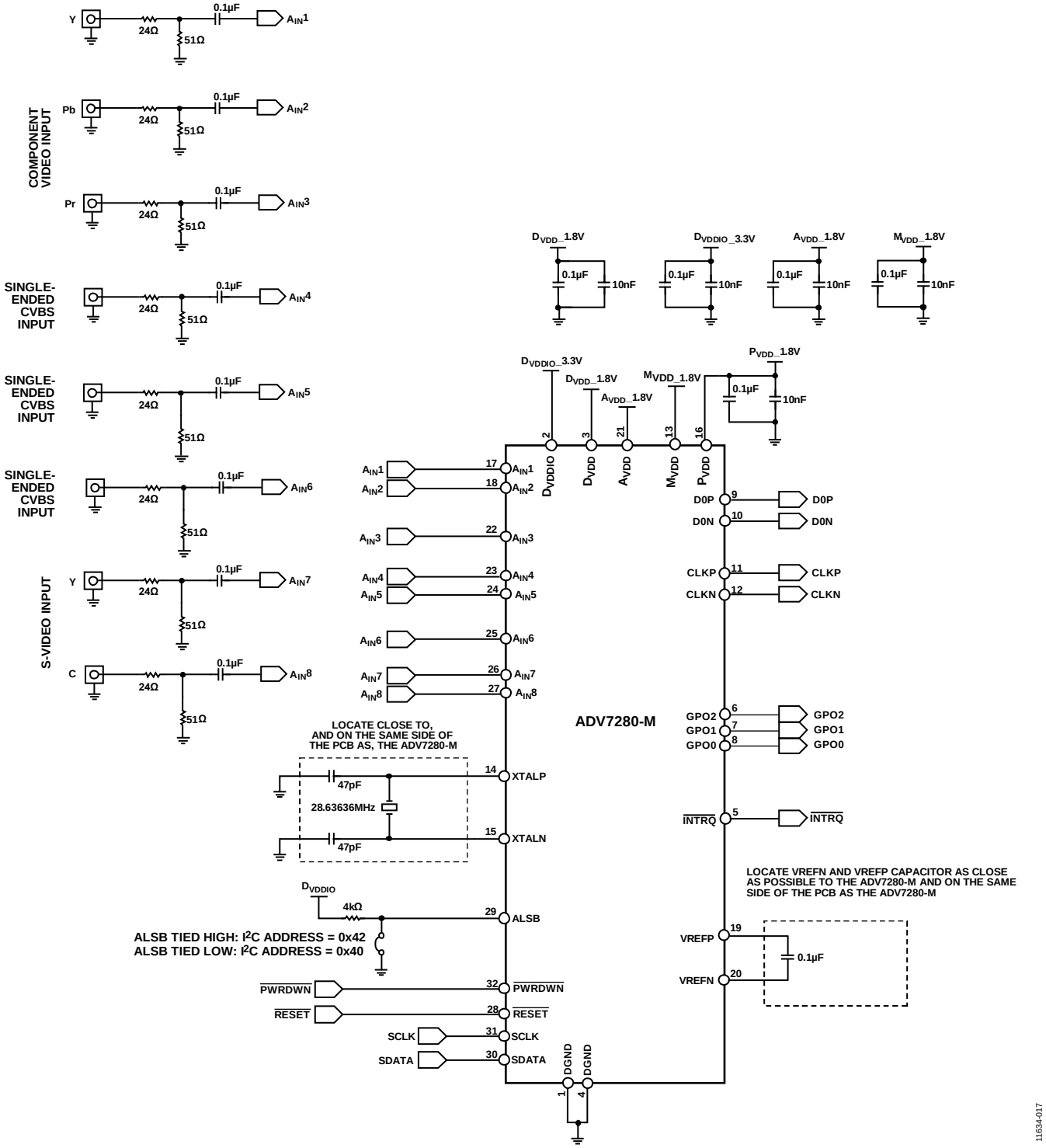

Figure 17. Typical Connection Diagram, ADV7280-M

OUTLINE DIMENSIONS

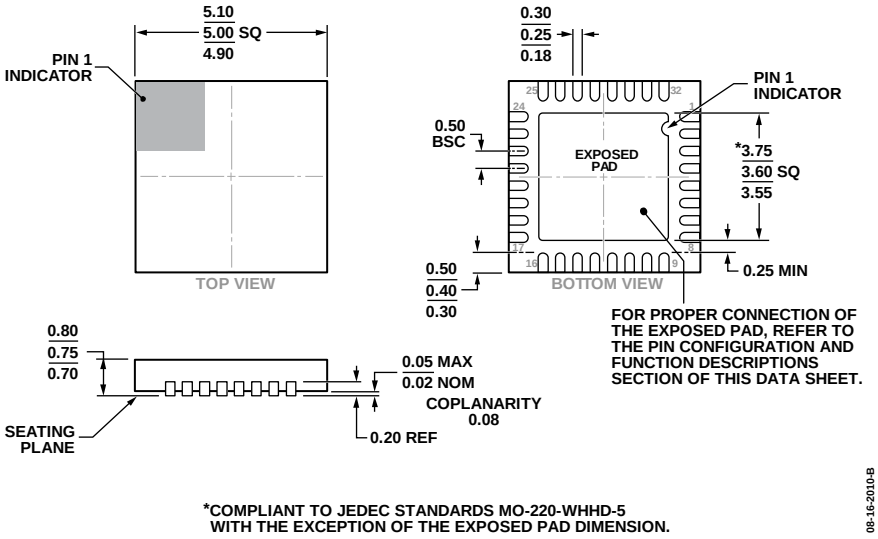

Figure 18. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADV7280WBCPZ	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADV7280WBCPZ-RL	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADV7280BCPZ	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADV7280BCPZ-RL	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADV7280KCPZ	−10°C to +70°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADV7280KCPZ-RL	−10°C to +70°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADV7280WBCPZ-M	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADV7280WBCPZ-M-RL	−40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADV7280BCPZ-M	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADV7280BCPZ-M-RL	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADV7280KCPZ-M	−10°C to +70°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADV7280KCPZ-M-RL	−10°C to +70°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
EVAL-ADV7280EBZ		Evaluation Board for the ADV7280	
EVAL-ADV7280MEBZ		Evaluation Board for the ADV7280-M	

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADV7280W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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