



## LP61L256B Series

### 32K X 8 Bit High SPEED LOW VCC CMOS SRAM

#### Features

- Single +3.3 volt power supply
- Access times: 12 ns (max.)
- Current: Operating: 100mA (max.)  
Standby: 10mA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs directly TTL compatible
- Common I/O using three-state output
- Data retention voltage: 2V (min.)
- Available in 28-pin SOJ and TSOP packages

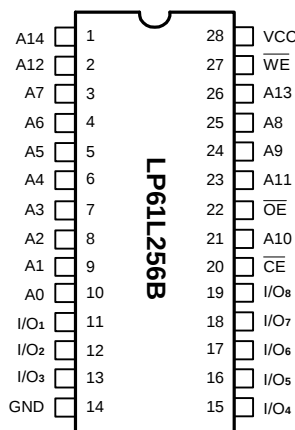
#### General Description

The LP61L256B is a high-speed, low-power 262,144-bit static random access memory organized as 32,768 words by 8 bits that operates on a single 3.3V power supply. Input and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

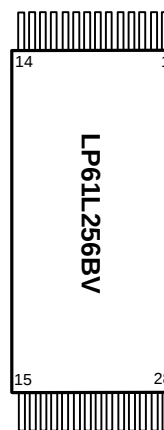
Minimum standby power is drawn by this device when  $\overline{CE}$  is at a high level, independent of the other input levels. Data retention is guaranteed at a power supply voltage as low as 2V.

#### Pin Configurations

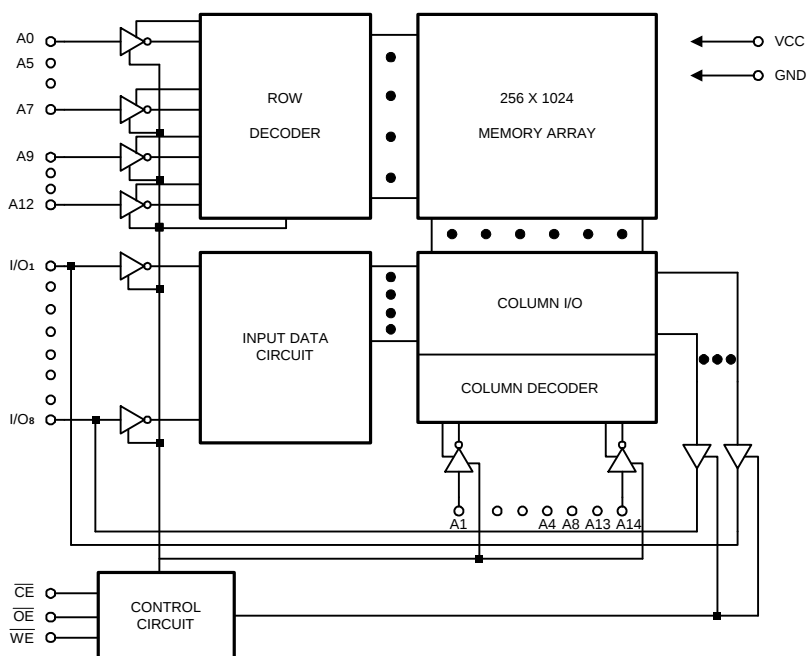
##### ■ SOJ



##### ■ TSOP



|          |                 |     |    |                  |                  |                  |     |                  |                  |                  |                  |                  |                 |     |
|----------|-----------------|-----|----|------------------|------------------|------------------|-----|------------------|------------------|------------------|------------------|------------------|-----------------|-----|
| Pin No.  | 1               | 2   | 3  | 4                | 5                | 6                | 7   | 8                | 9                | 10               | 11               | 12               | 13              | 14  |
| Pin Name | $\overline{OE}$ | A11 | A9 | A8               | A13              | $\overline{WE}$  | VCC | A14              | A12              | A7               | A6               | A5               | A4              | A3  |
| Pin No.  | 15              | 16  | 17 | 18               | 19               | 20               | 21  | 22               | 23               | 24               | 25               | 26               | 27              | 28  |
| Pin Name | A2              | A1  | A0 | I/O <sub>1</sub> | I/O <sub>2</sub> | I/O <sub>3</sub> | GND | I/O <sub>4</sub> | I/O <sub>5</sub> | I/O <sub>6</sub> | I/O <sub>7</sub> | I/O <sub>8</sub> | $\overline{CE}$ | A10 |

**Block Diagram**

**Pin Descriptions -SOJ**

| Pin No.             | Symbol                              | Description          |
|---------------------|-------------------------------------|----------------------|
| 1 - 10, 21, 23 - 26 | A0 - A14                            | Address Inputs       |
| 11 - 13, 15 - 19    | I/O <sub>1</sub> - I/O <sub>8</sub> | Data Inputs/Outputs  |
| 14                  | GND                                 | Ground               |
| 20                  | $\overline{CE}$                     | Chip Enable          |
| 22                  | $\overline{OE}$                     | Output Enable        |
| 27                  | $\overline{WE}$                     | Write Enable         |
| 28                  | VCC                                 | Power Supply (+3.3V) |

**Pin Description - TSOP**

| Pin No.           | Symbol                              | Description         |
|-------------------|-------------------------------------|---------------------|
| 1                 | $\overline{OE}$                     | Output Enable       |
| 2 - 5, 8 - 17, 28 | A0 - A14                            | Address Inputs      |
| 6                 | $\overline{WE}$                     | Write Enable        |
| 7                 | VCC                                 | Power Supply        |
| 18 - 20, 22 - 26  | I/O <sub>1</sub> - I/O <sub>8</sub> | Data Inputs/Outputs |
| 21                | GND                                 | Ground              |
| 27                | $\overline{CE}$                     | Chip Enable         |

**Recommended DC Operating Conditions**
 $(T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C})$ 

| Symbol          | Parameter          | Min. | Typ. | Max.      | Unit |
|-----------------|--------------------|------|------|-----------|------|
| VCC             | Supply Voltage     | 3.0  | 3.3  | 3.6       | V    |
| GND             | Ground             | 0    | 0    | 0         | V    |
| V <sub>IH</sub> | Input High Voltage | 2.2  | -    | VCC + 0.3 | V    |
| V <sub>IL</sub> | Input Low Voltage  | -0.3 | 0    | 0.8       | V    |
| C <sub>L</sub>  | Output Load        | -    | -    | 30        | pF   |
| TTL             | Output Load        | -    | -    | 1         | -    |

**Absolute Maximum Ratings\***

VCC to GND ..... -0.5V to +4.6V  
 IN, IN/OUT Volt to GND ..... -0.3V to VCC +0.3V  
 Operating Temperature, T<sub>opr</sub> ..... 0°C to +70°C  
 Storage Temperature, T<sub>stg</sub> ..... -55°C to +125°C  
 Power Dissipation, P<sub>t</sub> ..... 1.0W

**\*Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**DC Electrical Characteristics** ( $T_A = 0^{\circ}\text{C to } 70^{\circ}\text{C}$ , VCC = 3.3V  $\pm$  10%, GND = 0V)

| Symbol               | Parameter                    | LP61L256B-12 |      | Unit          | Conditions                                                                                                                  |
|----------------------|------------------------------|--------------|------|---------------|-----------------------------------------------------------------------------------------------------------------------------|
|                      |                              | Min.         | Max. |               |                                                                                                                             |
| I <sub>LI</sub>      | Input Leakage Current        | -            | 2    | $\mu\text{A}$ | V <sub>IN</sub> = GND to VCC                                                                                                |
| I <sub>LO</sub>      | Output Leakage Current       | -            | 2    | $\mu\text{A}$ | $\overline{\text{CE}} = V_{IH}$ or $\overline{\text{OE}} = V_{IH}$<br>V <sub>I/O</sub> = GND to VCC                         |
| I <sub>CC1</sub> (1) | Dynamic Operating Current    | -            | 100  | mA            | $\overline{\text{CE}} = V_{IL}$ , I <sub>I/O</sub> = 0 mA                                                                   |
| I <sub>SB</sub>      | Standby Power Supply Current | -            | 20   | mA            | $\overline{\text{CE}} = V_{IH}$                                                                                             |
| I <sub>SB1</sub>     |                              | -            | 10   | mA            | $\overline{\text{CE}} \geq \text{VCC} - 0.2\text{V}$<br>V <sub>IN</sub> $\geq$ VCC - 0.2V or<br>V <sub>IN</sub> $\leq$ 0.2V |
| V <sub>OL</sub>      | Output Low Voltage           | -            | 0.4  | V             | I <sub>OL</sub> = 8 mA                                                                                                      |
| V <sub>OH</sub>      | Output High Voltage          | 2.4          | -    | V             | I <sub>OH</sub> = -4 mA                                                                                                     |

Notes: 1. I<sub>CC1</sub> is dependent on output loading, cycle rates, and Read/Write patterns.

**Truth Table**

| Mode           | $\overline{\text{CE}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | I/O Operation    | Supply Current                  |
|----------------|------------------------|------------------------|------------------------|------------------|---------------------------------|
| Standby        | H                      | X                      | X                      | High Z           | $I_{\text{SB}}, I_{\text{SB1}}$ |
| Output Disable | L                      | H                      | H                      | High Z           | $I_{\text{CC1}}$                |
| Read           | L                      | L                      | H                      | $D_{\text{OUT}}$ | $I_{\text{CC1}}$                |
| Write          | L                      | X                      | L                      | $D_{\text{IN}}$  | $I_{\text{CC1}}$                |

**Capacitance** ( $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ )

| Symbol            | Parameter                | Min. | Max. | Unit | Conditions                   |
|-------------------|--------------------------|------|------|------|------------------------------|
| $C_{\text{IN}}^*$ | Input Capacitance        | -    | 10   | pF   | $V_{\text{IN}} = 0\text{ V}$ |
| $C_{\text{IO}}^*$ | Input/Output Capacitance | -    | 10   | pF   | $V_{\text{IO}} = 0\text{ V}$ |

\* These parameters are sampled and not 100% tested.

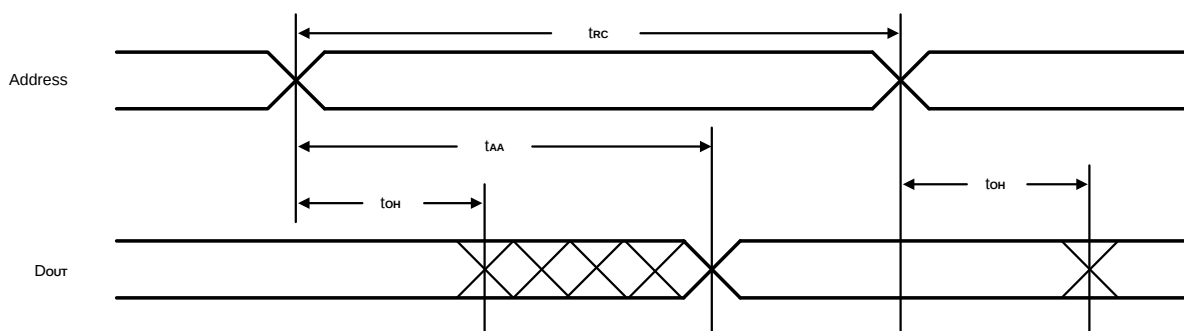
**AC Characteristics** ( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{\text{CC}} = 3.3\text{V} \pm 10\%$ )

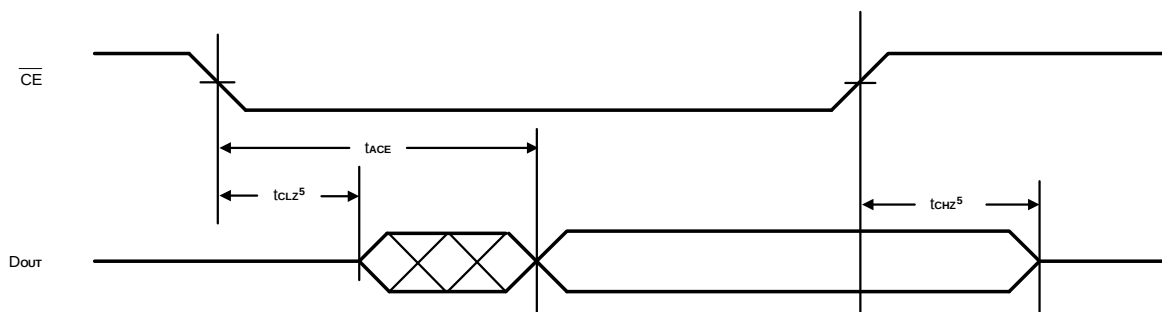
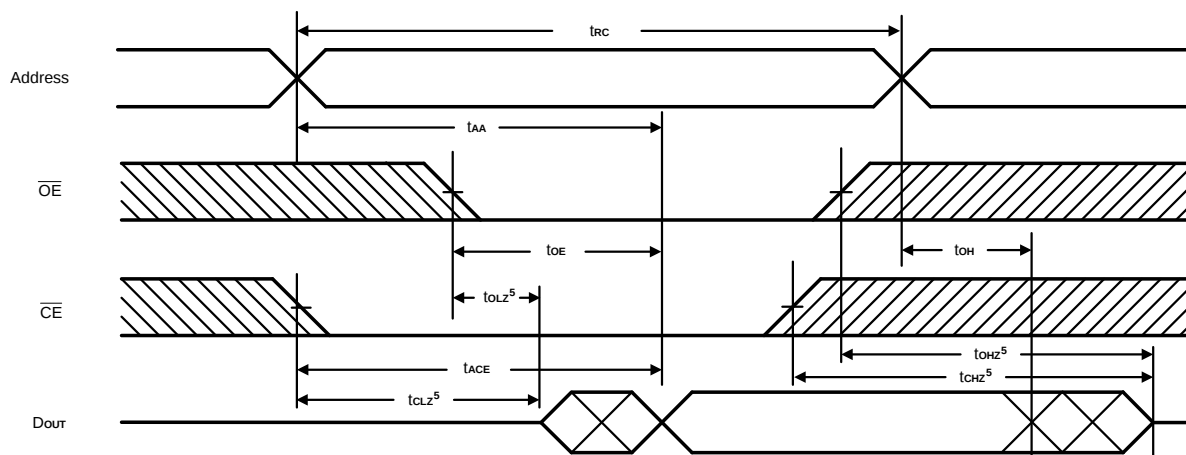
| Symbol           | Parameter                          | LP61L256B-12 |      | Unit |
|------------------|------------------------------------|--------------|------|------|
|                  |                                    | Min.         | Max. |      |
| Read Cycle       |                                    |              |      |      |
| t <sub>RC</sub>  | Read Cycle Time                    | 12           | -    | ns   |
| t <sub>AA</sub>  | Address Access Time                | -            | 12   | ns   |
| t <sub>ACE</sub> | Chip Enable Access Time            | -            | 12   | ns   |
| t <sub>OE</sub>  | Output Enable to Output Valid      | -            | 7    | ns   |
| t <sub>CLZ</sub> | Chip Enable to Output in Low Z     | 2            | -    | ns   |
| t <sub>OLZ</sub> | Output Enable to Output in Low Z   | 2            | -    | ns   |
| t <sub>CHZ</sub> | Chip Disable to Output in High Z   | 0            | 7    | ns   |
| t <sub>OHZ</sub> | Output Disable to Output in High Z | 2            | 6    | ns   |
| t <sub>OH</sub>  | Output Hold from Address Change    | 2            | -    | ns   |

**AC Characteristics (continued)**

| Symbol           | Parameter                       | LP61L256B-12 |      | Unit |
|------------------|---------------------------------|--------------|------|------|
|                  |                                 | Min.         | Max. |      |
| Write Cycle      |                                 |              |      |      |
| t <sub>wc</sub>  | Write Cycle Time                | 12           | -    | ns   |
| t <sub>cw</sub>  | Chip Enable to End of Write     | 10           | -    | ns   |
| t <sub>as</sub>  | Address Setup Time of Write     | 0            | -    | ns   |
| t <sub>aw</sub>  | Address Valid to End of Write   | 10           | -    | ns   |
| t <sub>wP</sub>  | Write Pulse Width               | 8            | -    | ns   |
| t <sub>wR</sub>  | Write Recovery Time             | 0            | -    | ns   |
| t <sub>whZ</sub> | Write to Output in High Z       | 0            | 7    | ns   |
| t <sub>dW</sub>  | Data to Write Time Overlap      | 8            | -    | ns   |
| t <sub>dH</sub>  | Data Hold from Write Time       | 0            | -    | ns   |
| t <sub>ow</sub>  | Output Active from End of Write | 5            | -    | ns   |

Notes: t<sub>chZ</sub>, t<sub>ohZ</sub> and t<sub>whZ</sub> are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

**Timing Waveforms**
**Read Cycle 1<sup>(1, 2, 4)</sup>**


**Timing Waveforms (continued)**
**Read Cycle 2<sup>(1, 3, 4)</sup>**

**Read Cycle 3<sup>(1)</sup>**


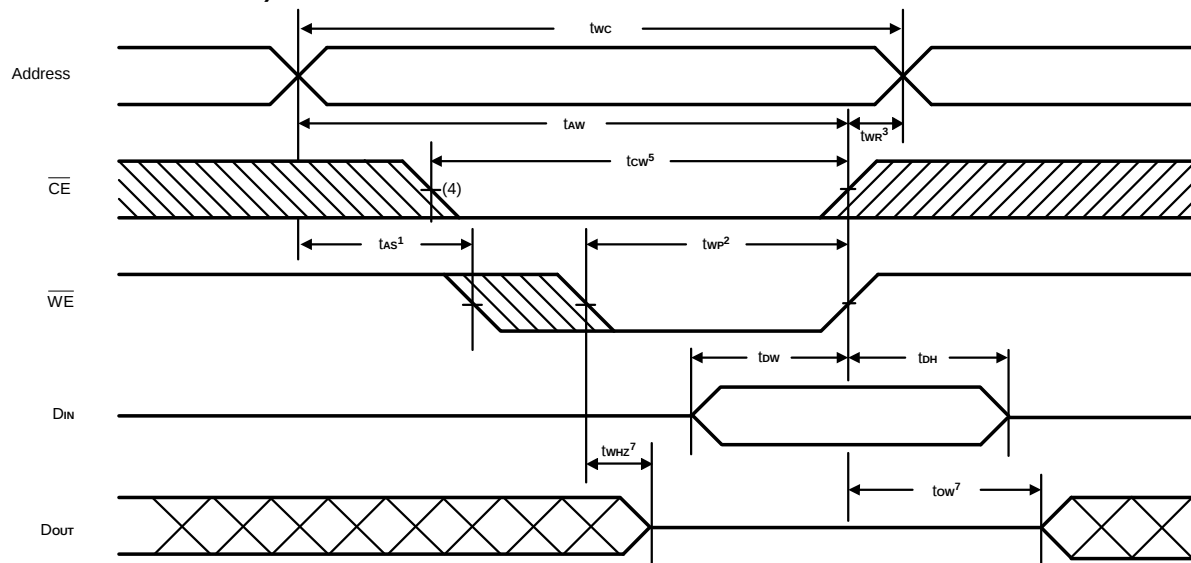
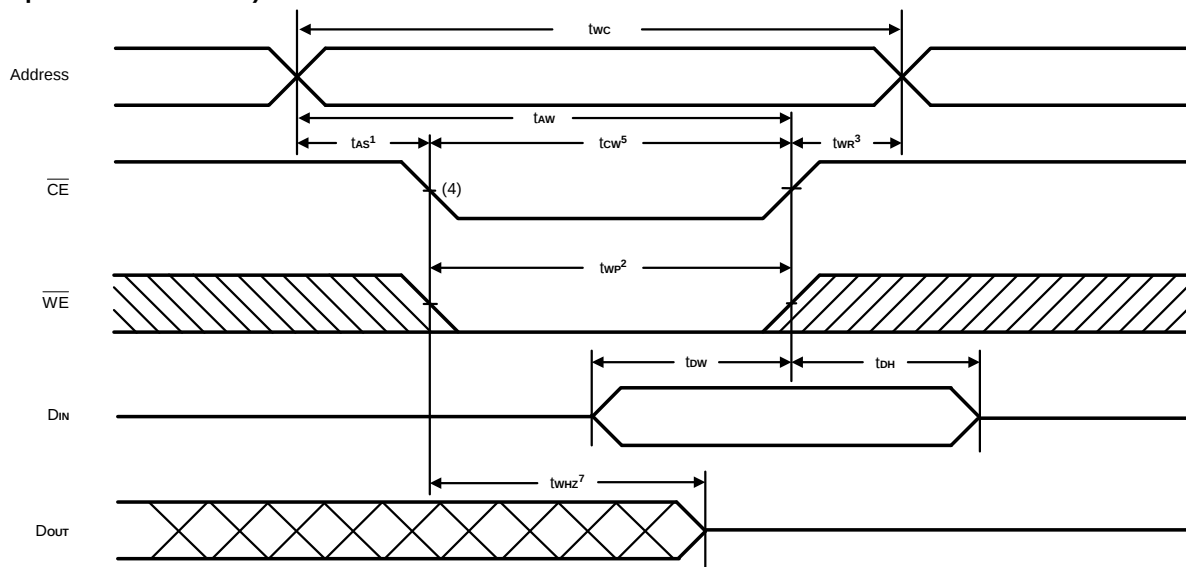
Note: 1.  $\overline{WE}$  is high for Read cycle.

2. Device is continuously enabled,  $\overline{CE} = V_{IL}$ .

3. Address valid prior to or coincident with  $\overline{CE}$  transition low.

4.  $\overline{OE} = V_{IL}$ .

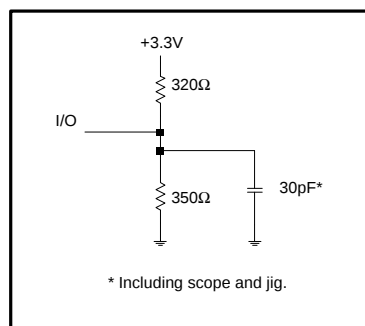
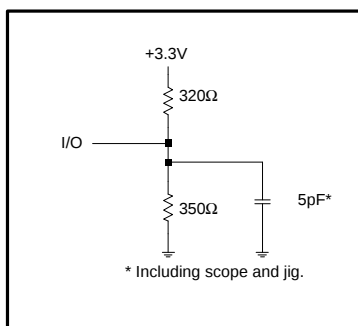
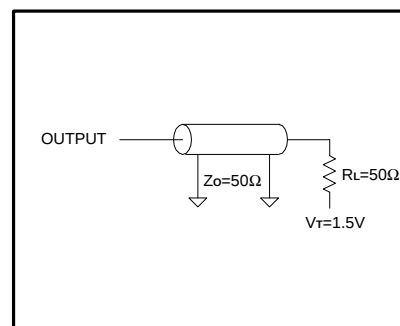
5. Transition is measured  $\pm 200\text{mV}$  from steady state. This parameter is sampled and not 100% tested.

**Timing Waveforms (continued)**
**Write Cycle<sup>(6)</sup>**
**(Write Enable Controlled)**

**Write Cycle 2**
**(Chip Enable Controlled)**


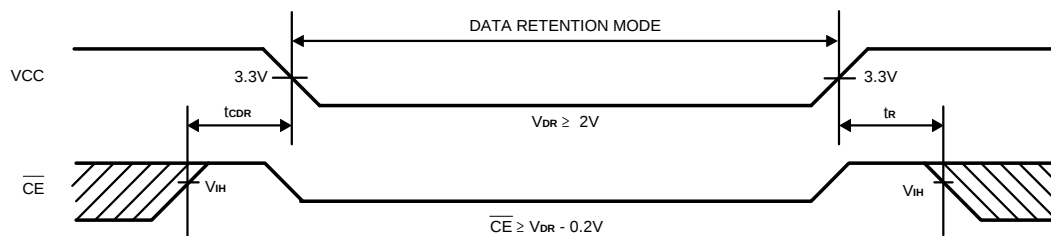
- Notes:
1.  $t_{AS}$  is measured from address valid to the beginning of Write.
  2. A Write occurs during the overlap ( $t_{WP}$ ) of a low  $\overline{CE}$  and a low  $\overline{WE}$ .
  3.  $t_{WR}$  is measured from  $\overline{CE}$  or  $\overline{WE}$  going high to the end of the Write cycle.
  4. If the  $\overline{CE}$  low transition occurs simultaneously with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  transition, outputs remain in a high impedance state.
  5.  $t_{CW}$  is measured from  $\overline{CE}$  going low to the end of Write.
  6.  $\overline{OE}$  is continuously low ( $\overline{OE} = V_{IL}$ ).
  7. Transition is measured  $\pm 200\text{mV}$  from steady state. This parameter is sampled and not 100% tested.

**AC Test Conditions**

|                                           |                        |
|-------------------------------------------|------------------------|
| Input Pulse Levels                        | 0V - 3V                |
| Input Rise and Fall Times                 | 3 ns                   |
| Input and Current Timing Reference Levels | 1.5V                   |
| Output Load                               | See Figures 1, 2 and 3 |


**Figure 1. Output Load**

**Figure 2. Output Load for  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$ , and  $t_{OW}$** 

**Figure 3. Output Load**
**Data Retention Characteristics** ( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ )

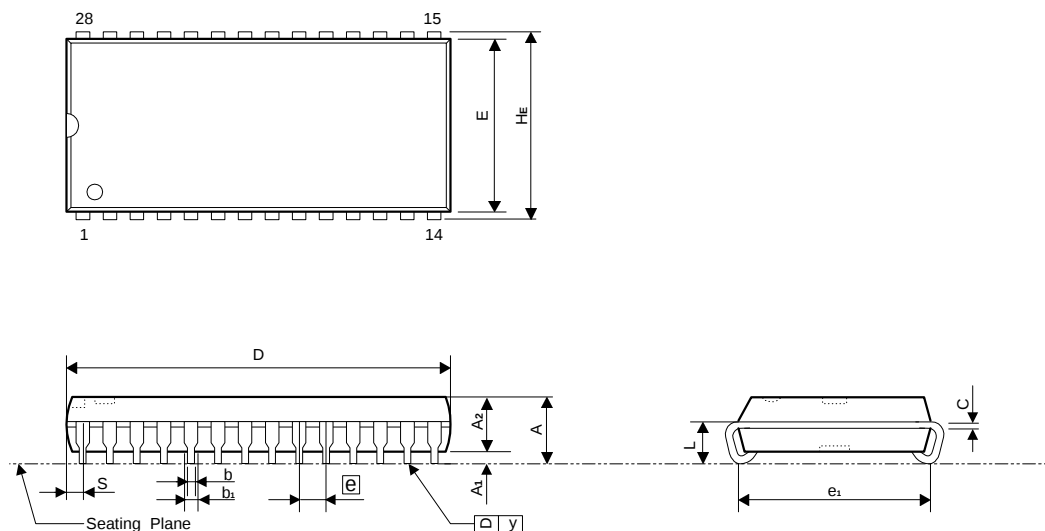
| Symbol     | Parameter                           | Min. | Max. | Unit | Conditions                                                                                                 |
|------------|-------------------------------------|------|------|------|------------------------------------------------------------------------------------------------------------|
| $V_{DR}$   | VCC for Data Retention              | 2.0  | 3.6  | V    | $\overline{CE} \geq V_{CC} - 0.2V$                                                                         |
| $I_{CCDR}$ | Data Retention Current              | -    | 0.5  | mA   | $V_{CC} = 2V$ , $\overline{CE} \geq V_{CC} - 0.2V$<br>$V_{IN} \geq V_{CC} - 0.2V$ or<br>$V_{IN} \leq 0.2V$ |
| $t_{CDR}$  | Chip Disable to Data Retention Time | 0    | -    | ns   | See Retention Waveform                                                                                     |
| $t_R$      | Operation Recovery Time             | 5    | -    | ms   |                                                                                                            |

**Low VCC Data Retention Waveform**

**Ordering Information**

| Part No.      | Access Time (ns) | Operating Current<br>Max. (mA) | Standby Current<br>Max. (mA) | Package  |
|---------------|------------------|--------------------------------|------------------------------|----------|
| LP61L256BS-12 | 12               | 100                            | 10                           | 28L SOJ  |
| LP61L256BV-12 | 12               | 100                            | 10                           | 28L TSOP |

**Package Information**
**SOJ 28L Outline Dimensions**

unit: inches/mm



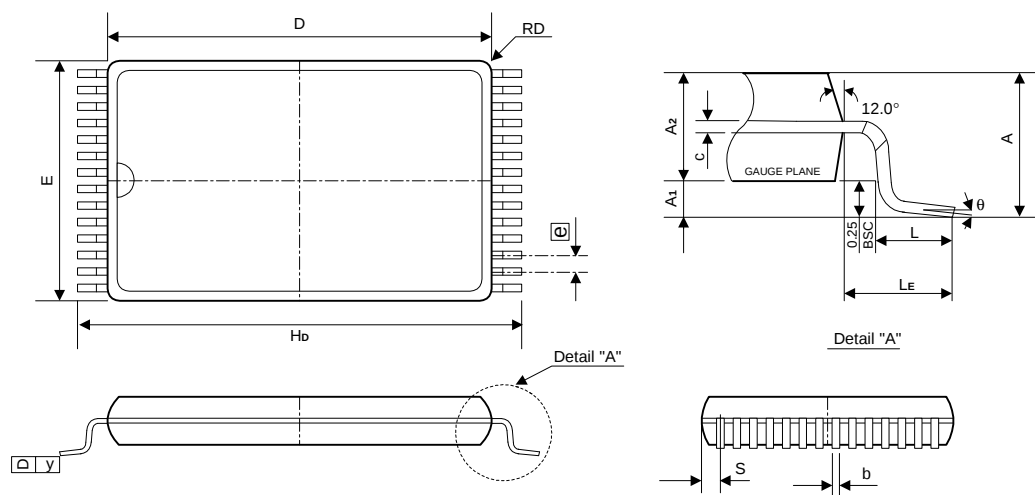
| Symbol | Dimensions in inches    | Dimensions in mm        |
|--------|-------------------------|-------------------------|
| A      | 0.140 Max.              | 3.56 Max.               |
| A1     | 0.027 Min.              | 0.69 Min.               |
| A2     | 0.100±0.005             | 2.54±0.13               |
| b1     | 0.028 Typ.              | 0.71 Typ.               |
| b      | 0.018 Typ.              | 0.46 Typ.               |
| C      | 0.010 Typ.              | 0.25 Typ.               |
| D      | 0.710 Typ. (0.730 Max.) | 18.03 Typ. (18.54 Max.) |
| E      | 0.300±0.005             | 7.62±0.13               |
| e      | 0.050 Typ.              | 1.27 Typ.               |
| e1     | 0.265±0.010             | 6.73±0.25               |
| HE     | 0.337±0.008             | 8.56±0.20               |
| L      | 0.087±0.10              | 2.21±0.25               |
| S      | 0.045 Max.              | 1.14 Max.               |
| y      | 0.004 Max.              | 0.10 Max.               |

**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

**Package Information**
**TSOP 28L TYPE I (8 X 13.4mm) Outline Dimensions**

unit: inches/mm



| Symbol         | Dimensions in inches | Dimensions in mm |
|----------------|----------------------|------------------|
| A              | 0.049 Max.           | 1.25 Max.        |
| A <sub>1</sub> | 0.002 Min.           | 0.05 Min.        |
| A <sub>2</sub> | 0.039±0.002          | 1.00±0.05        |
| b              | 0.0079±0.0012        | 0.20±0.03        |
| c              | 0.006±0.0003         | 0.15±0.008       |
| D              | 0.465±0.004          | 11.80±0.10       |
| E              | 0.315±0.004          | 8.00±0.10        |
| e              | 0.0217 TYP.          | 0.55 TYP.        |
| H <sub>D</sub> | 0.528±0.008          | 13.40±0.20       |
| L              | 0.02±0.008           | 0.50±0.20        |
| LE             | 0.0266 TYP.          | 0.675 TYP.       |
| S              | 0.0167 TYP.          | 0.425 TYP.       |
| y              | 0.004 Max.           | 0.10 Max.        |
| θ              | 0° ~ 6°              | 0° ~ 6°          |

**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.



**Стандарт  
Электрон  
Связь**

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