

15 GHz Divide-by-1 to 232-1 32-Bit Programmable Integer Divider

Features

- Wide operating range: DC-15 GHz
- Divide ratios: 1 to $2^{32}-1$
- Large output swings: 0.8 Vpp/side
- Adjustable output amplitude
- Single-ended or differential drive
- Serial Control Lines
- Low SSB phase noise
- Ceramic 4 mm x 4 mm package
- USB powered eval board with PC interface

Application

The SuperDivider can be used as a general purpose, highly configurable, divider in a variety of high frequency synthesizer applications.

Pad Metallization

The QFN package pad metallization is 500-1000 micro-inches of Sn63 solder dip.

Description

The SuperDivider is a highly programmable integer divider covering all integer divide ratios between 1 and 4,294,967,295 (232-1). The device features single-ended or differential inputs and outputs. 3-wire serial control inputs are CMOS and LVTTTL compatible for ease of system integration. The SuperDivider is packaged in a 24-pin, 4 mm x 4 mm leadless ceramic surface mount package.

A Windows PC user interface is available with the eval board (UXN14M32KE). The interface makes it convenient to adjust the output amplitude and the divide ratio. It is powered by USB bus so it is easy to use. Just plug the UXN14M32KE into your PC, install the Microsemi software, and you are using the most powerful frequency divider on the market.



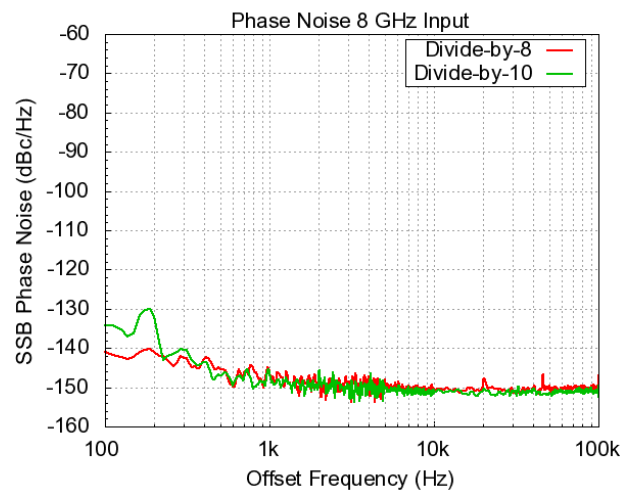
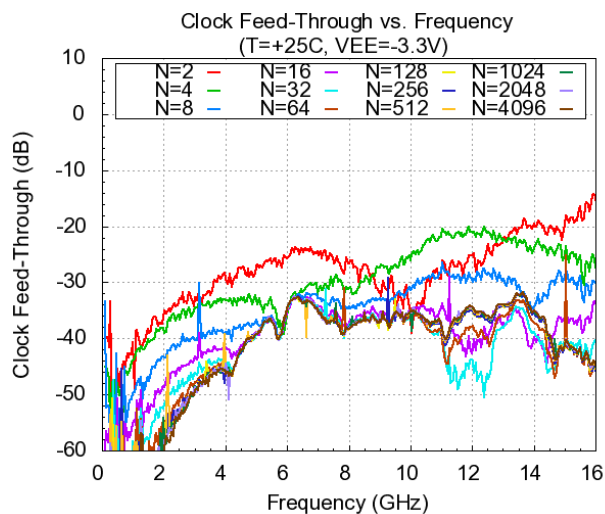
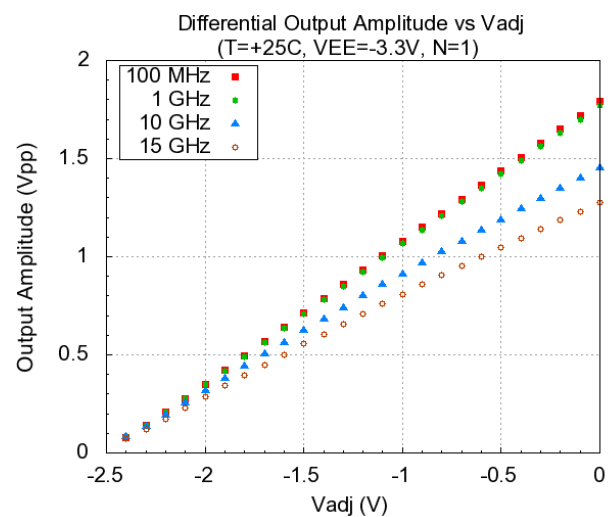
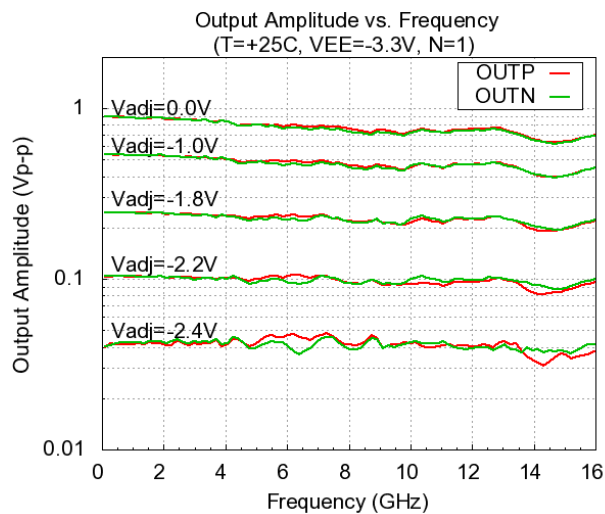
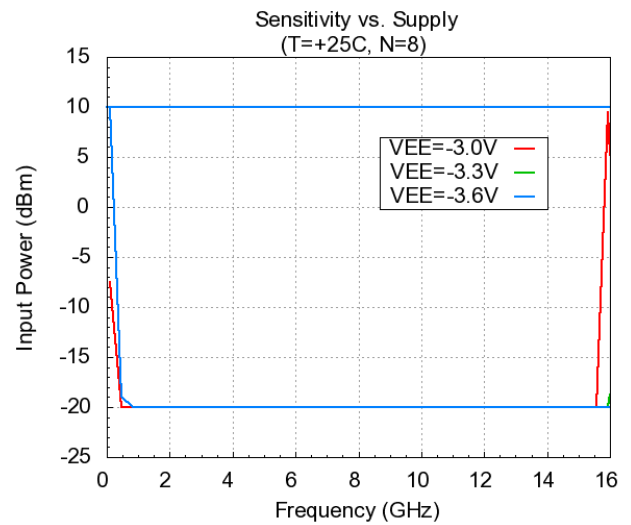
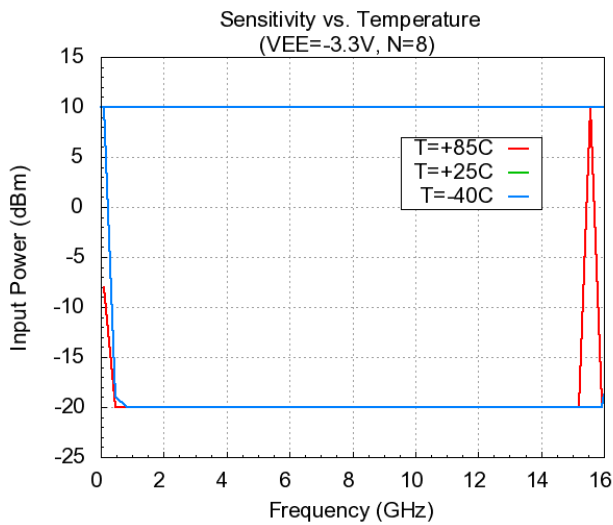
Key Characteristics @ 25°C: VEE= -3.3 V, IEE=110-220 mA, Zi=50 Ω, Zo=60Ω

| Parameter | Description | Min | Typ | Max |
|------------|-----------------------------------|-----------------|-----|-----|
| Fin (GHz) | Input Frequency | DC ¹ | - | 15 |
| Pin (dBm) | Input Power | -20 | 0 | 10 |
| Vout (Vpp) | Output Voltage Per Side | - | 0.8 | - |
| PDC (W) | DC Power Dissipation ² | 0.3 | - | 0.8 |
| θjc (°C/W) | Junction-Case Thermal Resistance | - | 51 | - |

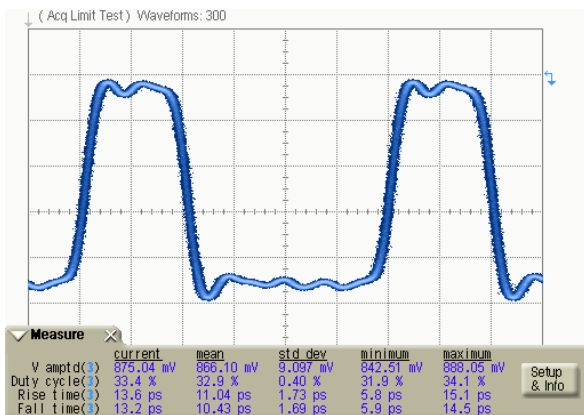
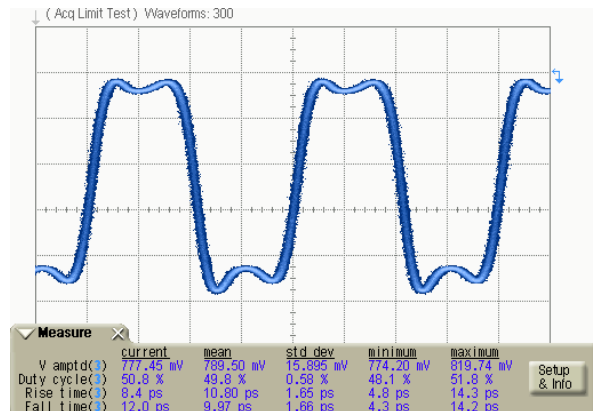
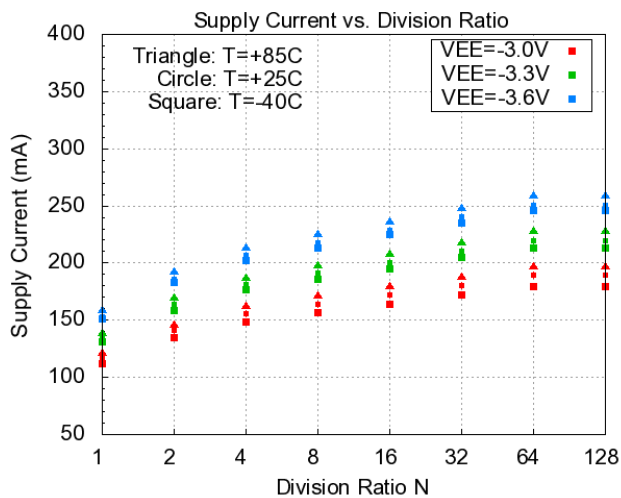
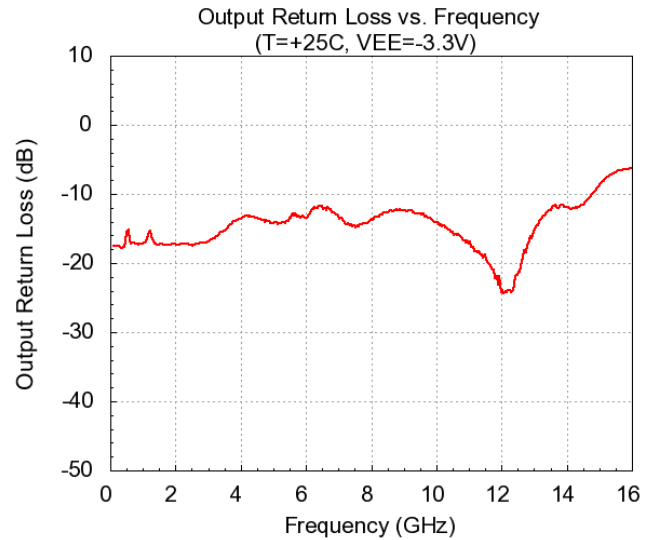
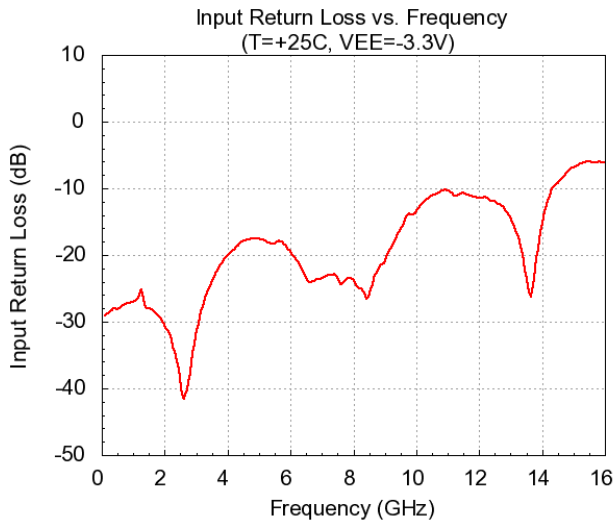
¹ Low frequency dependent on input edge speed

² Depends on divide ratio

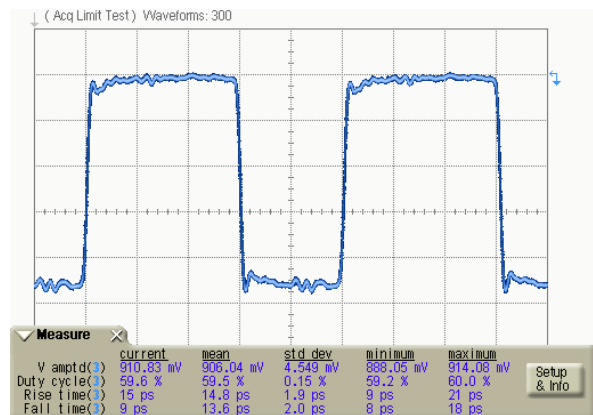
Typical Performance



Typical Performance



Divide-by-3
Input Frequency = 10 GHz



Divide-by-10
Input Frequency = 10 GHz

Functional Block Diagram

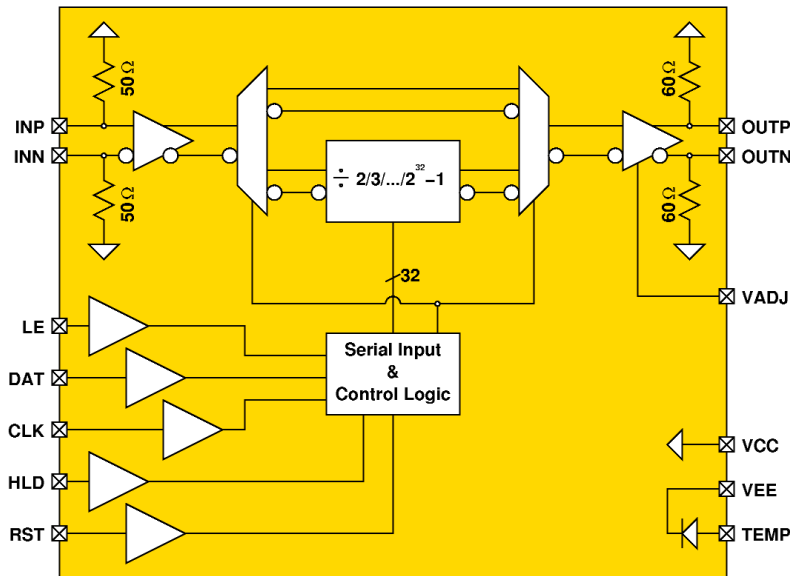


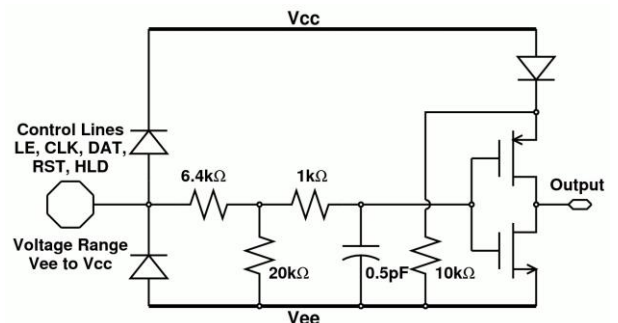
Table 1: Pin Description

| Port Name | Description | Notes |
|-----------|-----------------------------------|--------------------------------------------------|
| INP | Divider input, positive terminal | CML signal levels |
| INN | Divider input, negative terminal | CML signal levels |
| OUTP | Divider output, positive terminal | Requires DC return path to VCC |
| OUTN | Divider output, negative terminal | Requires DC return path to VCC |
| VCC | RF & DC ground | - |
| VEE | -3.3 V @ 220 mA | Negative supply voltage |
| LE | Load enable | CMOS levels, defaults to logic 0 |
| DAT | Serial data input | CMOS levels, defaults to logic 0 |
| CLK | Serial clock input | CMOS levels, defaults to logic 0 |
| HLD | Output hold control | CMOS levels, defaults to logic 0 |
| RST | Divider reset control | CMOS levels, defaults to logic 0 |
| VADJ | Output amplitude control | Tie to VCC via resistor, refer to text for value |
| TEMP | Temperature diode | Optional temperature diode, refer to text |

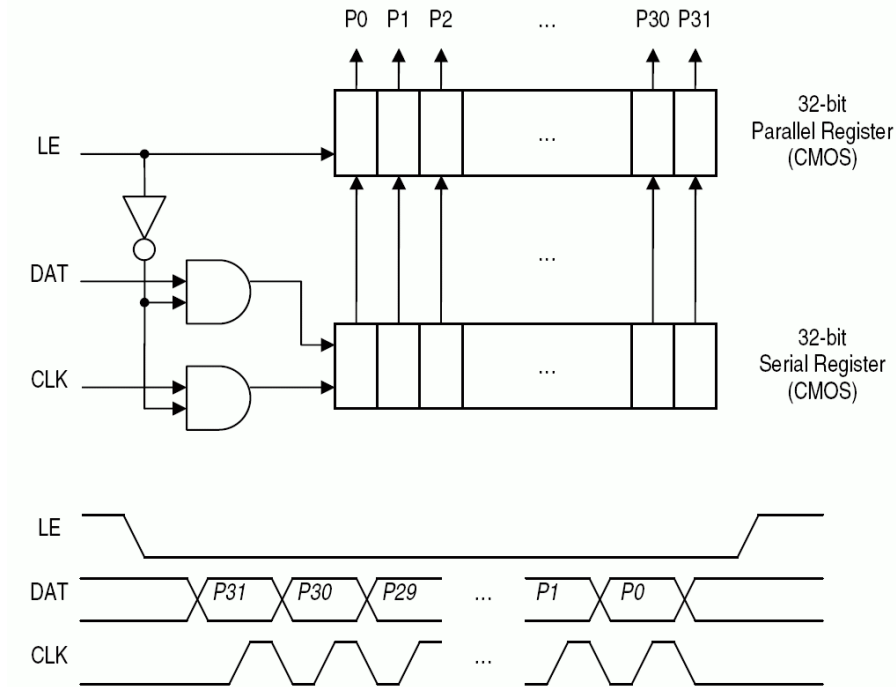
Table 2: Pin Description

| Logic Level | Minimum | Typical | Maximum |
|-------------|------------|---------|------------|
| 1 (High) | VCC-1.25 V | VCC | VCC |
| 0 (Low) | VEE | VEE | VEE+1.25 V |

Simplified Control Logic Schematic



Programming Divide Ratio



Note: Maximum CLK frequency is estimated to be 30 MHz.

Equation 1

$$\text{Divider Modulus} = N = P0 \cdot 20 + P1 \cdot 21 + P2 \cdot 22 + \dots + P31 \cdot 231 \quad \text{for } 1 < N < (232-1)$$

Note: When N=0, HLD must be pulled high to ensure that the output does not enter meta-stable state.

Table 3: OEE vs. Divide Ratio

| N | IEE (mA) |
|-------|----------|
| 0 | 110 |
| 1 | 135 |
| 2-3 | 165 |
| 4-7 | 180 |
| 8-15 | 190 |
| 16-31 | 200 |
| 32-63 | 210 |
| ≥64 | 220 |

Application Notes

Low Frequency Operation:

Low frequency operation is limited by external bypass capacitors and the slew rate of the input clock. The next paragraph shows the calculations for the bypass capacitors. If DC coupled, the device operates down to DC for square-wave inputs. Sine-wave inputs are limited to ~50 MHz due to the 10 dBm max input power limitation.

The values of the coupling capacitors for the high-speed inputs and outputs (I/O's) is determined by the lowest frequency the IC will be operated at.

$$C \gg \frac{1}{2 \cdot \pi \cdot 50 \Omega \cdot f_{\text{lowest}}}$$

For example: to use the device below 30 kHz, coupling capacitors should be larger than 0.1 μF

IC Assembly:

The device is designed to operate with either single-ended or differential inputs. Figures 4, 5 & 6 show the IC assembly diagrams for positive and negative supply voltages. In either case the supply should be capacitively bypassed to the ground to provide a good AC ground over the frequency range of interest. The backside paddle of the QFN package should be connected to a good thermal heat sink.

All RF I/O's are connected to V_{cc} through on-chip termination resistors. This implies that when V_{cc} is not DC grounded (as in the case of positive supply), the RF I/O's should be AC coupled through series capacitors unless the connecting circuit can generate the correct levels through level shifting.

ESD Sensitivity:

Although SiGe IC's have robust ESD sensitivities, preventive ESD measures should be taken while storing, handling, and assembling.

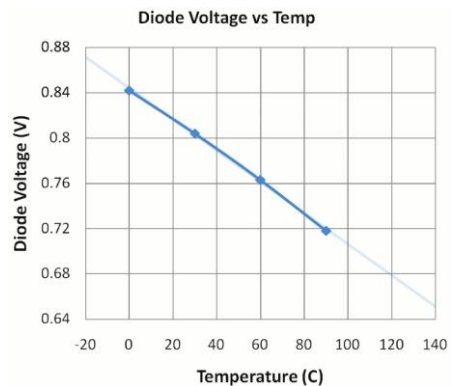
Inputs are more ESD susceptible as they could expose the base of a BJT or the gate of a MOSFET. For this reason, all the inputs are protected with ESD diodes. These inputs have been tested to withstand voltage spikes up to 400 V.

Table 4: Negative CML Logic Levels for DC Coupling (T=25°C) Assuming 50 Ω terminations at inputs and outputs

| Parameter | | Minimum | Typical | Maximum | |
|-----------|-----------------------|-----------------------------|---------------------------|--------------------------|------------------------|
| Input | Differential | Logic Input _{high} | V_{cc} | V_{cc} | V_{cc} |
| | | Logic Input _{low} | $V_{cc} - 0.05 \text{ V}$ | $V_{cc} - 0.3 \text{ V}$ | $V_{cc} - 1 \text{ V}$ |
| | Single | Logic Input _{high} | $V_{cc} + 0.05 \text{ V}$ | $V_{cc} + 0.3 \text{ V}$ | $V_{cc} + 1 \text{ V}$ |
| | | Logic Input _{low} | $V_{cc} - 0.05 \text{ V}$ | $V_{cc} - 0.3 \text{ V}$ | $V_{cc} - 1 \text{ V}$ |
| Output | Differential & Single | Logic Input _{high} | V_{cc} | V_{cc} | V_{cc} |
| | | Logic Input _{low} | $V_{cc} - 0.2 \text{ V}$ | $V_{cc} - 0.3 \text{ V}$ | $V_{cc} - 1 \text{ V}$ |

Temperature Diode:

An optional on chip temperature diode is provided for users interested in evaluating the IC's temperature. A single resistor to VCC establishes a nominal current through the diode. The voltage developed across the temperature pin (pin 20) referenced to VEE (pin 22) can then be used to indicate the surface temperature to the IC. The plot in figure 1 was obtained by forcing a fixed current of approximately 120 μ A through the diode for an unbiased device at multiple temperatures and fitting a line to the data to allow extrapolation over a range of temperatures. In this case, the temperature can be calculated by the following formula:



$$T = \frac{V_d - 0.84}{-0.00133}$$

Package Heatsink:

The package backside provides the primary heat conduction path and should be attached to a good heatsink on the PC board to maximize performance. User PC boards should maximize the contact area to the package paddle and contain an array of vias to aid thermal conduction to either a backside heatsink or internal copper planes.

Divider Outputs:

The equivalent circuit of the divider outputs is shown below. The outputs require a DC return path capable of handling ~20 mA per side. If DC coupling is employed, the DC resistance of the receiving circuits should be ~50 ohms (or less) to VCC to prevent excessive common mode voltage from saturating the prescaler outputs. If AC coupling is used, the recommended configuration is shown in figure 3. The discrete R/L/C elements should be resonance free up to the maximum frequency of operation for broadband applications.

The output amplitude can be adjusted over a 10:1 range by one of two methods. Voltage at the VADJ pin can be set to a value between VCC, for maximum amplitude, and VCC-2.4 V for an amplitude ~1/10 the max swing. Voltages between these two values will produce a linear change in output swing.

$$V_{out} \sim [1.1 - 0.44 \cdot (V_{CC} - V_{ADJ})] \cdot (V_{CC} - V_{EE} - 0.8) / 2.5$$

Alternatively, output amplitude can be adjusted by connecting a 10 k Ω potentiometer between VADJ and VCC. Resistor values approaching 0 Ohms will lead to the maximum swing, while values approaching 10 k Ω will lead to the minimum output swing. If adjustable output amplitude is not needed, users can either tie VADJ to VCC for maximum swing, or insert a resistor Rx between VADJ and VCC for a lower fixed swing.

$$V_{out} \sim [1.1 - 0.44 \cdot R_x \cdot (V_{CC} - V_{EE} - 0.8) / (R_x + 580)] \cdot (V_{CC} - V_{EE} - 0.8) / 2.5$$

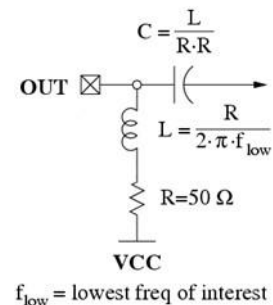
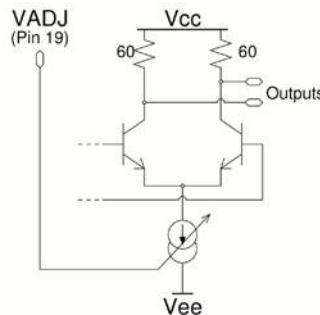
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NOTE: The formulas provided are approximations only, and do not account for process, temperature and frequency variations.



Differential vs. Single-Ended:

The UXN14M32K is fully differential to maximize signal-to-noise ratios for high-speed operation. All high speed inputs and outputs are terminated to VCC with on-chip resistors (refer to functional block diagram for specific resistor values). The maximum DC voltage on any terminal must be limited to VCC +/- 1 V to prevent damaging the termination resistors with excessive current. Regardless of bias conditions, the following equation should be satisfied when driving the inputs differentially:

$$V_{CC} - 1 < V_{AC}/4 + V_{DC} < V_{CC} + 1$$

where VAC is the input signal p-p voltage and VDC is common-mode voltage.

In addition to the maximum input signal levels, single-ended operation imposes additional restrictions: the average DC values at the two inputs to the IC should be equal for the best sensitivity. The unused input should be terminated to ground through the same elements on the active input side to reduce reflections at high frequencies and to achieve equal DC values. For example, if the active input source termination is 50 Ohms and has a DC-blocking capacitor, then the unused input should be terminated through 50 Ohms and the same value of DC-blocking capacitance to ground.

Note that a potential oscillation mechanism exists if both inputs are static (i.e. no signal) and have identical DC voltages; a small DC offset on either input is sufficient to prevent possible oscillations. Connecting a 10k ohm resistor between either the unused input and VEE should provide sufficient offset to prevent oscillation. The RST and HLD controls can also be used to prevent such oscillations from occurring.

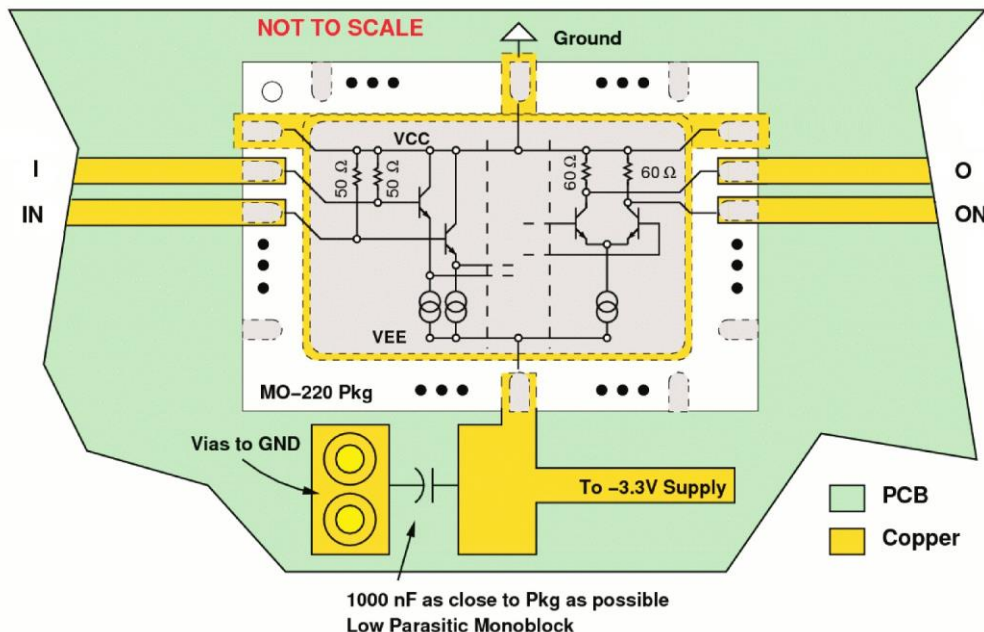
Rest and Hold:

There are several different ways to disable the divider output, apart from removing the DC bias altogether. The control line RST resets all divider states to logic low, preventing any circuits from toggling while invoked. OUTP will be low and OUTN will be high. HLD also holds the outputs constant, but unlike RST, the divider core is still functional. In either case, the divide ratio is not affected and can be updated independent of whether RST and/or HLD are enabled or disabled. While HLD is enabled, the divide ratio can be set to zero in order to achieve minimum supply current draw. Finally, VADJ can be pulled down to VEE in order to fully shut down the output buffer, achieving even lower current draw. In that case, both output voltages will be near VCC.

Table 5: RST and HLD Logic

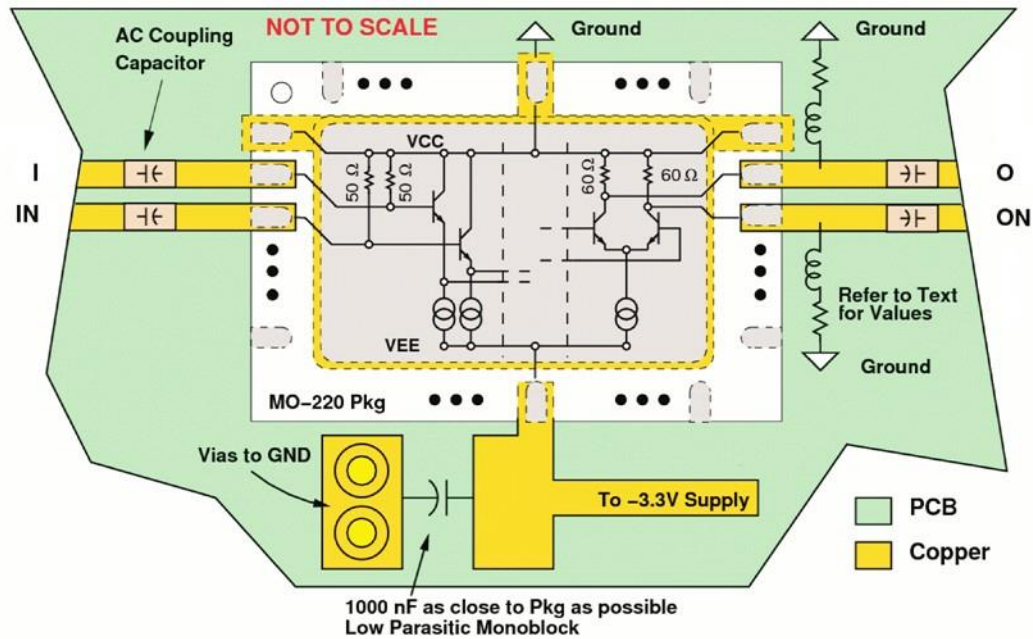
| Control | Logic Level | Mode |
|---------|-------------|----------------|
| RST | 0 | Reset Disabled |
| | 1 | Reset Enabled |
| HLD | 0 | Hold Disabled |
| | 1 | Hold Enabled |

Negative Supply (DC Coupling)



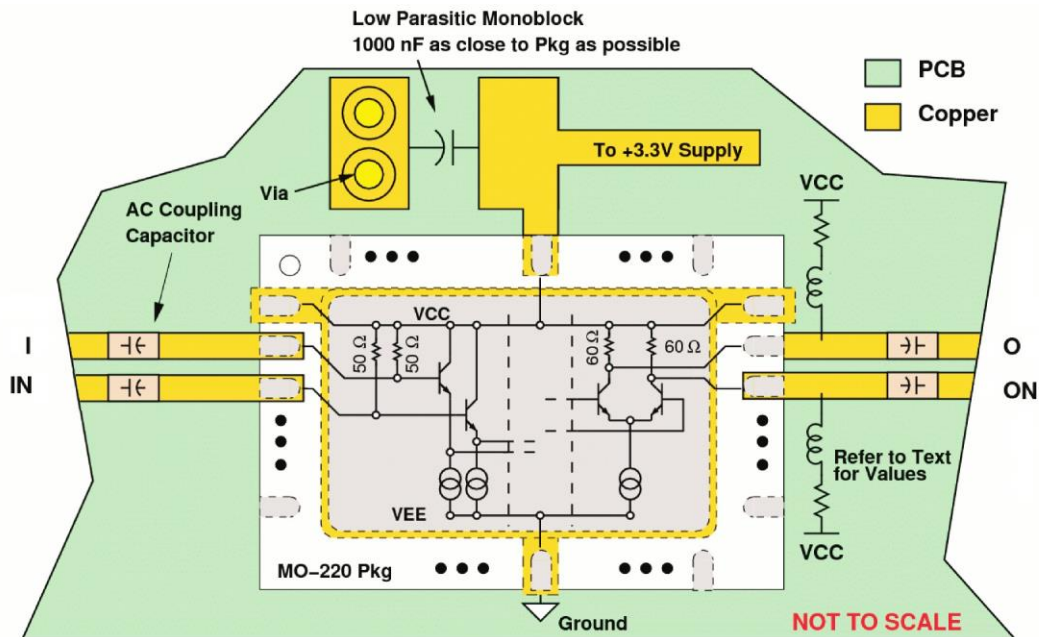
Biasing recommendations for negative supply with DC coupling applications

Negative Supply (AC Coupling)



Biasing recommendations for negative supply with AC coupling applications

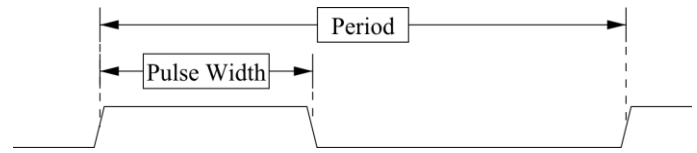
Positive Supply (AC Coupling)



Biasing recommendations for positive supply with AC coupling applications

Duty Cycle:

The SuperDivider duty cycle varies between 33% and 66% as a function of the divide ratio, N. When N is a power of 2, the duty cycle is exactly 50%. As N deviates from a power of 2, so does the duty cycle deviate from 50%. For example, N=64 has 50% duty cycle, N=60 has 47% duty cycle, and N=56 has 43% duty cycle. Equations 2 and 3 provide formulas for calculating pulse width and duty cycle as a function of N, for any integer N from 2 to (2³²-1). Table 5 shows the pulse width and duty cycle for N from 2 to 16, and duty cycle versus N is plotted below for N from 2 to 1024.


Table 6: Duty Cycle for N = 2 to 16

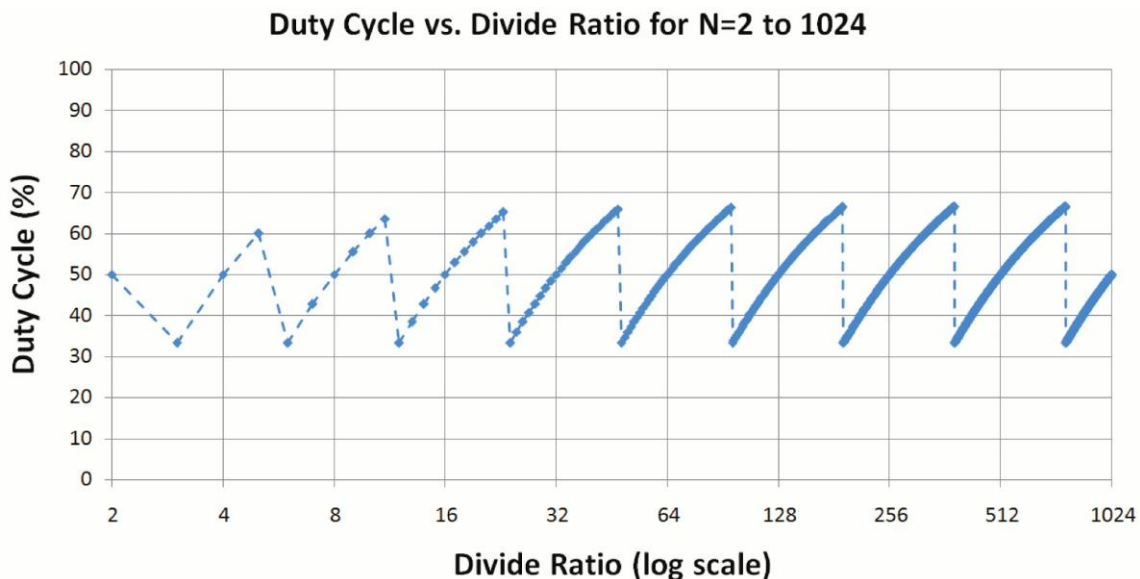
| Divide Ratio | Pulse Width (Input Cycles) | Duty Cycle (%) |
|--------------|----------------------------|----------------|
| 2 | 1 | 50 |
| 3 | 1 | 33 |
| 4 | 2 | 50 |
| 5 | 3 | 60 |
| 6 | 2 | 33 |
| 7 | 3 | 43 |
| 8 | 4 | 50 |
| 9 | 5 | 55 |
| 10 | 6 | 60 |
| 11 | 7 | 63 |
| 12 | 4 | 33 |
| 13 | 5 | 38 |
| 14 | 6 | 43 |
| 15 | 7 | 47 |
| 16 | 8 | 50 |

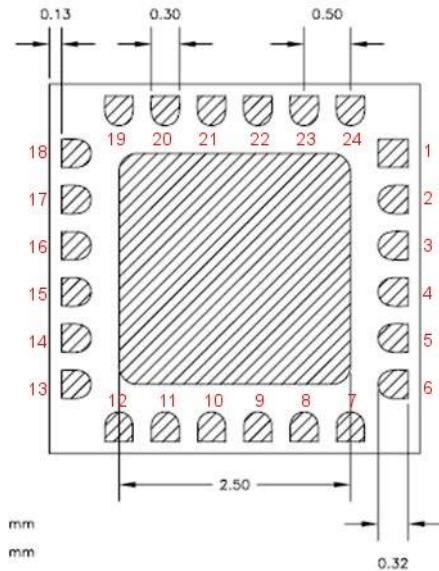
Equation 2:

$$\text{Pulse Width (input cycles)} = N - 2^{\text{floor}[\log_2(N/3) + 1]}$$

Equation 3:

$$\text{Duty Cycle (1\%)} = \frac{\text{Pulse Width}}{\text{Period}} \times 100\%$$



UXN14M32K Physical Characteristics


| | |
|---------------------|-----------------|
| Pkg size: | 4.00 x 4.00 mm |
| Pkg size tolerance: | +/- 0.25 mm |
| Pkg thickness: | 1.05 +/- 0.1 mm |
| Pad dimensions: | 0.30 x 0.35 mm |
| Center paddle: | 2.5 x 2.5 mm |
| JEDEC designator: | MO-220 |

Bottom View
Table 7: UXN14M32K Pin Assignment

| | Function | Notes |
|-------------------------|--------------------------|-------------------------------------------------|
| 1,7,9,18,22,23 (VEE) | Negative supply voltage | Nominally -3.3 V |
| 2,5,8,14,17,21,24 (VCC) | RF and DC ground | 0 V |
| 3 (INN) | Divider input | Negative terminal of differential input |
| 4 (INP) | Divider input | Positive terminal of differential input |
| 6 (RST) | Divider reset control | Defaults to logic 0, connect to VCC for logic 1 |
| 10 (DAT) | Serial input data | Defaults to logic 0, connect to VCC for logic 1 |
| 11 (CLK) | Serial input clock | Defaults to logic 0, connect to VCC for logic 1 |
| 12 (LE) | Load enable | Defaults to logic 0, connect to VCC for logic 1 |
| 13 (HLD) | Hold output control | Defaults to logic 0, connect to VCC for logic 1 |
| 15 (OUTP) | Divider output | Positive terminal of differential output |
| 16 (OUTN) | Divider output | Negative terminal of differential output |
| 19 (VADJ) | Output amplitude control | Tie to VCC for max swing, refer to text |
| 20 (TEMP) | Temperature diode | IC surface temperature, refer to text |
| Paddle | Package paddle | Tie to heatsink, refer to text |

Table 8: Absolute Maximum Ratings

| Parameter | Value | Unit |
|--------------------------|------------|------|
| Supply voltage (VEE) | -3.8 | V |
| RF input power (INP,INN) | 10 | dBm |
| Operating temperature | -40 to 85 | °C |
| Storage temperature | -85 to 125 | °C |
| Junction Temperature | 125 | °C |

Operation beyond the values listed under the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Operating Specifications is not implied. Prolonged use at the absolute maximum rating conditions may affect device reliability.

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