

High Speed, Dual MOSFET Driver

Features

- ▶ 10ns average rise and fall time with 1000pF load
- ▶ 2.0A peak output source/sink current
- ▶ 1.2V to 5.0V input CMOS compatible
- ▶ 4.5V to 13V total supply voltage
- ▶ Dual matched channels
- ▶ Reduced clock skew
- ▶ Low input capacitance
- ▶ Green packaging

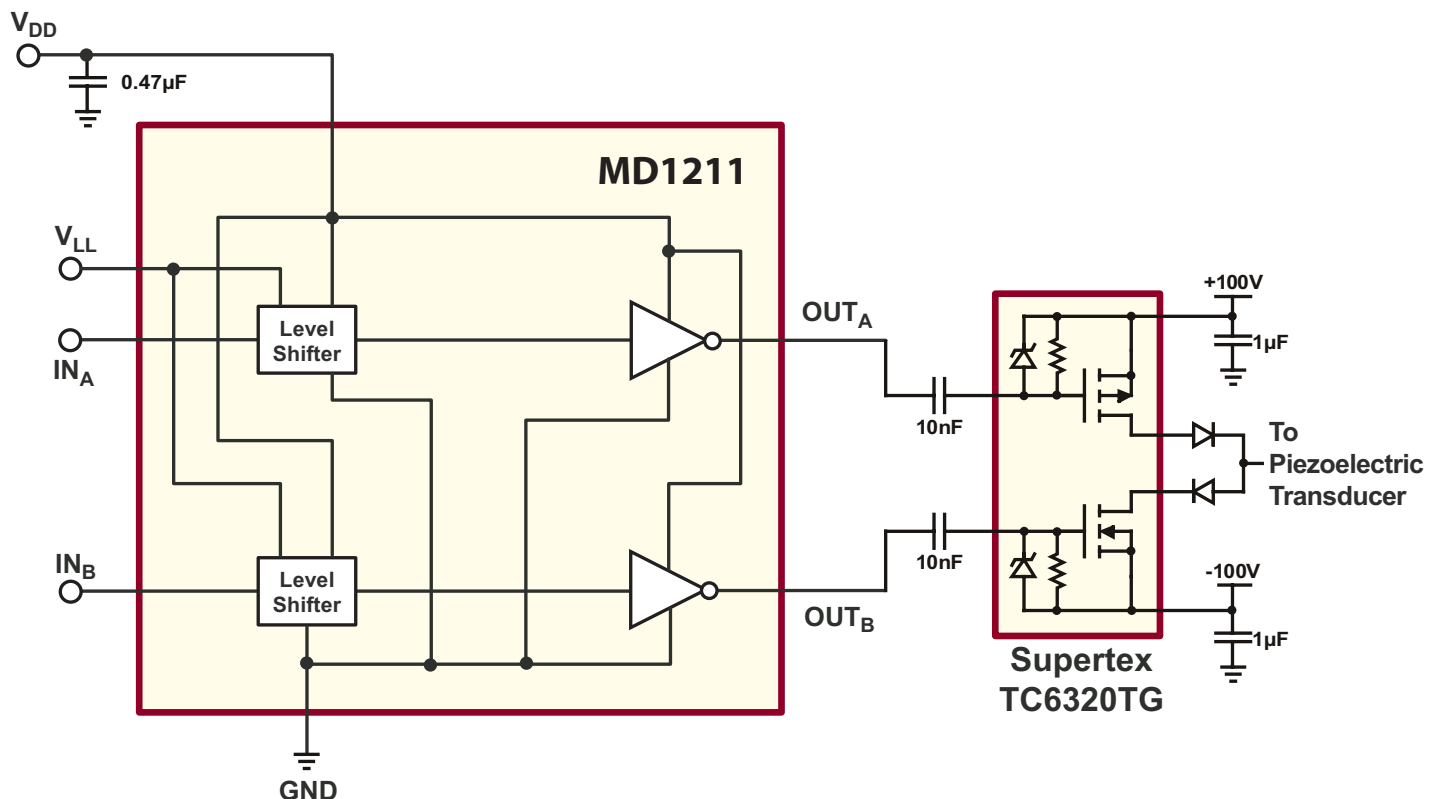
General Description

The Supertex MD1211 is a high speed, dual MOSFET driver. It is designed to drive high voltage N- and P-channel MOSFET transistors for medical ultrasound and other applications requiring a high output current for a capacitive load. The high-speed input stage of the MD1211 can operate from 1.2 to 5.0 volt logic interface with an optimum operating input signal range of 1.8 to 3.3 volts. The level translator uses a proprietary circuit, which provides DC coupling together with high-speed operation.

Applications

- ▶ Medical ultrasound imaging
- ▶ Piezoelectric transducer drivers
- ▶ Nondestructive evaluation
- ▶ PIN diode driver
- ▶ High speed level translator
- ▶ Clock/line drivers

Typical Application Circuit



Ordering Information

DEVICE	Package Option
	8-Pin SOIC
MD1211	MD1211LG-G



-G indicates package is RoHS compliant ("Green")

Absolute Maximum Ratings

Parameter	Value
Logic Supply Voltage	-0.5V to +5.5V
Main Supply Voltage	-0.5V to +13.5V
Logic Input Levels	-0.5V to $V_{LL} + 0.5V$
Maximum Junction Temperature	+125°C
Storage Temperature	-65°C to 150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

DC Electrical Characteristics

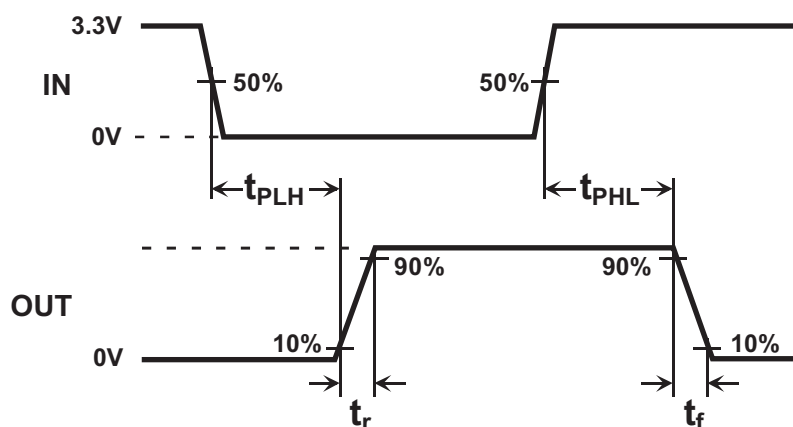
(Over operating conditions unless otherwise specified, $V_{DD} = 12V$, $T_J = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Main supply voltage	4.5	-	13	V	---
V_{LL}	Logic supply voltage	1.2	-	5.0	V	---
V_{IH}	Input logic voltage high	$V_{LL} - 0.3$	-	V_{LL}	V	For Logic Inputs IN_A and IN_B
V_{IL}	Input logic voltage low	0	-	0.8	V	
I_{IH}	Input logic current high	-	-	10	μA	
I_{IL}	Input logic current low	-	-	10	μA	
C_{IN}	Logic input capacitance	-	5.0	10	pF	
Outputs						
R_{SINK}	Output sink resistance	-	-	12	Ω	$I_{SINK} = 50mA$
R_{SOURCE}	Output source resistance	-	-	12	Ω	$I_{SOURCE} = 50mA$
I_{SINK}	Peak output sink current	-	2.0	-	A	---
I_{SOURCE}	Peak output source current	-	2.0	-	A	---

AC Electrical Characteristics

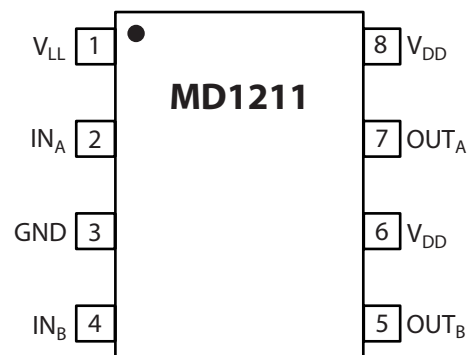
Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{PLH}	Propagation delay when output is from low to high	-	10	-	ns	$C_{LOAD} = 1000pF$, (see timing diagram) Input signal rise/fall time 2ns
t_{PHL}	Propagation delay when output is from high to low	-	10	-	ns	
t_r	Output rise time	-	10	-	ns	
t_f	Output fall time	-	10	-	ns	
$ t_r - t_f $	Rise and fall time matching	-	2.0	-	ns	For each channel
$ t_{PLH} - t_{PHL} $	Propagation low to high and high to low matching	-	2.0	-	ns	
Δt_{dm}	Propagation delay match	-	3.0	-	ns	Device to device delay match

Timing Diagram

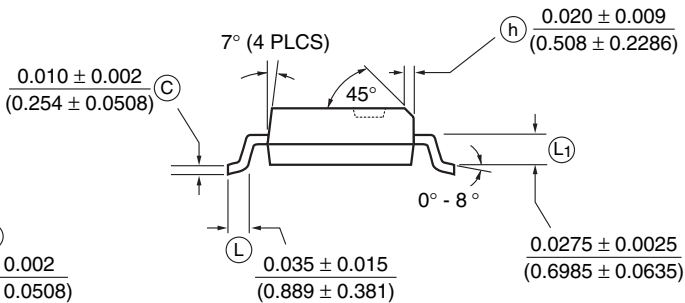
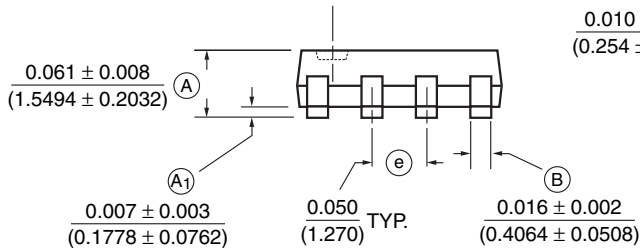
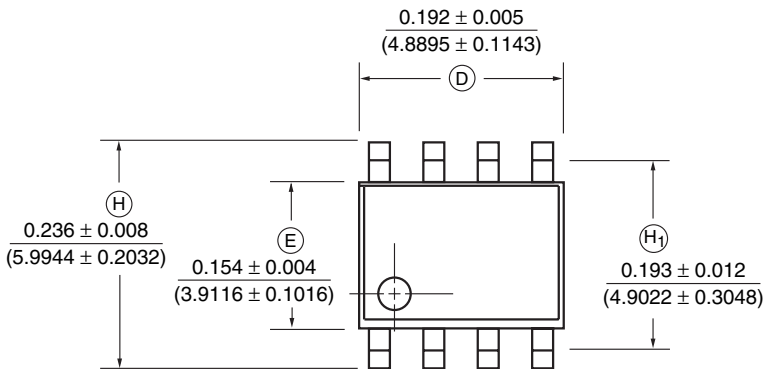


Pin Description

Pin #	Function	Description
1	V_{LL}	Logic supply voltage
2	IN_A	Logic input
3	GND	Device ground
4	IN_B	Logic input
5	OUT_B	Output driver
6	V_{DD}	Main supply voltage
7	OUT_A	Output driver
8	V_{DD}	Main supply voltage



8-LEAD SMALL OUTLINE PACKAGE (SOIC) (LG)



Note: Circle (e.g. (B)) indicates JEDEC Reference.

Measurement Legend = $\frac{\text{Dimensions in Inches}}{\text{(Dimensions in Millimeters)}}$

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