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Dual Common Drain N-Channel PowerTrench[®] MOSFET 20 V, 9.7 A, 16.5 m Ω

Features

- Max r_{S1S2(on)} = 16.5 mΩ at V_{GS} = 4.5 V, I_D = 8 A
- Max r_{S1S2(on)} = 18 mΩ at V_{GS} = 4.2 V, I_D = 7.4 A
- Max $r_{S1S2(on)}$ = 21 m Ω at V_{GS} = 3.1 V, I_D = 7 A
- Max $r_{S1S2(on)}$ = 24 m Ω at V_{GS} = 2.5 V, I_D = 6.7 A
- Low Profile 0.8 mm maximum in the new package MicroFET 2x3 mm
- HBM ESD protection level > 2 kV (Note 3)
- RoHS Compliant

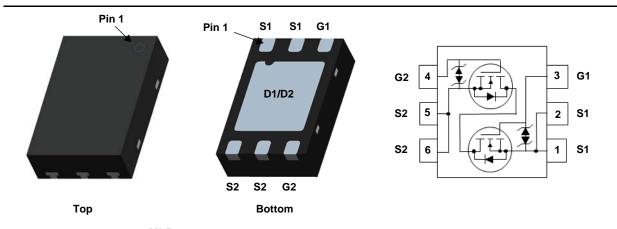


General Description

This device is designed specifically as a single package solution for Li-Ion battery pack protection circuit and other ultra-portable applications. It features two common drain N-channel MOSFETs, which enables bidirectional current flow, on Fairchild's advanced PowerTrench[®] process with state of the art MicroFET Leadframe, the FDMB2307NZ minimizes both PCB space and r_{S1S2(on)}.

Application

Li-Ion Battery Pack



MLP 2x3

MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
V _{S1S2}	Source1 to Source2 Voltage			20	V
V _{GS}	Gate to Source Voltage		(Note 4)	±12	V
	Source1 to Source2 Current -Continuous	T _A = 25°C	(Note 1a)	9.7	٨
I _{S1S2}	-Pulsed			40	— A
D	Power Dissipation	T _A = 25 °C	(Note 1a)	2.2	W
P _D	Power Dissipation	T _A = 25 °C	(Note 1b)	0.8	vv
T _J , T _{STG}	Operating and Storage Junction Temperature	Range		-55 to +150	°C

Thermal Characteristics

$R_{ ext{ heta}JA}$	Thermal Resistance, Junction to Ambient(Dual Operation)	(Note 1a)	57	°C/W	
$R_{ ext{ heta}JA}$	Thermal Resistance, Junction to Ambient(Dual Operation)	(Note 1b)	161	C/W	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
307	FDMB2307NZ	MLP 2x3	7"	8 mm	3000 units

FDMB2307NZ Dual Common Drain N-Channel PowerTrench®
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Common
Drain
N-Channel
PowerTrench
N [®] MOSFET

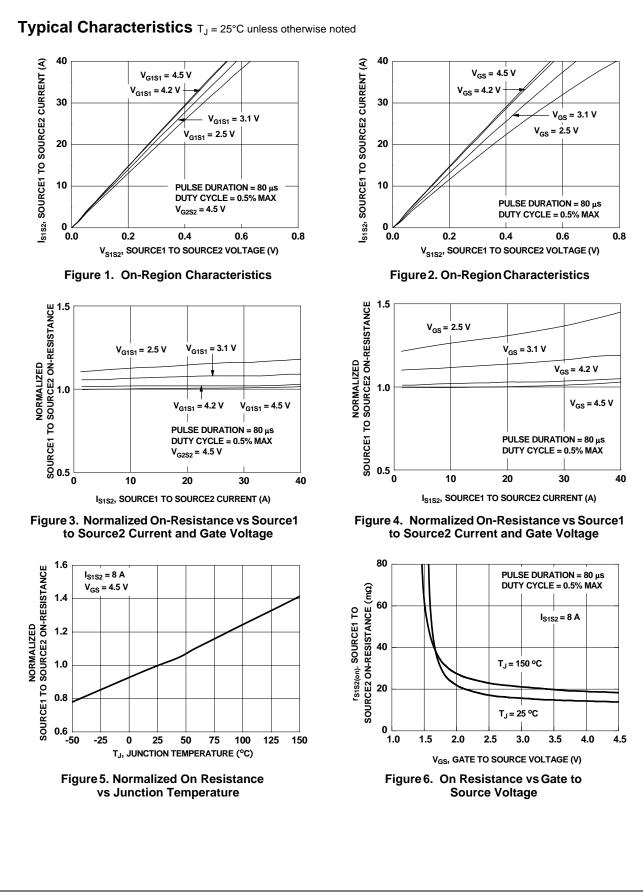
Symbol	Parameter	Test Condi	tions	Min	Тур	Max	Units		
Off Chara	cteristics								
I _{S1S2}	Zero Gate Voltage Source1 to Source2 Current	$V_{S1S2} = 16 \text{ V}, V_{GS} =$	0 V			1	μΑ		
I _{GSS}	Gate to Source Leakage Current	V _{GS} = 12 V, V _{S1S2} = 0	D V C			10	μA		
On Chara	cteristics								
		V - V I -	250 4	0.6	1	15	V		
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{S1S2}, I_{S1S2} =$		0.6	1	1.5	V		
		$V_{GS} = 4.5 \text{ V}, \ I_{S1S2} =$		10.5	13.5	16.5	-		
		$V_{GS} = 4.2 \text{ V}, \ I_{S1S2} =$		11	14	18	_		
r _{S1S2(on)}	Static Source1 to Source2 On Resistance	$V_{GS} = 3.1 \text{ V}, \ I_{S1S2} =$		11.5	16	21	mΩ		
0102(01)		$V_{GS} = 2.5 \text{ V}, \ I_{S1S2} =$		12	18	24	24		
		$V_{GS} = 4.5 \text{ V}, I_{S1S2} = T_J = 125 \text{ °C}$	8 A,	11	20	29			
9 _{FS}	Forward Transconductance	$V_{S1S2} = 5 V, I_{S1S2} =$	8 A		41		S		
	Ok energia tin tin a	5152 5 5152	-						
-	Characteristics				4700	00.40			
C _{iss}	Input Capacitance	V _{S1S2} = 10 V, V _{GS} = 0 V, f = 1 MHz			1760	2640	pF		
C _{oss}	Output Capacitance				229	345	pF		
C _{rss}	Reverse Transfer Capacitance				211	320	pF		
R _g	Gate Resistance (Note 5)		0.1	2.6	8	Ω		
Switching	g Characteristics								
t _{d(on)}	Turn-On Delay Time				12	22	ns		
t _r	Rise Time	V_{S1S2} = 10 V, I_{S1S2} = 8 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω			19	34	ns		
t _{d(off)}	Turn-Off Delay Time				32	51	ns		
t _f	Fall Time		t		9.5	17	ns		
, Q _g	Total Gate Charge	$V_{C1S1} = 0 V \text{ to } 5 V$	1		20	28	nC		
Q _g	Total Gate Charge	$V_{C1S1} = 0 V \text{ to } 4.5 V$	V _{S1S2} = 10V,		18	25	nC		
Q _{gs}	Gate1 to Source1 Charge	$V_{G1S1} = 0 V \text{ to } 5 V$ $V_{G1S1} = 0 V \text{ to } 4.5 V$	I _{S1S2} = 8 A,		2.8	-	nC		
Q _{gd}	Gate1 to Source2 "Miller" Charge	-	$V_{G2S2} = 0 V$		5.3		nC		
					0.0				
Source1-	Source2 Diode Characteristics								
I _{fss}	Maximum Continuous Source1-Source2 Die					8	A		
V _{fss}	Source1 to Source2 Diode Forward Voltage	$V_{G1S 1} = 0 V, V_{G2S2} = 4.5 V,$ $I_{fss} = 8 A$ (Note 2)			0.8	1.2	V		
NOTES: 1. R _{0JA} is determ the user's boa	ined with the device mounted on a 1 in ² pad 2 oz copper pad rd design. a. 57 °C/W when mounted or a 1 in ² pad of 2 oz copper		b. 16	i1 °C/W whe	ny design whil	on	termined b		

2. Pulse Test: Pulse Width < 300 $\mu s,$ Duty cycle < 2.0%.

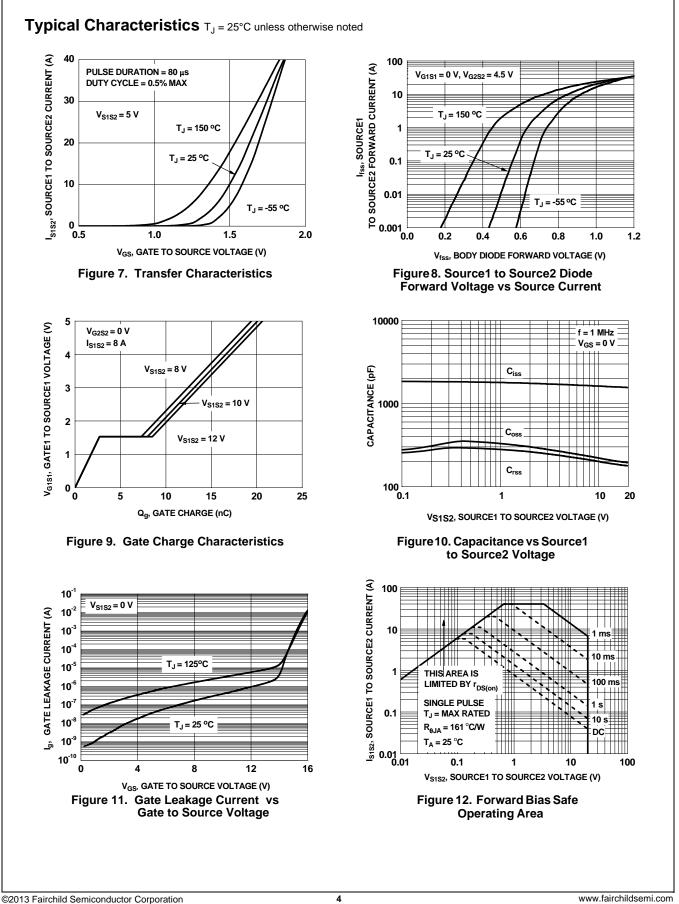
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

4. As an N-ch device, the negative Vgs rating is for low duty cycle pulse ocurrence only. No continuous rating is implied.

5. Rg is measured on 100% of the die at wafer level.



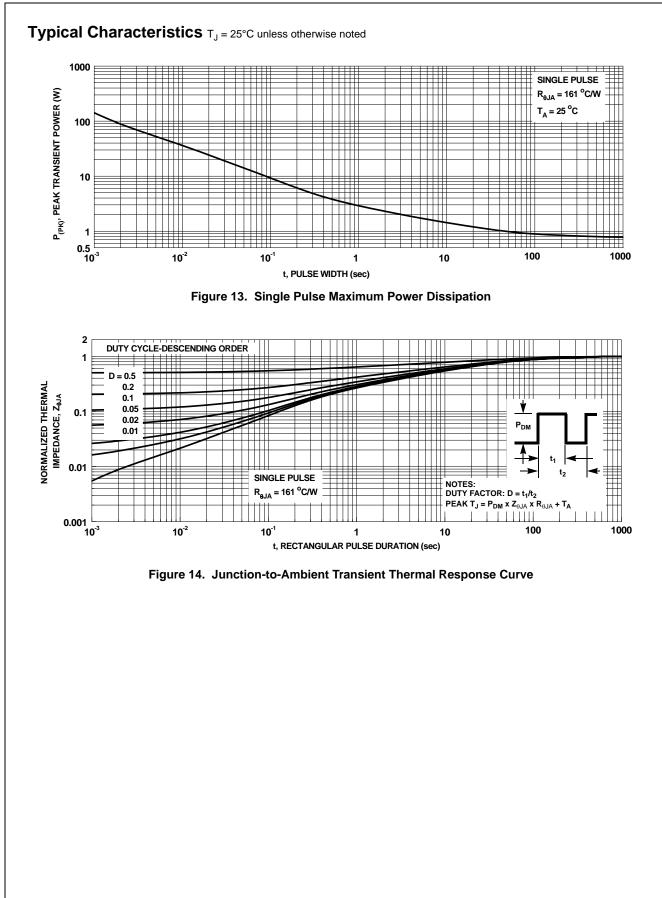
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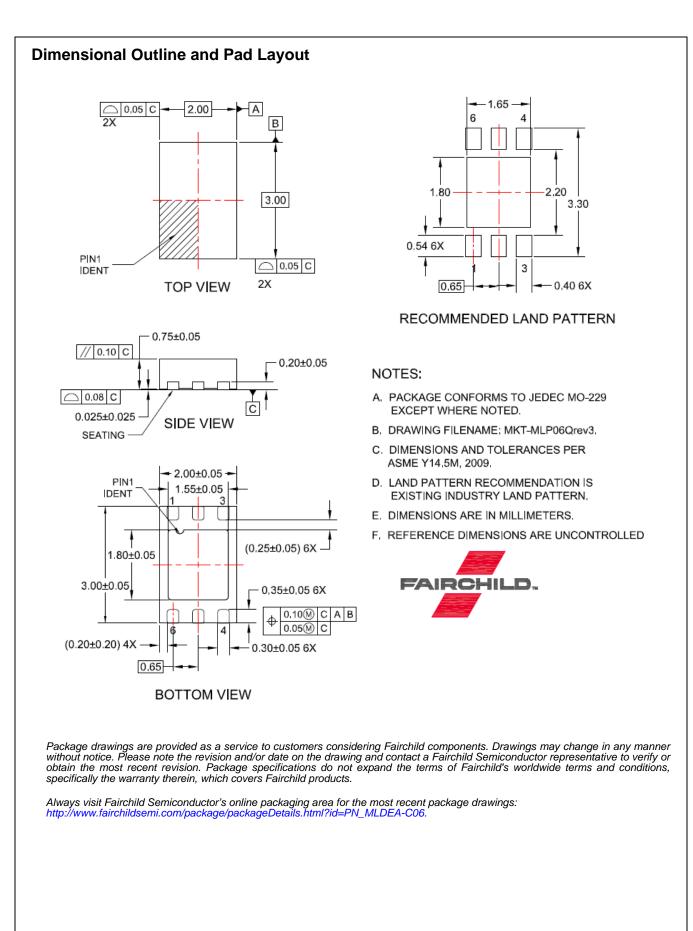


FDMB2307NZ Rev.C7

www.fairchildsemi.com

FDMB2307NZ Dual Common Drain N-Channel PowerTrench[®] MOSFET







No Identification Needed

Obsolete

Full Production

Not In Production

Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.

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