



SY88808L

10.3Gbps Transceiver with Programmable Equalization

General Description

The SY88808L high-speed transceiver is optimized for active copper cable assembly, backplane, and transmission line data-path management applications. The SY88808L is capable of equalizing serial data up to 10.3Gbps across up to 36 inches of FR4 or 10 meters of 26 AWG cable.

The SY88808L differential inputs can directly interface to any differential signal as small as 150mV_{PK}. Both channels of the transceiver have programmable EQ on the receiving end. The output of the transmitter can be programmed to provide an output swing from 100mV_{PK} to 350mV_{PK}. The output is optimized to drive into a 50Ω load.

The AnyLength equalization circuit in the receiver can be programmed to optimize the eye of the data signal received from 0" to 36" of FR4 or 0m to 10m of 26AWG cable. Unlike discrete EQ settings, patent-pending AnyLength EQ provides optimal results as well as saves power.

The SY88808L operates at 3.3V ±5% supply and its operation is guaranteed over the commercial temperature range of 0°C to +70°C. The SY88808L is part of Micrel's high-speed, Precision Edge[®] product line.

Datasheets and support documentation can be found on Micrel's web site at www.micrel.com.



Precision Edge[®]

Features

- Programmable equalizing network optimize incoming data pattern
- Equalization is optimized for any transmission length
- Receives up to 36" FR4 PCB trace, or 10m of cable
- 1Gbps through 10.3Gbps data rate throughput
- Flexible I/O:
 - AC-coupled inputs and outputs
 - 50Ω source-terminated CML outputs minimize round-trip reflections
 - Wide input voltage range: 150mV_{PK} to 350mV_{PK}
 - Output disable
- Input Loss-of-Signal
 - Hysteresis included
- 3.3V ±5% supply voltage
- 0°C to +70°C temperature range
- Available in 28-pin (4mm x 4mm) QFN package

Applications

- Active Copper Cable Assembly
- ATE, T&M backplane management
- Serial backplane management
- Combination FR4+cable+interconnect receiver
- Fibre Channel, Ethernet, SONET/SDH data transmission

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Paralink is a registered trademark of LEONI

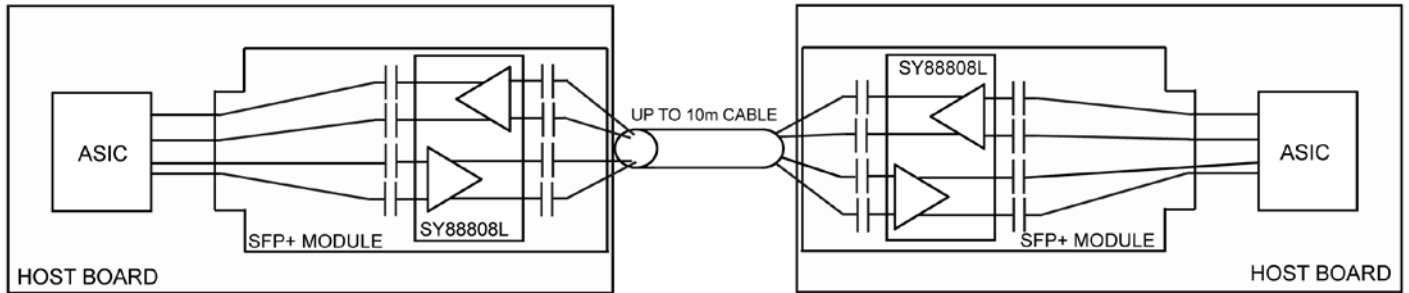
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June 2010

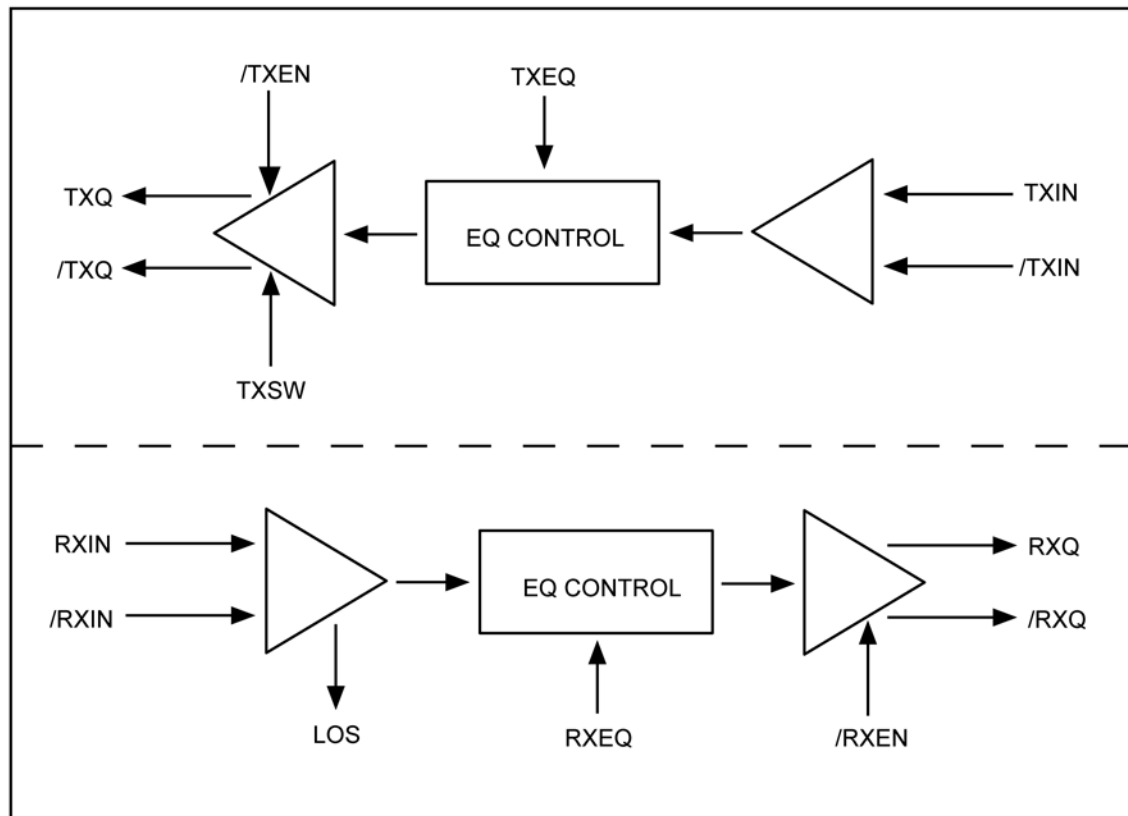
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hbwhelp@micrel.com or (408) 955-1690

Typical Application Circuit



Functional Block Diagram



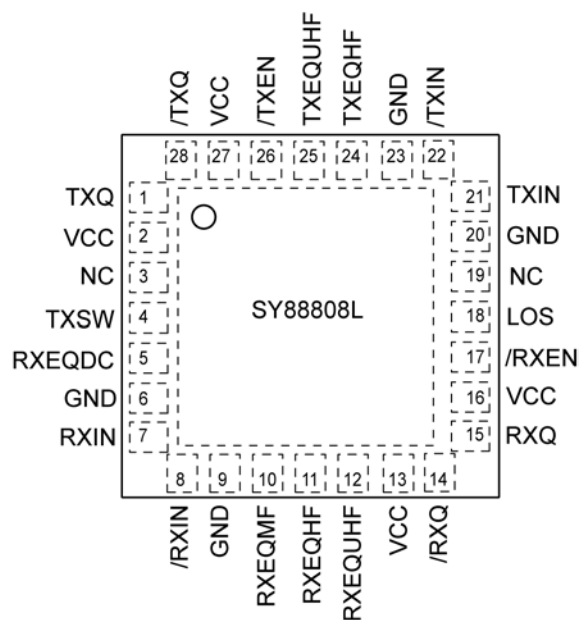
Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking
SY88808LMH	QFN-28	Commercial	SY88808L with Pb-Free Bar-Line Indicator
SY88808LMHTR ⁽²⁾	QFN-28	Commercial	SY88808L with Pb-Free Bar-Line Indicator

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC Electricals only.
2. Tape and Reel.

Pin Configuration



28-Pin QFN

Pin Description

Pin Number	Pin Name	Pin Function
1, 28	TXQ, /TXQ	Differential Transmitter Output: This CML output pair is designed to drive 50Ω signals with variable output swing.
2, 13, 16, 27	VCC	Positive power supply: Connect to 3.3V power supply. Bypass with 0.1μF 0.01μF low-ESR capacitors as close to VCC pins as possible.
3, 19	NC	No connect.
4	TXSW	Programmable Swing Input pin: This input pin allows the user to set variable output swing. This pin can be programmed via external potentiometer (or a resistor) to output a swing from 100mV _{PK} to 350mV _{PK} . See "Programmable TX Output Swing" table for details.
5, 10, 11, 12 24, 25	RXEQDC, RXEQMF, RXEQHF, RXEQUHF, TXEQHF, TXEQUHF	Programmable EQ: Equalization circuit can recover degraded signals after long traces of FR4 board. Equalization can be programmed via an external potentiometer (or resistor). This equalization scheme is optimized to recover degraded signal from any length of transmission line. The receiver of the RX channel can equalize up to 36" FR4 or 10m 26AWG cable. The receiver of the TX channel can equalize up to 9" FR4 or 3m 26AWG cable. RXEQDC, RXEQMF, RXEQHF, and RXEQUHF control DC, medium, high, and ultra high components of input data signals of RX channel respectively. TXEQHF and TXEQUHF control high and ultra high components of input data signals of TX channel respectively. See "Programmable Equalization" table for details.
6, 9, 20, 23	GND, Exposed Pad	Ground: Ground pins and exposed pad must be connected to the same ground plane.
7, 8	RXIN, /RXIN	Differential Receiver Input: This input pair is the differential input to the receive channel. It accepts differential AC-coupled signals as small as 150mV _{PK} at the input of the transmission line. The input signal is fed in to an equalization circuit. The loss-of-signal (LOS) level includes a small amount of hysteresis to prevent the LOS output from oscillating when no signal is present.
14, 15	/RXQ, RXQ	Differential Receiver Output: This CML output pair is designed to drive 250mV _{PK} swing in to 50Ω.
17, 26	/RXEN, /TXEN	Single-Ended Input: TTL/CMOS compatible control input for the output pairs. The disable pins are internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state (Disable) if left open. When disabled, the Q goes LOW, and /Q goes HIGH. Default threshold is V _{CC} /2.
18	LOS	Single-Ended Output: This TTL/CMOS output signal switches LOW when the input signal of the receiver channel is valid and switches HIGH when the input signal is not valid. LOS is an open-collector output.
21, 22	TXIN, /TXIN	Differential Transmitter Input: This input pair is the differential input to the transmit channel and accepts differential AC-coupled signals which are fed in to equalization circuit. Input swing is recommended to be ≥150mV _{PK} at the input of the transmission line to ensure valid outputs.

TX Output Swing Table

Output Swing (mV _{PK})	100	250	350
TXSW (Ω)	open	27	13

RX Channel Programmable Equalization Table

Transmission Medium	FR4 ⁽¹⁾				Cable ⁽²⁾
Length	36"	24"	18"	9"	10m
RXEQDC (Ω)	95	45	35	25	60
RXEQMF (Ω)	305	330	215	230	330
RXEQHF (Ω)	180	195	290	1120	0
RXEQUHF (Ω)	50	105	260	850	0

TX Channel Programmable Equalization Table

Transmission Medium	FR4 ⁽¹⁾	
Length	9"	0"
TXEQHF(Ω)	1k	1M
TXEQUHF (Ω)	1M	1M

Notes:

- 6mil wide 6.25mil thick strip line traces on FR4i room temperature; 1010 clock pattern and PRBS-23 data pattern.
- 26 AWG, 10m LEONI Paralink® 11 cable, L45468-J14-C245; 1010 clock pattern and PRBS-23 data pattern.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{CC}) -0.5V to +4.0V
 Input Voltage (V_{IN}) -0.5V to V_{CC}
 CML Output Voltage (V_{OUT}) $V_{CC}-1.0V$ to $V_{CC}+0.5V$
 Input Current
 Source or Sink Current on (IN, /IN) $\pm 50mA$
 Maximum Operating Junction Temperature +125°C
 Lead Temperature (soldering, 20sec.) +260°C
 Storage Temperature (T_s) -65°C to +150 °C

Operating Ratings⁽²⁾

Supply Voltage (V_{IN}) +3.14V to +3.46V
 Ambient Temperature (T_A) 0°C to +70°C
 Package Thermal Resistance⁽³⁾
 QFN (θ_{JA})
 Still-Air 61°C/W
 QFN (ψ_{JB})
 Junction-to-Board 30°C/W

Electrical Characteristics⁽⁴⁾

$V_{CC} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to +70°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power Supply		3.14	3.3	3.46	V
I_{EE}	Power Supply Current	Maximum V_{CC} , includes 50 Ω internal source resistors, no external load current, maximum EQ settings.		180	235	mA
	Power	Includes 50 Ω internal source resistors, no external load current, maximum EQ settings.		594	814	mW
R_{DIFF_IN}	Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IN}	Input Voltage Swing	RXIN, TXIN (Note 5)	150		350	mV _{PK}
V_{DIFF_IN}	Differential Input Voltage Swing IN-/IN		300		700	mV _{PP}
LOS	Loss-of-Signal Levels	LOS De-Assert (Note 6)		75	90	mV _{PK}
		LOS Assert (Note 6)	45	55		
	Hysteresis			3		dB

Outputs DC Electrical Characteristics⁽⁵⁾

$V_{CC} = 3.3V \pm 5\%$; $V_{EE} = 0V$; $T_A = 0^\circ C$ to + 70°C; $R_L = 100\Omega$ across output pair; unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{SWING}	Output Swing	RXOUT	200	250	300	mV _{PK}
		TXOUT, Programmable Swing	100		350	
R_{OUT}	Output Resistance		45	50	55	Ω

LVTTTL/CMOS DC Electrical Characteristics⁽⁷⁾

$V_{CC} = +3.3V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input HIGH Voltage		2			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		-125		30	μA
I_{IL}	Input LOW Current		-300			μA

AC Electrical Characteristics⁽⁸⁾

$V_{CC} = 3.3V \pm 5\%$; $V_{EE} = 0V$; $T_A = 0^\circ C$ to $+70^\circ C$; $R_L = 100\Omega$ across output pair; unless otherwise stated.

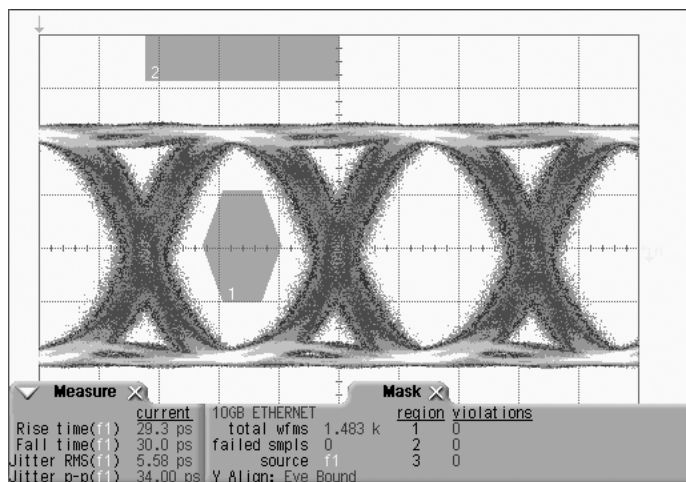
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
FREQ	Data Rate Throughput	NRZ Data	1		10.3	Gbps
t_{pd}	Differential Propagation Delay	RXIN-to-RXQ	150	250	450	ps
		TXIN-to-TXQ	150	250	450	
t_{SKEW}	Part-to-Part Skew	Note 9			200	ps
t_{EN}	TXQ Enable/Disable Time	/TXEN		450	600	ps
	RXQ Enable/Disable Time	/RXEN		450	600	
t_{JITTER}	Deterministic Jitter (DJ)	Note 10			10	ps _{pp}
	Total Jitter (TJ)	Note 11			20	
LOS_{DELAY}	LOS Delay	t_{los_on} and t_{los_off} (see Figure 1)			100	μs
t_r, t_f	Output Rise/Fall Time (20% to 80%)	At Full Output Swing	20	30	60	ps

Notes:

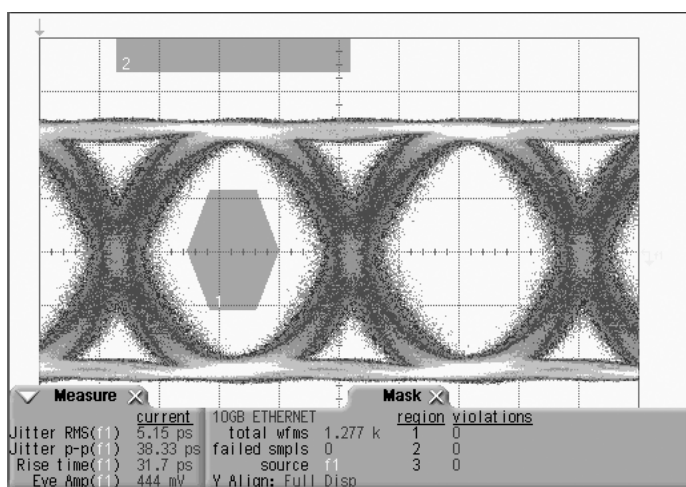
1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JA} and Ψ_{JB} values are determined for a 4-layer board in still air unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. $T_J \leq 125^\circ C$.
5. Measured at input of the transmission line.
6. Measured with 101010 pattern at 10.3Gbps.
7. The circuit is designed to meet the DC specifications, shown in the above table, after thermal equilibrium has been established. $T_J \leq 125^\circ C$.
8. High-frequency AC-parameters are guaranteed by design and characterization.
9. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
10. Deterministic jitter is measured with $2^{11}-1$ PRBS pattern at 10.3Gbps.
11. Total jitter is measured with $2^{11}-1$ PRBS pattern at 10.3Gbps.

Typical Operating Characteristics

$V_{CC} = 3.3V \pm 5\%$; $V_{IN} = 350mV$; $T_A = 25^\circ C$, $R_L = 100\Omega$ across output pair, unless otherwise stated.

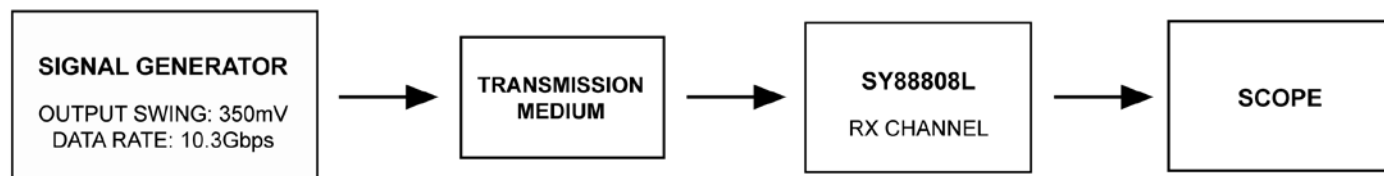


Transmission Medium: 36in FR4



Transmission Medium: 10m, 26AWG Cable

Test Set-Up



Timing Diagram

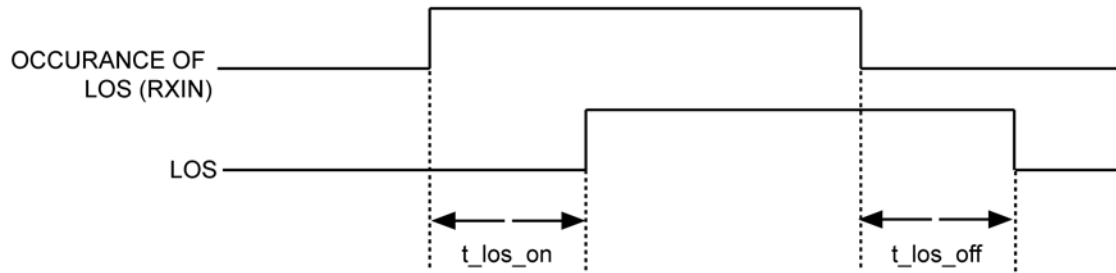


Figure 1. LOS Delay

Output Interface Applications

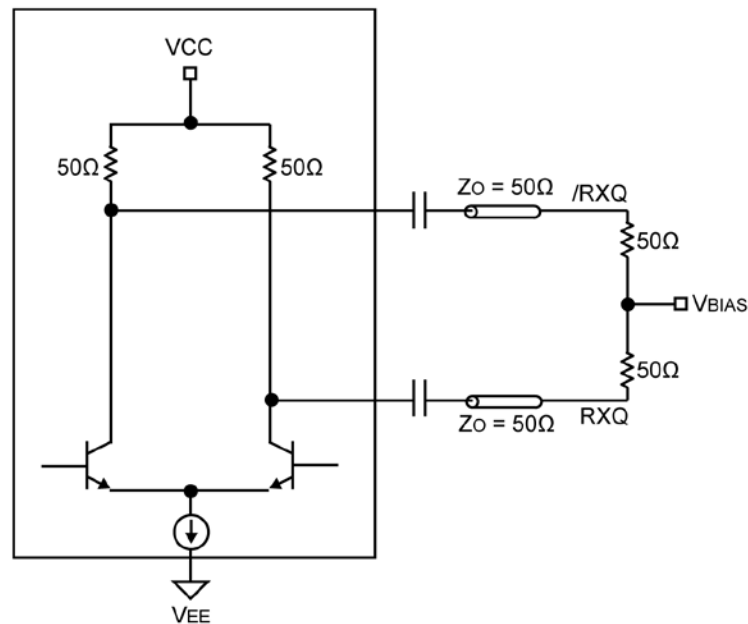
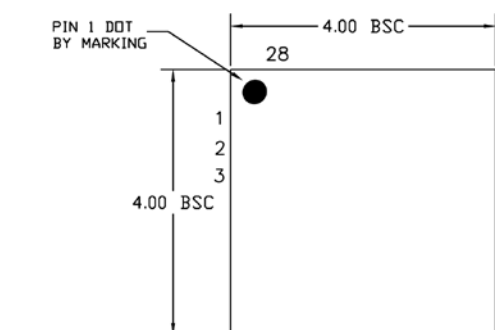


Figure 2. CML AC-Coupled Termination

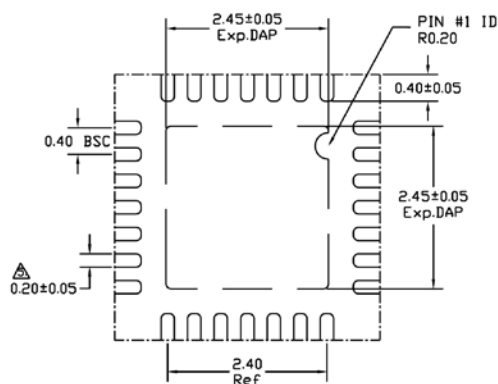
Related Product and Support Information

Part Number	Function	Data Sheet Link
SY56216R	6.4Gbps, Low-Voltage CML Dual Channel EQ Buffer	www.micrel.com/_PDF/HBW/sy56216r.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

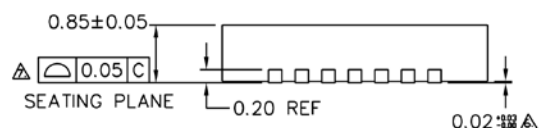
Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.08 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.

28-Pin QFN

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