Dual Hot Swap Controllers

FEATURES

- **Allows Safe Board Insertion and Removal from a Live Backplane**
- **Programmable Electronic Circuit Breaker**
- **FAULT Output Indication**
- Programmable Supply Voltage Power-Up Rate
- High Side Drive for External MOSFET Switches
- Controls Supply Voltages from 2.7V to 16.5V
- Undervoltage Lockout

APPLICATIONS

- Hot Board Insertion
- Electronic Circuit Breaker
- Portable Computer Device Bays
- Hot Plug Disk Drive

DESCRIPTION

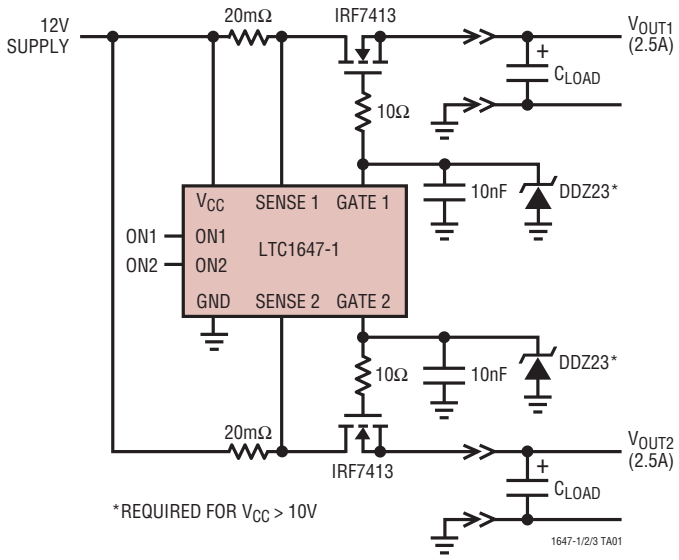
The LTC®1647-1/LTC1647-2/LTC1647-3 are dual Hot Swap™ controllers that permit a board to be safely inserted and removed from a live backplane.

Using external N-channel MOSFETs, the board supply voltages can be ramped up at a programmable rate. A high side switch driver controls the MOSFET gates for supply voltages ranging from 2.7V to 16.5V. A programmable electronic circuit breaker protects against overloads and shorts. The ON pins are used to control board power or clear a fault.

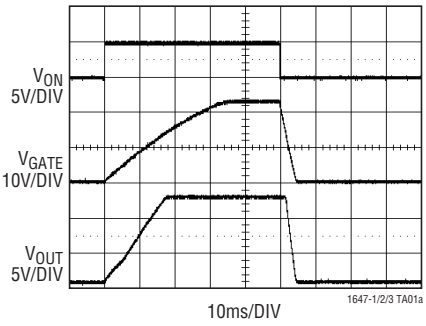
The LTC1647-1 is a dual Hot Swap controller with a common V_{CC} pin, separate ON pins and is available in an SO-8 package. The LTC1647-2 is similar to the LTC1647-1 but combines a fault status flag with automatic retry at the ON pins and is also available in the SO-8 package. The LTC1647-3 has individual V_{CC} pins, ON pins and $\overline{FAULT}$ status pins for each channel and is available in a 16-lead narrow SSOP package.

TYPICAL APPLICATION

Dual Motherboard Resident Hot Swap Controller



ON/OFF Sequence



ABSOLUTE MAXIMUM RATINGS

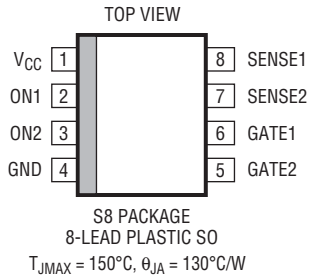
(Note 1)

Supply Voltage (V_{CC}) 17V
Input Voltage (SENSE) ..... –0.3V to (V_{CC} + 0.3V)
Input Voltage (ON) ..... –0.3V to 17V
Output Voltage ($\overline{FAULT}$) ..... –0.3V to 17V
Output Voltage (GATE) ..... Internally Limited (Note 3)

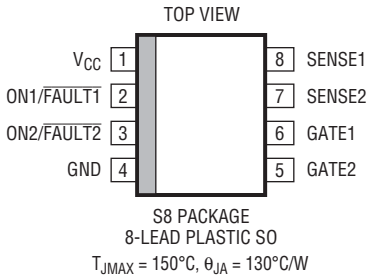
PIN CONFIGURATION

Operating Temperature Range
C-Grade ..... 0°C to 70°C
I-Grade ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

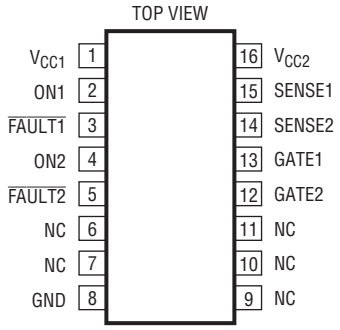
PIN CONFIGURATION



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 130°C/W



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 130°C/W



GN PACKAGE
16-LEAD PLASTIC SSOP
T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1647-1CS8#PBF	LTC1647-1CS8#TRPBF	16471	8-Lead (4mm × 3mm) Plastic SO	0°C to 70°C
LTC1647-1IS8#PBF	LTC1647-1IS8#TRPBF	16471I	8-Lead (4mm × 3mm) Plastic SO	–40°C to 85°C
LTC1647-2CS8#PBF	LTC1647-2CS8#TRPBF	16472	8-Lead (4mm × 3mm) Plastic SO	0°C to 70°C
LTC1647-2IS8#PBF	LTC1647-2IS8#TRPBF	16472I	8-Lead (4mm × 3mm) Plastic SO	–40°C to 85°C
LTC1647-3CGN#PBF	LTC1647-3CGN#TRPBF	16473	16-Lead Plastic SSOP	0°C to 70°C
LTC1647-3IGN#PBF	LTC1647-3IGN#TRPBF	16473I	16-Lead Plastic SSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	V_{CCX} Supply Range	Operating Range	●	2.7		16.5	V
I_{CC}	V_{CC} Supply Current (Note 4)	ON1, ON2 = V_{CC1} = V_{CC2}, I_{CC} = I_{CC1} + I_{CC2}	●		1.0	6	mA
I_{CCX}	V_{CCX} Supply Current (Note 5, LTC1647-3)	ONX = V_{CCX}, I_{CCX} Individually Measured, V_{CC1} = 5V, V_{CC2} = 12V or V_{CC1} = 12V, V_{CC2} = 5V	●		0.5	5	mA
V_{LKO}	V_{CCX} Undervoltage Lockout	Coming Out of UVLO (Rising V_{CCX})	●	2.30	2.45	2.60	V
V_{LKH}	V_{CCX} Undervoltage Lockout Hysteresis				210		mV
V_{CB}	Circuit Breaker Trip Voltage	V_{CB} = V_{CCX} – V_{SENSEX}	●	40	50	60	mV
I_{CP}	GATEX Output Current	ONX High, $\overline{FAULTX}$ High, V_{GATE} = GND (Sourcing) ONX Low, $\overline{FAULTX}$ High, V_{GATE} = V_{CC} (Sinking) ONX High, $\overline{FAULTX}$ Low, V_{GATE} = 15V (Sinking)	●	6	10 50 50	14	µA µA mA
ΔV_{GATE}	External MOSFET Gate Drive	(V_{GATE} – V_{CC}), V_{CC1} = V_{CC2} = 5V (V_{GATE} – V_{CC}), V_{CC1} = V_{CC2} = 12V	● ●	10 10	13 15	17 19	V V
V_{ONHI}	ONX Threshold High		●	1.20	1.29	1.38	V
V_{ONLO}	ONX Threshold Low		●	1.17	1.21	1.25	V
V_{ONHYST}	ONX Hysteresis				70		mV
I_{IN}	ONX Input Current	ON = GND or V_{CC}	●		±1	±10	µA
V_{OL}	$\overline{FAULTX}$ Output Low Voltage (LTC1647-2, LTC1647-3)	I_O = 1mA, V_{CC} = 5V I_O = 5mA, V_{CC} = 5V	●		 0.8	0.4	V V
I_{LEAK}	$\overline{FAULTX}$ Output Leakage Current (LTC1647-3)	No Fault, $\overline{FAULTX}$ = V_{CC} = 5V			±1	±10	µA
t_{FAULT}	Circuit Breaker Delay Time	V_{CCX} – V_{SENSEX} = 0 to 100mV			0.3		µs
t_{RESET}	Circuit Breaker Reset Time	ONX High to Low, to $\overline{FAULTX}$ High	●		50	100	µs
t_{ON}	Turn-On Time	ONX Low to High, to GATEX On			2		µs
t_{OFF}	Turn-Off Time	ONX High to Low, to GATEX Off			1		µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 3: An internal Zener on the GATE pins clamp the charge pump voltage to a typical maximum operating voltage of 28V. External overdrive of the GATE pin beyond the internal Zener voltage may damage the device. The GATE capacitance must be <0.15µF at maximum V_{CC}. If a lower GATE pin clamp voltage is desired, use an external Zener diode.

Note 4: The total supply current I_{CC} is measured with V_{CC1} and V_{CC2} connected internally (LTC1647-1, LTC1647-2) or externally (LTC1647-3).

Note 5: The individual supply current I_{CCX} is measured on the LTC1647-3. The lower of the two supplies, V_{CC1} and V_{CC2}, will have its channel's current. The higher supply will carry the additional supply current of the charge pump and the bias generator beside its channel's current.

PIN TABLES

LTC1647-1 Pinout

PIN	DESCRIPTION
1	V_{CC}
2	ON1
3	ON2
4	GND

PIN	DESCRIPTION
5	GATE2
6	GATE1
7	SENSE2
8	SENSE1

LTC1647-1 Does Not Have the FAULT Status Feature.

LTC1647-2 Pinout

PIN	DESCRIPTION
1	V_{CC}
2	ON1 and $\overline{\text{FAULT1}}$ (Internally Tied Together)
3	ON1 and $\overline{\text{FAULT2}}$ (Internally Tied Together)
4	GND

PIN	DESCRIPTION
5	GATE2
6	GATE1
7	SENSE2
8	SENSE1

The ONX/$\overline{\text{FAULTX}}$ must be connected to a driver via a resistor if the autoretry feature is being used.

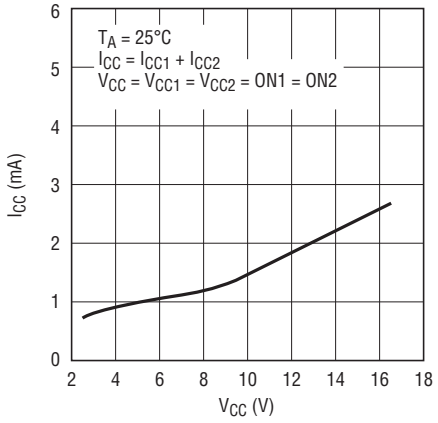
LTC1647-3 Pinout

PIN	DESCRIPTION
1	V_{CC}
2	ON1
3	$\overline{\text{FAULT1}}$
4	ON2
5	$\overline{\text{FAULT2}}$
6	NC
7	NC
8	GND

PIN	DESCRIPTION
9	NC
10	NC
11	NC
12	GATE2
13	GATE1
14	SENSE2
15	SENSE1
16	V_{CC2}

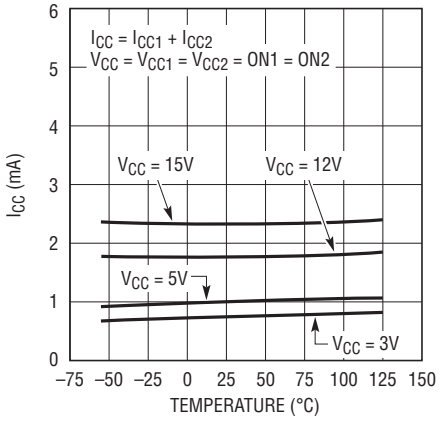
TYPICAL PERFORMANCE CHARACTERISTICS

I_{CC} vs V_{CC}



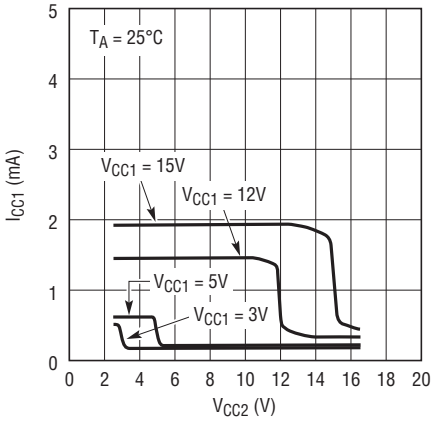
1647-1/2/3 G01

I_{CC} vs Temperature



1647-1/2/3 G02

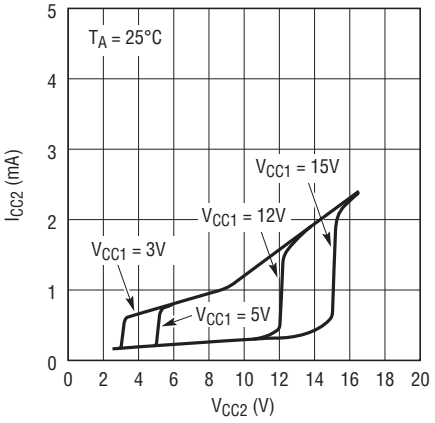
I_{CC1} vs V_{CC2}



1647-1/2/3 G03

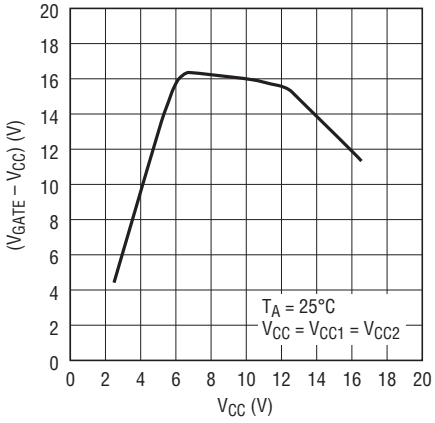
TYPICAL PERFORMANCE CHARACTERISTICS

I_{CC2} vs V_{CC2}



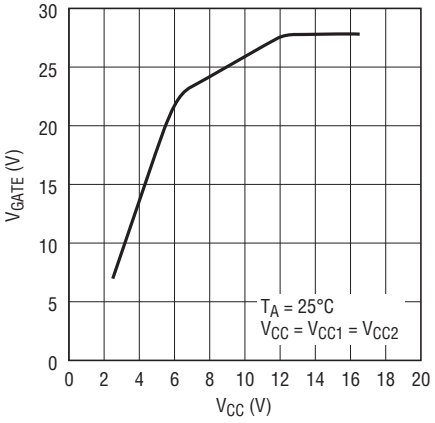
1647-1/2/3 G04

(V_{GATE} – V_{CC}) vs V_{CC}



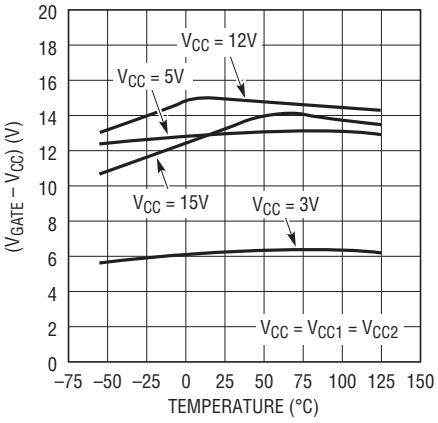
1647-1/2/3 G05

V_{GATE} vs V_{CC}



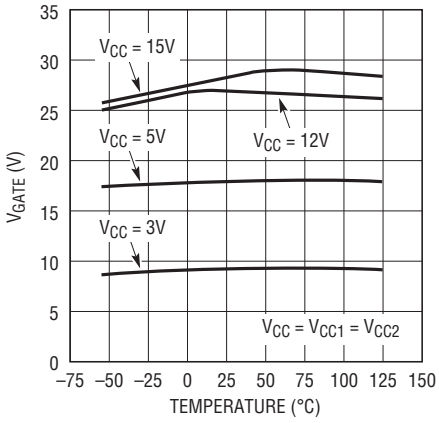
1647-1/2/3 G06

(V_{GATE} – V_{CC}) vs Temperature



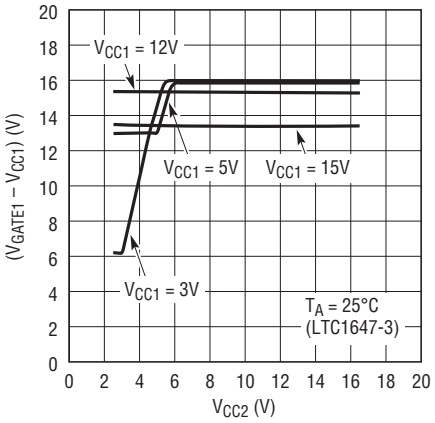
1647-1/2/3 G07

V_{GATE} vs Temperature



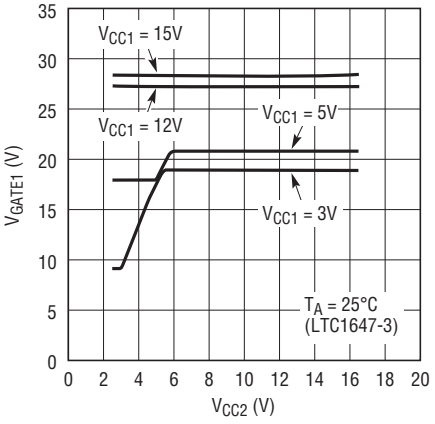
1647-1/2/3 G08

(V_{GATE1} – V_{CC1}) vs Temperature



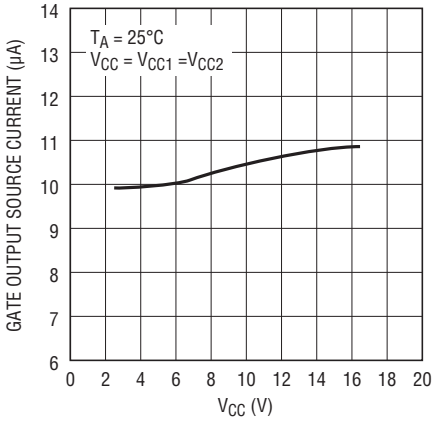
1647-1/2/3 G09

V_{GATE1} vs V_{CC2}



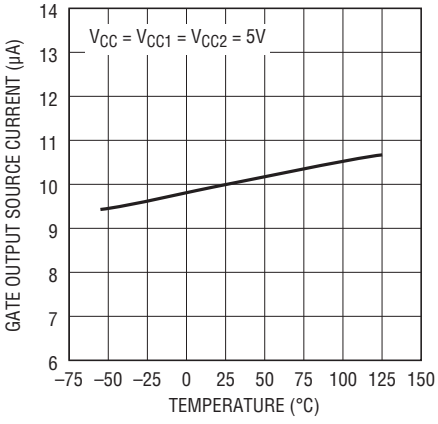
1647-1/2/3 G10

GATE Output Source Current vs V_{CC}



1647-1/2/3 G11

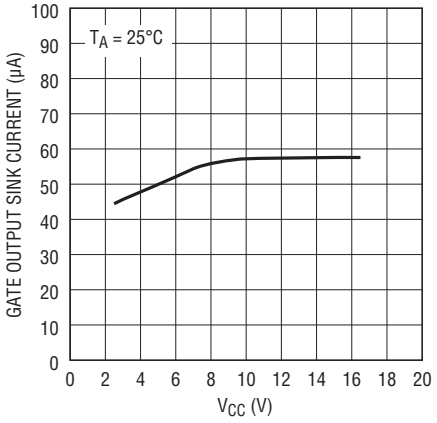
GATE Output Source Current vs Temperature



1647-1/2/3 G12

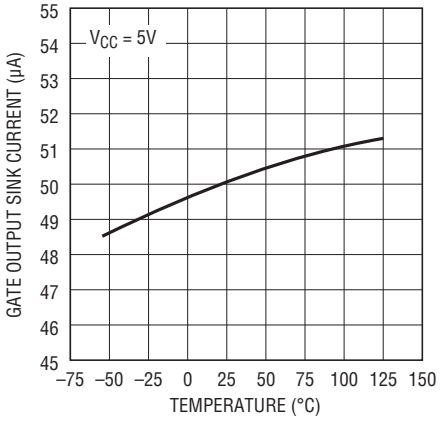
TYPICAL PERFORMANCE CHARACTERISTICS

GATE Output Sink Current vs V_{CC}



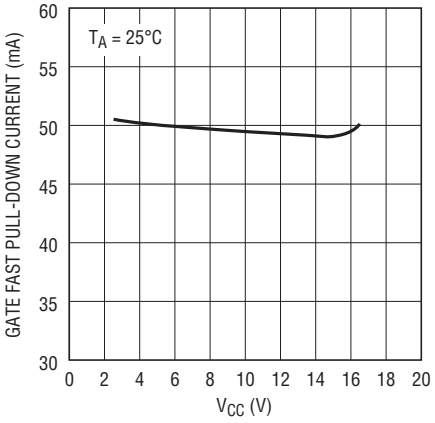
1647-1/2/3 G13

GATE Output Sink Current vs Temperature



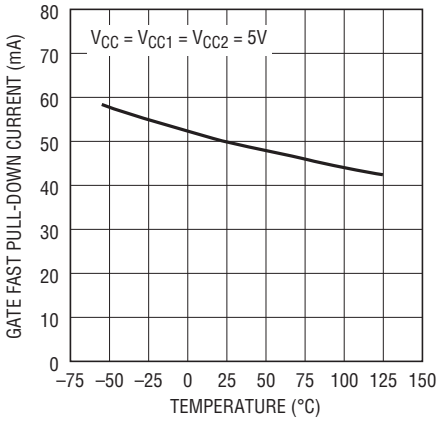
1647-1/2/3 G14

GATE Fast Pull-Down Current vs V_{CC}



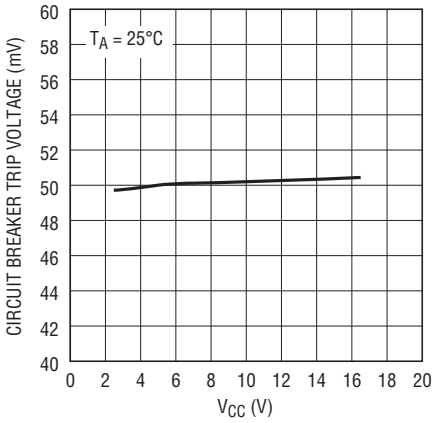
1647-1/2/3 G15

GATE Fast Pull-Down Current vs Temperature



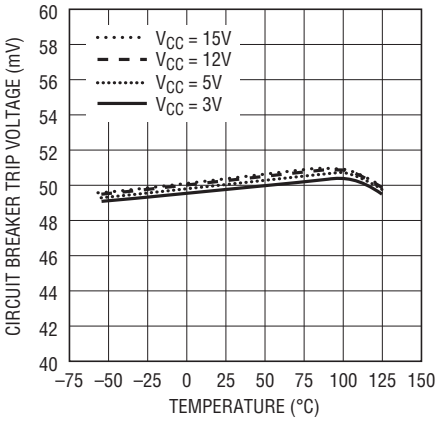
1647-1/2/3 G16

Circuit Breaker Trip Voltage vs V_{CC}



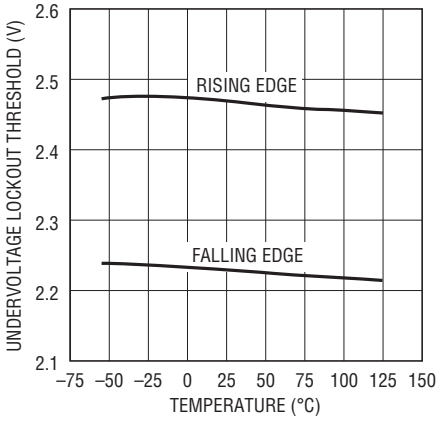
1647-1/2/3 G17

Circuit Breaker Trip Voltage vs Temperature



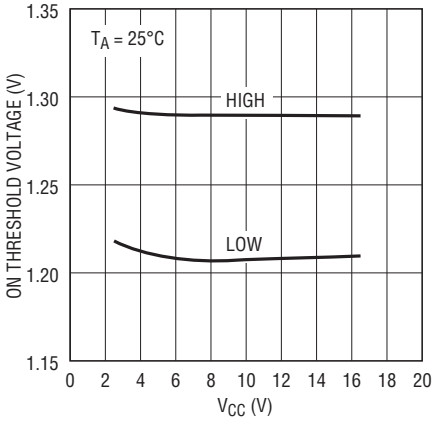
1647-1/2/3 G18

Undervoltage Lockout Threshold vs Temperature



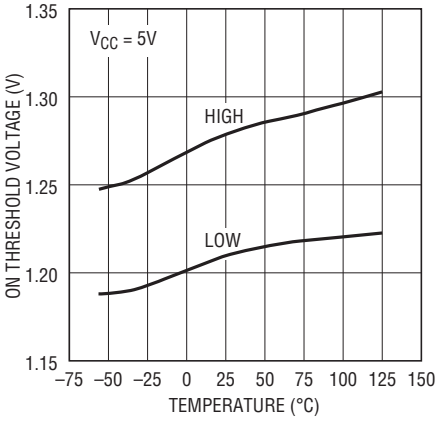
1647-1/2/3 G19

ON Threshold Voltage vs V_{CC}



1647-1/2/3 G20

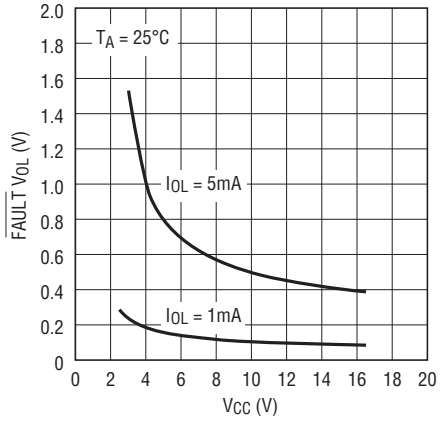
ON Threshold Voltage vs Temperature



1647-1/2/3 G21

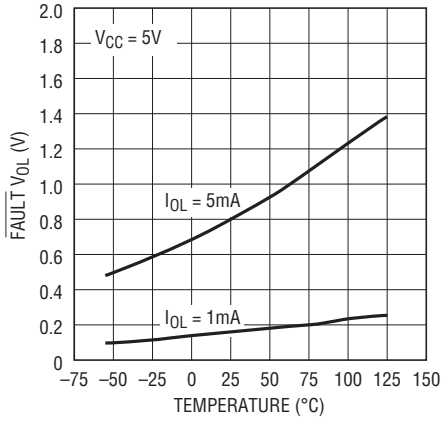
TYPICAL PERFORMANCE CHARACTERISTICS

$\overline{FAULT}$ V_{OL} vs V_{CC}



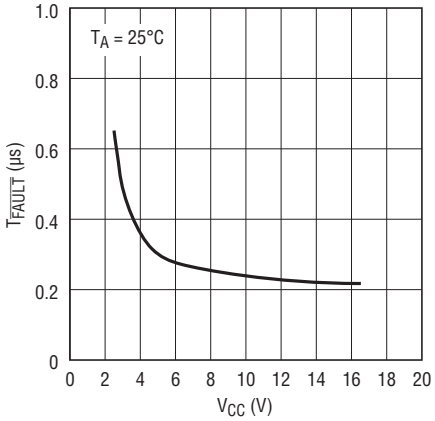
1647-1/2/3 G22

$\overline{FAULT}$ V_{OL} vs Temperature



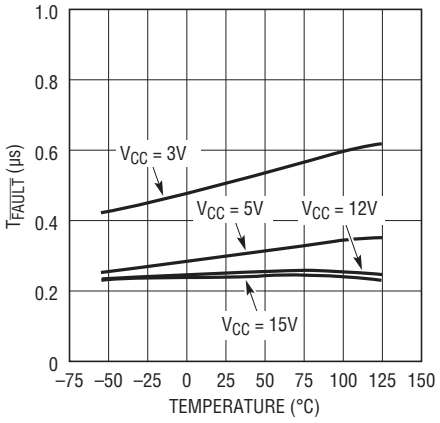
1647-1/2/3 G23

t_{FAULT} vs V_{CC}



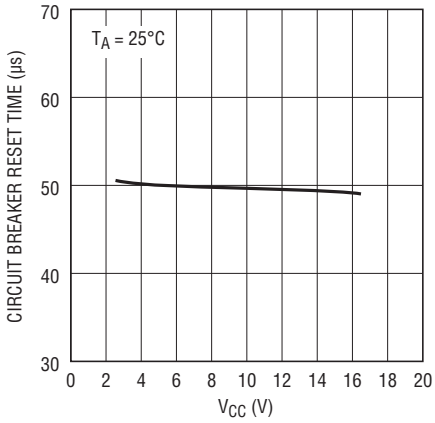
1647-1/2/3 G24

t_{FAULT} vs Temperature



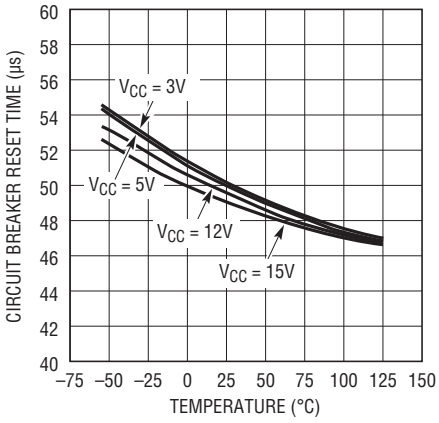
1647-1/2/3 G25

Circuit Breaker Reset Time vs V_{CC}



1647-1/2/3 G26

Circuit Breaker Reset Time vs Temperature



1647-1/2/3 G27

PIN FUNCTIONS

V_{CC1} (LTC1647-3): Channel 1 Positive Supply Input. The supply range for normal operation is 2.7V to 16.5V. The supply current, I_{CC1}, is typically 1mA. Channel 1's undervoltage lockout (UVLO) circuit disables GATE 1 until the supply voltage at V_{CC1} is greater than V_{LKO} (typically 2.45V). GATE 1 is held at ground potential until UVLO deactivates. If ON1 is high and V_{CC1} is above the UVLO threshold voltage, GATE 1 is pulled high by a 10µA current source. If V_{CC1} falls below ($V_{LKO} – V_{LKH}$), GATE 1 is pulled immediately to ground. The internal reference and the common charge pump are powered from the higher of the two V_{CC} inputs, V_{CC1} or V_{CC2}.

V_{CC2} (LTC1647-3): Channel 2 Positive Supply Input. See V_{CC1} for functional description.

V_{CC}: The Common Positive Supply Input for the LTC1647-1 and the LTC1647-2. V_{CC1} and V_{CC2} are internally connected together.

GND: Chip Ground.

ON1: Channel 1 ON Input. The threshold at the ON1 pin is set at 1.29V with 70mV hysteresis. If UVLO and the circuit breaker of channel 1 are inactive, a logic high at ON1 enables the 10µA charge pump current source, pulling the GATE 1 pin above V_{CC1}. If the ON1 pin is pulled low, the GATE 1 pin is pulled to ground by a 50µA current sink.

ON1 resets channel 1's electronic circuit breaker by pulling ON1 low for greater than one t_{RESET} period (50µs). A low-to-high transition at ON1 restarts a normal GATE 1 pull-up sequence.

ON2: Channel 2 ON Input. See ON1 for functional description.

$\overline{\text{FAULT1}}$: Channel 1 Open-Drain Fault Status Output. $\overline{\text{FAULT1}}$ pin pulls low after 0.3µs (t_{FAULT}) if the circuit breaker measures greater than 50mV across the sense resistor connected between V_{CC1} and SENSE 1. If $\overline{\text{FAULT1}}$ pulls low, GATE 1 also pulls low. $\overline{\text{FAULT1}}$ remains low until ON1 is pulled low for at least one t_{RESET} period.

$\overline{\text{FAULT2}}$: Channel 2 Open-Drain Fault Status Output. See $\overline{\text{FAULT 1}}$ for functional description.

SENSE1: Channel 1 Circuit Breaker Current Sense Input. Load current is monitored by a sense resistor connected between V_{CC1} and SENSE 1. The circuit breaker trips if the voltage across the sense resistor exceeds 50mV (V_{CB}). To disable the circuit breaker, connect SENSE 1 to V_{CC1}. In order to obtain optimum performance, use Kelvin-sense connections between the V_{CC} and SENSE pins to the current sense resistor.

SENSE2: Channel 2 Circuit Breaker Current Sense Input. See SENSE 1 for functional description.

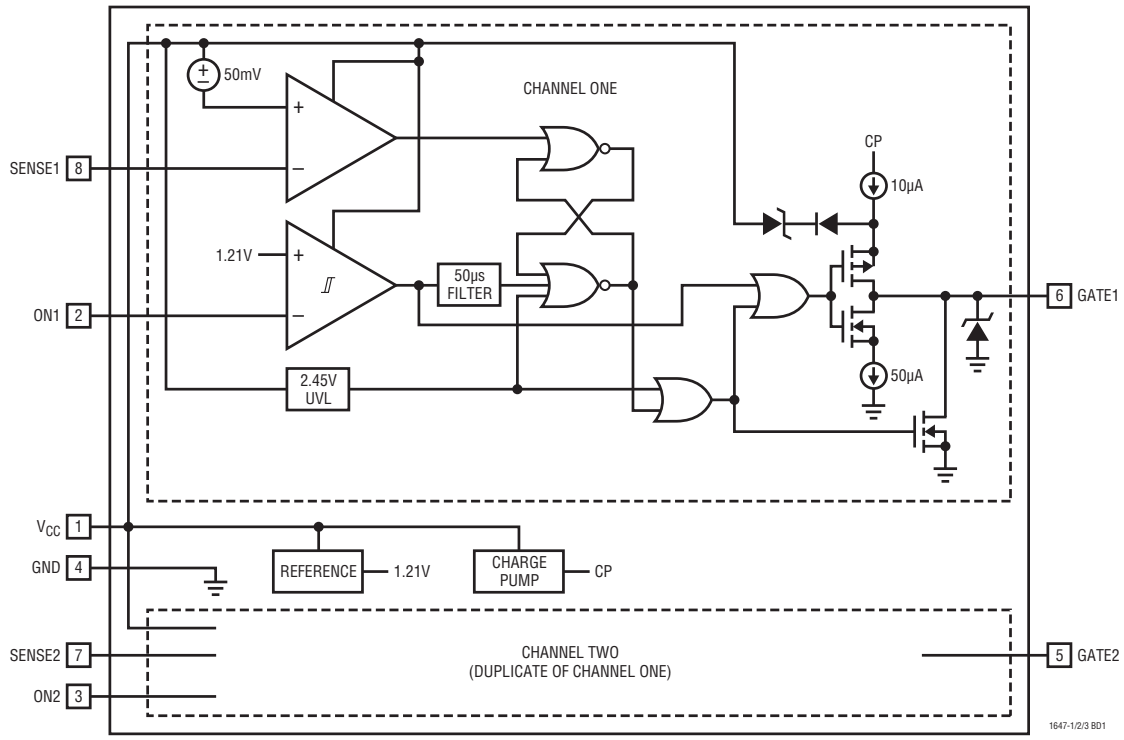
GATE1: Channel 1 N-channel MOSFET Gate Drive Output. An internal charge pump guarantees at least 10V of gate drive from a 5V supply. Two Zener clamps are incorporated at the GATE 1 pin; one Zener clamps GATE 1 approximately 15V above V_{CC} and the second Zener clamps GATE 1 appoximately 28V above GND. The rise time at GATE 1 is set by an external capacitor connected between GATE 1 and GND and an internal 10µA current source provided by the charge pump. The fall time at GATE 1 is set by the 50µA current sink if ON1 is pulled low. If the circuit breaker is tripped or the supply voltage hits the UVLO threshold, a 50mA current sink rapidly pulls GATE 1 low. An external 23V Zener from GATE1 to GND is required for supply voltages (V_{CC1}) greater than 10V.

GATE2: Channel 2 N-channel MOSFET Gate Drive Output. See GATE 1 for functional description.

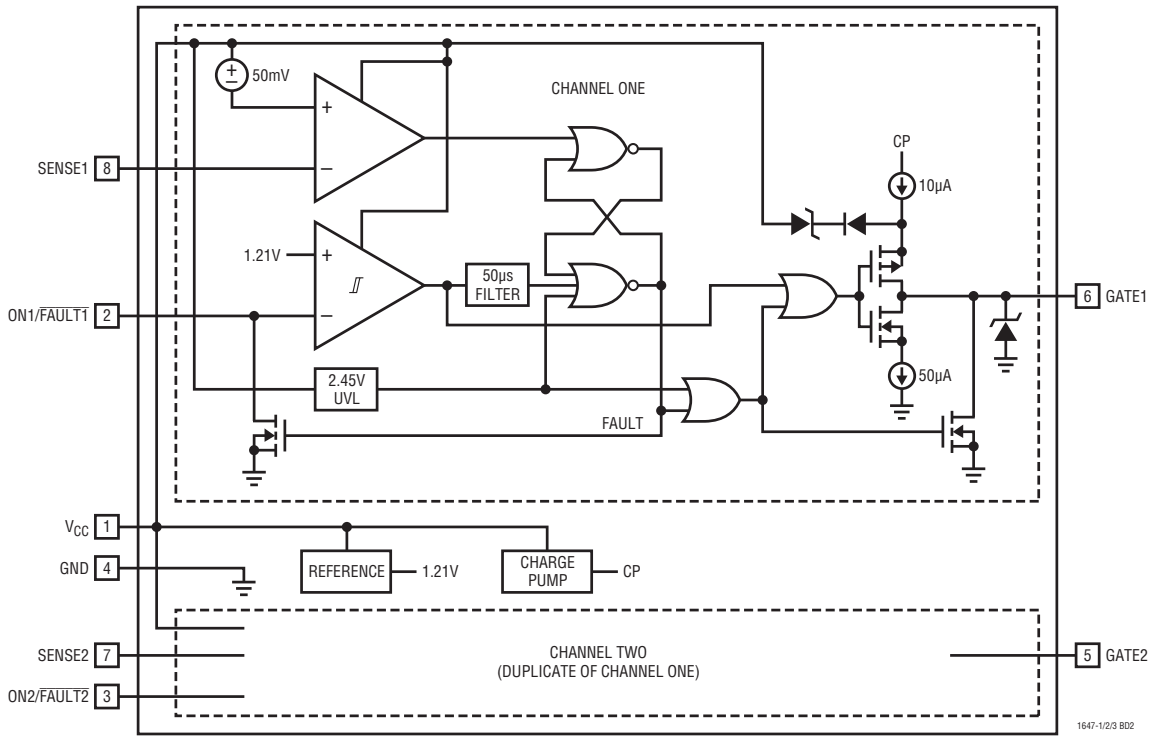
NC: No Connection.

BLOCK DIAGRAMS

LTC1647-1

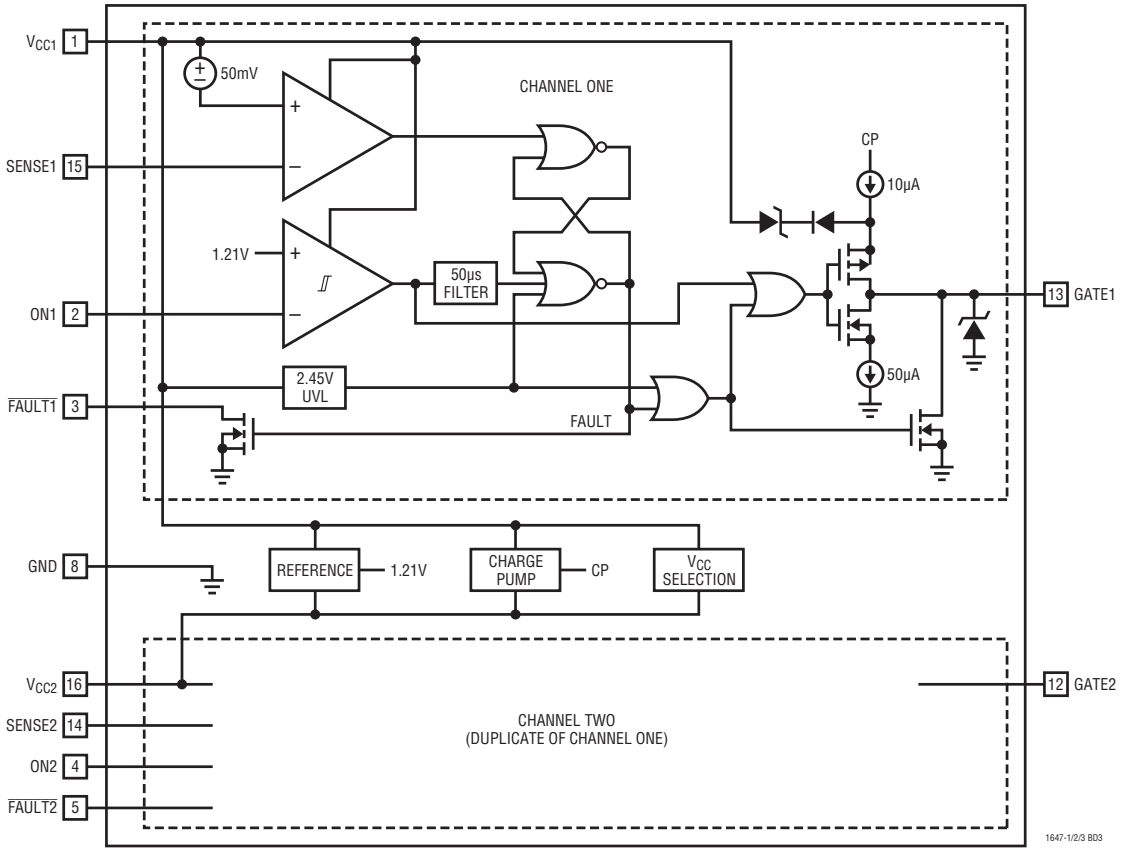


LTC1647-2



BLOCK DIAGRAMS

LTC1647-3



APPLICATIONS INFORMATION

V_{CC} Selection Circuit

The LTC1647-3 features separate supply inputs (V_{CC1} and V_{CC2}) for each channel. The reference and charge pump circuit draw supply current from the higher of the two supplies. An internal V_{CC} selection circuit detects and makes the power connection automatically. This allows a 3V channel to have standard MOSFET gate overdrive when the other channel is 5V. An internal Zener clamps GATE about 15V above V_{CC}.

If both supplies are connected together (internally for LTC1647-1 and LTC1647-2 or externally for LTC1647-3), the reference and charge pump circuit draw equal current from both pins.

Electronic Circuit Breaker

Each channel of the LTC1647 features an electronic circuit breaker to protect against excessive load current and short-circuits. Load current is monitored by sense resistor R1 as shown in Figure 1. The circuit breaker threshold, V_{CB}, is 50mV and it exhibits a response time, t_{FAULT}, of approximately 300ns. If the voltage between V_{CC} and SENSE exceeds V_{CB} for more than t_{FAULT}, the circuit breaker trips and immediately pulls GATE low with a 50mA current sink. The MOSFET turns off and $\overline{FAULT}$ pulls low. The circuit breaker is cleared by pulling the ON pin low for a period of at least t_{RESET} (50µs). A timing diagram of these events is shown in Figure 2.

The value of the sense resistor R1 is given by:

$$R1 = V_{CB}/I_{TRIP}(\Omega)$$

APPLICATIONS INFORMATION

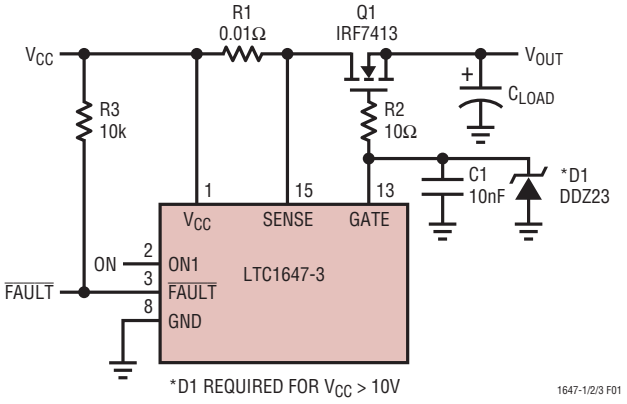


Figure 1. Supply Control Circuitry

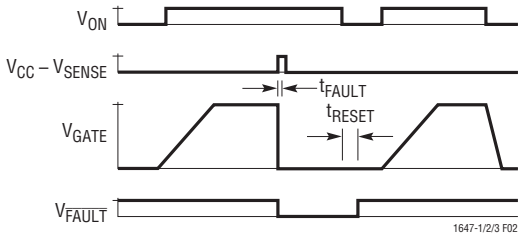


Figure 2. Current Fault Timing

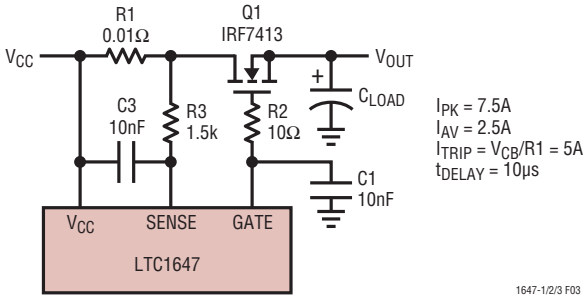
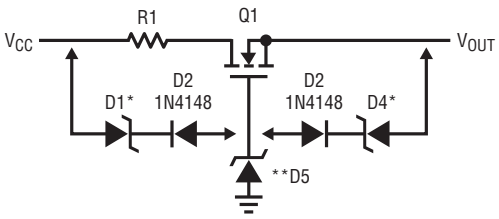


Figure 3. Filtering Current Ripple/Glitches



*D1, D4 USER SELECTED VOLTAGE CLAMP
1N4688 (5V)
1N4692 (7V): LOGIC-LEVEL MOSFET
1N4695 (9V)
1N4702 (15V): STANDARD-LEVEL MOSFET
**D5 DDZ23 (23V) REQUIRED FOR V_{CC} > 10V

1647-1/2/3 F04

Figure 4. Optional Gate Clamp

where V_{CB} is the circuit breaker trip voltage (50mV) and I_{TRIP} is the value of the load current at which the circuit breaker trips. Kelvin-sense layout techniques between the sense resistor and the V_{CC} and SENSE pins are highly recommended for proper operation.

The circuit breaker trip voltage has a tolerance of 20%; combined with a 5% sense resistor, the total tolerance is 25%. Therefore, calculate R1 based on a trip current I_{TRIP} of no less than 125% of the maximum operating current. Do not neglect the effect of ripple current, which adds to the maximum DC component of the load current. Ripple current may arise from any of several sources, but the worst offenders are switching supplies.

A switching regulator on the load side will attempt to draw some ripple current from the backplane and this current passes through the sense resistor. Similarly, output ripple from a switching regulator supplying the backplane will flow through the sense resistor and into the load capacitor.

Minimize the effects of ripple current by either filtering the V_{OUT} line or adding an RC filter to the SENSE pin. A series inductance of 1µH to 10µH inserted between Q1 and C_{LOAD} is adequate ripple current suppression in most cases. Alternatively, a filter, consisting of R3 and C3 (Figure 3), simply filters the ripple component from the SENSE pin at the expense of response time. The added delay is given by:

$$t_{DELAY} = -R3 \bullet C3 \bullet \ln[1 - (V_{CB}/R1 - I_{AV})/(I_{PK} - I_{AV})]$$

Power MOSFET Selection

Power MOSFETs are classified into two catagories: standard MOSFETs ($R_{DS(ON)}$ specified at V_{GS} = 10V) and logic-level MOSFETs ($R_{DS(ON)}$ specified at V_{GS} = 5V). The absolute maximum rating for V_{GS} is typically 20V for standard MOSFETs. The maximum rating for logic-level MOSFETs is lower and ranges from 8V to 16V depending on the manufacturer and specific part number. Some logic-level MOSFETs have a 20V maximum V_{GS} rating. The LTC1647 is primarily targeted for standard MOSFETs; low supply voltage applications should use logic-level MOSFETs. GATE overdrive as a function of V_{CC} is illustrated in the Typical Performance Curves. If lower GATE overdrive is desired, connect a diode in series with a Zener between GATE and V_{CC} or between GATE and V_{OUT} as shown in Figure 4. For

APPLICATIONS INFORMATION

an input supply greater than 10V at V_{CC1} or V_{CC2}, a 24V Zener is recommended between the corresponding GATE1 or GATE2 pin and GND as shown in Figures 1 and 4.

The $R_{DS(ON)}$ of the external pass transistor must be low to make V_{DS} a small percentage of V_{CC}. At V_{CC} = 3.3V, V_{DS} + V_{CB} = 0.1V yields 3% error at maximum load current. This restricts the choice of MOSFETs to very low $R_{DS(ON)}$. At higher V_{CC} voltages, the $R_{DS(ON)}$ requirement can be relaxed. MOSFET package dissipation (P_D and T_J) may restrict the value of $R_{DS(ON)}$.

Power Supply Ramping

V_{OUT} is controlled by placing MOSFET Q1 in the power path (Figure 1). R1 provides load current fault detection and R2 prevents MOSFET high frequency oscillation. By ramping the gate of the pass transistor at a controlled rate (dV/dt = 10µA/C1), the transient surge current ($I = C_{LOAD} \bullet dV/dt = 10\mu A \bullet C_{LOAD}/C1$) drawn from the main backplane is limited to a safe value when the board is inserted into the connector.

When power is first applied to V_{CC}, the GATE pin pulls low. A low-to-high transition at the ON pin initiates GATE ramp-up. The rising dV/dt of GATE is set by 10µA/C1 (Figure 5), where C1 is the total external capacitance between GATE and GND. The ramp-up time for V_{OUT} is equal to $t = (V_{CC} \bullet C1)/10\mu A$.

A high-to-low transition at the ON pin initiates a GATE ramp-down at a slope of –50µA/C1. This rate is usually adequate as the supply bypass capacitors take time to discharge through the load.

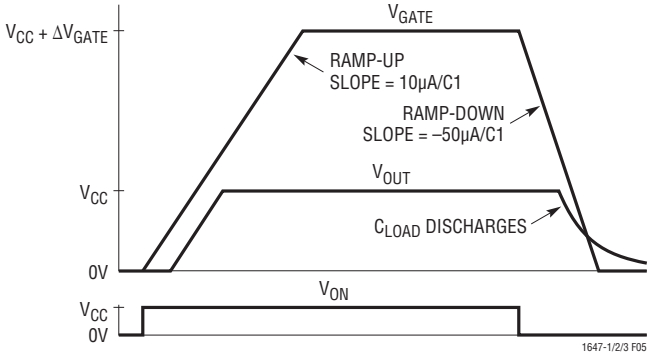


Figure 5. Supply Turn-On/Off with ON

If the ON pin is connected to V_{CC}, or is pulled high before V_{CC} is first applied, GATE is held low until V_{CC} rises above the undervoltage lockout threshold, V_{LKO} (Figure 6). Once the threshold is exceeded, GATE ramps at a controlled rate of 10µA/C1. When the power supply is disconnected, the body diode of Q1 holds V_{CC} about 700mV below V_{OUT}. The GATE voltage droops at a rate determined by V_{CC}. If V_{CC} drops below $V_{LKO} – V_{LKH}$, the LTC1647 enters UVLO and GATE pulls down to GND.

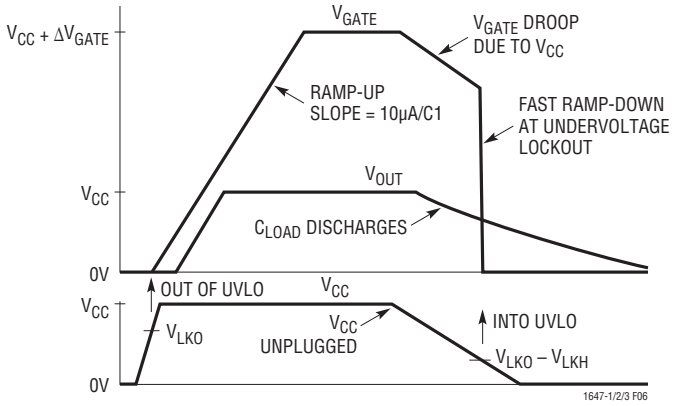


Figure 6. Supply Turn-On/Off with V_{CC}

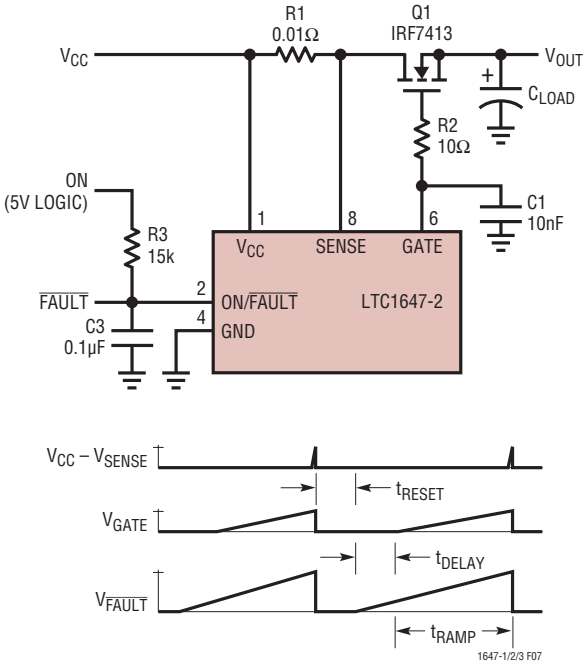


Figure 7. Autoretry Sequence

APPLICATIONS INFORMATION

Autoretry

The LTC1647-2 and LTC1647-3 are designed to allow an automatic reset of the electronic circuit breaker after a fault condition occurs. This is accomplished by pulling the ON/$\overline{FAULT}$ (LTC1647-2) pin or the ON and $\overline{FAULT}$ pins tied together (LTC1647-3) high through a resistor, R3, as shown in Figure 7. An autoretry sequence begins if a fault occurs. If the circuit breaker trips, $\overline{FAULT}$ pulls the ON pin low. After a t_{RESET} interval elapses, $\overline{FAULT}$ resets and R3 pulls the ON pin up. C3 delays GATE turn-on until the voltage at the ON pin exceeds V_{IH}. The delay time is

$$t_{DELAY} = -R3 \bullet C3 \bullet \ln[1-(V_{IH} - V_{OL})/(V_{ON} - V_{OL})]$$

GATE ramps up at 10µA/C1 until Q1 conducts. If V_{OUT} is still shorted to GND, the cycle repeats. The ramp interval is about $t_{RAMP} = V_{TH} \bullet C1/10\mu A$ where V_{TH} is the threshold voltage of the external MOSFET.

Hot Circuit Insertion

When circuit boards are inserted into a live backplane or a device bay, the supply bypass capacitors on the board can draw huge transient currents from the backplane or the device bay power bus as they charge up. The transient currents can damage the connector pins and glitch the system supply, causing other boards in the system to reset or malfunction.

The LTC1647 is designed to turn two positive supplies on and off in a controlled manner, allowing boards to be safely inserted or removed from a live backplane or device bay. The LTC1647 can be located before or after the connector as shown in Figure 8. A staggered PCB connector can sequence pin conections when plugging and unplugging circuit boards. Alternatively, the control signal can be generated by processor control.

Ringing

Good engineering practice calls for bypassing the supply rail of any circuit. Bypass capacitors are often placed at the supply connection of every active device, in addition to one or more large value bulk bypass capacitors per supply rail. If power is connected abruptly, the bypass capacitors slow the rate of rise of voltage and heavily damp any parasitic resonance of lead or trace inductance working against the supply bypass capacitors.

The opposite is true for LTC1647 Hot Swap circuits on a daughterboard. In most cases, on the powered side of the MOSFET switch (V_{CC}) there is no supply bypass capacitor present. An abrupt connection, produced by plugging a board into a backplane connector, results in a fast rising edge applied to the V_{CC} line of the LTC1647.

No bulk capacitance is present to slow the rate of rise and heavily damp the parasitic resonance. Instead, the fast edge shock excites a resonant circuit formed by a combination of wiring harness, backplane and circuit board parasitic inductances and MOSFET capacitance. In theory, the peak voltage should rise to 2X the input supply, but in practice the peak can reach 2.5X, owing to the effects of voltage dependent MOSFET capacitance.

The absolute maximum V_{CC} potential for the LTC1647 is 17V; any circuit with an input of more than 6.8V should be scrutinized for ringing. A well-bypassed backplane should not escape suspicion: circuit board trace inductances of as little as 10nH can produce sufficient ringing to overvoltage V_{CC}.

Check ringing with a fast storage oscilloscope (such as a LECROY 9314AL DSO) by attaching coax or a probe to V_{CC} and GND, then repeatedly inserting the circuit board into the backplane. Figures 9a and 9b show typical results in a 12V application with different V_{CC} lead lengths. The peak amplitude reaches 22V, breaking down the ESD protection diode in the process.

There are two methods for eliminating ringing: clipping and snubbing. A transient voltage suppressor is an effective means of limiting peak voltage to a safe level. Figure 10 shows the effect of adding an ON Semiconductor, 1SMA12CAT3, on the waveform of Figure 9.

Figures 11a and 11b show the effects of snubbing with different RC networks. The capacitor value is chosen as 10X to 100X the MOSFET C_{OSS} under bias and R is selected for best damping—1Ω to 50Ω depending on the value of parasitic inductance.

APPLICATIONS INFORMATION

Supply Glitching

LTC1647 Hot Swap circuits on the backplane are generally used to provide power-up/down sequence at insertion/removal as well as overload/short-circuit protection. If a short-circuit occurs at supply ramp-up, the circuit breaker trips. The partially enhanced MOSFET, Q1, is easily disconnected without any supply glitch.

If a dead short occurs after a supply connection is made (Figure 12), the sense resistor R1 and the $R_{DS(ON)}$ of fully enhanced Q1 provide a low impedance path for nearly unlimited current flow. The LTC1647 discharges the GATE pin in a few microseconds, but during this discharge time current on the order of 150 amperes flows from the V_{CC} power supply. This current spike glitches the power supply, causing V_{CC} to dip (Figure 12a and 12b).

On recovery from overload, some supplies may overshoot. Other devices attached to this supply may reset or malfunction and the overshoot may also damage some components. An inductor (1µH to 10µH) in series with Q1's source limits the short-circuit di/dt, thereby limiting the peak current and the supply glitch (Figure 12a and 12b). Additional power supply bypass capacitance also reduces the magnitude of the V_{CC} glitch.

V_{ID} Power Controller

The two Hot Swap channels of the LTC1647 are ideally suited for V_{ID} power control in portable computers. Figure 13 shows an application using the LTC1647-2 on the system side of the device bay interface (1394 PHY and/or USB). The controller detects the presence of a peripheral in each device bay and controls the LTC1647-2. The timing waveform illustrates the following sequence of events: t1, rising out of undervoltage lockout with GATE 1 ramping up; t2, load current fault at R1; t3, circuit breaker resets with R5/C3 delay; t4/t5, controller gates off/on device supply with RC delay; t6, device enters undervoltage lockout.

If C6 is not connected in Figure 13, $\overline{FAULT2}$ and ON2 will have similar waveforms. t7 initiates an ON sequence; t8, a load fault is detected at R7 with $\overline{FAULT2}$ pulling low. If the controller wants to stretch the interval between retries, it can pull ON2 low at t9 (t9 – t8 < 0.4•t_{RESET}). At t10/t11, the controller initiates a new power-up/down sequence.

APPLICATIONS INFORMATION

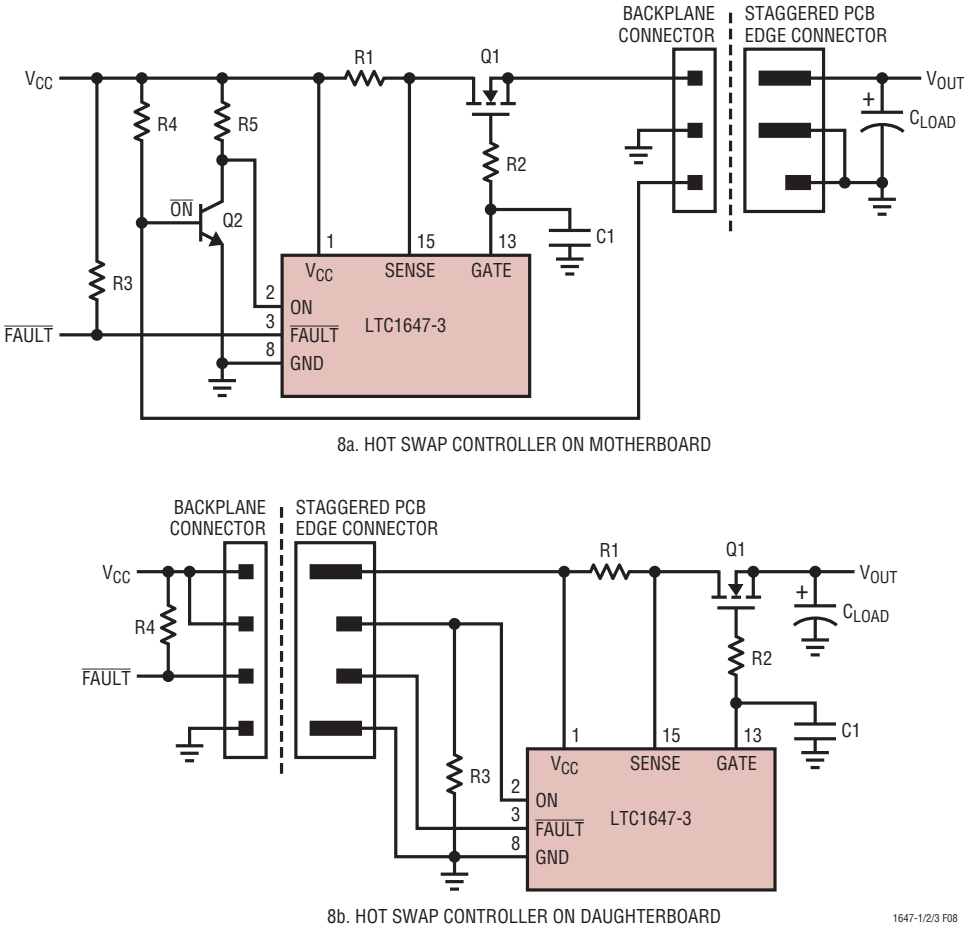
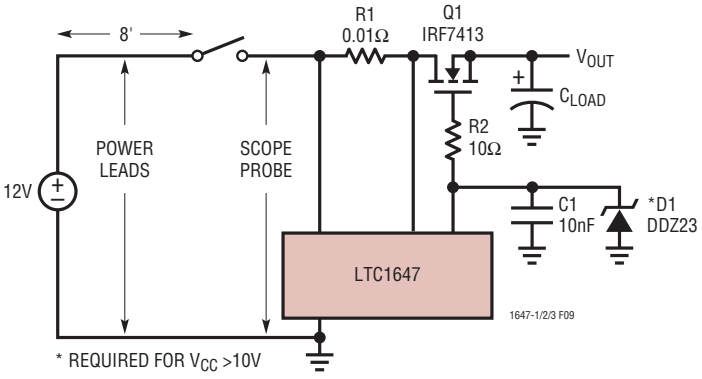
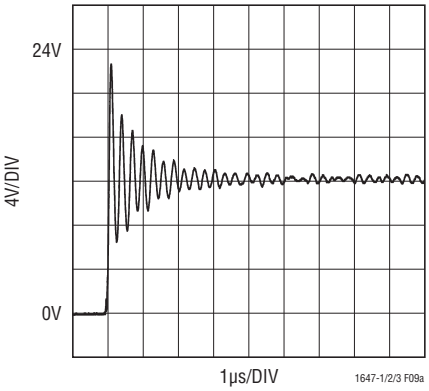


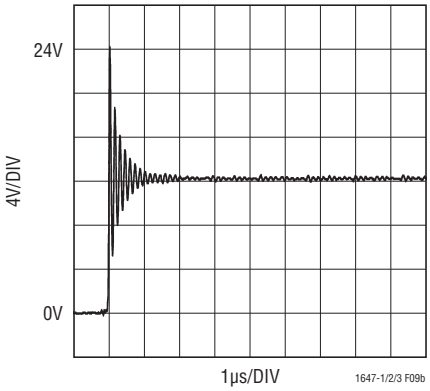
Figure 8. Staggered Pins Connection

APPLICATIONS INFORMATION





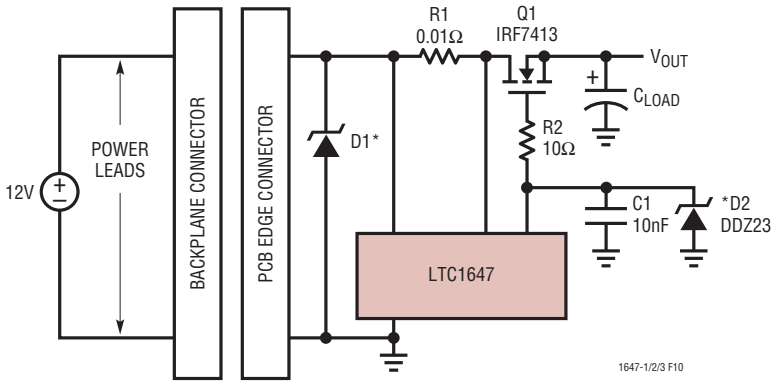
9a. Undamped V_{CC} Waveform (48" Leads)



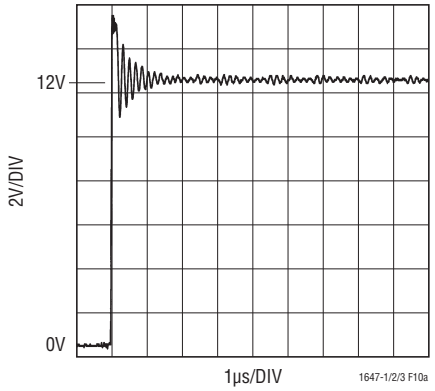
9b. Undamped V_{CC} Waveform (8" Leads)

Figure 9. Ring Experiment

APPLICATIONS INFORMATION

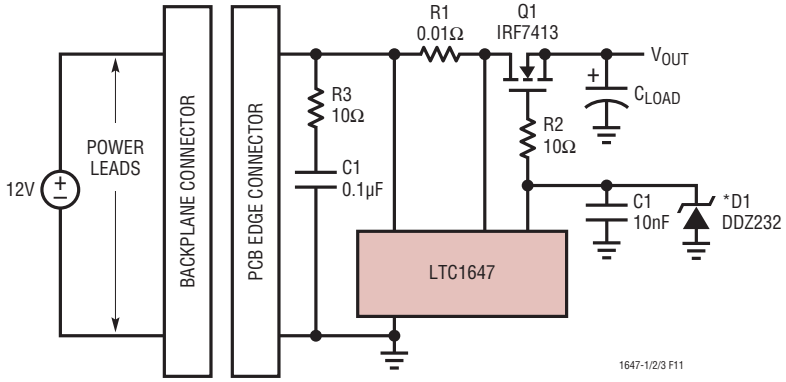


ON SEMICONDUCTOR
* 1SMA12CAT3, REQUIRED FOR V_{CC} > 10V

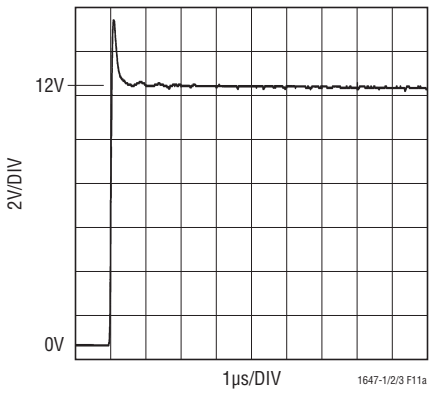


V_{CC} Waveform Clamped by a Transient Suppressor

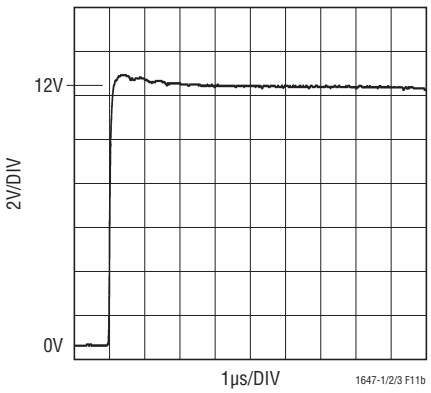
Figure 10. Transient Suppressor Clamp



*REQUIRED FOR V_{CC} > 10V



11a. V_{CC} Waveform Damped by a Snubber (15Ω, 6.8nF)



11b. V_{CC} Waveform Damped by a Snubber (10Ω, 0.1µF)

Figure 11. Snubber "Fixes"

APPLICATIONS INFORMATION

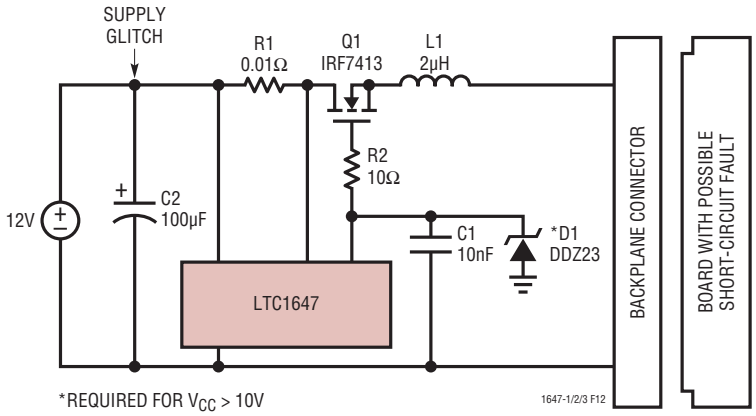
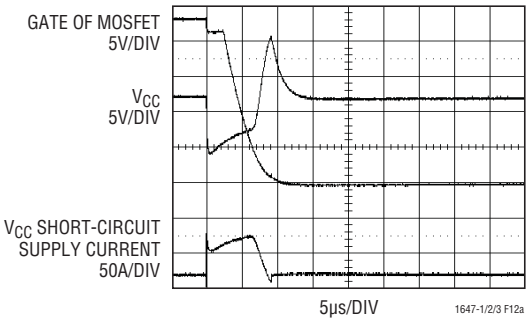
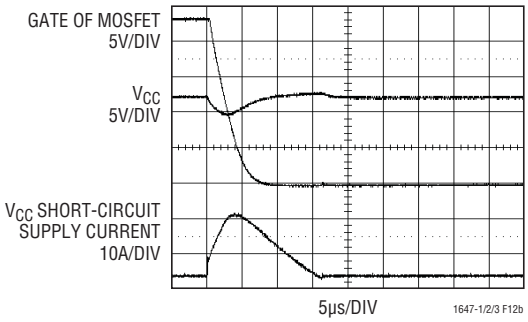


Figure 12. Supply Glitch



12a. V_{CC} Short-Circuit Supply Current Glitch without Any Limiting



12b. V_{CC} Supply Glitch with 2µH Series Inductor

APPLICATIONS INFORMATION

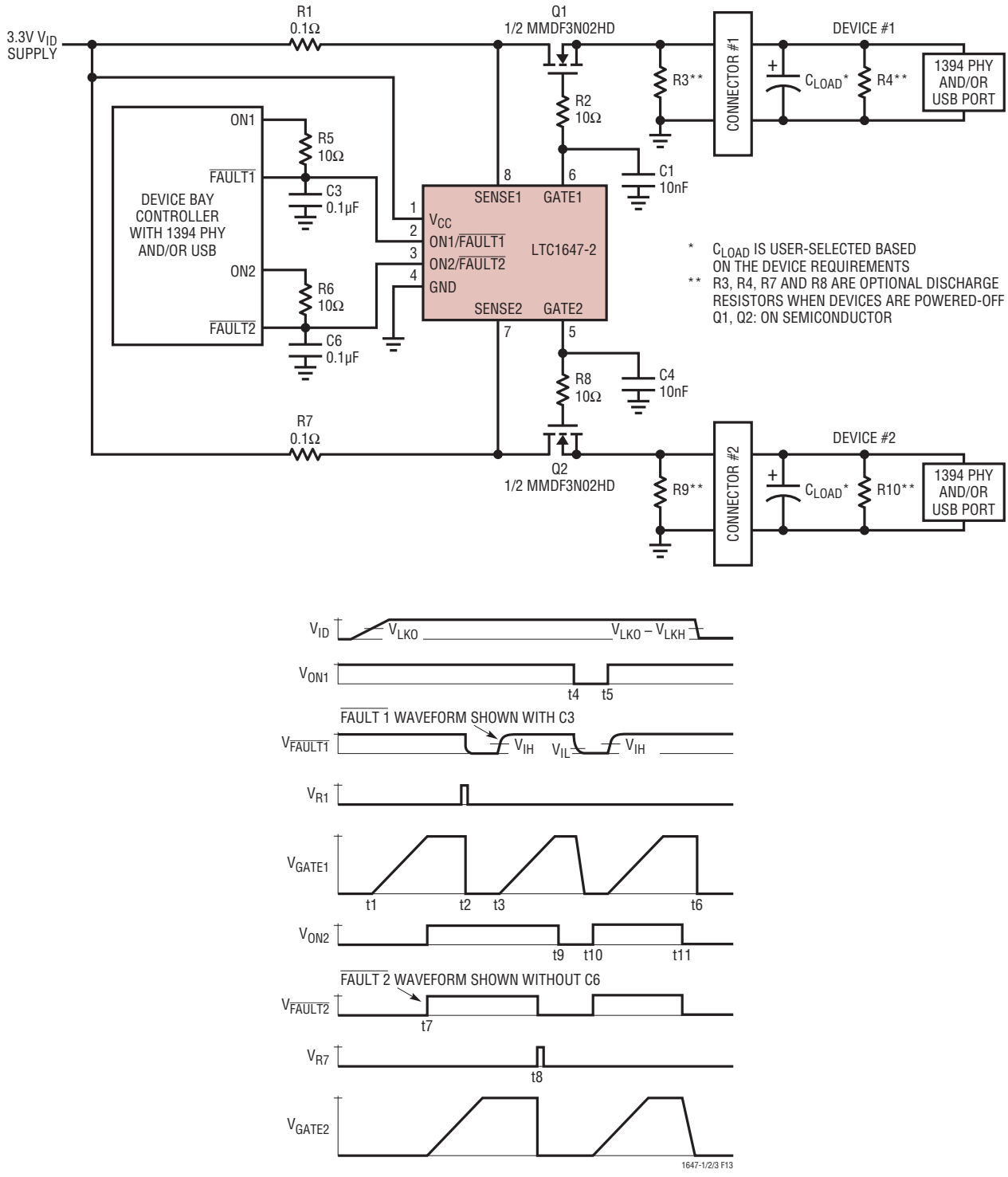
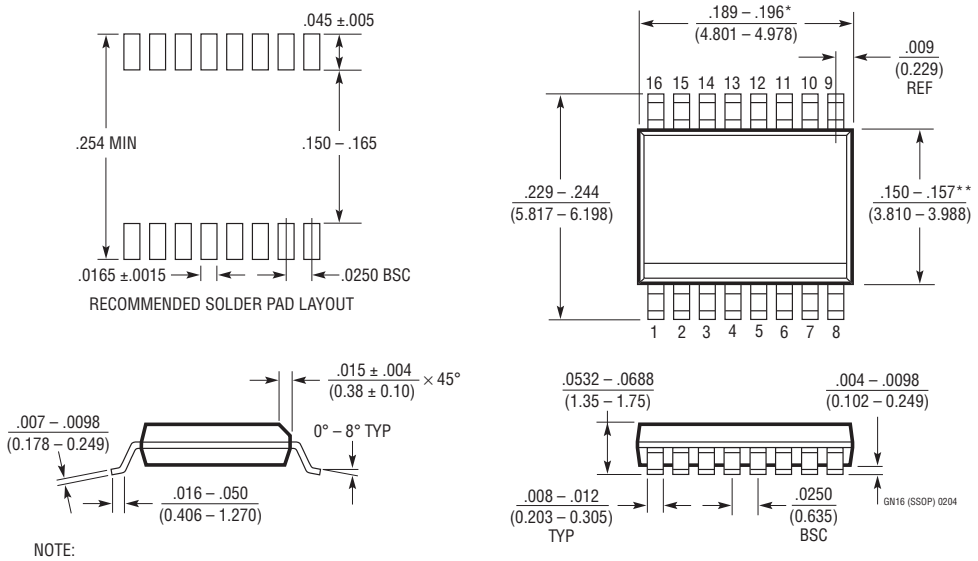


Figure 13. V_{ID} Power Controller with Fault Status and Retry Sequence

PACKAGE DESCRIPTION

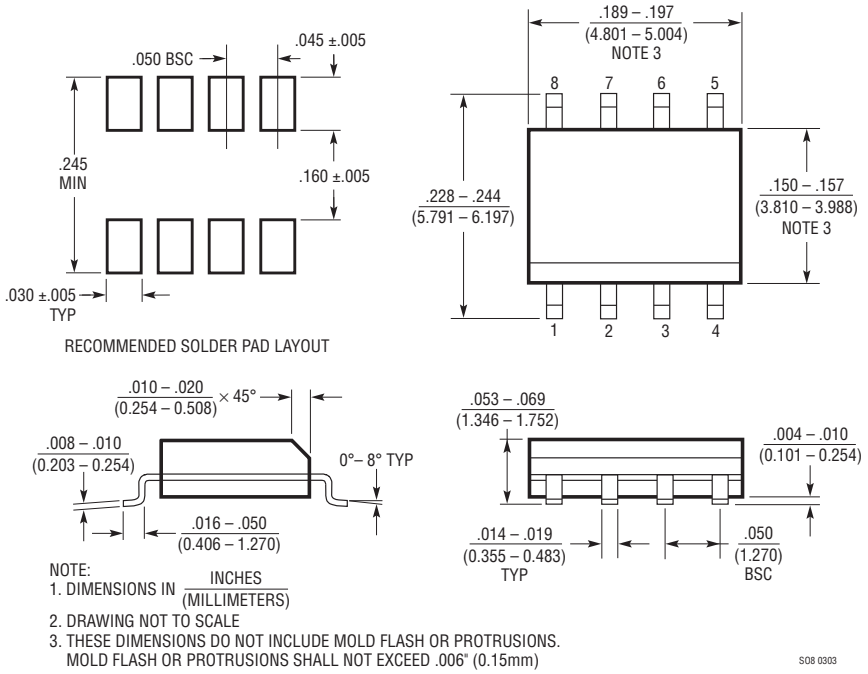
GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/10	Replaced Typical Application circuit	1
		Updated Order Information section	2
		Revised GATE1 description in Pin Functions section	8
		Revised Figures 1, 4, 6, 7, 8, 9, 10, 11 and 12 in Applications Information section	11, 12, 15, to 18
		Updated references to Figure 12a and 12b in Applications Information section	14
		Revised Figure 14 in Typical Applications and updated Related Parts list	20

TYPICAL APPLICATION

Hot Swapping Two Supplies

Two separate supplies can be independently controlled by using the LTC1647-3. In some applications, sequencing between the two power supplies is a requirement. For example, it may be necessary to ramp-up one supply first before allowing the second supply to power-up, as well as requiring that this same supply ramp-down last on power-down. Figure 14's circuit illustrates how to program the delays between the two pass transistors using the ON1 and ON2 pins (time events t1 to t4). t5 and t7 show both channels being switched on simultaneously where sequencing is not crucial.

Some applications require that both channels be gated off if a fault occurs in one channel. This is accomplished in Figure 14 by using a crisscross $\overline{\text{FAULT}}$-to-SENSE arrangement of R3/R4 and R7/R8. t6 and t9 illustrate the circuit's operation.

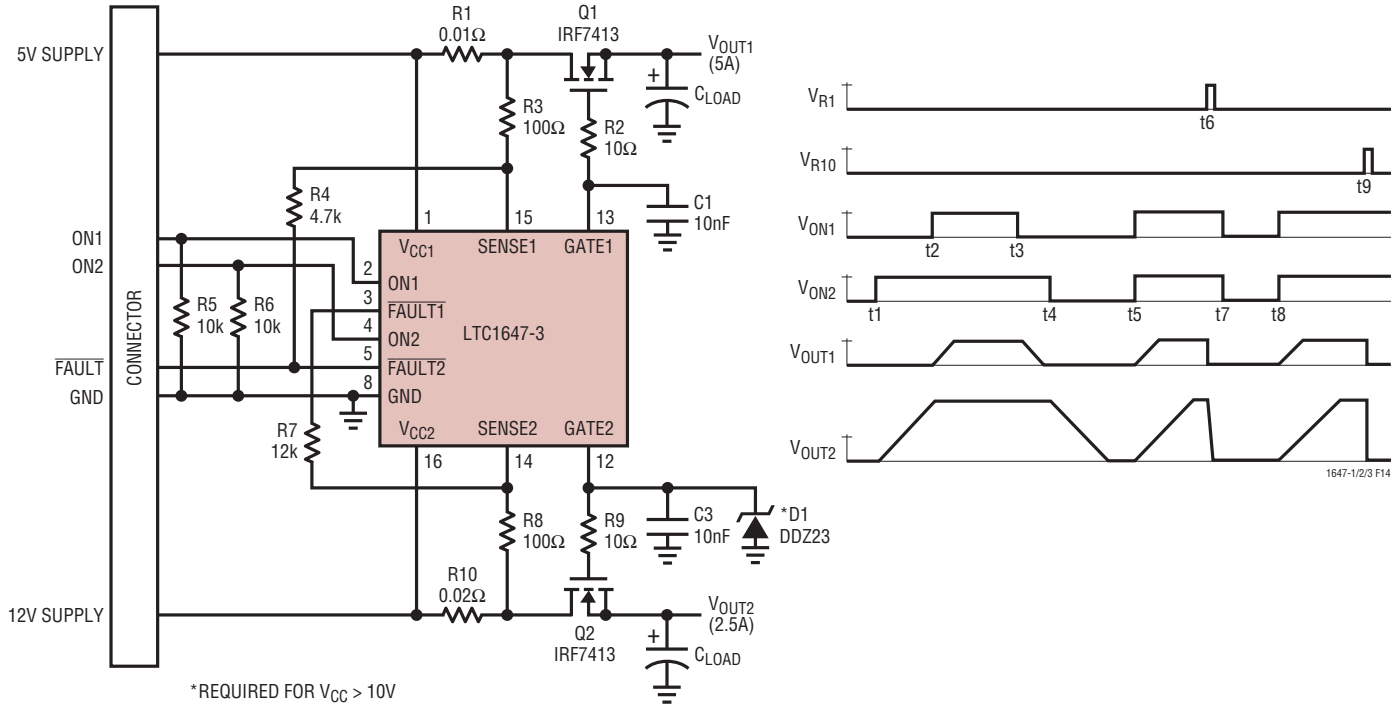


Figure 14. Hot Swapping Two Supplies

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1421	2-Channel Hot Swap Controller	24-Pin, Operates from 3V to 12V and Supports –12V
LTC1422	Hot Swap Controller in SO-8	System Reset Output with Programmable Delay
LT1640AL/LT1640AH	Negative Voltage Hot Swap Controller in SO-8	Operates from –10V to –80V
LT1641	High Voltage Hot Swap Controller in SO-8	Operates from 9V to 80V
LT1642	Fault Protected Hot Swap Controller	Operates Up to 16.5V, Protected to 33V
LTC1643L/LTC1643H	PCI-Bus Hot Swap Controller	3.3V, 5V and ±12V in Narrow 16-Pin SSOP
LT1645	2-Channel Hot Swap Controller	Operates from 1.2V to 12V, Power Sequencing

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