

Automotive P-Channel 200 V (D-S) 175 °C MOSFET

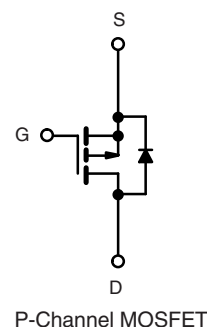
PowerPAK® SO-8L Single


FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE



PRODUCT SUMMARY

V_{DS} (V)	-200
$R_{DS(on)}$ (Ω) at $V_{GS} = -10$ V	0.305
$R_{DS(on)}$ (Ω) at $V_{GS} = -6$ V	0.315
I_D (A)	-9.4
Configuration	Single
Package	PowerPAK SO-8L

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	-200	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current	I_D	-9.4	A
		-5.4	
Continuous source current (diode conduction)	I_S	-60	
Pulsed drain current ^a	I_{DM}	-37	
Single pulse avalanche current	I_{AS}	-30	mJ
Single pulse avalanche energy	E_{AS}	45	
Maximum power dissipation ^a	P_D	68	W
		22	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^{c, d}		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	R_{thJA}	68	°C/W
Junction-to-case (drain)	R_{thJC}	2.2	

Notes

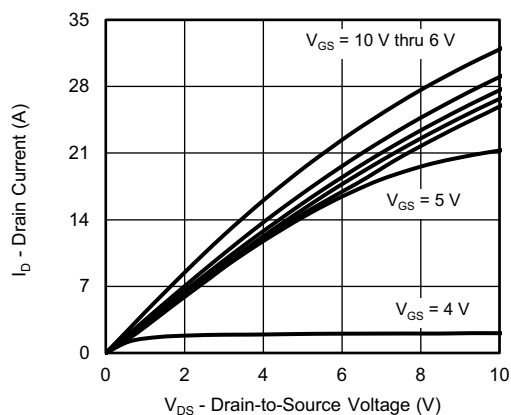
- Pulse test; pulse width $\$



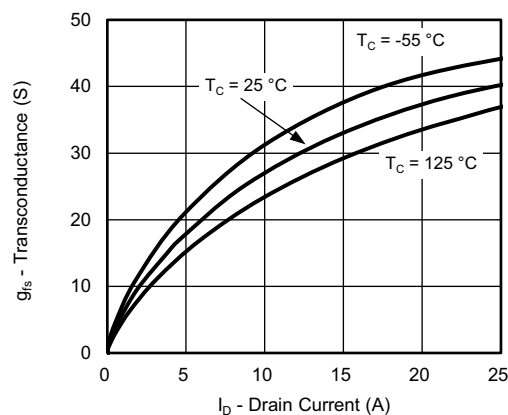
SPECIFICATIONS ($T_C = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0$, $I_D = -250\text{ }\mu\text{A}$		-200	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$		-2.5	-3.0	-3.5	
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = -200\text{ V}$	-	-	-1	μA
		$V_{GS} = 0\text{ V}$	$V_{DS} = -200\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$	-	-	-50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = -200\text{ V}$, $T_J = 175\text{ }^{\circ}\text{C}$	-	-	-150	
On-state drain current ^a	$I_{D(on)}$	$V_{GS} = -10\text{ V}$	$V_{DS} \leq -5\text{ V}$	-5	-	-	A
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = -3.8\text{ A}$	-	0.254	0.305	Ω
		$V_{GS} = -10\text{ V}$	$I_D = -3.8\text{ A}$, $T_J = 125\text{ }^{\circ}\text{C}$	-	-	0.591	
		$V_{GS} = -10\text{ V}$	$I_D = -3.8\text{ A}$, $T_J = 175\text{ }^{\circ}\text{C}$	-	-	0.763	
		$V_{GS} = -6\text{ V}$	$I_D = -3.8\text{ A}$	-	0.261	0.315	
Forward transconductance ^b	g_{fs}	$V_{DS} = -15\text{ V}$, $I_D = -3.8\text{ A}$		-	15	-	S
Dynamic ^b							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$	$V_{DS} = -25\text{ V}$, $f = 1\text{ MHz}$	-	2734	3700	pF
Output capacitance	C_{oss}						



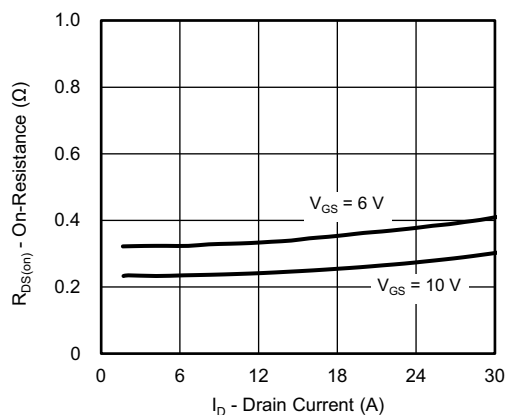
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



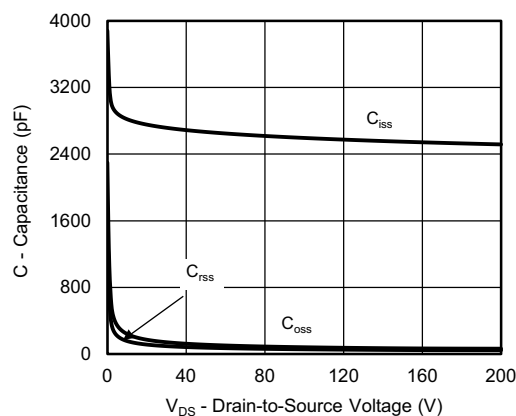
Output Characteristics



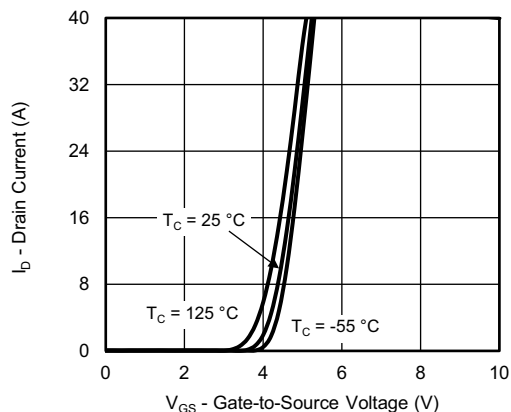
Transconductance



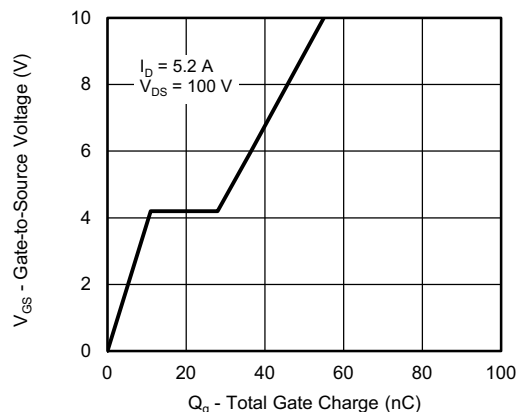
On-Resistance vs. Drain Current



Capacitance



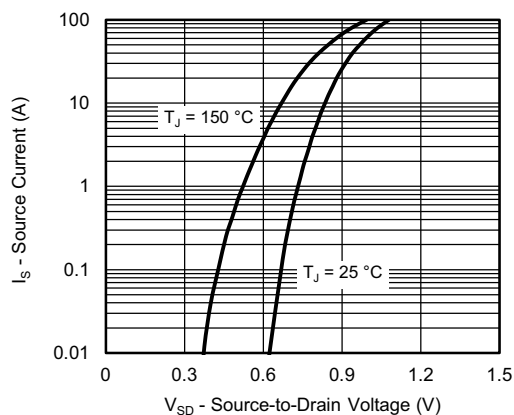
Transfer Characteristics



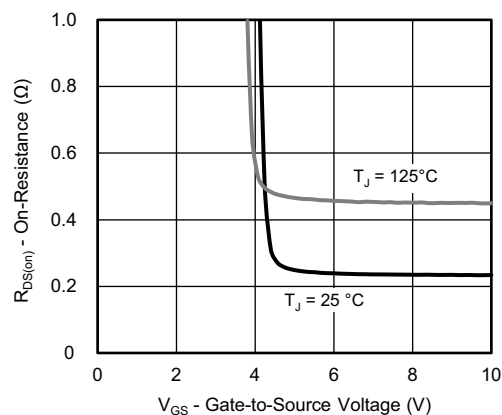
Gate Charge



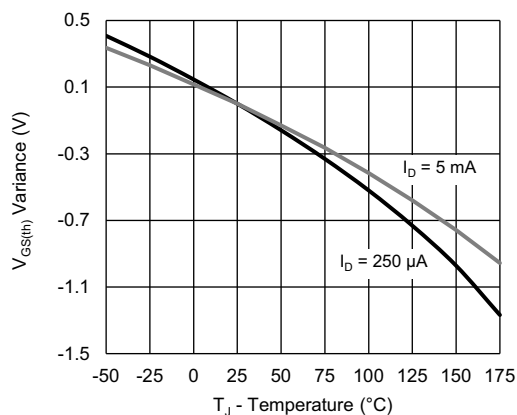
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



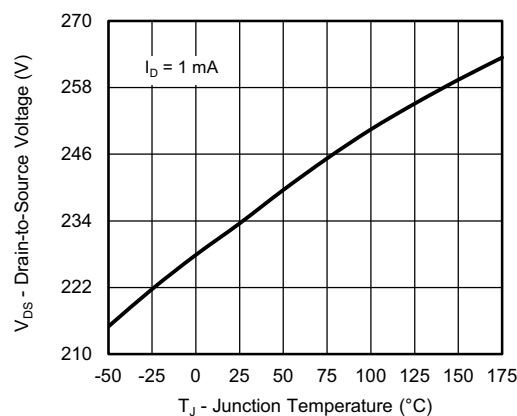
Source Drain Diode Forward Voltage



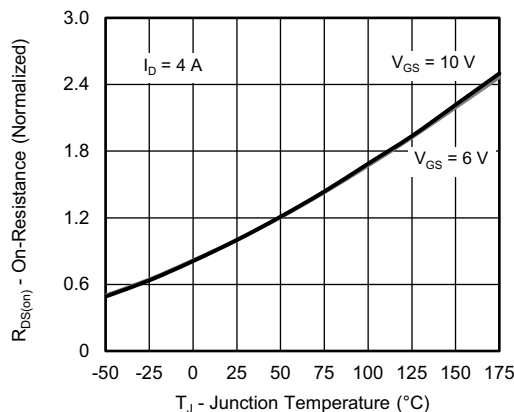
On-Resistance vs. Gate-to-Source Voltage



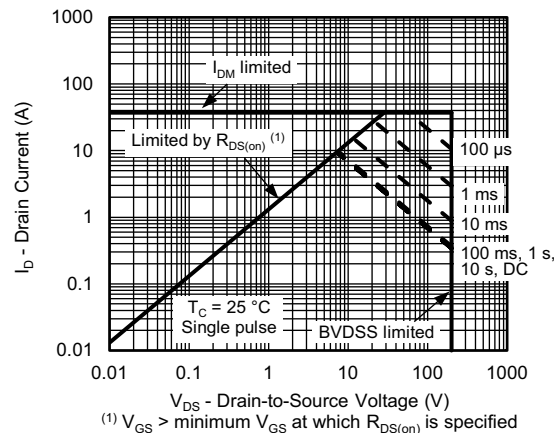
Threshold Voltage



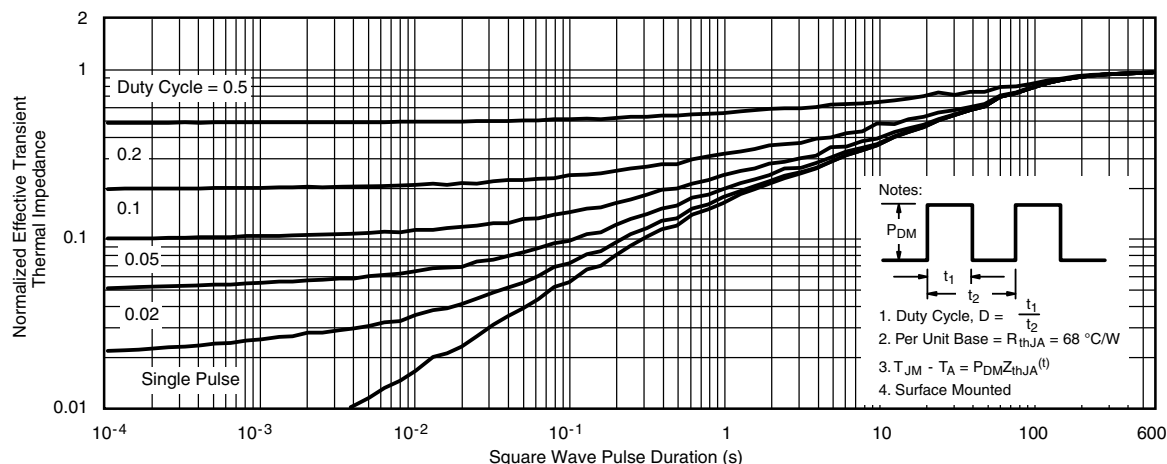
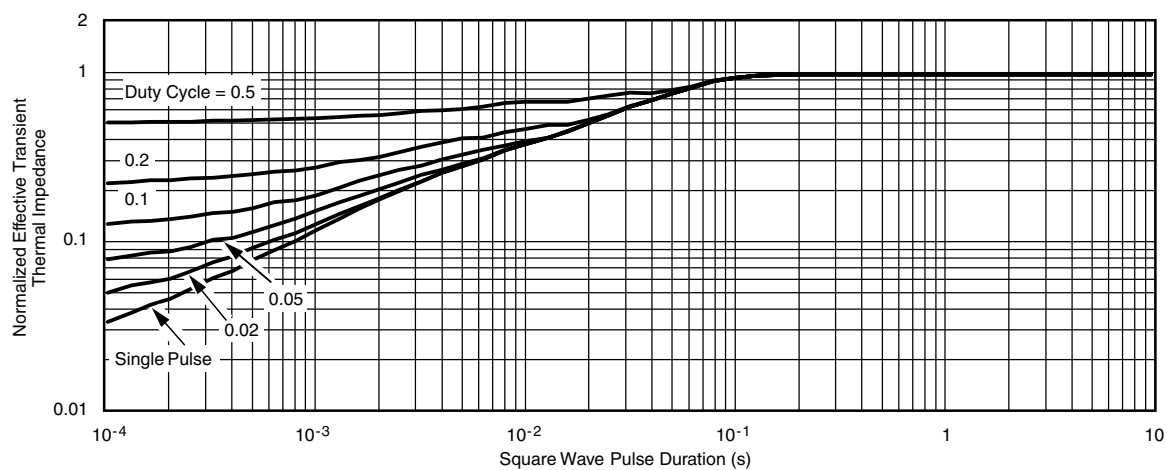
Drain Source Breakdown vs. Junction Temperature



On-Resistance vs. Junction Temperature



Safe Operating Area

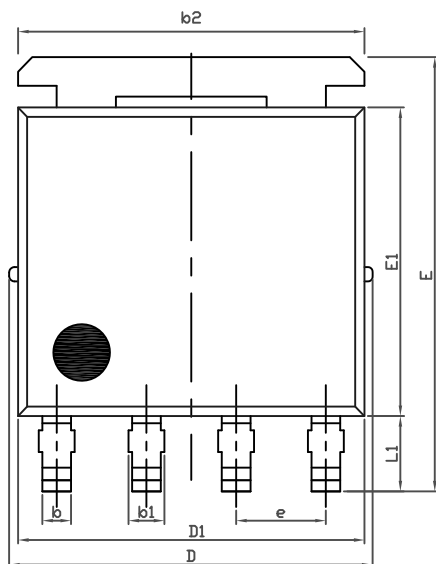
THERMAL RATINGS ($T_C = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Case
Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

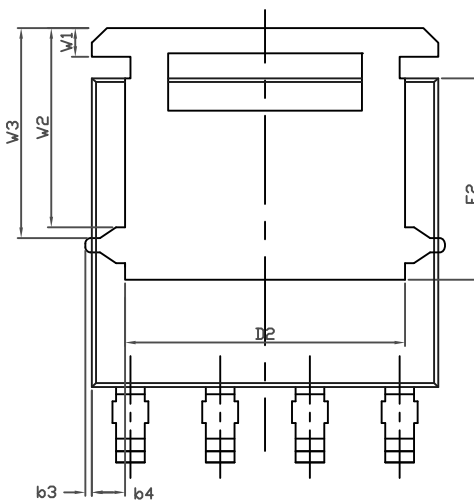
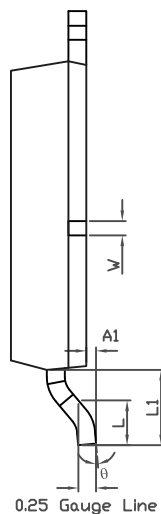
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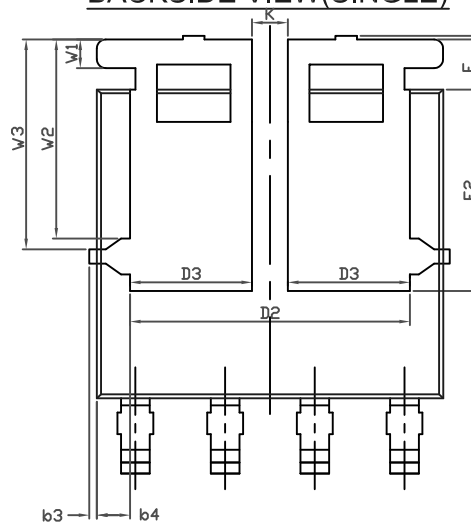
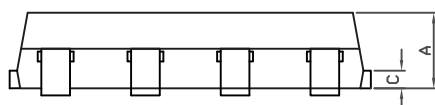
PowerPAK® SO-8L Case Outline for Al Parts



TOPSIDE VIEW



BACKSIDE VIEW(SINGLE)



BACKSIDE VIEW(DUAL)



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3	0.094			0.004		
b4	0.47			0.019		
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
e	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	2.75	2.85	2.95	0.108	0.112	0.116
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.51			0.020		
W	0.23			0.009		
W1	0.41			0.016		
W2	2.82			0.111		
W3	2.96			0.117		



RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE





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