

# LTC2408

## 4-/8-Channel 24-Bit $\mu$ Power No Latency $\Delta\Sigma$ ADC

### DESCRIPTION

The LTC<sup>®</sup>2408, an 8-channel 24-bit no latency  $\Delta\Sigma$  ADC is featured on the DC273A demonstration board. The LTC2408 features a 4ppm linearity, 4ppm full-scale accuracy, 1ppm offset accuracy, and 0.3ppm RMS noise.

The LTC2408 performs interleaved auto-zero and calibration cycles which are transparent to the user.

The device does not require initialization or configuration, other than selecting the multiplexer channel.

The board includes a precision 2.5V reference (LT1019-2.5), as well as bypassing capacitors, and jumpers to select line frequency rejection and on board /external reference.

The demonstration board is designed to be incorporated into a target system, as well as give an example of good placement of bypass and partitioning of an analog and digital ground.

**Design files for this circuit board are available at <http://www.linear.com/demo>**

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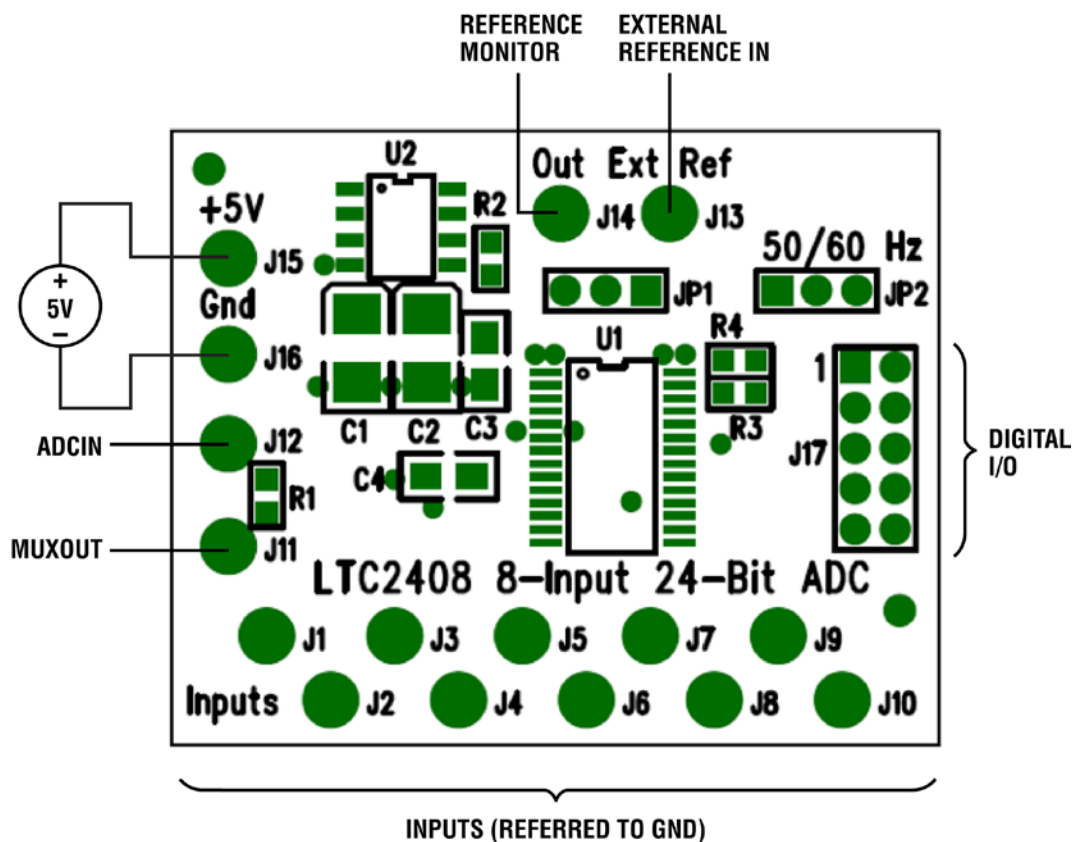


Figure 1. DC273A Set-Up

# DEMO MANUAL DC273A

## QUICK START PROCEDURE

All of the digital control lines are on a 0.070" header (J17). On the DC273A demonstration board CSMUX and  $\overline{\text{CSADC}}$  are tied together, as are SLK and CLK. This allows the ADC to be addressed through a minimum of control lines. When the CSMUX and  $\overline{\text{CSADC}}$  are logic High, address data can be clocked into the MUX. When CSMUX and  $\overline{\text{CSADC}}$  are logic low, conversion data can be clocked out of the ADC. Refer to the LTC2408 data sheet for a complete description of the various serial interface modes.

The DC273A incorporates 2 jumpers: JP1, which allows the on-board or an external reference, to be selected; and JP2, which allows selection of 50Hz/60Hz line frequency rejection.

All the analog inputs are provided with turrets along one edge of the board, positioned to be compatible with clip leads. Two ground connections (J9 and J10) are provided for interconnection into an analog subsystem or to be used as separate returns for two signal groups.

Power and ground are provided on J15 and J16, and reference in and out are provided on J13 and J14.

Interconnection of analog and digital subsystems can be made through these ground connections, or all should return to a star ground at a point in the target system.

All ground connections should be as short as possible. The multiplexer output is linked to the ADC through a 5k resistor. Both terminals are available, J11 for MUXOUT, and J12 for ADCIN. As the multiplexer output can be disabled, multiplexer expansion can be brought to either of these terminals. Optionally, an amplifier (buffer) can be used to drive ADCIN, without necessarily removing the 5k resistor. If an amplifier with voltage gain is introduced, it is recommended that the resistor be removed. Depending on the source resistance or drive capabilities of nodes driving the multiplexer inputs, J11 can be tied directly to J12. Please see the LTC2400 data sheet for more information on driving the input of the LTC2408.

See the timing diagram for MUX, and Data Output operation.

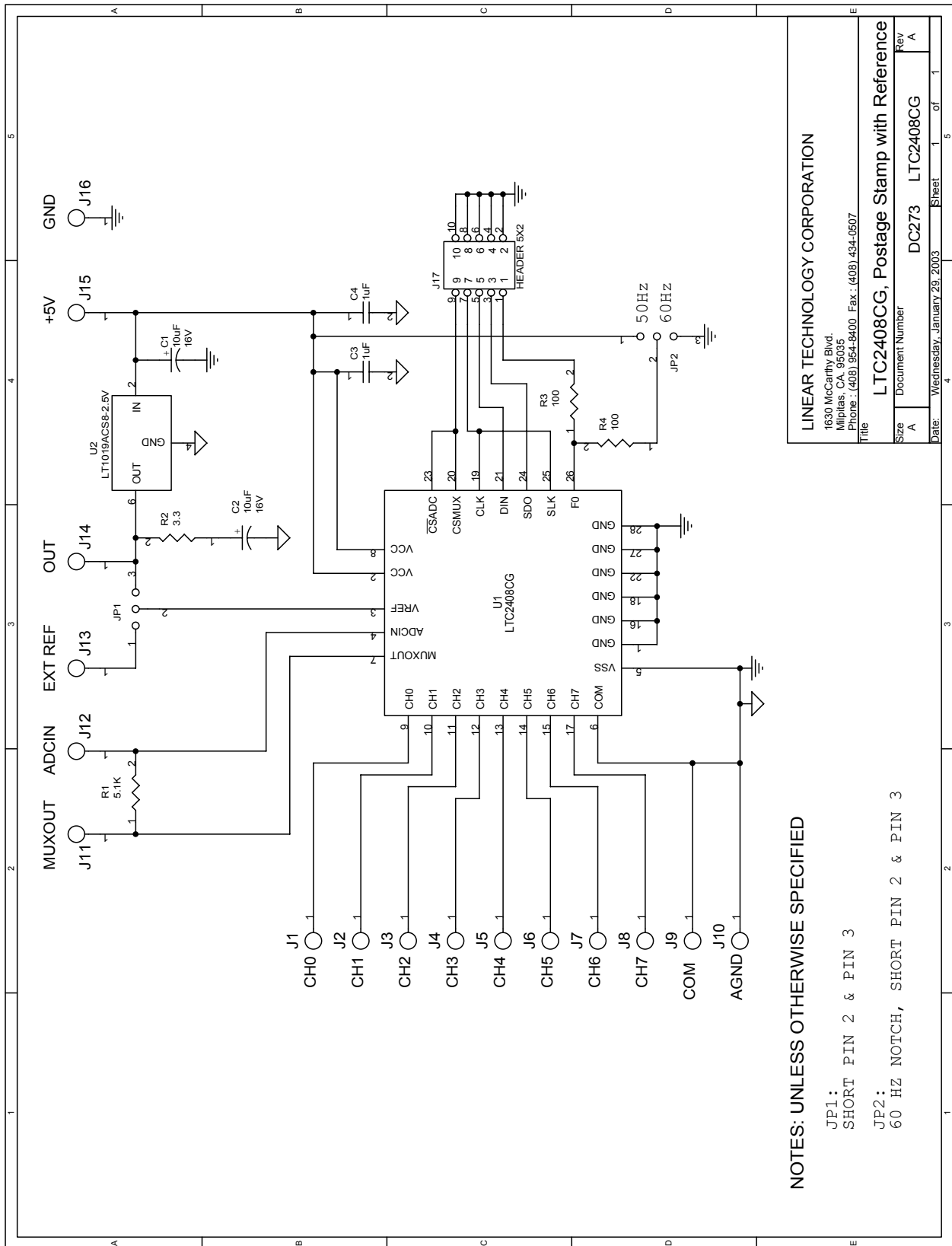
F0 is available on J17 for external conversion clock. See full data sheet for use of this line, otherwise, leave open. Use of external clock requires removal of JP2.

The LTC2408's F0 pin is available on J17 for those applications where an external oscillator controls the conversion time of the ADC. JP2 must be removed in this case. Please consult the LTC2408 data sheet for more information on the use of F0. If an external oscillator is not required, leave pin 1 on J17 open.

## PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	2	C1, C2	CAP., TAN 10 $\mu$ F 16V	AVX, TAJB106M016, 3528
2	2	C3, C4	CAP., X7R 1 $\mu$ F 10V	AVX, 0805ZC105KAT1A, 0805
3	1	R2	RES., CHIP 3.3 5%	TAD CR16-3R3JM, 0603
4	2	R3, R4	RES., CHIP 100 5%	TAD CR16-101JM, 0603
5	1	R1	RES., CHIP 5.1k 5%	TAD CR16-512JM, 0603
6	16	J1-J16	TERMINAL, TURRET .065"	MIL-MAX 2308-02
7	2	JP1-JP2	HEADER, 3 $\times$ 1 .079" CENTER	COMM CON 2802S-3G2
8	1	JP3	HEADER, 5 $\times$ 2 .079" CENTER	COMM CON 2202S-10G2
9	3	JP1-JP3	SHUNT, CCIJ2MM-138-G	COMM CON. CCIJ2MM-138-G
10	1	U2	IC., LT1019ACS8-2.5V	LINEAR LT1019ACS8-2.5V, S08
11	1	U1	IC., LTC2408CG	LINEAR LTC2408CG

**SCHEMATIC DIAGRAM**



**NOTES: UNLESS OTHERWISE SPECIFIED**

JP1: SHORT PIN 2 & PIN 3

JP2: 60 HZ NOTCH, SHORT PIN 2 & PIN 3

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