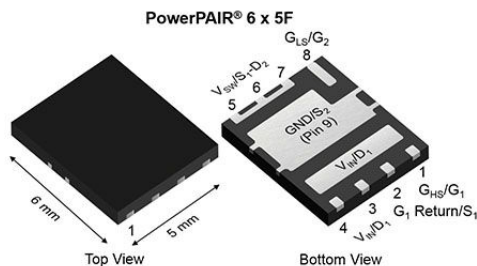


Dual N-Channel 30 V (D-S) MOSFET with Schottky Diode



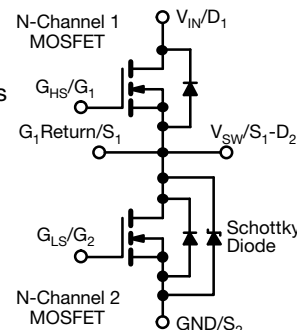
RoHS
COMPLIANT
HALOGEN
FREE

FEATURES

- TrenchFET® Gen IV power MOSFET
- SkyFET® low-side MOSFET with integrated Schottky
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- CPU core power
- Computer / server peripherals
- POL
- Synchronous buck converter
- Telecom DC/DC



PRODUCT SUMMARY		
	CHANNEL-1	CHANNEL-2
V _{DS} (V)	30	30
R _{DS(on)} max. (Ω) at V _{GS} = 10 V	0.00400	0.0019
R _{DS(on)} max. (Ω) at V _{GS} = 4.5 V	0.00670	0.0027
Q _g typ. (nC)	7	17.3
I _D (A) ^a	40	60
Configuration	Dual	

ORDERING INFORMATION		
Package	PowerPAIR 6 x 5F	
Lead (Pb)-free and halogen-free	SiZF918DT-T1-GE3	

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)						
PARAMETER		SYMBOL	CHANNEL-1	CHANNEL-2	UNIT	
Drain-source voltage		V _{DS}	30	30	V	
Gate-source voltage		V _{GS}	+20, -16	+16, -12		
Continuous drain current (T _J = 150 °C)	T _C = 25 °C	I _D	40 ^a	60 ^a	A	
	T _C = 70 °C		40 ^a	60 ^a		
	T _A = 25 °C		23 ^{b, c}	35 ^{b, c}		
	T _A = 70 °C		18.4 ^{b, c}	28 ^{b, c}		
Pulsed drain current (t = 100 μs)		I _{DM}	130	100		
Continuous source-drain diode current	T _C = 25 °C	I _S	22	60 ^a		
	T _A = 25 °C		2.8 ^{b, c}	6.1 ^{b, c}		
Single pulse avalanche current	L = 0.1 mH	I _{AS}	15	18		
Single pulse avalanche energy		E _{AS}	11.3	16	mJ	
Maximum power dissipation	T _C = 25 °C	P _D	26.6	50	W	
	T _C = 70 °C		17	32		
	T _A = 25 °C		3.4 ^{b, c}	3.7 ^{b, c}		
	T _A = 70 °C		2.2 ^{b, c}	2.4 ^{b, c}		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150		°C	
Soldering recommendations (peak temperature) ^{d, e}			260			

THERMAL RESISTANCE RATINGS							
PARAMETER		SYMBOL	CHANNEL-1		CHANNEL-2		UNIT
			TYP.	MAX.	TYP.	MAX.	
Maximum junction-to-ambient ^{b, f}	t ≤ 10 s	R _{thJA}	30	37	27	34	°C/W
Maximum junction-to-case (source)	Steady state	R _{thJC}	3.8	4.7	2	2.5	

Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- t = 10 s
- See solder profile (www.vishay.com/doc?73257). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 77 °C/W for channel-1 and 70 °C/W for channel-2



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)									
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT		
Static									
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	Ch-1	30	-	-	V		
			Ch-2	30	-	-			
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	Ch-1	1.1	-	2.4			
			Ch-2	1.0	-	2.3			
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = +20 V, -16 V	Ch-1	-	-	± 100	nA		
		V _{DS} = 0 V, V _{GS} = +16 V, -12 V	Ch-2	-	-	± 100			
Zero Gate voltage drain current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	Ch-1	-	-	1	μA		
			Ch-2	-	20	350			
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C	Ch-1	-	-	5			
			Ch-2	-	200	3000			
On-state drain current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	Ch-1	20	-	-	A		
			Ch-2	20	-	-			
Drain-source on-state resistance ^b	R _{DS(on)}	V _{GS} = 10 V, I _D = 10 A	Ch-1	-	0.00290	0.00400	Ω		
		V _{GS} = 10 V, I _D = 10 A	Ch-2	-	0.00120	0.00190			
		V _{GS} = 4.5 V, I _D = 5 A	Ch-1	-	0.00470	0.00680			
		V _{GS} = 4.5 V, I _D = 5 A	Ch-2	-	0.00180	0.00270			
Forward transconductance ^b	g _{fs}	V _{DS} = 10 V, I _D = 20 A	Ch-1	-	53	-	S		
		V _{DS} = 10 V, I _D = 20 A	Ch-2		87	-			
Dynamic ^a									
Input capacitance	C _{iss}	Channel-1 V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	Ch-1	-	1060	-	pF		
Output capacitance	C _{oss}		Ch-2	-	2650	-			
			Ch-1	-	600	-			
			Ch-2	-	1240	-			
Reverse transfer capacitance	C _{rss}	Channel-2 V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	Ch-1	-	45	-			
C _{rss} /C _{iss} ratio			Ch-2	-	140	-			
	Total gate charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 10 A	Ch-1	-	14.6	22	nC	
			Ch-2	-	37	56			
Gate-source charge	Q _{gs}	Channel-1 V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 10 A	Ch-1	-	7	11			
			Ch-2	-	17.4	27			
		Gate-drain charge	Q _{gd}	Channel-2 V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 10 A	Ch-1	-	3		-
					Ch-2	-	6.1		-
Output charge	Q _{oss}	V _{DS} = 15 V, V _{GS} = 0 V	Ch-1	-	1.5	-			
			Ch-2	-	3.5	-			
Gate resistance	R _g	f = 1 MHz	Ch-1	-	14	-			
			Ch-2	-	31	-			
Turn-on delay time	t _{d(on)}	Channel-1 V _{DD} = 15 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 4.5 V, R _g = 1 Ω	Ch-1	0.2	1	2	Ω		
			Ch-2	0.1	0.50	1.00			
Turn-off delay time	t _{d(off)}	Channel-2 V _{DD} = 15 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 4.5 V, R _g = 1 Ω	Ch-1	-	17	35	ns		
			Ch-2	-	22	45			
			Ch-1	-	45	90			
			Ch-2	-	55	110			
Fall time	t _f	Channel-2 V _{DD} = 15 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 4.5 V, R _g = 1 Ω	Ch-1	-	20	40			
			Ch-2	-	30	60			
Turn-on delay time	t _{d(on)}	Channel-1 V _{DD} = 15 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 4.5 V, R _g = 1 Ω	Ch-1	-	10	20			
			Ch-2	-	10	20			
Rise time	t _r	Channel-1 V _{DD} = 15 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 10 V, R _g = 1 Ω	Ch-1	-	10	20			
			Ch-2	-	15	30			
Turn-off delay time	t _{d(off)}	Channel-2 V _{DD} = 15 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 10 V, R _g = 1 Ω	Ch-1	-	5	10			
			Ch-2	-	26	50			
Fall time	t _f	Channel-2 V _{DD} = 15 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 10 V, R _g = 1 Ω	Ch-1	-	20	40			
			Ch-2	-	30	60			
Turn-on delay time	t _{d(on)}	Channel-1 V _{DD} = 15 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 10 V, R _g = 1 Ω	Ch-1	-	10	20			
			Ch-2	-	15	30			
Rise time	t _r	Channel-2 V _{DD} = 15 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 10 V, R _g = 1 Ω	Ch-1	-	5	10			
			Ch-2	-	26	50			
Turn-off delay time	t _{d(off)}	Channel-2 V _{DD} = 15 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 10 V, R _g = 1 Ω	Ch-1	-	20	40			
			Ch-2	-	30	60			
Fall time	t _f	Channel-2 V _{DD} = 15 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 10 V, R _g = 1 Ω	Ch-1	-	5	10			
			Ch-2	-	5	10			

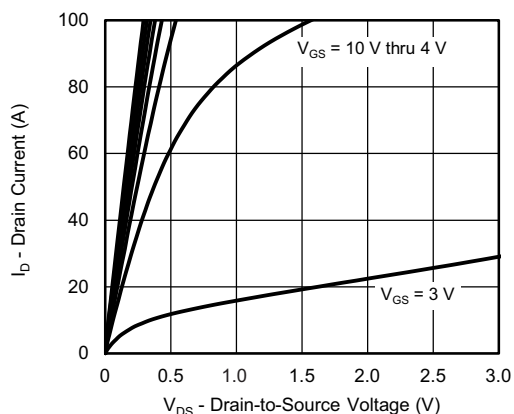
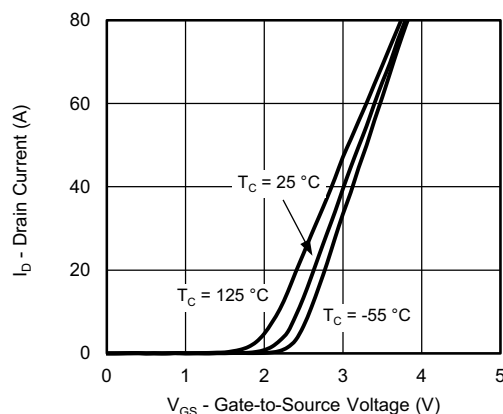
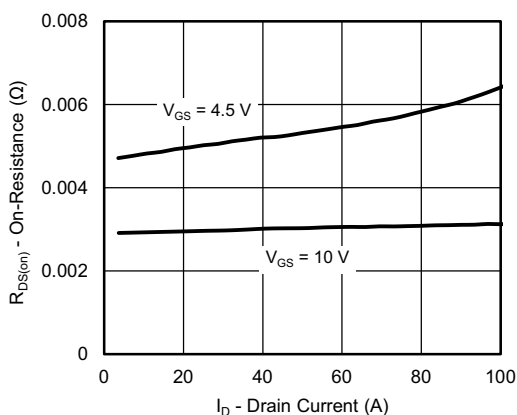
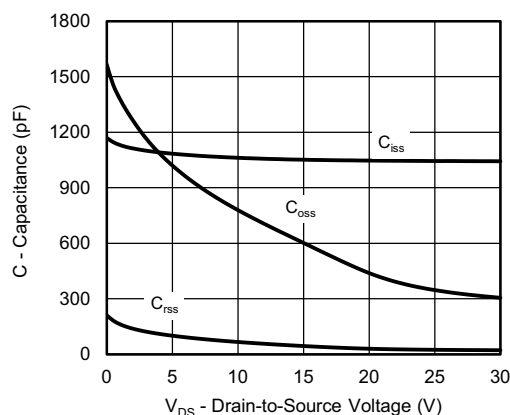
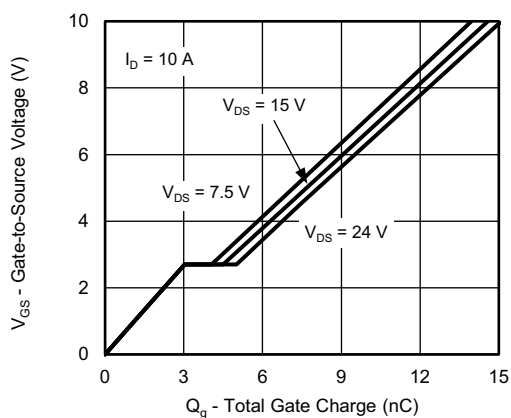
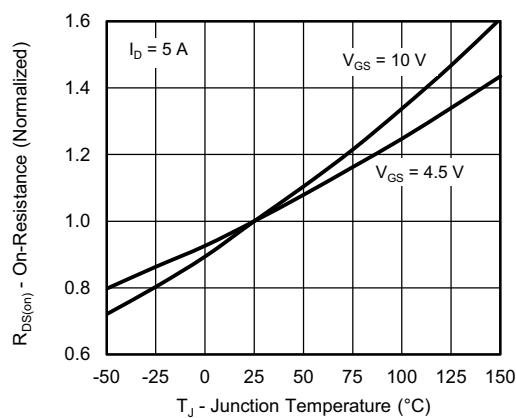


SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	T _C = 25 °C	Ch-1	-	-	22	A
			Ch-2	-	-	60	
Pulse diode forward current ^a	I _{SM}		Ch-1	-	-	130	
			Ch-2	-	-	100	
Body diode voltage	V _{SD}	I _S = 5 A, V _{GS} = 0 V	Ch-1	-	0.8	1.2	V
		I _S = 3 A, V _{GS} = 0 V	Ch-2	-	0.40	0.60	
Body diode reverse recovery time	t _{rr}	Channel-1 I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C Channel-2 I _F = 5 A, di/dt = 100 A/μs, T _J = 25 °C	Ch-1	-	32	70	ns
			Ch-2	-	55	110	
Body diode reverse recovery charge	Q _{rr}		Ch-1	-	24	50	nC
			Ch-2	-	66	135	
Reverse recovery fall time	t _a		Ch-1	-	18	-	ns
			Ch-2	-	27	-	
Reverse recovery rise time	t _b		Ch-1	-	14	-	
			Ch-2	-	28	-	

Notes

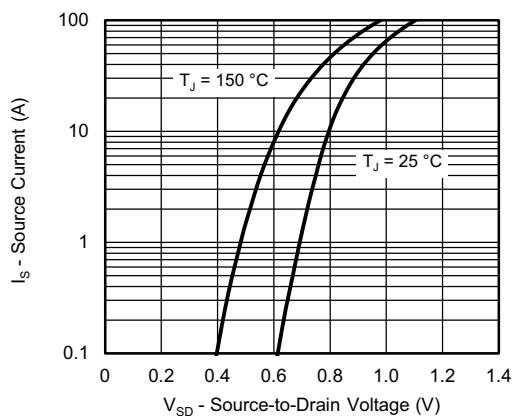
- a. Guaranteed by design, not subject to production testing
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

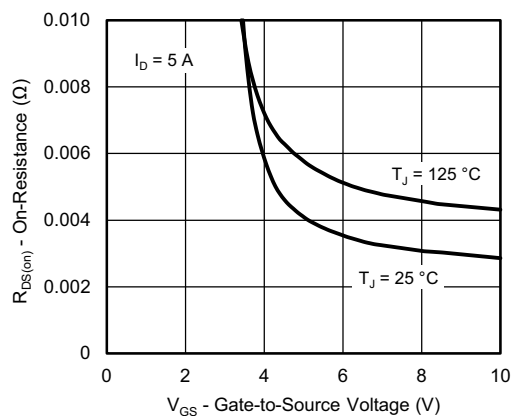
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature



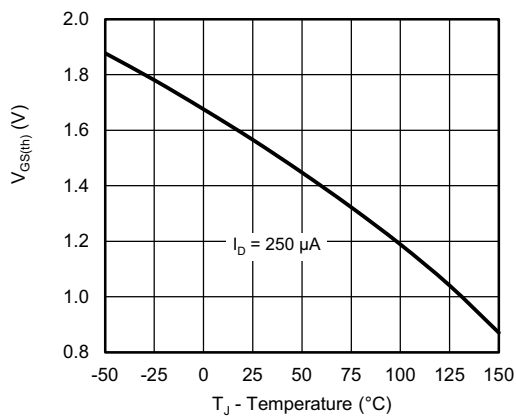
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



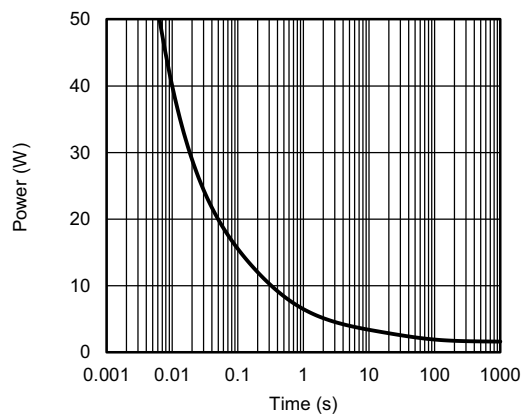
Source-Drain Diode Forward Voltage



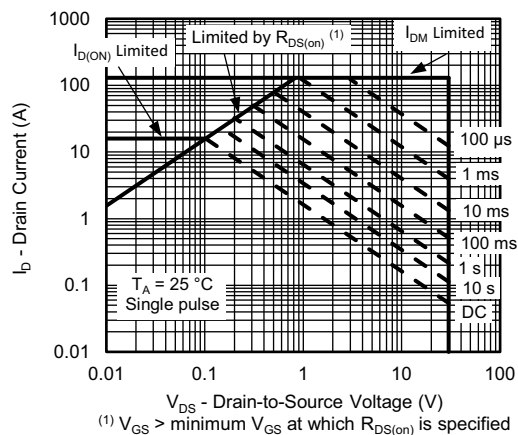
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



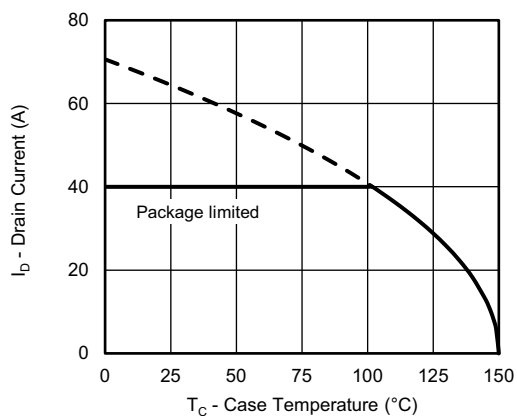
Single Pulse Power, Junction-to-Ambient



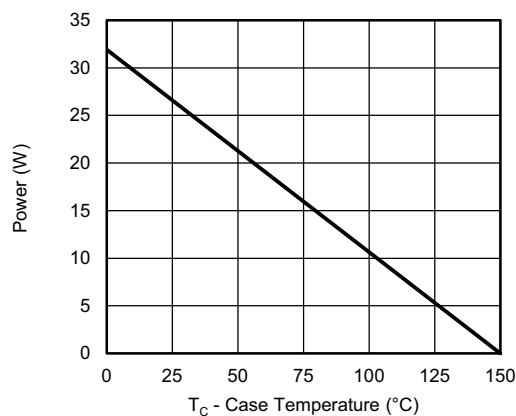
Safe Operating Area, Junction-to-Ambient



CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



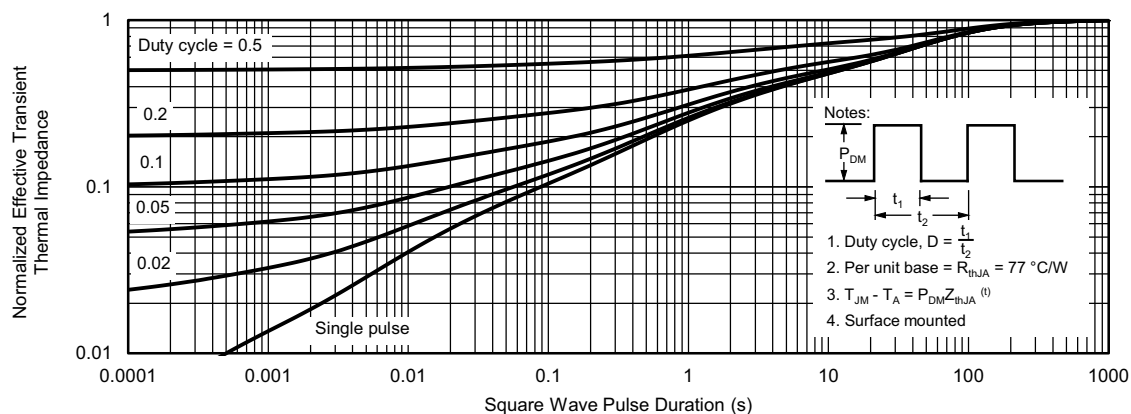
Power, Junction-to-Case

Note

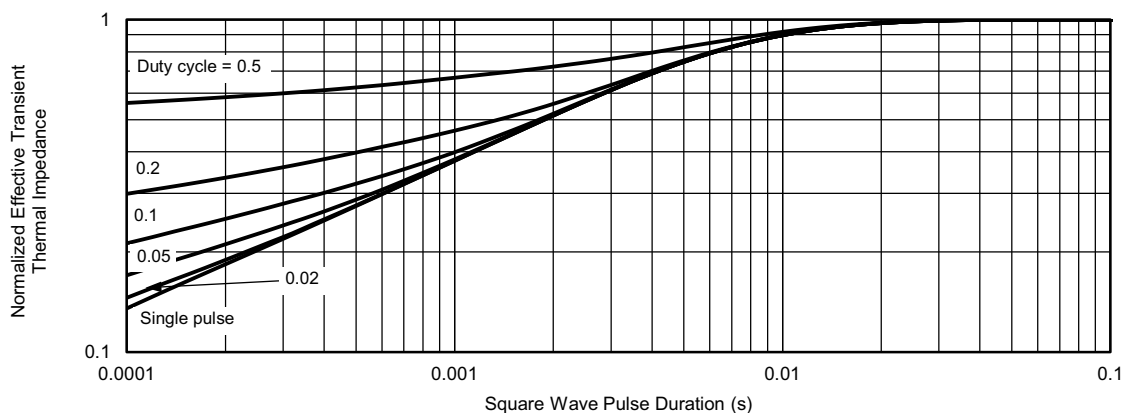
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



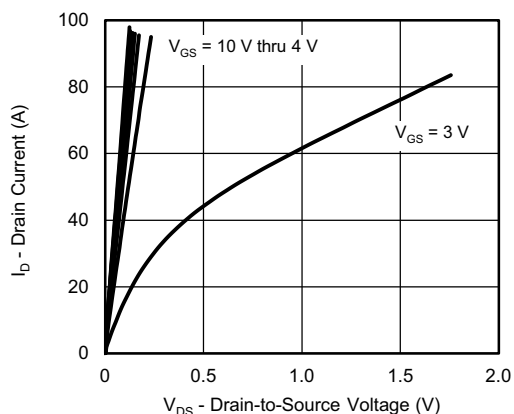
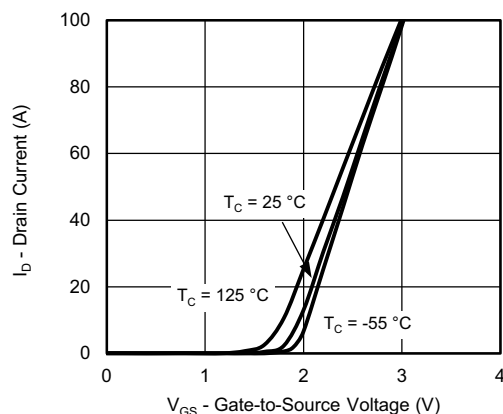
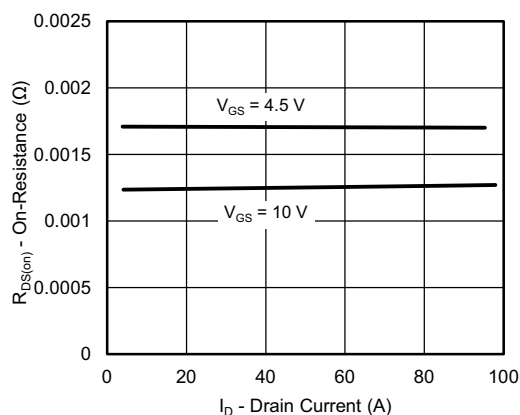
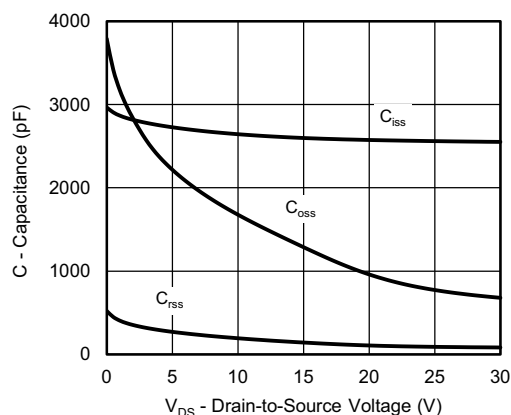
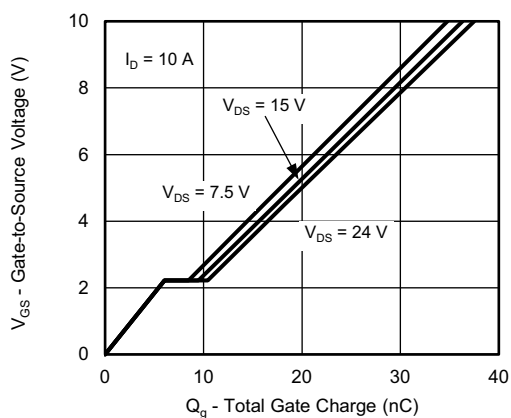
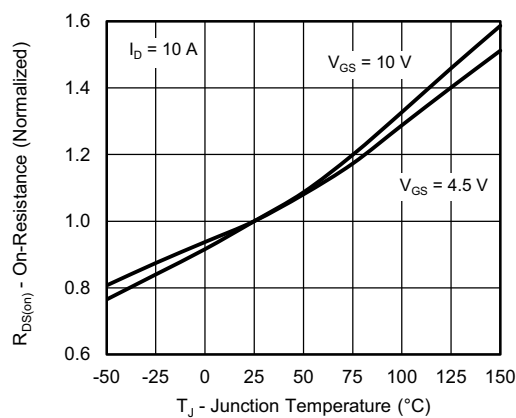
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

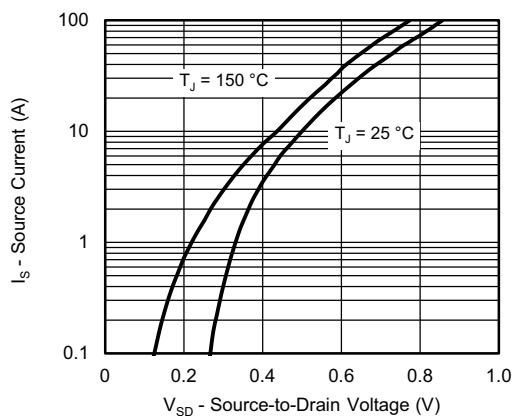
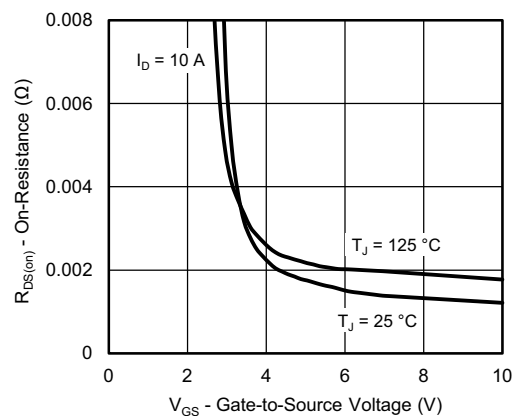
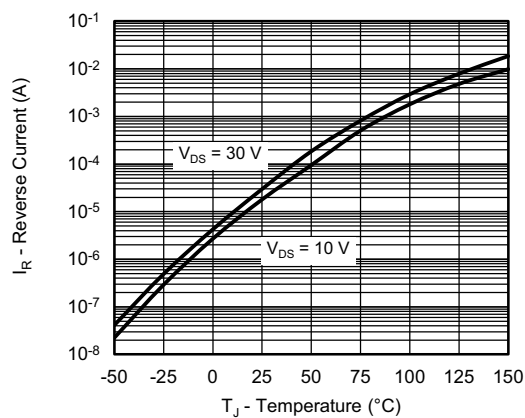
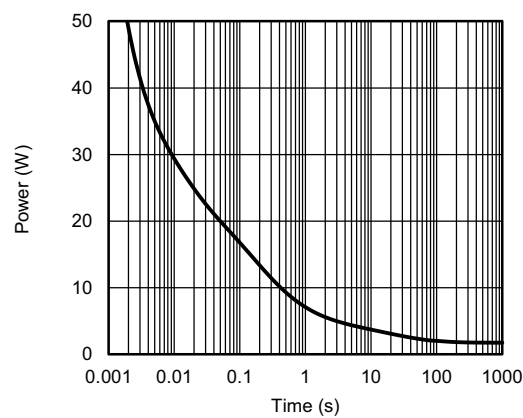
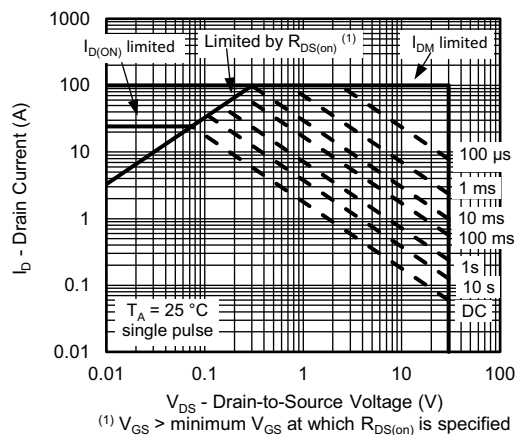


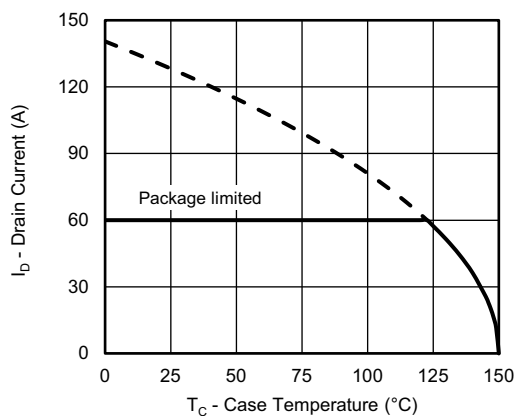
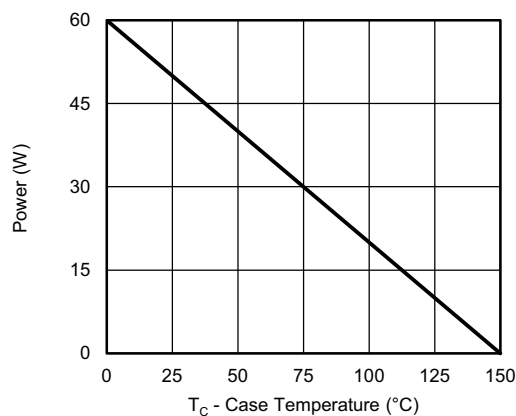
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

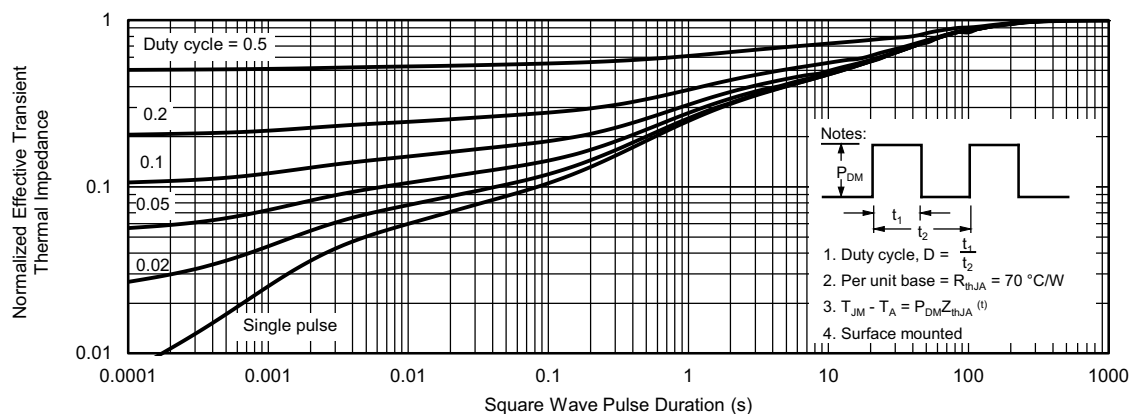
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Reverse Current (Schottky)

Single Pulse Power, Junction-to-Ambient

Safe Operating Area, Junction-to-Ambient

CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating ^a

Power, Junction-to-Case
Note

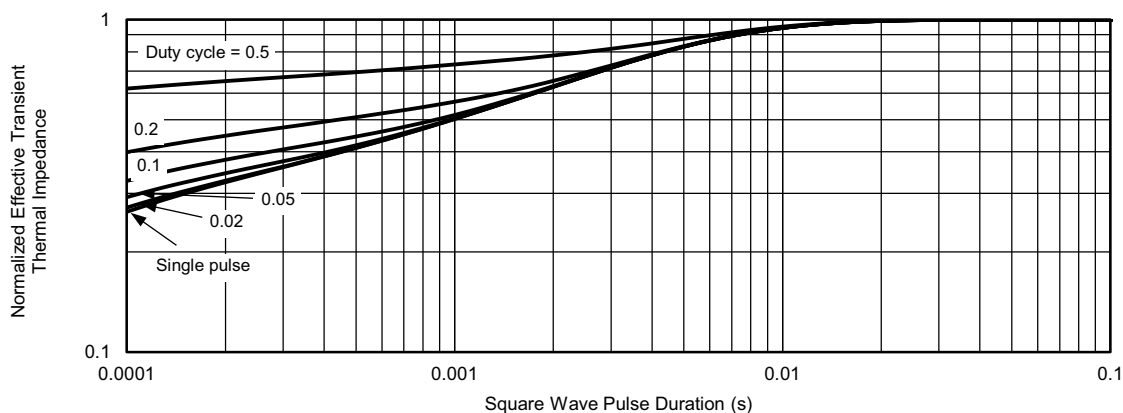
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

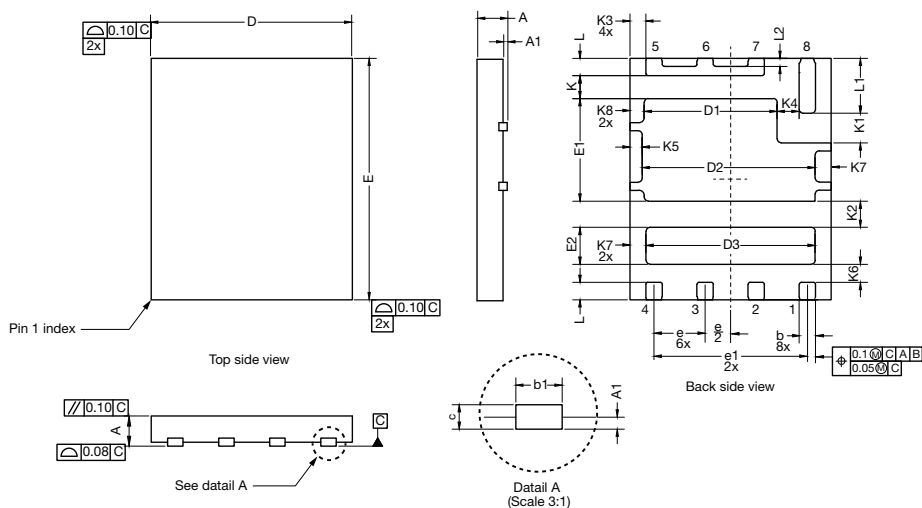


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75963.



PowerPAIR® 6 x 5 F Case Outline



DIMENSION	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	-	0.10	0.000	-	0.004
b	0.35	0.41	0.46	0.014	0.016	0.018
b1	0.38 ref.			0.015 ref.		
c	0.15	0.20	0.25	0.006	0.008	0.010
D	4.90	5.00	5.10	0.193	0.197	0.201
D1	3.26	3.31	3.36	0.128	0.130	0.132
D2	4.20	4.30	4.40	0.165	0.169	0.173
D3	4.15	4.20	4.25	0.163	0.165	0.167
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	2.50	2.55	2.60	0.098	0.100	0.102
E2	0.87	0.92	0.97	0.034	0.036	0.038
e	1.27 BSC			0.050 BSC		
e1	3.81 BSC			0.150 BSC		
K	0.52	0.57	0.62	0.020	0.022	0.024
K1	0.69	0.74	0.79	0.027	0.029	0.031
K2	0.60	0.65	0.70	0.024	0.026	0.028
K3	0.60 BSC			0.024 BSC		
K4	0.50	0.55	0.60	0.020	0.022	0.024
K5	0.25	0.30	0.35	0.010	0.012	0.014
K6	0.40	0.45	0.50	0.016	0.018	0.020
K7	0.35	0.40	0.45	0.014	0.016	0.018
K8	0.30	0.35	0.40	0.012	0.014	0.016
L	0.33	0.43	0.53	0.013	0.017	0.021
L1	1.31	1.36	1.41	0.052	0.054	0.056
L2	0.20 ref.			0.008 ref.		
ECN: T18-0249-Rev. B, 28-May-2018						
DWG: 6043						

Note

- Millimeters will govern



Disclaimer

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