2×20W STEREO CLASS-D AUDIO AMPLIFIER WITH POWER LIMIT

Preliminary Information
May 2018

DESCRIPTION

The IS31AP2112 is a high efficiency stereo Class-D audio amplifier with adjustable power limit function. The loudspeaker driver operates from 4.5V~26V supply voltage and analog circuit operates at 5V supply voltage. It can deliver 20W/CH output power into 8Ω loudspeaker within 1% THD+N at 24V supply voltage and without external heat sink when playing music.

IS31AP2112 provides parallel BTL (Mono) application, and it can deliver 40W into 4Ω loudspeaker at 24V supply voltage. The adjustable power limit function allows user to set a voltage rail lower than half of 5V to limit the amount of current through the speaker.

Output DC detection prevents speaker damage from long-time current stress. IS31AP2112 provides the spread spectrum function to improve EMI performance. The output short circuit and over temperature protection include auto-recovery feature.

APPLICATIONS

- TV audio
- Boom-box
- Powered speaker
- Monitors
- Consumer audio equipment

FEATURES

- Single supply voltage
- 4.5V ~ 26V for loudspeaker driver
- Built-in LDO output 5V for others
- Loudspeaker power from 24V supply
- BTL Mode: 20W/CH into 8Ω @<1% THD+N
- PBTL Mode: 40W/CH into 4Ω @<10% THD+N
- Loudspeaker power from 12V supply
- BTL Mode: 10W/CH into 8Ω @10% THD+N
- 88% efficient Class-D operation eliminates need for heat sink
- Differential inputs
- Four selectable, fixed gain settings
- Internal oscillator
- Short-circuit protection with auto recovery option
- Under-voltage detection
- Over-voltage protection
- Pop noise and click noise reduction
- Adjustable power limit function for speaker protection
- Output DC detection for speaker protection
- Spread spectrum to optimize EMI
- Over temperature protection with auto recovery
- Superior EMC performance

TYPICAL APPLICATION CIRCUIT

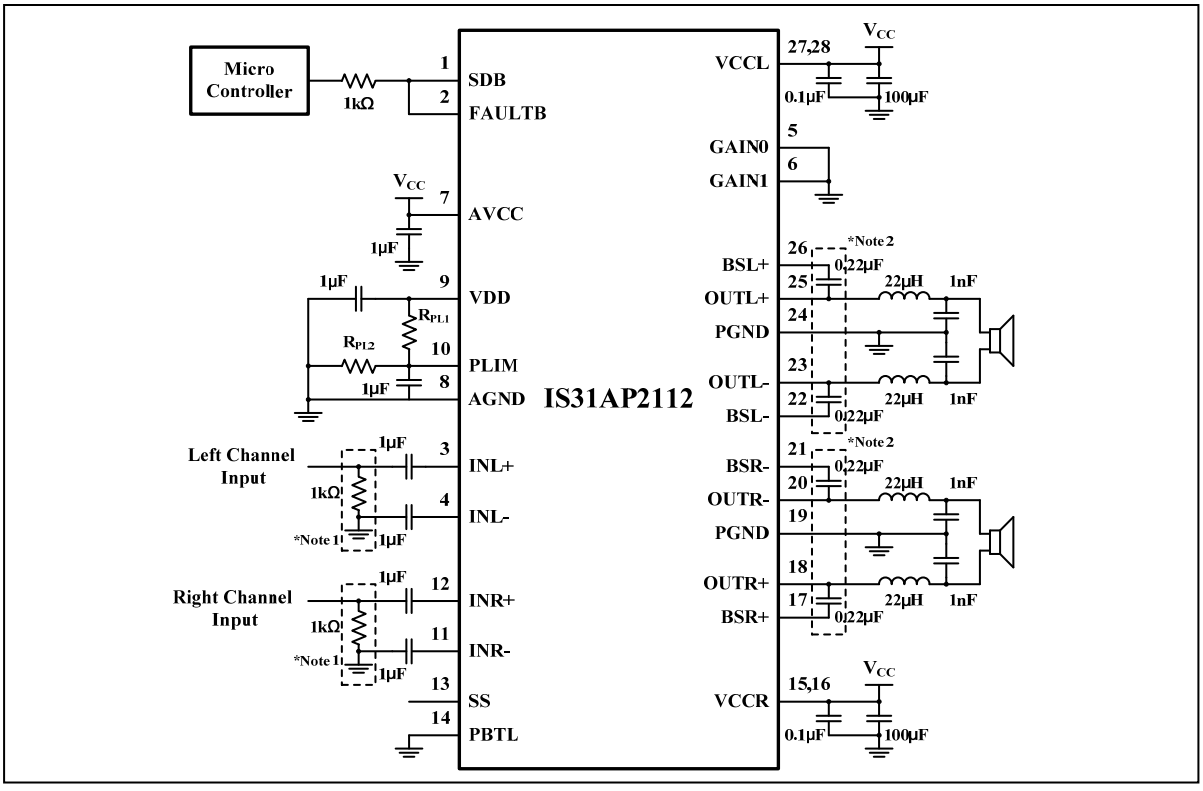


Figure 1 Typical Application Circuit For BTL (Stereo) Mode Configuration And Single-Ended Input

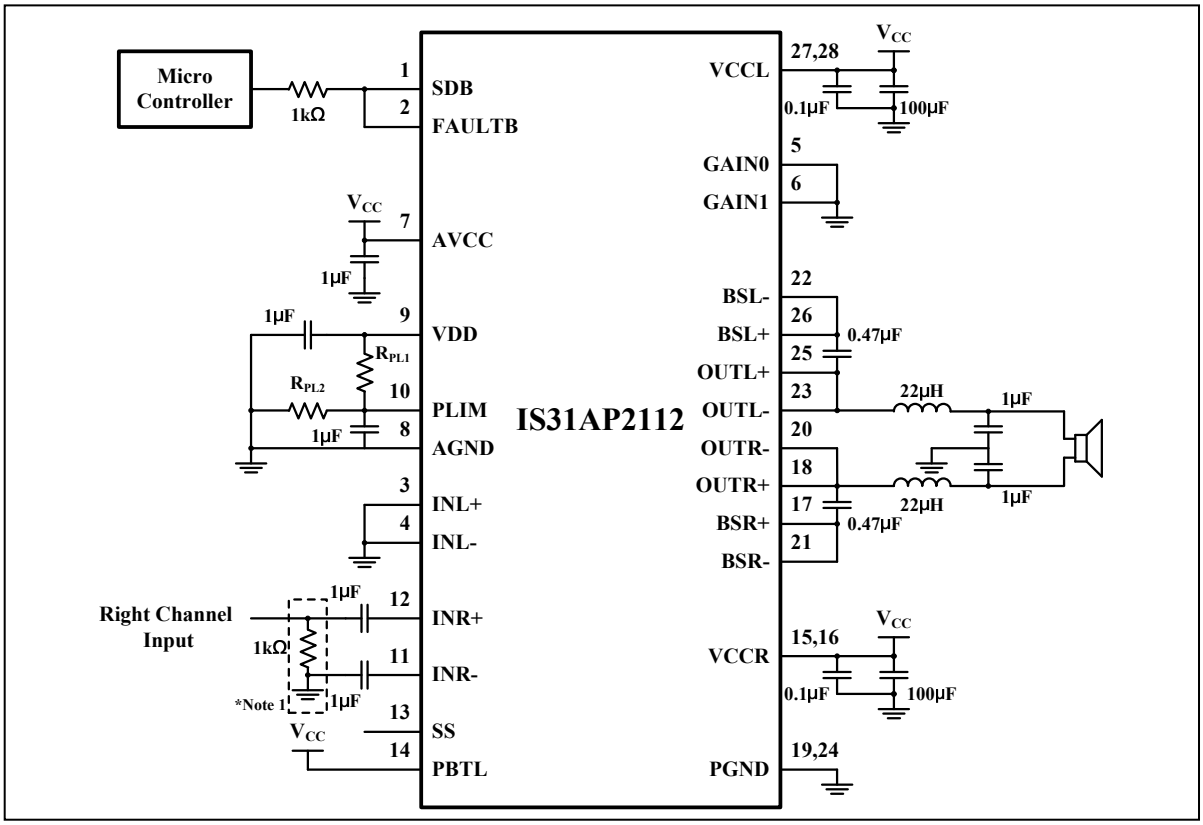
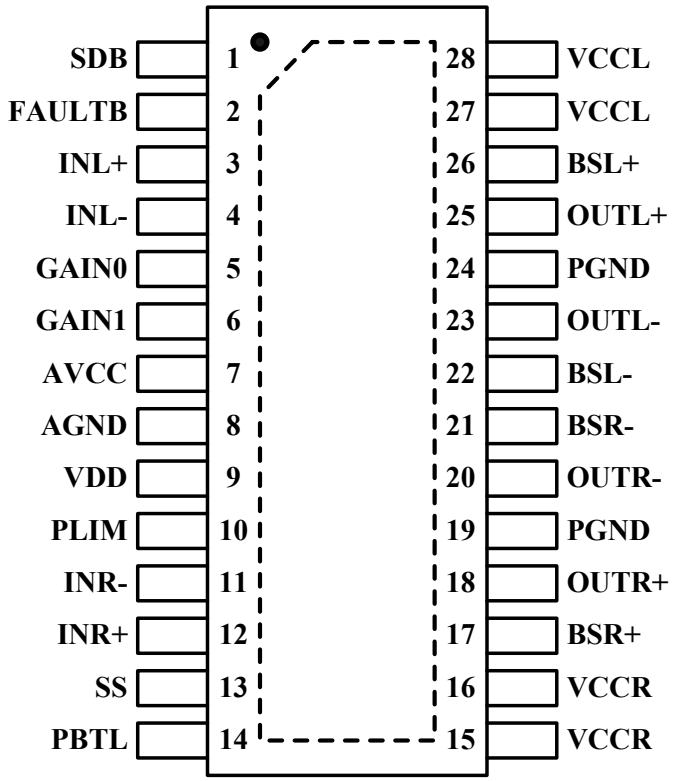


Figure 2 Typical Application Circuit For Parallel BTL (Mono) Mode Configuration And Single-Ended Input

Note 1: These resistances must be connected to ground, resistance= 1kΩ.
Note 2: These capacitors should be change to 0.47μF, while the V_{CC}≤ 5V.
Note 3: Be noted that input should be applied on R-channel only for Mono application.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
eTSSOP-28	

PIN DESCRIPTION

No.	Pin	Description
1	SDB	Shutdown signal for IC (low = disabled, high = operational). Voltage compliance to AVCC.
2	FAULTB	Open drain output used to display short circuit or dc detect fault. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting FAULTB pin to SDB pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling AVCC.
3	INL+	Positive audio input for left channel. Biased at 2.5V.
4	INL-	Negative audio input for left channel. Biased at 2.5V.
5	GAIN0	Gain select least significant bit. Voltage compliance to AVCC.
6	GAIN1	Gain select most significant bit. Voltage compliance to AVCC.
7	AVCC	Analog supply.
8	AGND	Analog signal ground. Connect to the thermal pad.
9	VDD	5V regulated output, also used as supply for PLIMIT function.
10	PLIMIT	Power limit level adjustment. Connect a resistor divider from VDD to GND to set power limit. Give V_{PLIMIT} <2.4V to set power limit level. Connect to V_{DD} (>2.4V) or GND to disable power limit function.
11	INR-	Negative audio input for right channel.
12	INR+	Positive audio input for right channel.
13	SS	Spread spectrum enable pin. Internally pulled up to 5V. Floating to enable and grounded to disable.
14	PBTL	Parallel BTL mode switch, high for parallel BTL output. Voltage compliance to AVCC.
15,16	VCCR	High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connect internal.
17	BSR+	Bootstrap I/O for right channel, positive high side FET.
18	OUTR+	Class-D H-bridge positive output for right channel.
19	PGND	Power ground for the H-bridges.
20	OUTR-	Class-D H-bridge negative output for right channel.
21	BSR-	Bootstrap I/O for right channel, negative high side FET.
22	BSL-	Bootstrap I/O for left channel, negative high side FET.
23	OUTL-	Class-D H-bridge negative output for left channel.
24	PGND	Power ground for the H-bridges.
25	OUTL+	Class-D H-bridge positive output for left channel.
26	BSL+	Bootstrap I/O for left channel, positive high side FET.
27,28	VCCL	High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connect internal.
Thermal Pad		Must be soldered to PCB's ground plane.

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31AP2112-ZLS2-TR	eTSSOP-28, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC} (VCCL, VCCR, AVCC)	-0.3V~30V
Interface pin voltage (SDB, GAIN0, GAIN1, PBTL, FAULTB) (SS, PLIMIT)	-0.3V~ 30V -0.3V~ 5.5V
Minimum load resistance, BTL: V_{CC}> 13V BTL: V_{CC}≤ 13V PBTL	4.8Ω (Min.) 3.2Ω (Min.) 3.2Ω (Min.)
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C~+85°C
Package thermal resistance, junction to ambient (4 layer standard test PCB based on JEDEC standard), θ_{JA}	28°C/W
ESD (HBM) ESD (CDM)	±2kV ±500V

Note 4: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{CC}	Supply voltage	AVCC, VCCL, VCCR	4.5	26	V
V_{IH}	High-level input voltage	SDB, GAIN0, GAIN1, PBTL, SS	2		V
V_{IL}	Low-level input voltage	SDB, GAIN0, GAIN1, PBTL, SS		0.8	V
V_{OL}	Low-level output voltage	FAULTB, $R_{PULL-UP}$= 100kΩ, V_{CC}= 16V		0.8	V
I_{IH}	High-level input current	SDB, GAIN0, GAIN1, PBTL, SS, V_I= 2V, V_{CC}= 18V		50	μA
I_{IL}	Low-level input current	SDB, GAIN0, GAIN1, PBTL, SS, V_I= 0.8V, V_{CC}= 18V		5	μA
I_{OH}	High-level output current	V_I= 2V, V_{CC}= 18V		50	μA
I_{OL}	Low-level output current	V_I= 0.8V, V_{CC}= 18V		50	μA
T_A	Operating free-air temperature		-40	85	°C

GENERAL ELECTRICAL CHARACTERISTICS

V_{CC}= 24V, R_L= 8Ω, T_A= 25°C (unless otherwise noted)

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
I_{CC}	Quiescent supply current	V_{SDB}= 2V, no load, V_{CC}= 12V			20	35	mA
I_{SD}	Quiescent supply current in shutdown mode	V_{SDB}= 0.8V, no load, V_{CC}= 12V			<12	25	μA
R_{DS_ON}	Drain-source on-state resistance-High side NMOS	V_{CC}= 12V, I_d= 500mA, T_J= 25°C			220		mΩ
	Drain-source on-state resistance-Low side NMOS				220		mΩ
$\|V_{OS}\|$	Class-D output offset voltage (measured differential)	V_{CC}= 12V, V_I= 0V, Gain= 36dB			1.5	15	mV
t_{ON}	Turn-on time	V_{SDB}= 2V			90		ms
t_{OFF}	Turn-off time	V_{SDB}= 0.8V			2		μs
V_{DD}	Regulator output	I_{VDD}= 0.1mA		4.75	5	5.25	V
GAIN	Gain	GAIN1= 0.8V	GAIN0= 0.8V	18	20	22	dB
			GAIN0= 2V	24	26	28	
		GAIN1= 2V	GAIN0= 0.8V	30	32	34	
			GAIN0= 2V	34	36	38	

ELECTRICAL CHARACTERISTICS AND SPECIFICATIONS OF LOUDSPEAKER DRIVER

V_{CC}= 24V, R_L= 8Ω, with passive LC low-pass filter (L= 22μH, C= 1μF).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
P_O	Output power	THD+N= 0.05%, f= 1kHz, V_{CC}= 24V		20		W
		THD+N= 10%, f= 1kHz, V_{CC}= 12V		10		
THD+N	Total harmonic distortion plus noise	V_{CC}= 24V, R_L= 8Ω, f= 1kHz, P_O= 10W (half-power)		0.038		%
		V_{CC}= 12V, R_L= 8Ω, f= 1kHz, P_O= 5W (half-power)		0.035		
SNR	Signal to noise ratio	Maximum output at THD+N<1%, f= 1kHz, Gain= 20dB, a-weighted		103		dB
V_{NO}	Output integrated noise	f= 20Hz ~ 20kHz, Gain= 20dB, a-weighted filter, R_L= 8Ω		93		μV
PSRR	Power Supply Rejection Ratio	V_{Ripple}= 200mVpp at 1kHz, Gain= 20dB, inputs ac-grounded		-60		dB
Crosstalk	Crosstalk	f= 1kHz, V_O= 1Vrms, Gain= 20dB		-90		dB
f_{OSC}	Oscillator frequency		250	310	370	kHz
R_{SS}	Spread spectrum frequency range			±15		%
T_{SENSOR}	Thermal trip point			150		°C
	Thermal hysteresis			25		°C

TYPICAL PERFORMANCE CHARACTERISTICS

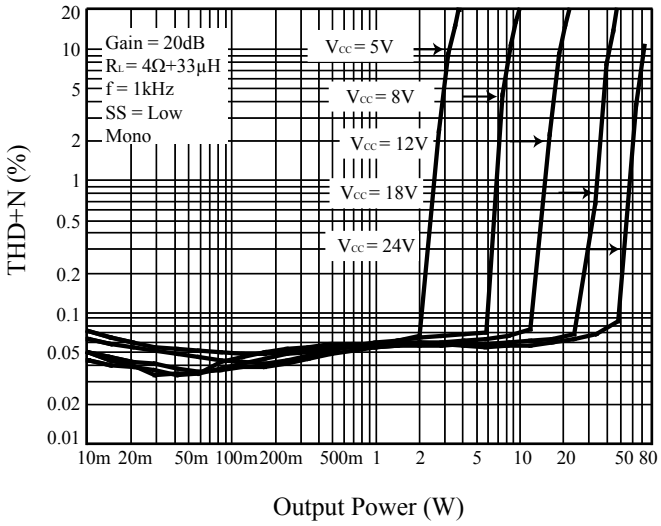


Figure 3 THD+N vs. Output Power

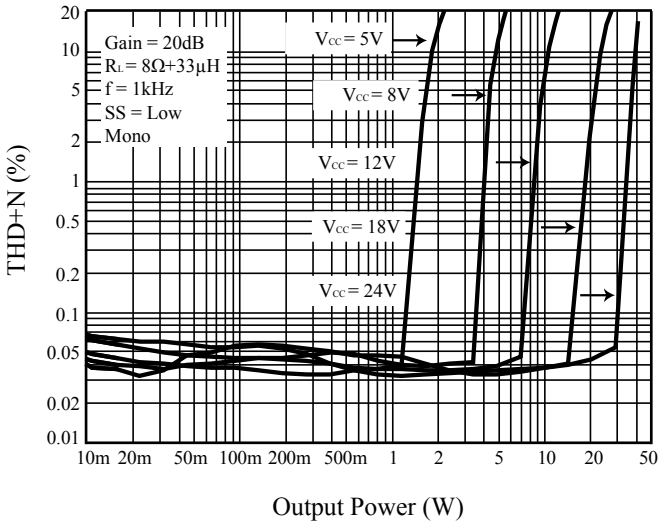


Figure 4 THD+N vs. Output Power

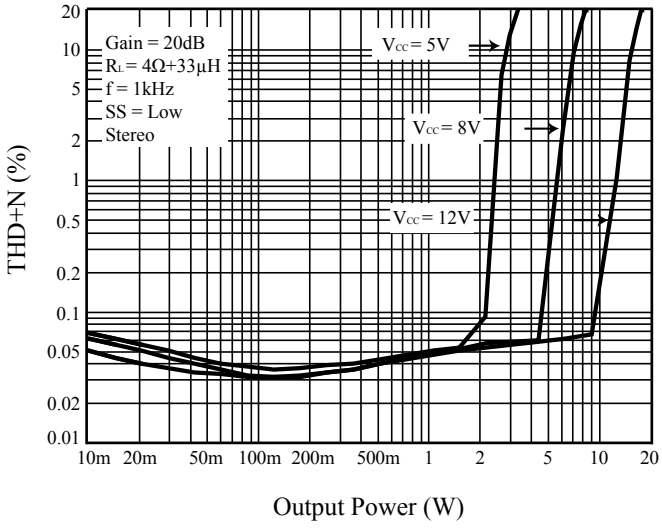


Figure 5 THD+N vs. Output Power

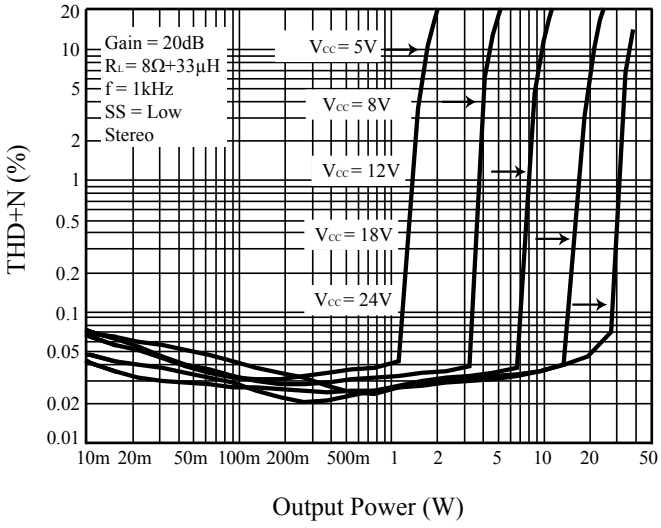


Figure 6 THD+N vs. Output Power

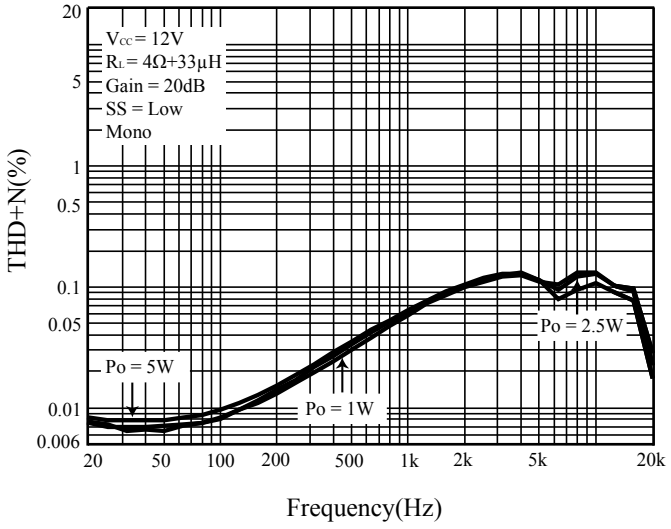


Figure 7 THD+N vs. Frequency

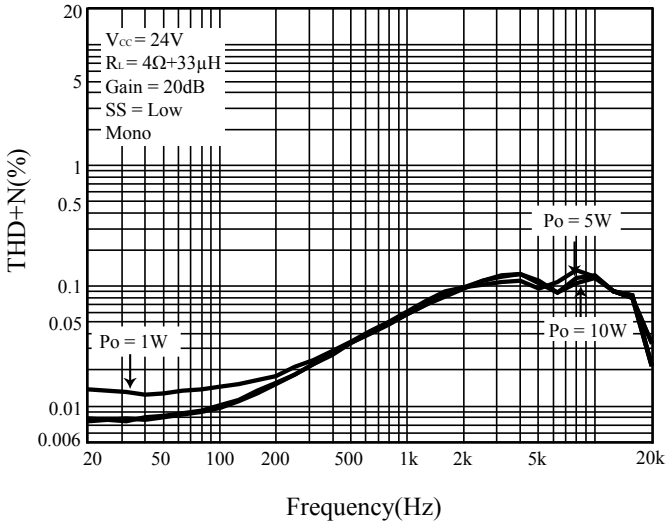


Figure 8 THD+N vs. Frequency

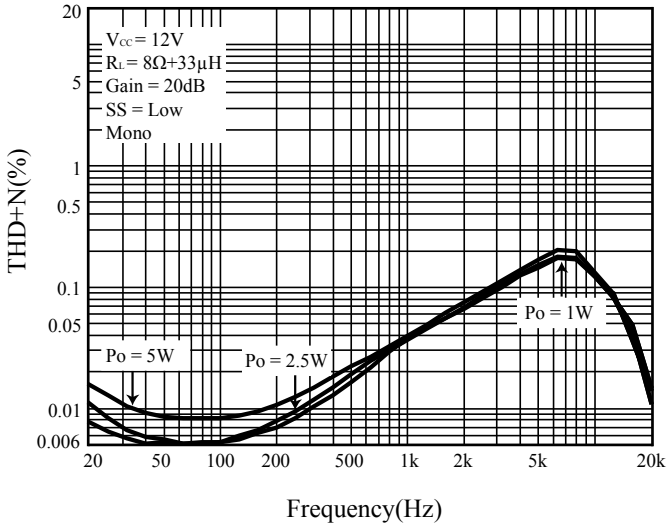


Figure 9 THD+N vs. Frequency

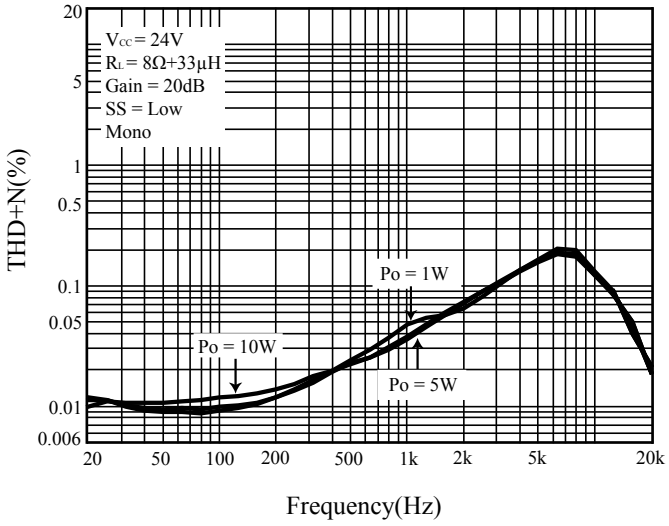


Figure 10 THD+N vs. Frequency

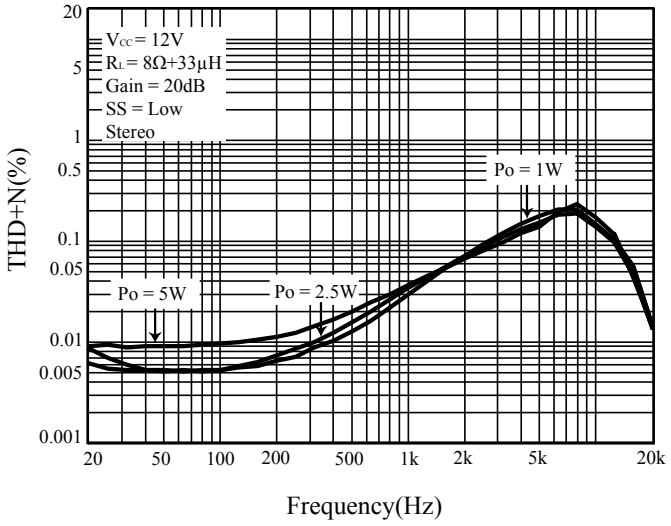


Figure 11 THD+N vs. Frequency

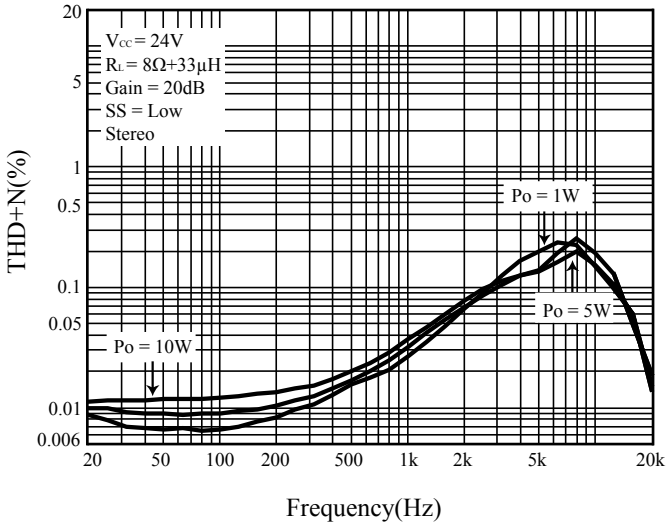


Figure 12 THD+N vs. Frequency

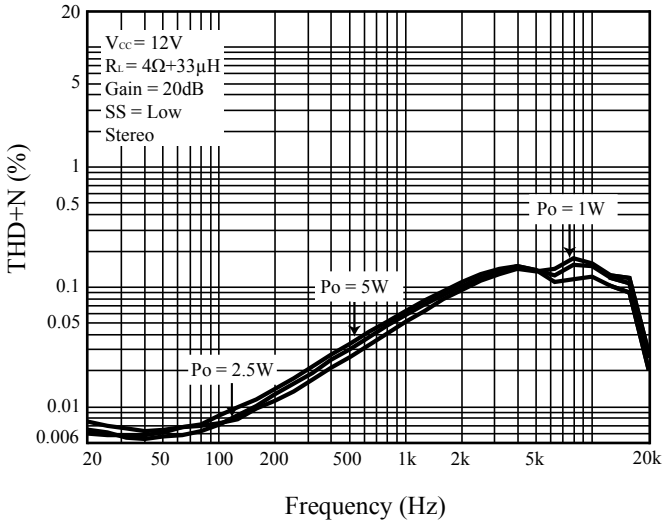


Figure 13 THD+N vs. Frequency

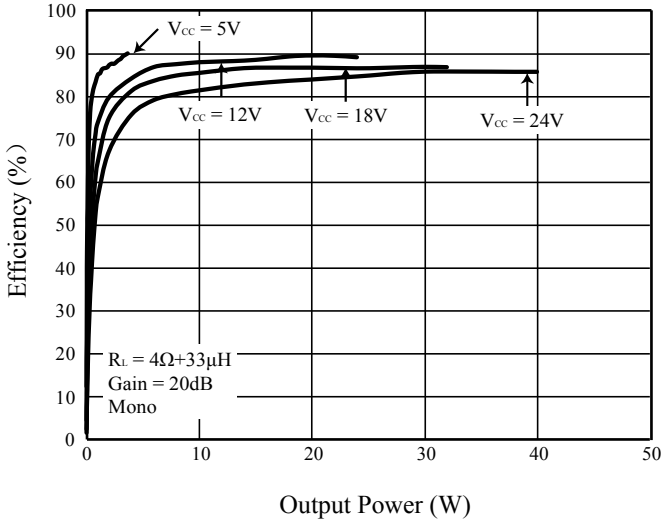


Figure 14 Efficiency vs. Output Power

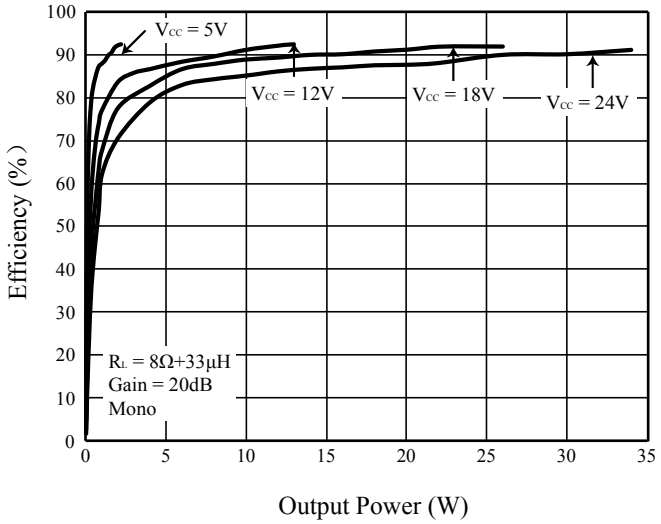


Figure 15 Efficiency vs. Output Power

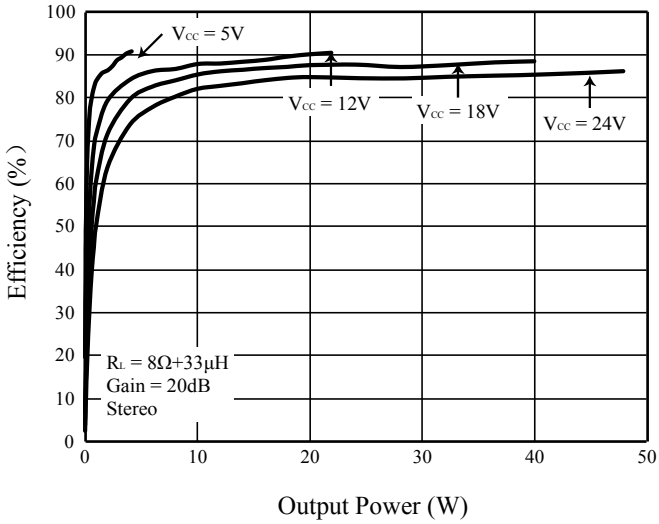


Figure 16 Efficiency vs. Output Power

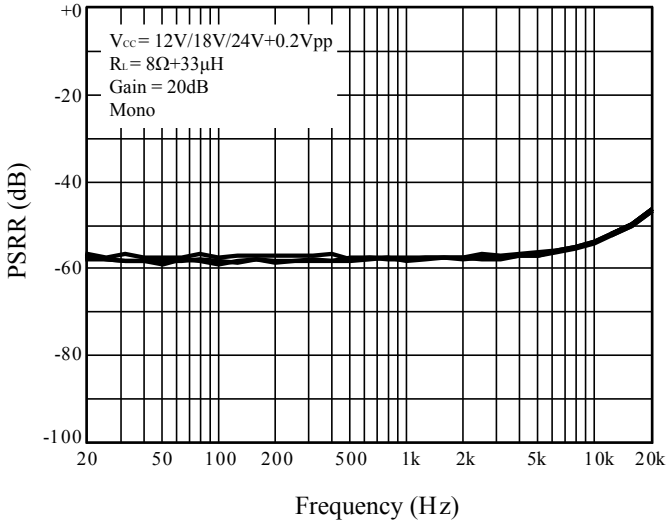


Figure 17 PSRR

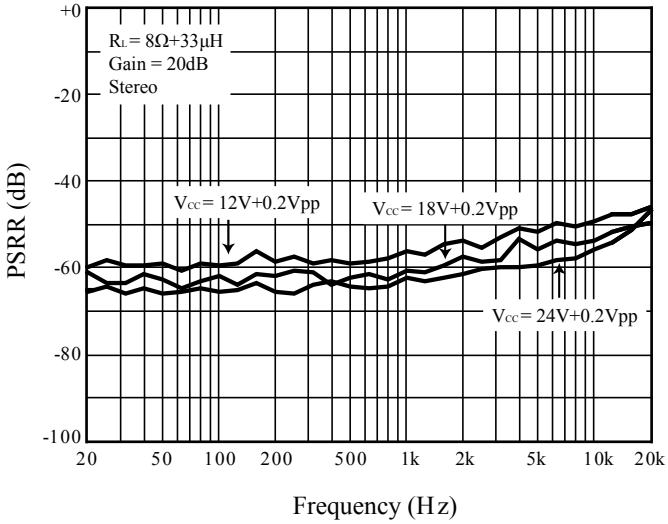


Figure 18 PSRR

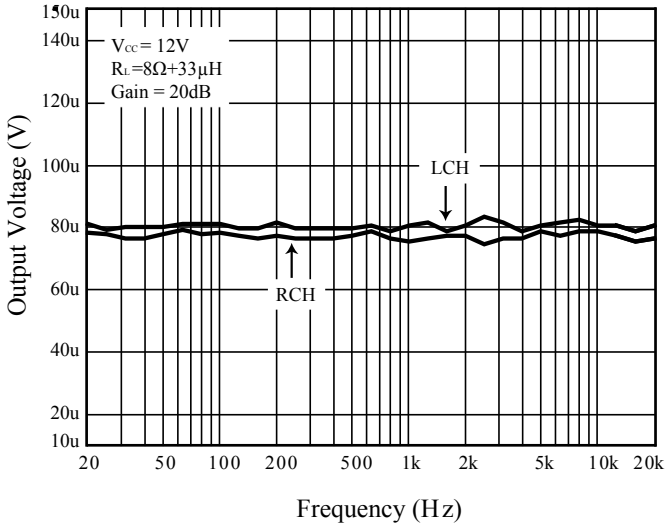


Figure 19 Noise

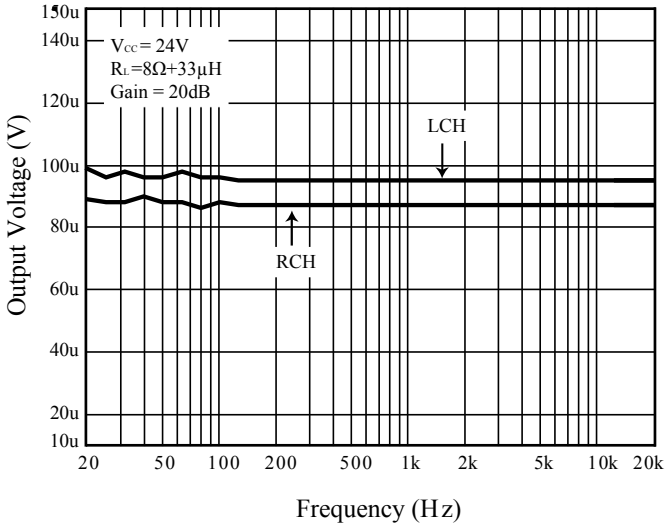


Figure 20 Noise

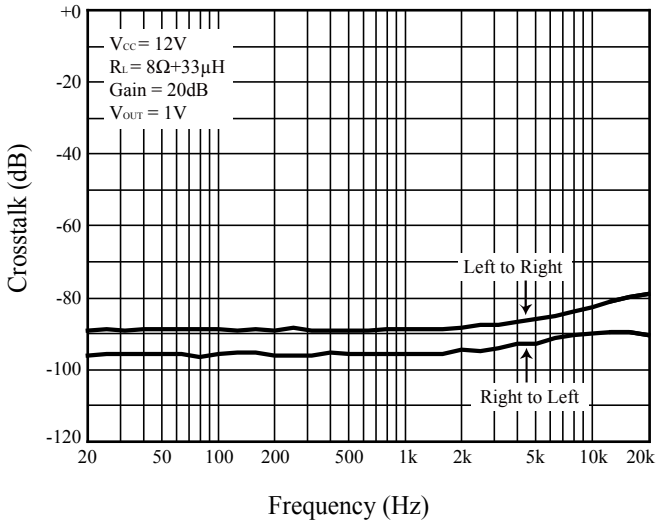


Figure 21 Crosstalk

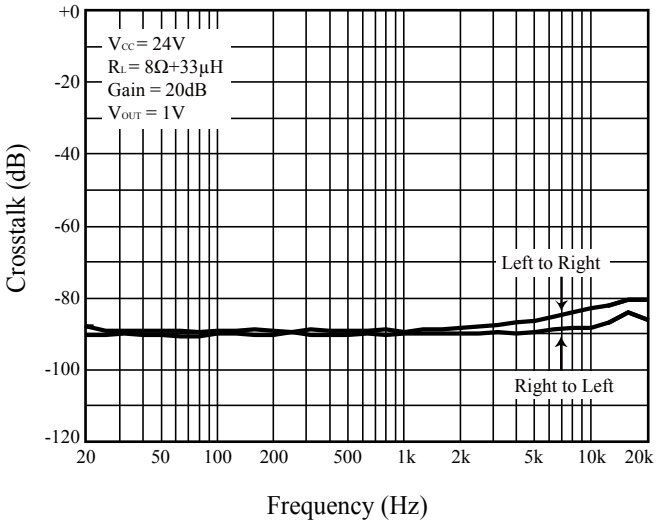


Figure 22 Crosstalk

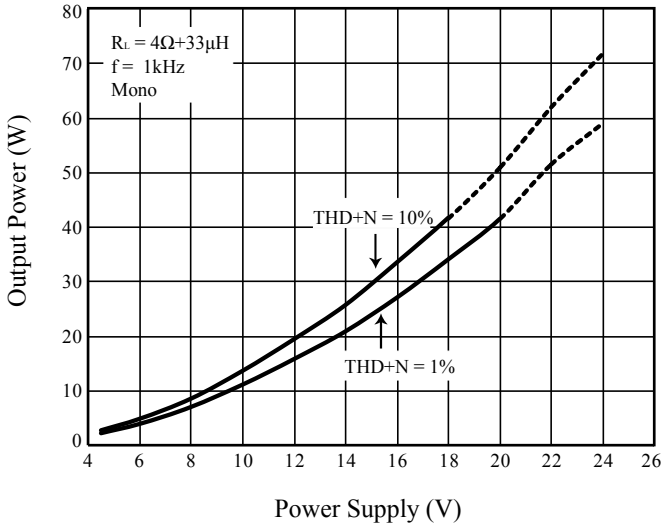


Figure 23 Output Power vs. Power Supply

Note: Dashed Line represent thermally limited regions.

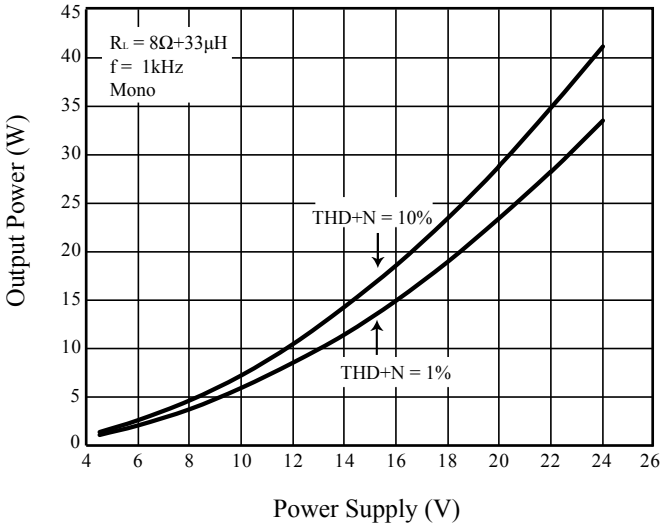


Figure 24 Output Power vs. Power Supply

Note: Dashed Line represent thermally limited regions.

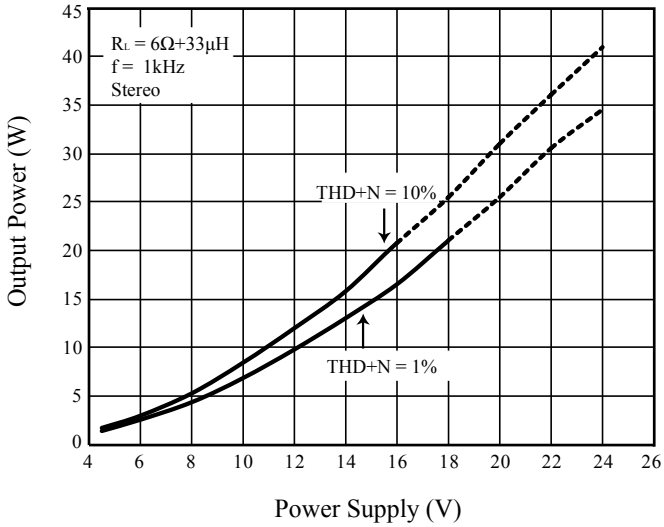


Figure 25 Output Power vs. Power Supply

Note: Dashed Line represent thermally limited regions.

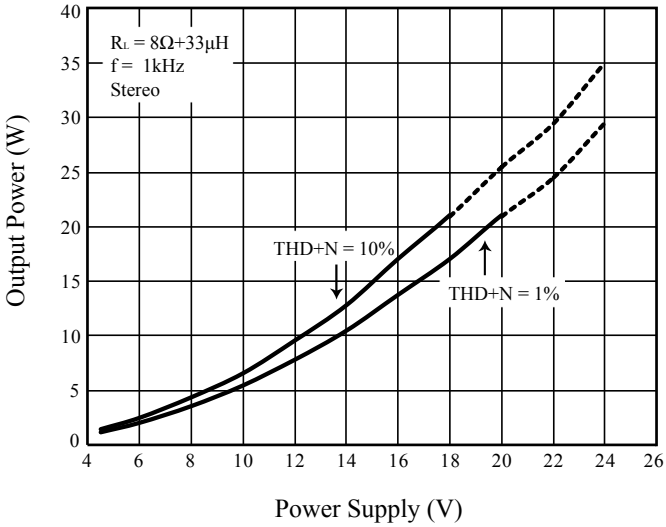
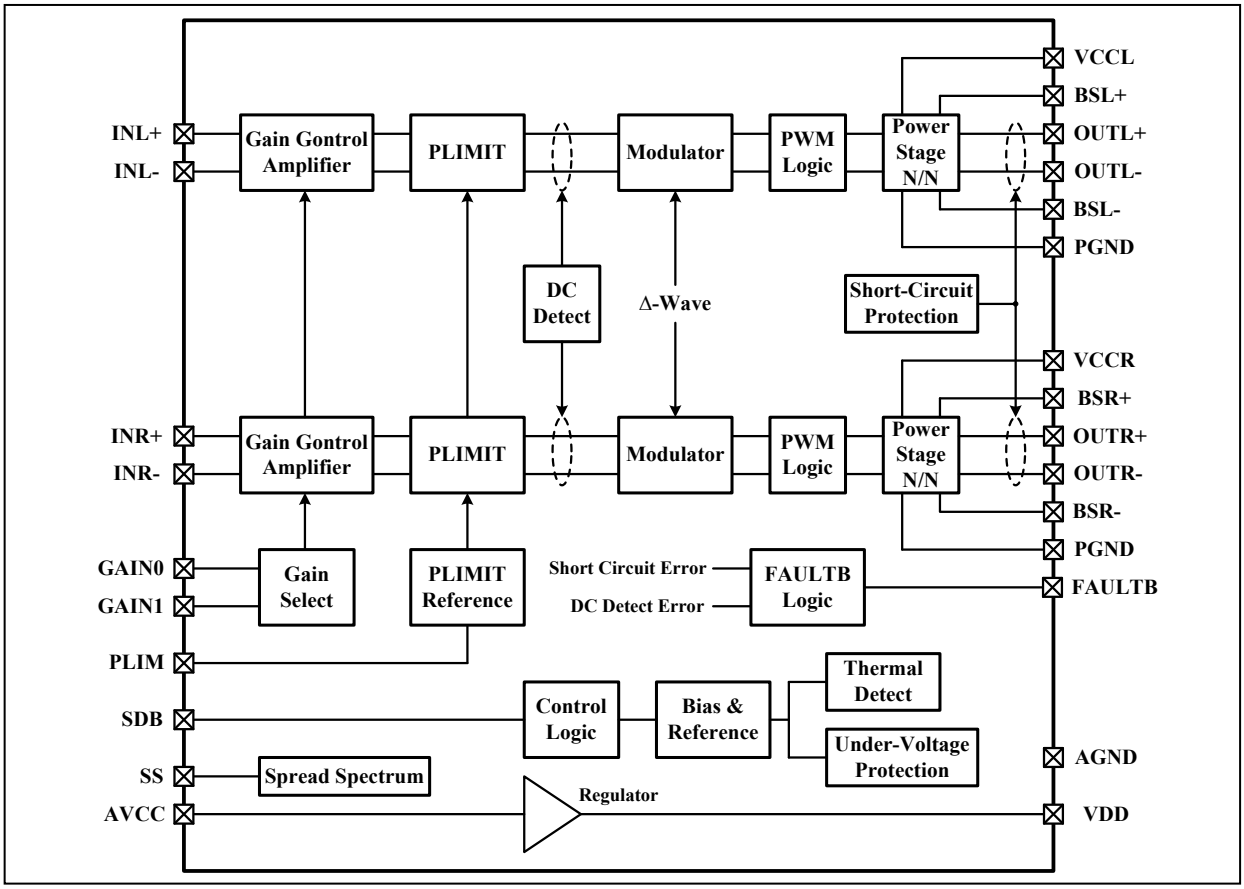


Figure 26 Output Power vs. Power Supply

Note: Dashed Line represent thermally limited regions.

FUNCTIONAL BLOCK DIAGRAM



OPERATION DESCRIPTIONS

GAIN SETTINGS

The gain of the IS31AP2112 is set by two input pins, GAIN0 and GAIN1. By varying input resistance in IS31AP2112, the various volume gains are achieved. The respective volume gain and input resistance are listed in Table 1. However, there is 20% variation in input resistance from production variation.

Table 1 Volume Gain And Input Impedance

GAIN1	GAIN0	Volume Gain (dB)	Input Resistance, R_{IN} (kΩ)
0	0	20	60
0	1	26	30
1	0	32	15
1	1	36	9

SHUTDOWN (SDB) CONTROL

Pulling SDB pin low will let IS31AP2112 operate in low-current state for power conservation. The IS31AP2112 outputs will enter mute once SDB pin is pulled low, and regulator will also disable to save power. If let SDB pin floating, the chip will enter shutdown mode because of the internal pull low resistor. For the best power-off performance, place the chip in the shutdown mode in advance of removing the power supply.

DC DETECTION

IS31AP2112 has dc detection circuit to protect the speakers from DC current which might be occurred as input capacitor defect or inputs short on printed circuit board. The detection circuit detects first volume amplifier stage output, when both differential outputs' voltage become higher than a determined voltage or lower than a determined voltage for more than 420ms, the dc detect error will occur and report to FAULTB pin. At the same time, loudspeaker drivers of right/left channel will disable and enter Hi-Z. This fault can not be cleared by cycling SDB, it is necessary to cycle the VCC supply.

The minimum differential input voltages required to trigger the DC detect function are shown in Table 2. The input voltage must keep above the voltage listed in the table for more than 420ms to trigger the DC detect fault. The equivalent Class-D output duty of the DC detect threshold is listed in Table 3.

Table 2 DC Detect Threshold

A_V (dB)	V_{IN} (mV, Differential)
20	250
26	125
32	63
36	35

Table 3 Output DC Detect Duty (for Either Channel)

V_{CC} (V)	Output Duty Exceeds
8	20.8%
12	20.8%
16	20.8%

THERMAL PROTECTION

If the internal junction temperature is higher than 150°C, the outputs of loudspeaker drivers will be disabled and at low state. The temperature for IS31AP2112 returning to normal operation is about 125°C. The variation of protected temperature is about 10%. Thermal protection faults are NOT reported on the FAULTB pin.

SHORT-CIRCUIT PROTECTION

To protect loudspeaker drivers from over-current damage, IS31AP2112 has built-in short-circuit protection circuit. When the wires connected to loudspeakers are shorted to each other or shorted to VSS or to VCC, overload detectors may activate. Once one of right and left channel overload detectors are active, the amplifier outputs will enter a Hi-Z state and the protection latch is engaged. The short protection fault is reported on FAULTB pin as a low state. The latch can be cleared by reset SDB or power supply cycling.

The short circuit protection latch can have auto-recovery function by connect the FAULTB pin directly to SDB pin. The latch state will be released after 420ms, and the short protection latch will re-cycle if output overload is detected again.

UNDER-VOLTAGE DETECTION

When the VDD voltage is lower than 2.8V or the PVDD voltage is lower than 4V, loudspeaker drivers of right/left channel will be disabled and kept at low state. Otherwise, IS31AP2112 return to normal operation.

OVER-VOLTAGE PROTECTION

When the VCC voltage is higher than 29.5V, loudspeaker will be disabled kept at low state. The protection status will be released as VCC lower than 29V.

POWER LIMIT FUNCTION

The voltage at PLIMIT pin can used to limit the power of first gain control amplifier output. Add a resistor divider from VDD to ground to set the voltage V_{PLIMIT} at the PLIMIT pin. The voltage V_{PLIMIT} sets a limit on the output peak-to-peak voltage. PLIMIT is adjustable from 1.33V~2.5V.

For normal BTL operation (Stereo) and PBTL (Mono) operation:

$$Po@1\% = \frac{\left[\frac{2.5V - P_{LIMIT}}{2.1V + 0.81 \times P_{LIMIT}} \times 2 \times PVDD \times (1.22 - 0.0092 \times PVDD)\right]^2}{2 \times R_L}$$

$$Po@10\% = (Po@1\%) \times (1.21 + 0.021 \times PVDD)$$

Connect PLIMIT pin to ground or VDD to disable power limit function. The output variation during power limit feature enable may have ±20% variation due to process window.

Table 4 PLIMIT Typical Operation Ⅰ

Test Conditions	Output P_O (W)	V_{PLIMIT} (V) @ THD+N=10%
V_{CC}=24V R_L=8Ω	5	1.954
	8	1.835
	10	1.779
	12	1.731
	15	1.67

Table 4.1 PLIMIT Typical Operation Ⅱ

Test Conditions	Output P_O (W)	V_{PLIMIT} (V) @ THD+N=10%
V_{CC}=12V R_L=8Ω	3	1.756
	5	1.584
	8	1.37
	9	1.283

PBTL (MONO) FUNCTION

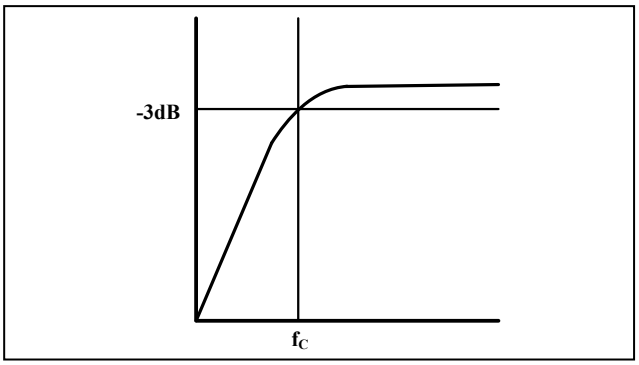
IS31AP2112 provides the application of parallel BTL operation with two outputs of each channel connected directly. If the PBTL pin is tied high, the positive and negative outputs of left and right channel are synchronized and in phase. Apply the input signal to the RIGHT channel input in PBTL mode and let the LEFT channel input grounded, and place the speaker between the LEFT and RIGHT outputs. The output swing is doubled of that in normal mode. See the application circuit example for PBTL (Mono) mode operation. For normal BTL (Stereo) operation, connect the PBTL pin to ground.

APPLICATION INFORMATION

INPUT CAPACITORS (C_{IN})

The performance at low frequency (bass) is affected by the corner frequency (f_C) of the high-pass filter composed of input resistor (R_{IN}) and input capacitor (C_{IN}), determined in Equation (2). Typically, a 0.1µF or 1µF ceramic capacitor is suggested for C_{IN}. The resistance of input resistors is different at different gain setting. The respective gain and input resistance are listed in Table 1 (shown at GAIN SETTING). However, there is 20% variation in input resistance from production variation.

$$f_C = \frac{1}{2\pi R_{IN} C_{IN}} (Hz) \qquad (2)$$



FERRITE BEAD SELECTION

If the traces from the IS31AP2112 to speaker are short, the ferrite bead filters can reduce the high frequency emissions to meet FCC requirements. A ferrite bead that has very low impedance at low frequency and high impedance at high frequency (above 1MHz) is recommended. The impedance of the ferrite bead can be used along with a small capacitor with a value around 1000pF to reduce the frequency spectrum of the signal to an acceptable level.

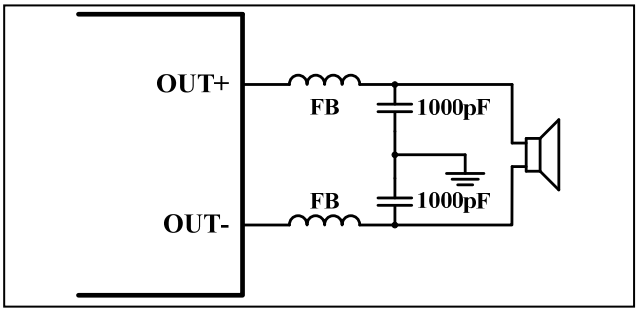


Figure 27 Typical Ferrite Bead Filter

OUTPUT LC FILTER

If the traces from the IS31AP2112 to speaker are not short, it is recommended to add the output LC filter to eliminate the high frequency emissions. Figure 28 shows the typical output filter for 8Ω speaker with a cut-off frequency of 33kHz and Figure 29 shows the typical output filter for 4Ω speaker with a cut-off frequency of 33kHz.

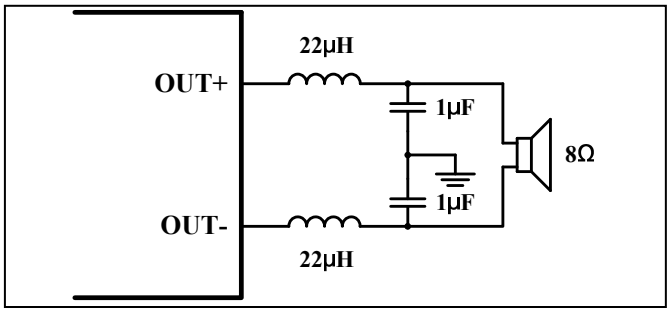


Figure 28 Typical LC Output Filter for 8Ω Speaker

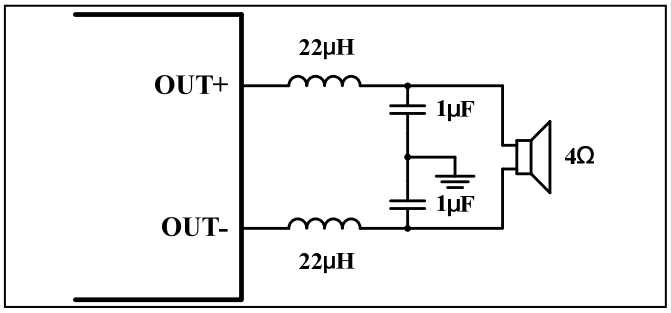


Figure 29 Typical LC Output Filter for 4Ω Speaker

POWER SUPPLY DECOUPLING CAPACITOR (C_S)

Because of the power loss on the trace between the device and decoupling capacitor, the decoupling capacitor should be placed close to VCC and PGND to reduce any parasitic resistor or inductor. A low ESR ceramic capacitor, typically 1000pF, is suggested for high frequency noise rejection. For mid-frequency noise filtering, place a capacitor typically 0.1µF or 1µF as close as possible to the device VCC leads works best. For low frequency noise filtering, a 100µF or greater capacitor (tantalum or electrolytic type) is suggested.

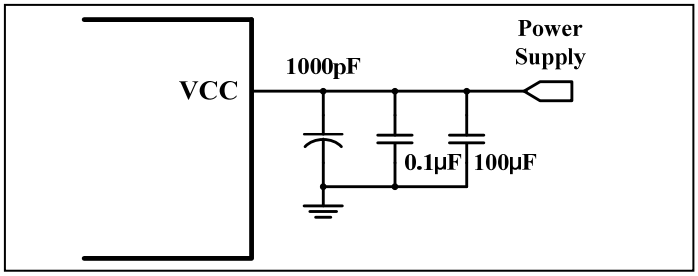


Figure 30 Recommended Power Supply Decoupling Capacitors

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

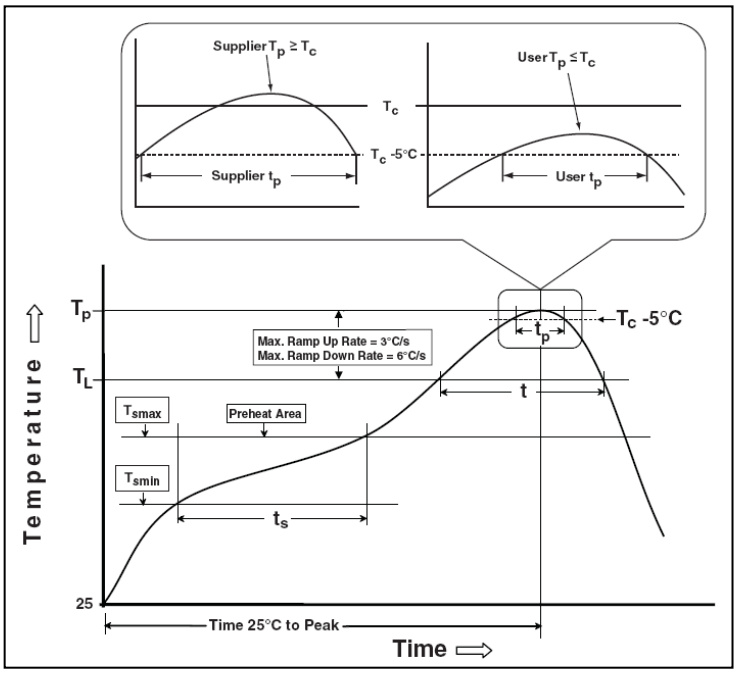
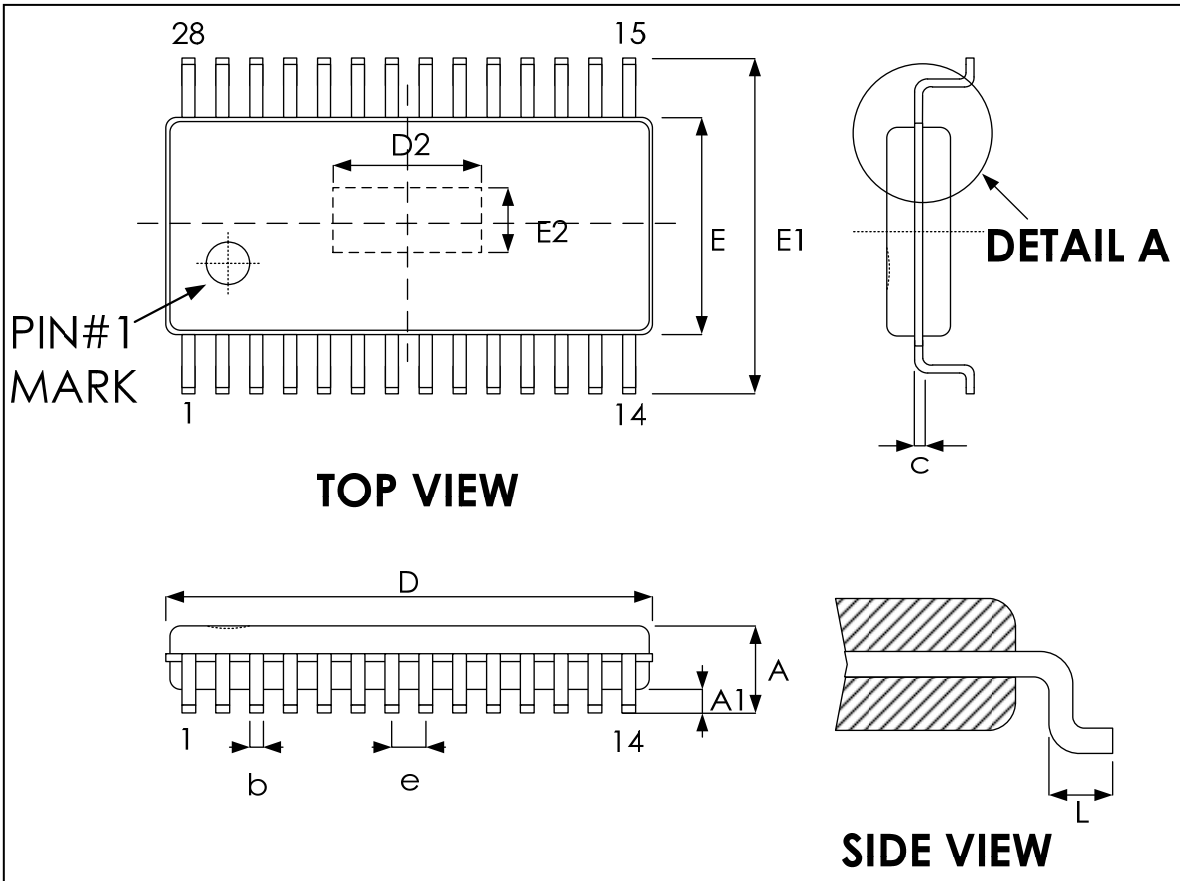


Figure 31 Classification Profile

PACKAGE INFORMATION

eTSSOP-28



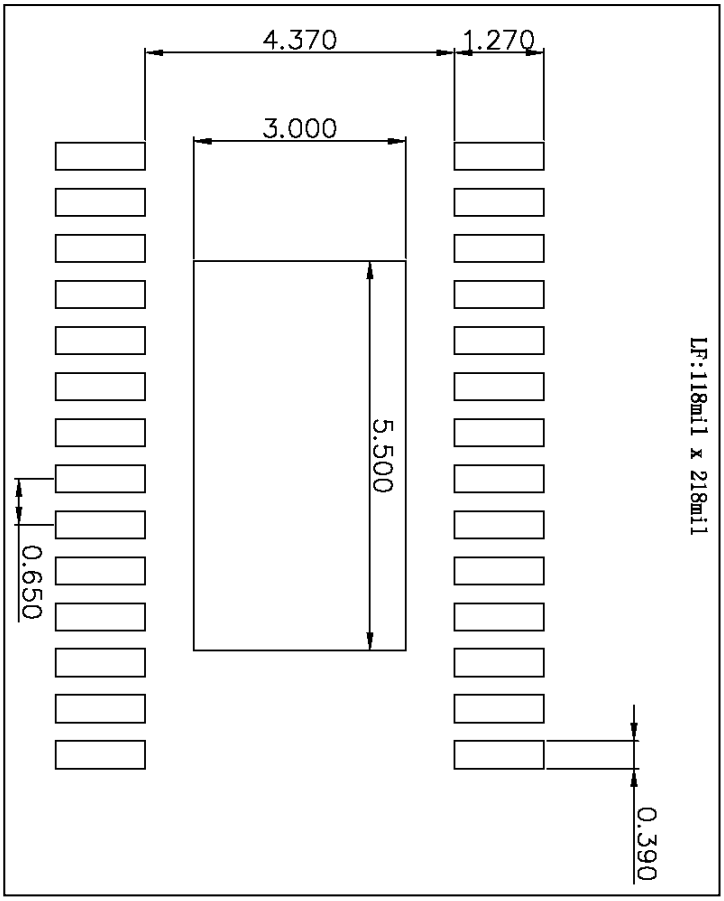
Symbol	Dimension in mm	
	Min	Max
A	--	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.09	0.20
D	9.60	9.80
E	4.30	4.50
E1	6.30	6.50
e	0.65 BSC	
L	0.45	0.75

Exposed pad

	Dimension in mm	
Option 1	Min	Max
D2	4.25	5.75
E2	2.44	3.18

RECOMMENDED LAND PATTERN

eTSSOP-28



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2018.05.10

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