Ballast Controller

Smart Ballast Control IC for Flourescent Lamp Ballasts

ICB2FL03G

Demoboard for 54W T5 Single Lamp Design with Voltage Mode Preheating

Application Note

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Product Highlights

- Lowest Count of external Components
- 650V-Half-Bridge driver with Coreless Transformer Technology
- Supports Customer In-Circuit Test Mode for reduced Tester Time
- Supports Multi-Lamp Designs (in series connection)
- Integrated digital Timers up to 40 seconds
- Numerous Monitoring and Protection Features for highest Reliability
- Very high accuracy of frequencies and timers over the whole temperature range
- Very low standby losses

Features PFC

- Discontinuous Mode PFC for Load Range 0 to 100%
- Integrated digital Compensation of PFC Control Loop
- Improved Compensation for low THD of AC Input Current also in DCM operation
- Adjustable PFC Current Limitation

Features Lamp Ballast Inverter

- Adjustable Detection of Overload and Rectifier Effect (EOL)
- Detection of Capacitive Load operation
- Improved Ignition control allows for operation close to magnetic saturation of Inductors
- Restart with skipped Preheating at short interruptions of Line Voltage (for Emergency Lighting)
- Parameters adjustable by resistors only
- Pb-free Lead Plating; RoHS compliant

1 Introduction

The fluorescent lamp Ballast Controller ICB2FL03G is designed to control a boost converter as an active power factor correction (PFC) filter in critical/discontinuous conduction mode (CritCM/DCM) and a half-bridge topology as a lamp inverter. The intelligent control concept enables designers to develop cost-effective ballasts for fluorescent lamps (FL) that fulfil the requirements of a high performance T5 lamp ballast as well as multi lamp topologies (series connection), T8 and T4 designs. A state machine controlling the operating modes, a completely integrated digital control loop for the PFC output voltage and low tolerances for reference voltages and operating frequency over the whole temperature range are a result of the advanced mixed signal technology with only few required components externally. Combined with a high voltage level shift driver with Coreless Transformer Technology for the half-bridge inverter the IC offers a significant number of exceptional features for FL ballasts.

The FL-Ballast Controller ICB2FL03G has an improved and enlarged functionality that enables high quality single or multi lamp ballasts (series connection) with a low number of external components. Its benefit is to save system costs and to reach class A2 of the energy efficiency index (EEI) for fluorescent lamp ballasts easily.

1.1 Functional description

The functional description shall be performed using the circuit diagram of a lamp ballast for the T5 fluorescent lamps (**Figure 1-1**).

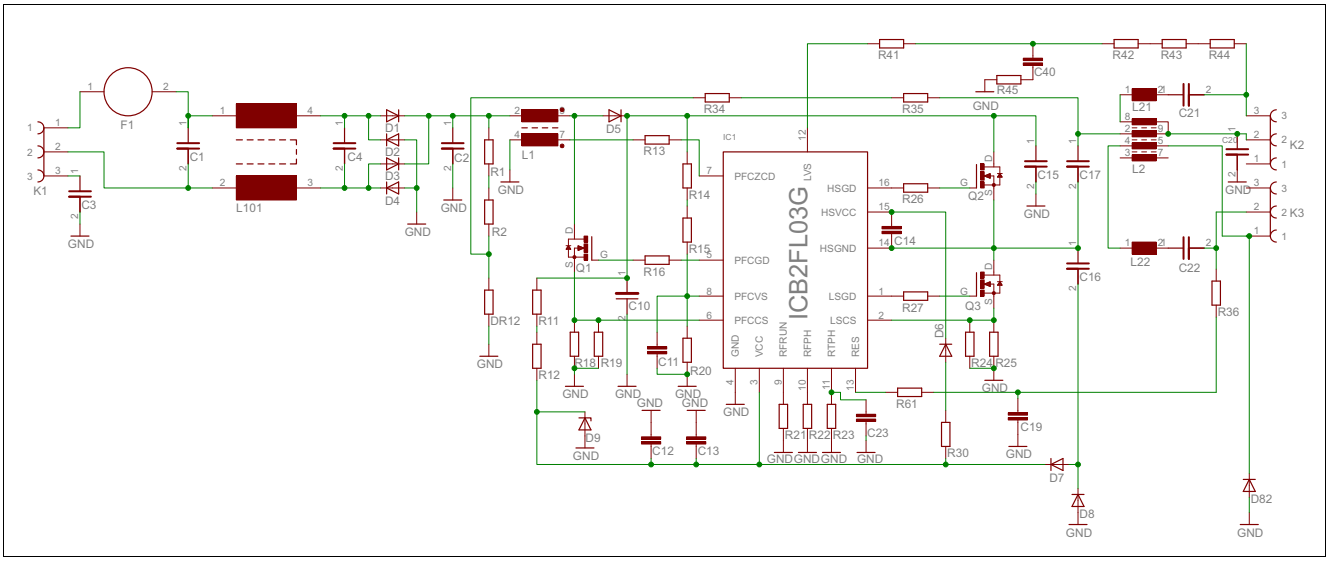


Figure 1-1 Schematic for 54W T5 Demo board

The Schematic shows the circuit of the Demo board with the reference name of each component for a single lamp design with voltage mode preheating. This schematic supports all protection functions of the IC.

After switching on the mains the filter capacitor C_2 and the bulk capacitor C_{10} are charged to the peak voltage of the mains supply. The capacitors C_{12} and C_{13} which support the IC-supply voltage VCC are charged via the Startup-resistors R_{11} and R_{12}. The current consumption of the IC at this stage is typically below 90 µA until the supply voltage has reached typ. 10.6 V. Above this level the current consumption is typ. 120 µA and a current source of typically 21.3 µA at the RES-Pin is activated which detects a connected low-side-filament. As long as the voltage-level at the RES-Pin is below 1.6 V the filament is assumed to be undamaged. In the path of the measured current a resistor R_{36} is placed which adjusts the voltage drop and - in conjunction with the capacitor C_{19} - filters the alternating voltage on the filament during Run-mode. Via the resistors R_{34} and R_{35} a current is fed to the high-side-filament and via the resistors R_{41}, R_{42}, R_{43} and R_{44} to the LVS-Pin. A filament is detected if the current is above typ. 12 µA. If the measured current at LVS-Pin is too small this fault generates a higher current level of typically 42.6 µA at the RES-Pin. The following points are checked in the sequence below before the IC activates the driver outputs.

- Connected filaments
- VCC > VVCCOn (14.0V)
- Bus-voltage between 12.5 % and 105 %

Inverter section

With the first pulse the low side MOSFET Q_3 of the half-bridge is turned on. Then the floating capacitor C_{14}, which supplies the high-side control logic like a battery, is charged from capacitor C_{13} via R_{30} and the diode D_6. The resistor R_{30} prevents the activation of the over current protection at the LSCS-Pin. Thus already with the next half cycle the high-side MOSFET Q_2 can be turned on. At the output of the half-bridge inverter the capacitor C_{16} together with the diodes D_7 and D_8 acts as a charge pump. The continuous recharging of C_{16} with the inverter frequency shifts energy for the supply voltage VCC of the IC to C_{13}. A surplus of energy is dissipated by the zener diode D_9. In addition C_{16} is used to limit the voltage slew rate and to produce zero voltage switching conditions. During operation C_{16} is recharged without losses in the deadtime periods of MOSFET Q_2 and Q_3 by the inductive driven current of the load circuit. So the succeeding turn-on of the MOSFET occurs at zero voltage. At turn-off C_{16} limits the voltage slew rate in such a way, that the MOSFET channel is already turned off before the Drain to Source voltage has reached considerable levels. Therefore the inverter creates negligible switching losses at normal operation. The load circuit of the inverter consists of a series resonant-circuit with the resonance-inductor L_2 and the resonance-capacitor C_{20}. The lamp is connected in parallel to the resonance-capacitor. This example shows voltage controlled preheating. This means that the resonance-inductor L_2 has two additional windings. Each of those windings drives a current in the filament via the band-pass consisting of L_{21}/C_{21} and L_{22}/C_{22}. The band-pass filter ensures that the current in the filaments is only flowing during the preheat phase. By reducing the frequency during Run-mode the heating current is almost completely blocked by the band-pass. The load circuit also contains a capacitor C_{17}. This capacitor is charged to half the value of the bus voltage thus operating the lamp symmetrically to the ground potential of the rectified mains supply is possible.

PFC

Simultaneously with the inverter the MOSFET Q_1 of the PFC boost converter starts the operation. This circuit consists of the inductor L_1, diode D_5, MOSFET Q_1 together with the bulk capacitor C_{10}. Such a boost converter can transform the input voltage to any arbitrary higher output voltage. Using a suitable control method this converter is used as an active harmonic filter and for the correction of the power factor. The input current follows the same sinusoidal waveform as the AC mains supply voltage. At the output of the PFC-preconverter a feedback controlled DC-voltage is available at capacitor C_{10} for the application. The PFC-stage is operated with a controlled turn-on time without input voltage sense. A turn-on time set by the control unit is followed by a turn-off time which is determined by the duration until the current in the inductor and hence in the diode too has reached the level zero. This point of time is detected by the voltage-level at the zero current detector winding on the inductor L_1 and is fed to the IC via the resistor R_{13} and the PFCZCD-Pin. The result is a gapless triangular shaped current through inductor L_1 (so called critical conduction mode) which is sustained for a turn-on time in the range of 24.0 µs down to 270 ns. A further reduction of the energy flow extends the turn-off time of the PFC-MOSFET causing triangular shaped currents with gaps (discontinuous conduction mode). Such a control method allows a stable operation of the boost converter over a large range of the input voltage as well as the output power. The current into the PFCZCD-pin is used to do a THD-correction for optimized THD.

The IC includes a couple of protection features for the PFC-preconverter. The overcurrent is sensed at the PFCCS-Pin. The bus voltage, overvoltage and undervoltage are monitored at the PFCVS-Pin as well as the open loop detection. The ICB2FL03G includes the error amplifier with entire compensation build up by a digital PI-regulator and a self calibrating notch filter to suppress the voltage ripple of the bulk-capacitor.

Startup

The inverter starts at a frequency of 135 kHz. Within 10 ms the frequency is reduced in 15 steps to the preheating frequency adjustable by the resistor R_{22}. The duration of preheating can be selected between zero and 2500 ms

by the resistor R_{23}. Subsequently the frequency is further reduced in 127 steps and a time period of 40 ms to the run frequency f_{RUN} adjustable by the resistor R_{21}. The ballast should be designed in such a way that during the preheating phase the voltage across the lamp is low and at the same time the current in the filaments is large. In the ignition phase following to the preheating period the frequency of the inverter should be at - or at least close to - the resonance frequency of the resonant circuit in order to reach a sufficient voltage for the ignition of the lamp. After successful ignition and frequency reduction to the Run-frequency the current in the lamp should reach its nominal value and the current in the filaments should become a minimum. During the ignition period a high voltage at the lamp and a large current in the resonant circuit is generated due to the unloaded resonant-circuit. The current in the resonant-circuit is monitored by the resistors R_{24} and R_{25}. As soon as the voltage at pin LSCS exceeds a level of 0.8 V, the operating frequency is controlled by the integrated Ignition regulator which works stable close to magnetic saturation of the resonant choke. If the level of 0.8 V at pin LSCS is not crossed any more, the operating frequency of the inverter decreases with the typical step width of the ignition phase towards the Run-frequency. As a result of this measure the Ignition-phase is enlarged from 40 ms up to 235 ms with a lamp not willing to ignite, while the voltage at the lamp keeps on the level of the Ignition voltage. If the Run-frequency is not achieved within 235 ms after finishing the preheating period the IC changes over into the failure mode. In such a situation the Gate drives will be shut down, the current consumption of the IC will be reduced to max. 170 µA and the detection of the filaments and the input voltage will be activated. A restart is initiated dependent on the failure counter directly or either by lamp removal or after a new cycle of turn-off and turn-on of the mains voltage. After successful ignition there is a fixed PreRun-time of typ. 625 ms implemented to block several protection functions until a stable lamp operation can be guaranteed.

Protection functions

Numerous protection functions complement the basic functions of the ICB2FL03G. As soon as the level at pin LSCS exceeds the voltage threshold of 0.8 V for longer than 500 ns, it is recognized as a risky operating condition as it can occur during lamp removal in a running device or during transients of mains voltage, and the IC changes over into the failure mode. During Run-mode of the inverter a deviation from the typical zero voltage switching is recognized as an operation with capacitive load. In such an operating condition peak currents occur during turn-on of the MOSFETs due to switched charging of the charge pump capacitor C_{16}. The IC distinguishes between two different types of capacitive load.

- Cap load 1 (Idling detection / current mode preheating) **Chapter 6.7.1**
- Cap load 2 (Overcurrent / operation below resonance) **Chapter 6.7.2**

Finally dangerous operating conditions can happen, when the fluorescent lamp reaches the end of lifetime or at operating conditions leading to thermal instability of the lamp. As a consequence the lamp voltage becomes unsymmetrical or increases. For detecting such operating conditions the resistors R_{41}, R_{42}, R_{43}, R_{44}, R_{45} and the capacitor C_{40} measure the lamp voltage by evaluating the current through these resistors at pin LVS. The turn-off threshold for EOL1 (End of Life 1) is at 210 μA_{PP} with a duration of 620 µs. The rectifier effect with unsymmetrical lamp voltage is called EOL2 (End of Life 2) and the turn-off threshold is at +/- 42 µA with a duration of typ. 2500 ms. Due to intelligent failure differentiation the ICB2FL03G is able to detect a Surge at the input voltage without latching this failure.

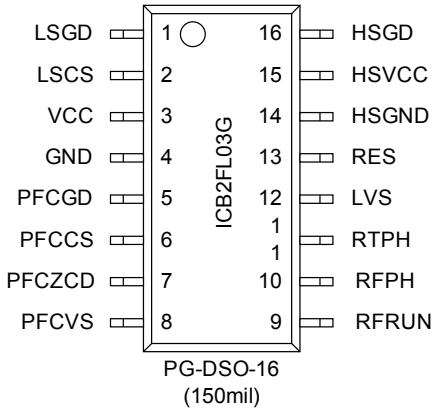
The IC controls the operating frequency of the inverter during the different operating sequences such as Soft start-, Preheat-, Ignition-, PreRun- and Run-mode. During the different operating sequences there are only some of the protection features active first. All the protection features are active during Run-mode only. The integrated circuit ICB2FL03G has a unique combination of features that make a design of high-quality lamp ballast with a low number of external components possible.

Further information and datasheet can be found on the subsequent link http://www.infineon.com/smartlighting

Unless otherwise specified, all values given in this Application Note are typical values.

1.2 Pinning and picture of the Demo board

The following Chapter shows the pinning of the IC and a picture of the Demo board which is described in this document.



Pin	Symbol	Function
1	LSGD	Low side Gate drive (inverter)
2	LSCS	Low side current sense (inverter)
3	VCC	Supply voltage
4	GND	Low side Ground
5	PFCGD	PFC Gate drive
6	PFCCS	PFC current sense
7	PFCZCD	PFC zero current detector
8	PFCVS	PFC voltage sense
9	RFRUN	Set R for run frequency
10	RFPH	Set R for preheat frequency
11	RTPH	Set R for preheating time
12	LVS	Lamp voltage sense
13	RES	Restart after lamp removal
14	HSGND	High side ground
15	HSVCC	High side supply voltage
16	HSGD	High side Gate drive (inverter)

Figure 1-2 Pinning of IC

The pinning and a short Pin description of the is given in Figure 1-2. A detailed Pin-description can be found in the Datasheet (Chapter 1.2)

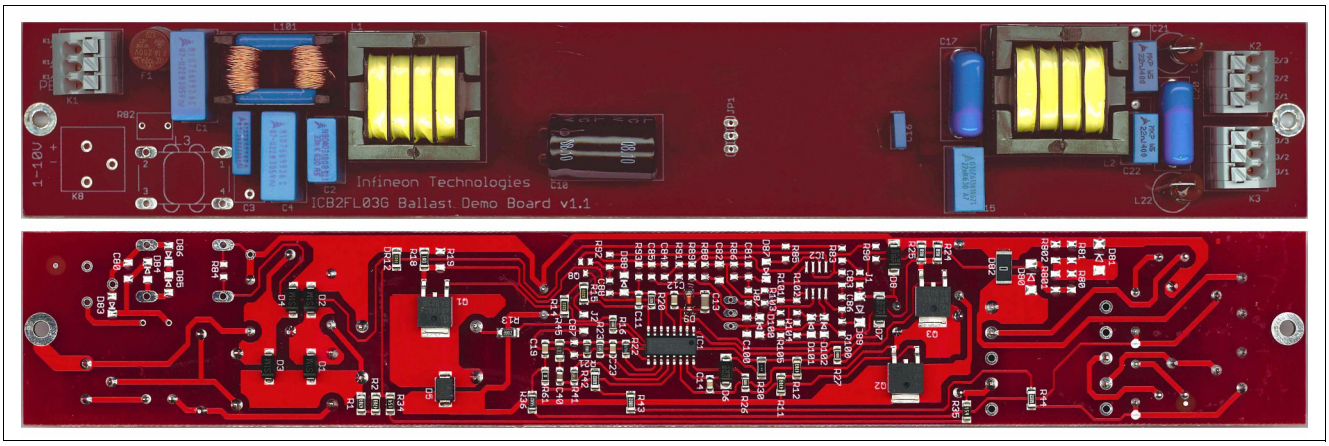


Figure 1-3 Top and Bottom view of the Demo board

Figure 1-3 shows the picture of the Demo board for the 54W T5 Design with voltage mode preheating. Please visit the Infineon Smart lighting Website (http://www.infineon.com/smartlighting) for further information.

1.3 Parameters of the Demo board

Table 1-1 gives an overview to the operational characteristics of the Demo board.

Table 1-1 Operational characteristics of the Demo board 54W T5

	Value	Unit	Comment
V_{IN}	230	V_{ACRMS}	(180 V - 270 V)
I_{IN}	257	mA_{RMS}	@230V input voltage
P_{IN}	59.1	W_{RMS}	@230V input voltage (EEI = A2 CELMA Efficiency class)
V_{BUS}	410	V_{RMS}	
f_{PH}	106.4	kHz	

Table 1-1 Operational characteristics of the Demo board 54W T5 (cont'd)

	Value	Unit	Comment
f_{RUN}	45.5	kHz	
t_{PH}	1000	ms	
V_{Lamp}	118	V_{RMS}	
I_{Lamp}	460	mA_{RMS}	
V_{IGN}	> 620	V_{RMS}	
n	> 93	%	With Lamp after 30 min. operation in Run-Mode @ 230 V_{ACRMS}
PF	> 0.99		@ 230 V_{ACRMS} input voltage
A_{THD}	< 4	%	@ 230 V_{ACRMS} input voltage

1.4 Description of normal Startup - Steps

This chapter describes the normal Startup procedure from phase 1 (UVLO) to phase 8 (Run mode), **Figure 1-4** shows a measurement and diagram from the Start-up procedure. Dependent on the voltage at RES-Pin, the current consumption of the IC can be higher due to I_{RES1} to I_{RES4}.

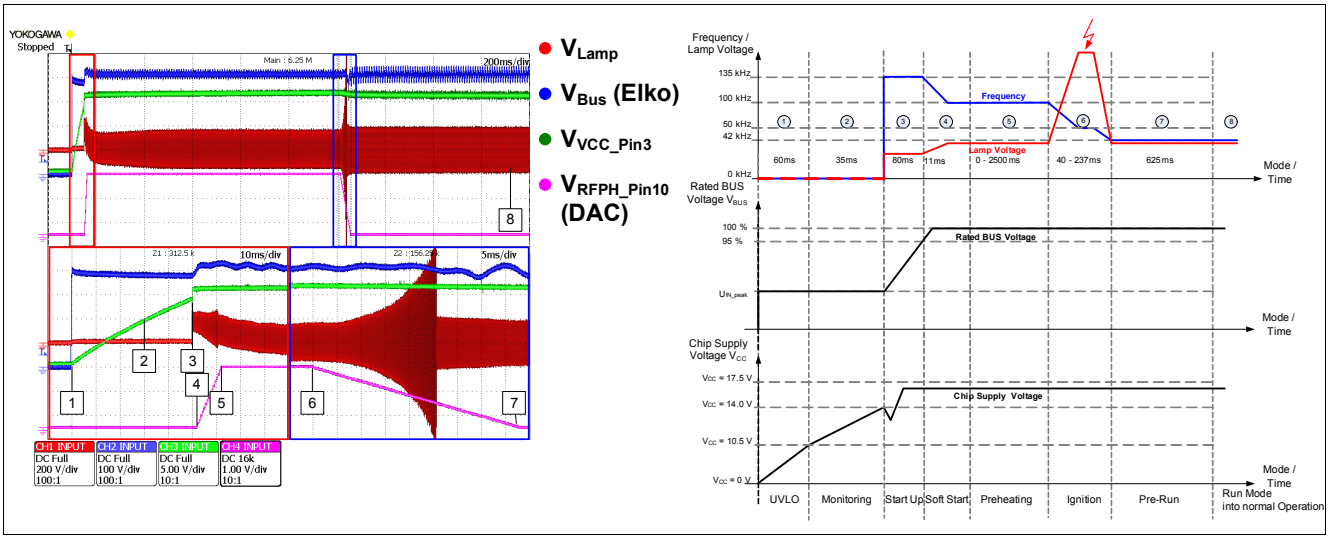


Figure 1-4 Start-up procedure

The current consumption of the IC in Phase 1 (UVLO) is I_{VCCqu1}. The current fed via the high ohmic VCC-Startup-resistors (R_{11} and R_{12}) charges the VCC-capacitor and delivers this quiescent current. After reaching a first threshold of V_{VCCOff} the IC goes into monitoring mode and checks for connected cathodes. The current consumption in this Phase 2 is I_{VCCqu2} and has to be also delivered via the Start-up resistors. The voltage at VCC-Pin rises up to V_{VCCOn} and the IC becomes active and starts inverter switching (preconditioned both cathodes are present). Phase 3, also called Startup activates the whole IC and leads to a current consumption of $I_{VCCSupply}$. Within the first 130 µs the internal reference starts up and the IC checks the level of the Bus-voltage. If the Bus-voltage is in the specified range of 12.5 % and 105 % the LSGSD switches on several times to charge the HSVCC-capacitor via R_{30} and D_6. After reaching the HSVCC turn-on-threshold of $V_{HSVCCOn}$ the HSGD starts working too (HSGD and LSGD alternating) and supplies the IC via a charge pump and the VCC voltage rises up to the voltage clamped by D_9. The inverter works with a Startup-frequency of $f_{StartUp}$. To prevent reaching the UVLO-threshold of V_{VCCOff} when all Gate Drives become active at the same time the PFC-section starts working with a delay of about 200 µs (see also **Figure 1-5**). After reaching a Bus-voltage of 95 % the IC enters Soft start, phase 4. In this phase the IC shifts the frequency down to the adjusted preheating frequency. This frequency shift can be seen at the signal at RFPH-Pin when the voltage rises up from GND to 2.5 V (**Figure 1-4**).

After reaching the preheating frequency the IC stays in this Preheating-phase (Phase 5) for the adjusted preheating time. After the preheating time the IC goes into Ignition-mode (Phase 6) and begins reducing the frequency down to the adjusted Run-frequency. This can be seen also on the signal at RFPH-Pin. The voltage at this Pin goes down until voltage at LSCS-Pin reaches the threshold of 0.8 V. Then the Ignition regulator begins regulating the Ignition voltage to this maximum Level, also during magnetic saturation of the resonant choke. During regulating the Ignition voltage, the voltage at RFPH-Pin stays at the reached level between 2.5 V and GND. After successful Ignition during $t_{NOIgnition}$ (limited duration of the Ignition-phase) the IC enters the PreRun-mode, Phase 7 and the voltage at RFPH-Pin goes down to GND. The PreRun Mode is a safety mode (with limited protection functions active for t_{PRERUN}) in order to prevent a malfunction of the IC due to an instable system e.g. the lamp parameters are not in a steady state condition. In this Phase the Ignition regulator is also active to re-ignite the lamp if the lamp shows very bad ignition behavior. After a duration of t_{PRERUN} the IC disables the Ignition regulator and goes over into the Run-mode (Phase 8) and all protection functions become active.

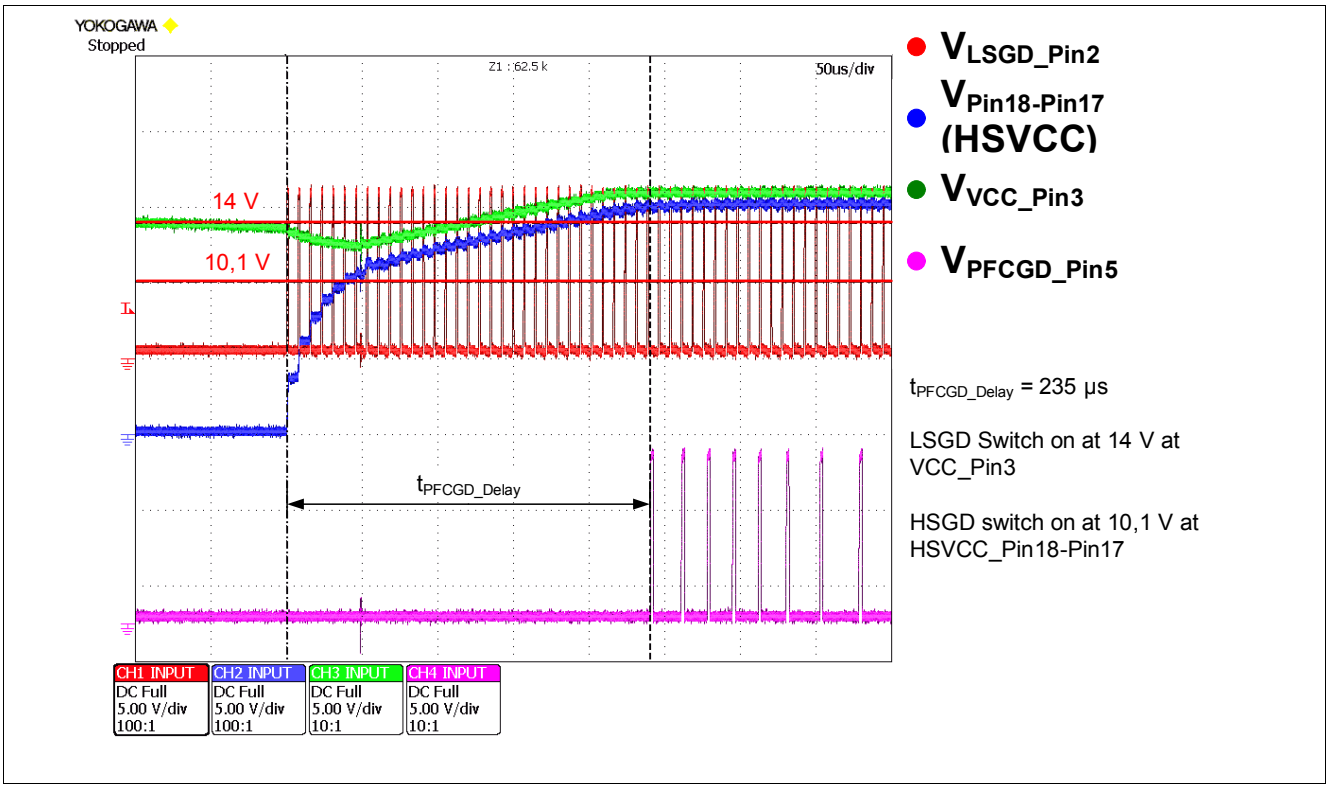


Figure 1-5 PFCGD Start-up delay

A detailed evaluation of the Startup is given in **Figure 1-5**. After reaching the V_{VCCOn} threshold the IC goes into Power-up-mode and starts LSGD switching with a short internal delay. The LSGD turns on several times to charge the HSVCC, in this time the voltage at VCC-Pin breaks down a little bit, because the IC current consumption is now higher than the fed current from the high ohmic Start-up resistors R_{11} and R_{12}. The VCC-capacitors C_{12} and/or C_{13} must be big enough to store the needed energy for charging the HSVCC-capacitor C_{14} to the $V_{HSVCCOn}$ threshold without reaching the UVLO-threshold at VCC. After reaching the $V_{HSVCCOn}$ threshold (typ. 10.4 V) the HSGD starts working too and the VCC supply is now generated from the working half-bridge via charge pump and the provided energy is high enough to rise the VCC-voltage up to the clamped limit of the external Z-Diode D_9. With a delay of about 235 µs the PFCGD starts working. This delay is implemented in the IC to ensure a stable VCC-supply before the current consumption of the IC gets higher due to the additional working PFCGD. This feature prevents going into UVLO during Startup process. **Chapter 8.3** gives advice if there are malfunctions to this described functional sequence.

2 VCC Chip supply

The high ohmic resistors (R_{11} and R_{12}) for the Startup-supply have to be connected to the Bus-Elko to ensure an IC-supply during Startup mode, Latch mode and short interruption of the input voltage (Emergency Lighting feature according VDE 0108). The IC-logic has implemented the ability for a self generated reset. The condition for reset is an active IC with a current consumption of about $I_{VCCSupply}$ with inactive gate drives. This results in a falling VCC-voltage down to the V_{VCCOff} threshold, also called UVLO (Undervoltage Lockout) and this resets the IC via the VCC. At this self generated UVLO the IC goes into active mode with inactive gate drives. Without working half-bridge there is no supply via the charge pump and the VCC-capacitor discharges down to V_{VCCOff} (UVLO threshold) and leads to a restart of the IC. When the Startup-resistors or an external supply can provide too much current, and the IC can't discharge the VCC-capacitor, please check Chapters 3.2 and 3.3 in the Datasheet for further information to the functional restrictions in this case. In latched failure-mode the IC has a current consumption of $I_{VCCLatch}$ and this current has to be delivered by the Startup-resistors. The current out of the RES-Pin has to be considered for calculation of the Startup-resistors together with $I_{VCCLatch}$.

2.1 While half-bridge is not working

Without active inverter section the Startup resistors have to supply the IC with a minimum current of $I_{VCCLatch}$. Note: This current must be possible at minimum input voltage. (This range is necessary for correct restart after internally generated UVLO and correct function of hiccup-mode). For correct IC function at self generated UVLO a maximum current of 2 mA is a good design proposal.

For the Startup of the IC-supply it is important to check the voltage level at the RES-Pin. Due to the capacitor and resistor at RES-Pin, the dv/dt at this Pin is limited and for example might be slower than the VCC dv/dt at external supply or with low-ohmic Startup-resistors. the voltage V_{RES} must reach the filament detection level before the IC-supply voltage VCC reaches the V_{VCCOn} threshold. Otherwise removed filaments can't be detected correctly because the filament detection status is checked between V_{VCCOff} and V_{VCCOn}.

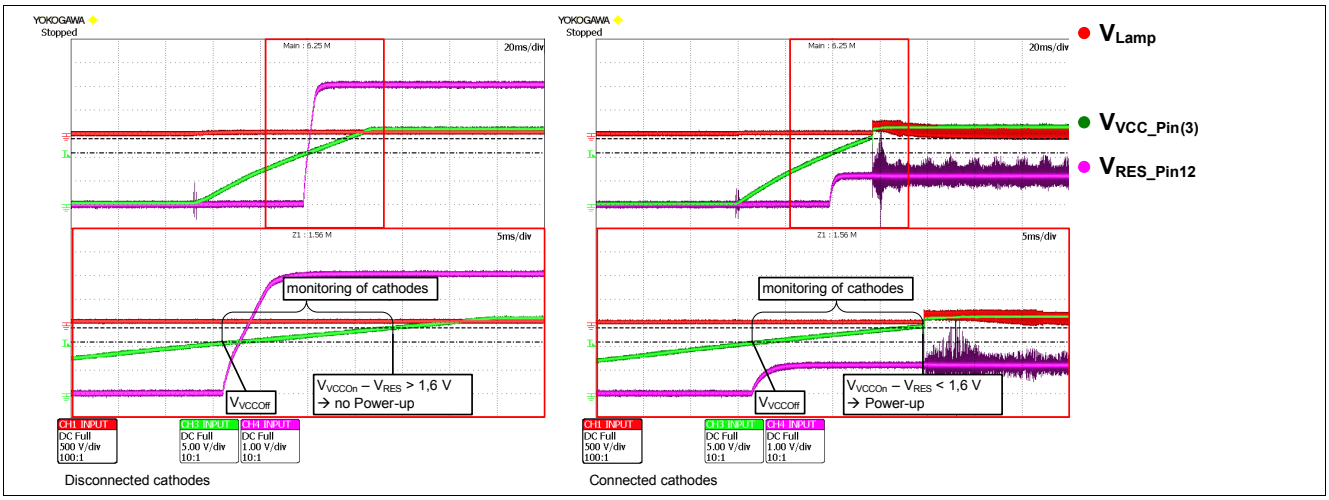


Figure 2-1 dv/dt at VCC- and RES-Pin @ Startup

Figure 2-1 shows two oscillograms with the signals at VCC- and RES-Pin when connecting the input voltage. The left oscillogram shows the signals when the cathodes are open and the voltage at RES-Pin rises > 1.6V. This voltage level must be reached while the IC monitors the cathodes for correct filament detection. The right oscillogram shows that the IC goes into Power-up when the cathodes are connected.

2.2 While half-bridge is working

At continuous working of the inverter section (LSGD and HSGD) the IC is supplied mainly via the charge pump (C_{16}, D_7 and D_8) connected to the half-bridge. With this solution of VCC-supply during Run-mode the IC can generate an UVLO by itself by stopping the inverter.

An example for a self generated UVLO is shown in **Figure 2-2**. For understanding the following explanation a view to the State-diagram in the Datasheet (Chapter 3.3) is necessary. Removing the Board-Supply V_{IN} in Run-mode leads to a discharging of the Bus-Elko. After V_{BUS} reaching the 75 % threshold the IC detects Bus-undervoltage and goes into “Fault U” failure handling with deactivation the gate drives and going into Power-down-mode. After about 750 ms the State-machine lefts the decision block “Counter Skip Preheat > 7” with “Y” and then goes into active mode with inactive gate drives. In consequence the VCC-capacitor is discharged to the V_{VCCOff} threshold (red circle). This UVLO resets the IC-logic.

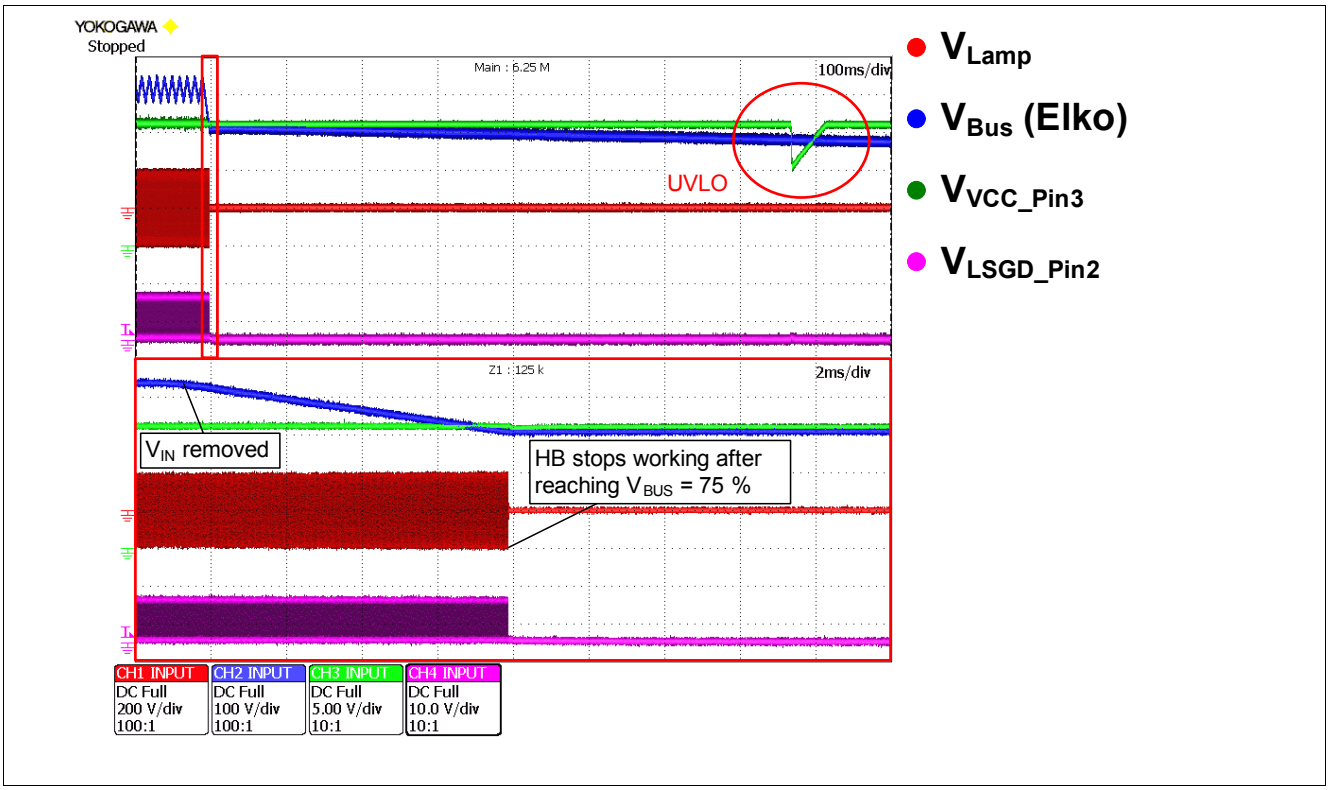


Figure 2-2 Example for self generated UVLO after Counter Skip Preheat >7 = Y

3 PFC

The control of the PFC starts with a fixed operating frequency and increasing on-time and changes over into critical conduction mode (CritCM) operation (also called borderline/transition conduction mode) as soon as sufficient signal level at the pin PFCZCD is available. The benefit of this feature is to save external components for the compensation and for the synchronization to the AC-input voltage. The dynamic response and the suppression of the superimposed ripple of the Bus-voltage fulfil even high requirements. Finally during light load conditions the PFC control changes the operating mode from CritCM to DCM (discontinuous conduction mode) which effects a stable operation even down to no load

A detailed description of the digital control loop for PFC can be found in the Datasheet (Chapter 2.4.3)

Figure 3-1 shows the PFC related Signals in Discontinuous conduction mode (DCM - Top) and in Critical conduction mode (CritCM - Bottom).

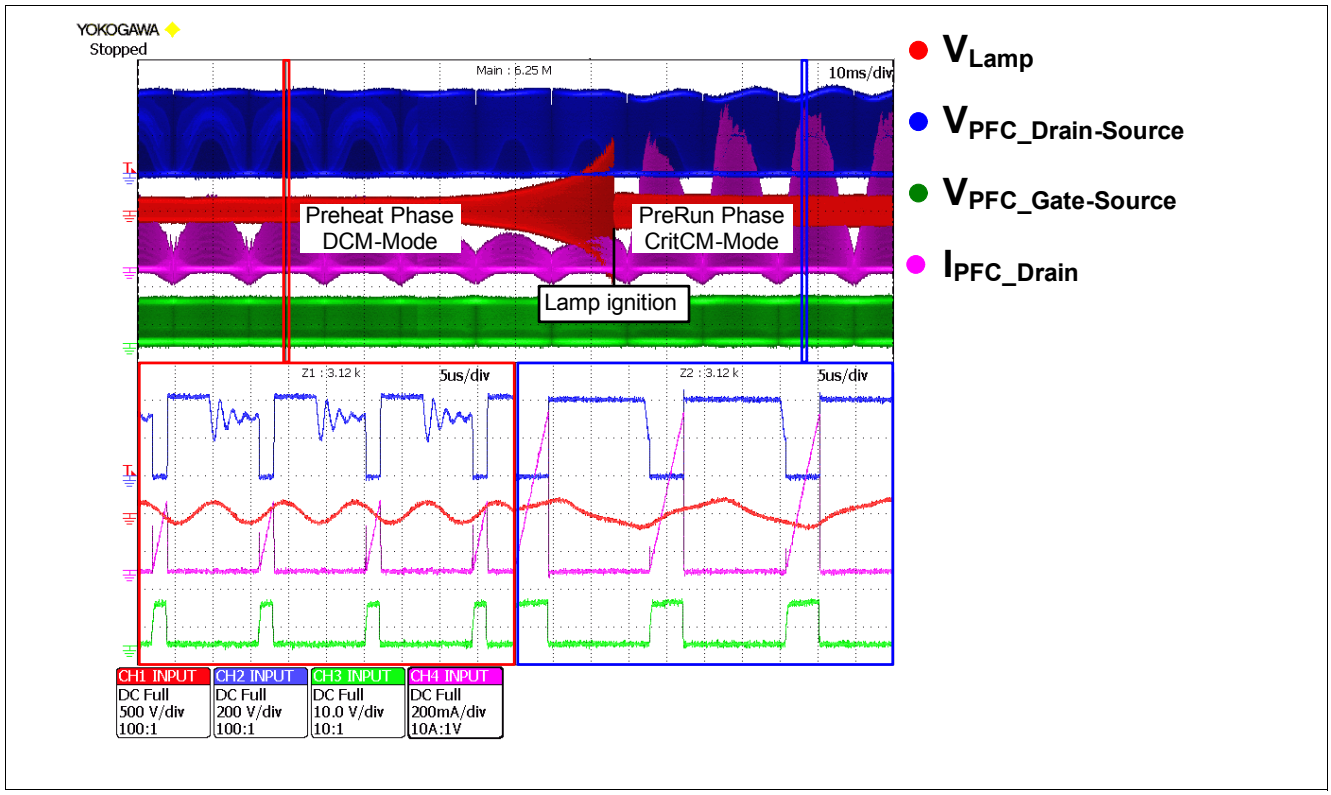


Figure 3-1 DCM- and CritCM-Mode of the PFC-Stage

Figure 3-1 shows an oscillogram of the two operating modes DCM and CritCM of the PFC. The bottom left of the oscillogram shows the DCM-waveforms at light load in the Preheating-phase. The bottom right illustrates the CritCM-waveforms during Run-mode with a higher load.

3.1 THD-correction

Figure 3-2 shows two oscillograms at different input voltages. The bottom third of the oscillograms show the PFCGD-On-time over one Input voltage half wave. When the input voltage is decreasing, the On-time of the PFCGD increases and has it's maximum in minimum of the input voltage. The oscillogram on the left side shows the On-time at 180 V_{AC} input voltage and the oscillogram on the right side is taken at an input voltage of 230 V_{AC}. The oscillograms demonstrates the excellent performance of the PFC-stage. In both cases the THD is below 4 % and there is no gap in current flowing near the input voltage minimum visible. For proper THD-correction in other

designs it is necessary to modify the resistance at PFCZCD-Pin in respect to the ratio and value of the PFC Choke and the MOSFET size. A good way to find the optimum is to calculate R_{ZCD} with **Equation (3.1)** in a first step.

Calculation of R_{ZCD} (3.1)

$$R_{ZCD} = \frac{\frac{R_{ZCD}}{N_{PFC}} \cdot V_{BUS}}{1.5\,mA}$$

In a second step a potentiometer can be used to evaluate the optimal value for best THD-optimization.

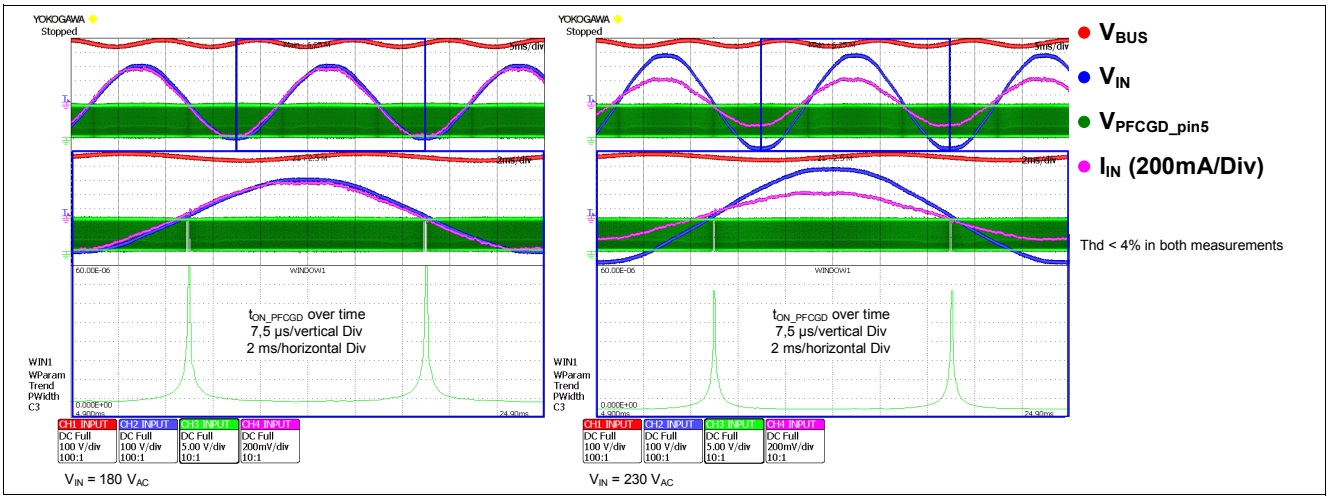


Figure 3-2 THD correction: PFC-On-time enlargement over input half wave

Figure 3-2 shows the waveform of the input current with an THD-optimized resistor at PFCZCD-Pin. The overall THD for the input current harmonics is < 4% with a gapless input current (magenta waveform). The bottom third of the oscillogram shows the On-time of the PFC-MOSFET. Near to the zero-crossing of the input voltage the On-time is increased by the IC via the signal at PFCZCD-Pin for THD-optimization.

4 Ignition regulator - control during ignition

After entering the Ignition-mode, the frequency will decrease from the Preheating-frequency to the Run-frequency. This frequency shift (generated by the internal Digital-Logic) can be measured at the RFPH-Pin. The voltage is 2.5 V during preheating mode and decreases down to GND potential. When the adjusted Ignition voltage is reached the first time, the digital frequency control stays at its working point and an analogue regulator takes over the Ignition voltage regulation in respect to the adjusted frequency of the Digital-Logic. Only when the working point leaves the regulation area of the analogue regulator the Digital-Logic readjusts the frequency. After Lamp ignition the resonant-circuit is damped by the lamp and the IC reduces the frequency down to the adjusted Run-frequency (**Figure 4-1**). The Ignition regulator is also active in PreRun-phase to improve the ignition of lamps with bad ignition behavior.

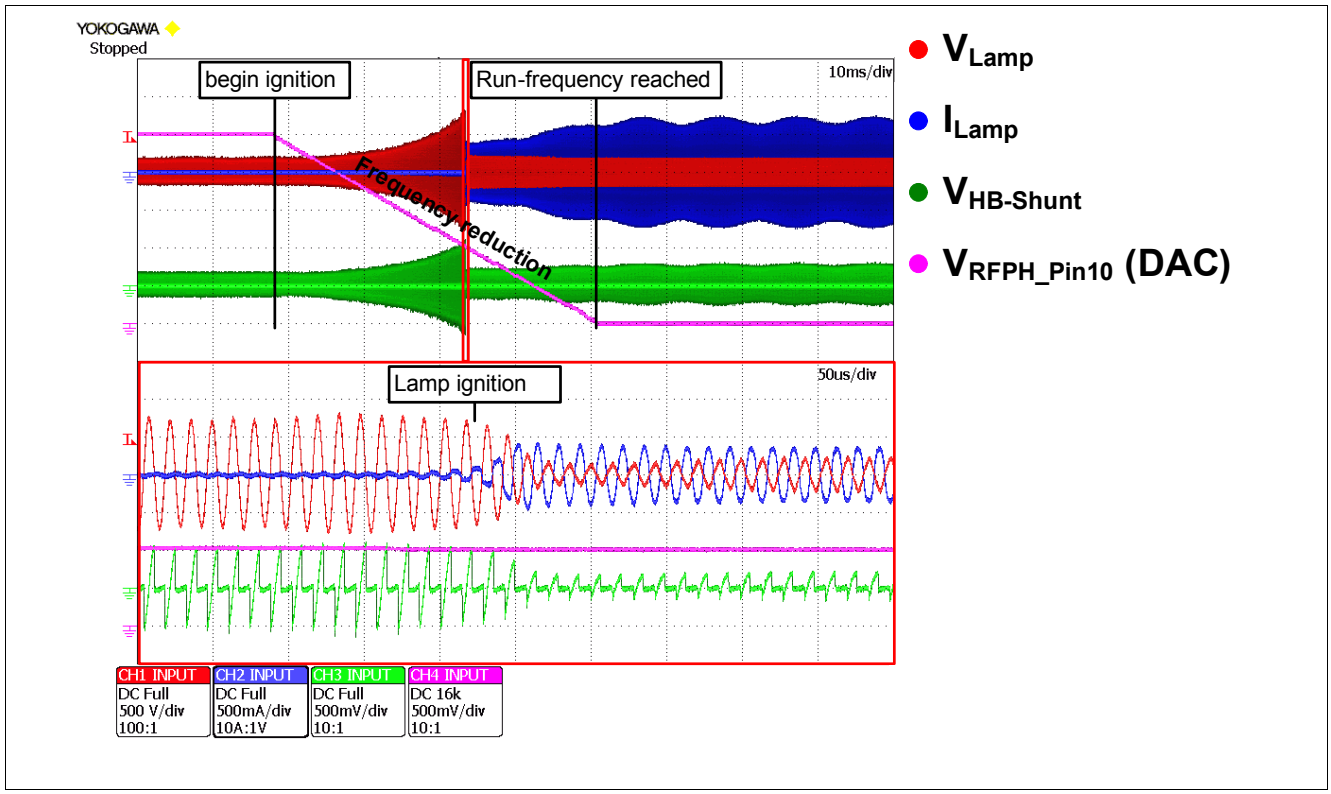


Figure 4-1 Normal Ignition phase

If the voltage at RFPH-Pin (DAC) reaches 0 V during Ignition-phase without successful lamp ignition the sequence control enters PreRun-phase with still activated Ignition regulator. This can be caused due to very high EMI at LSCS-Pin, worse calculation of the resonant-circuit and/or LSCS-shunt-resistors in that way that the Ignition-frequency is close to or below the Run-frequency. Several heavy Bus-voltage breakdowns during ignition can cause this behavior too. The ignition time-out timer can't be set and the Ignition voltage can stay about 625ms longer than the maximum ignition time at the lamp.

4.1 Operation close to different saturation levels

Figure 4-2 shows four oscillograms taken with chokes of different saturation level. The oscillogram in the top, left was taken with the standard choke of the Demo board, the other ones uses modified chokes with a smaller current capability and saturation effects. The Ignition voltage is approximately constant over the saturation behavior of the lamp choke and best Ignition voltage regulation also at high temperature of the lamp choke is possible.

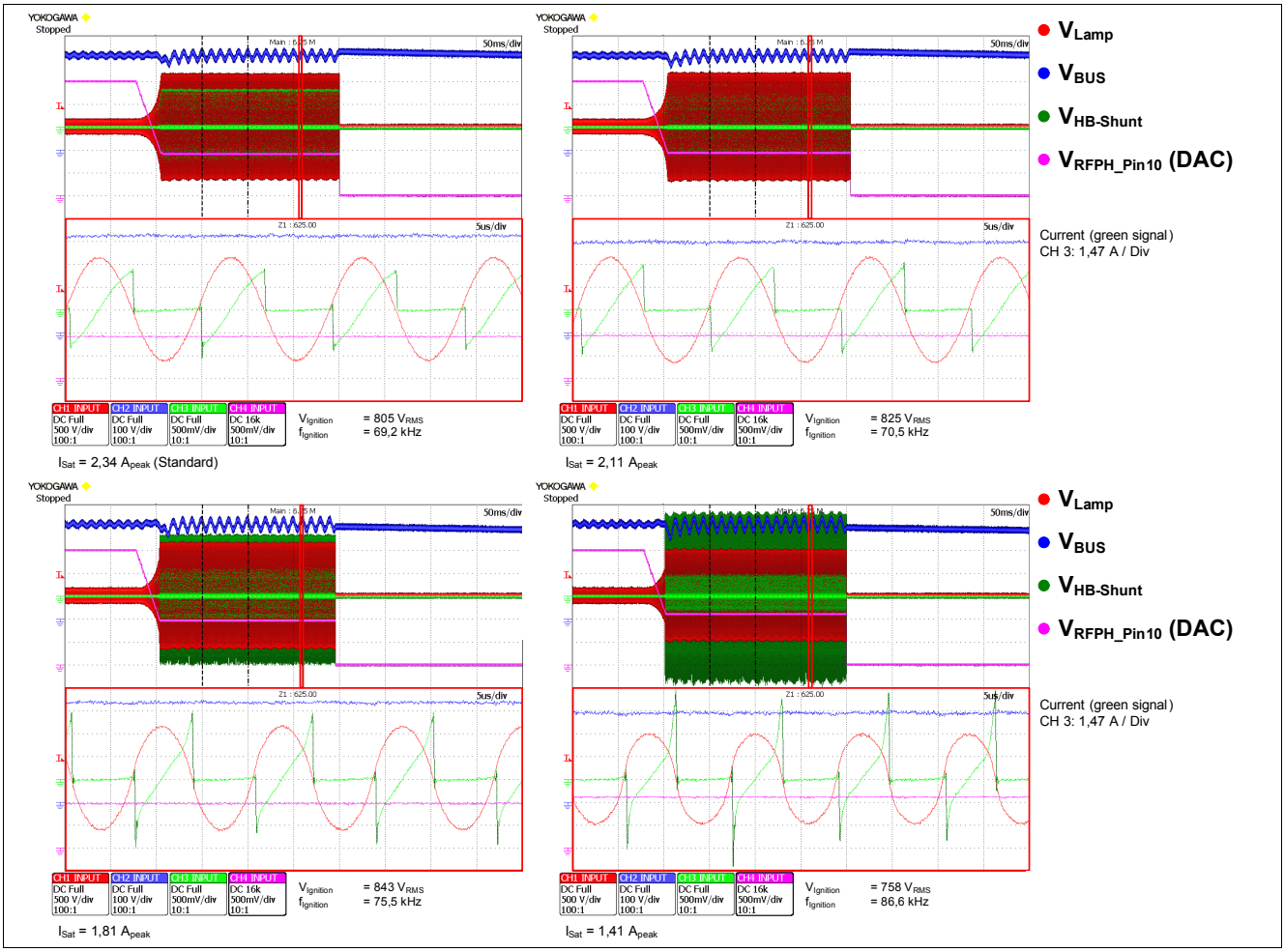


Figure 4-2 Ignition voltage @ different levels of saturation of the resonant choke

These oscillograms demonstrate the performance of the Ignition regulator at different levels of saturation. Actually at relatively low saturation levels the Ignition voltage is a little bit higher than with the standard choke. Even at very high saturation levels the ignition voltage breakdown is only about 5 %. Consequently this Ignition control concept is very suitable for designs working close to the magnetic saturation of the resonant choke and enables best ignition voltage regulating also at higher temperatures of the ballast components. Due to the thermal behavior of the ferrite the ability of the Ignition regulator to work with saturated chokes is a big advantage for restarts with a warmed-up ballast, for example after a certain running time.

4.2 Bus-voltage breakdown during ignition

The following measurements of the Ignition regulator at Bus-voltage breakdown are done with small modifications to the Demo board. The resonant capacitor C_{20} was mounted in a direction to realize current-mode preheating. The Demo board was prepared with 10 Ω substitution resistors for each cathode. This results in very high power consumption during Ignition-mode. The input voltage was also reduced to 170 V_{AC} to provoke Bus-voltage breakdown during Ignition-mode because the limited power that can be transferred by the PFC-stage. **Figure 4-3** shows two oscillograms taken under these conditions to demonstrate that the Ignition voltage control concept is also very suitable for current mode preheating ballasts where the load during ignition becomes very high.

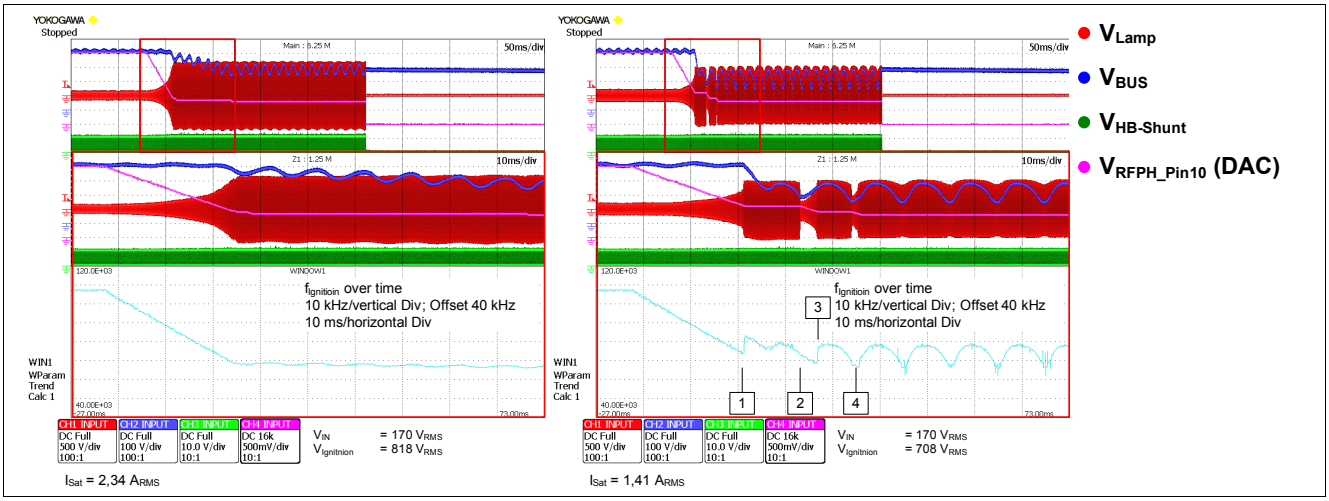


Figure 4-3 Ignition regulator at BUS-voltage breakdown during Ignition-phase

The left oscillogram shows the Ignition voltage without saturation effects of the resonance-inductor. In the bottom third of the oscillograms the Ignition frequency over time is illustrated. After entering the Ignition-mode, the frequency decreases from about 107 kHz down to 70 kHz. At this point the frequency is regulated by the analogue Ignition voltage regulator to the maximum Ignition voltage level. The oscillogram shows that there is no influence of the heavy Bus-voltage breakdown to the Ignition voltage. The Ignition regulator can compensate the Bus-voltage breakdown of about 25 % from 400 V down to 300 V completely.

The oscillogram in the right shows the behavior in the same application under the same conditions but with heavy saturated choke, see **Figure 4-2** bottom right. The Digital-Logic reduces the inverter frequency down to about 75 kHz, then the ignition voltage reaches the adjusted Ignition voltage and the analogue regulator takes over the voltage control (Point 1). Due to the high Bus-voltage breakdown the analogue regulator reaches the end of its working area and the Digital-Logic compensates this in reducing the inverter frequency again (Point 2 to Point 3). After this the analogue regulator takes over the regulation as seen at Point 1. At Point 4 the working area of the analogue regulator is left again and the digital frequency control reduces the frequency. From this point onward, the analogue Ignition control regulator takes over and almost entirely eliminates the high Bus-voltage ripple of about 150 V.

5 Filament detection

The high-side-filament is detected via the LVS-Pin and the low-side-filament is monitored via the RES-Pin. For proper filament detection the LVS- and RES- circuits have to be dimensioned correctly, because they act together and not independent. The RES-Pin acts as a current source and in order of the voltage at this Pin (generated with a resistor R_{36}, connected via the low-side-filament to GND) the IC detects the filaments. The current out of the RES-Pin depends on the voltage-level V_{RES} and the status of the high-side-filament.

When there is no current or a current below the filament detection limit flowing into the LVS-Pin, the current out of the RES-Pin is doubled and in consequence the voltage at this Pin rises and reaches the level for detecting missing filaments. Therefore the result from the high-side-filament detection is mirrored to the RES-Pin. When the low-side-filament at the RES-Pin isn't inserted the voltage at this Pin rises and reaches the Level for detecting missing filaments too because there is no GND connection.

5.1 LVS-Pin

These Pin has the function to detect the high-side cathode before the IC starts and a lamp removal in failure-mode. In the Run-mode this Pin detects the EOL1 (Overload) and EOL2 (Rectifier Effect) conditions. This is realized by analyzing the Amplitude and the DC-offset of the lamp-voltage via an equivalent current into these Pin. If this functions aren't needed, deactivating of the LVS-Pin can be realized by connecting the Pin directly to GND. In this case the EOL1 (Overload) and EOL2 (Rectifier Effect) detection via this Pin isn't possible. A deactivated LVS-Pin can be reactivated when the voltage at this Pin goes higher than $V_{LVSEnable1}$ during Run-Mode. For correct function of the LVS-Pin the resistors for filament detection have to be connected directly after the line rectifier to ensure that the short Input voltage interruption can be detected with the LVS-Pin. The charge of the preheating capacitor C_{21} must be covered by the capacitor in the EOL Network C_{40} in that way that no fail detection of inserted cathode occurs. Has the capacitor in the preheating circuit C_{21} a high capacitance and C_{40} is relatively low, a transient current flows via C_{21} and L_{21} that can be high enough to lead to a high-side-filament detection. For calculation of the LVS-current before startup an internal voltage of 5 V can be used (not specified in the Datasheet - see also chapter **Chapter 8.3.6**). That means that the current flowing into the LVS-Pin can be calculated with the voltage over the LVS-Series resistor (between R_{41} and R_{42}) related to GND subtract by 5 V and divided by the value of R_{41}. The safest solution is to design the LVS-Network in such a way that the voltage at C_{40} stays below 5 V without connected HS-filament.

Calculation $I_{LVSstartup}$ (5.1)

$$I_{LVSstartup} = \frac{V_{C40toGND} - V_{BUS}}{R_{41}}$$

Figure 5-1 shows an oscillogram with the waveforms for Startup without connected high-side-filament. The voltage across C_{40} referred to GND is below 5 V (green signal). Due to the internal voltage of 5 V there is no current flowing into the LVS-Pin and no wrongly high-side-filament detection can occur. When this voltage rises higher than 5 V + $I_{LVSSink}$ multiplied with the value of R_{41} a wrongly high-side-filament detection can provoke one single Startup of the IC. In this case the value of C_{40} or R_{41} can be increased. If possible, a decreasing of the capacitance in the preheating circuit can help to reduce the current flowing into LVS-Pin. A third option is to reduce the feeding voltage by divider R_1, R_2, D_{R12} from the rectified AC input voltage.

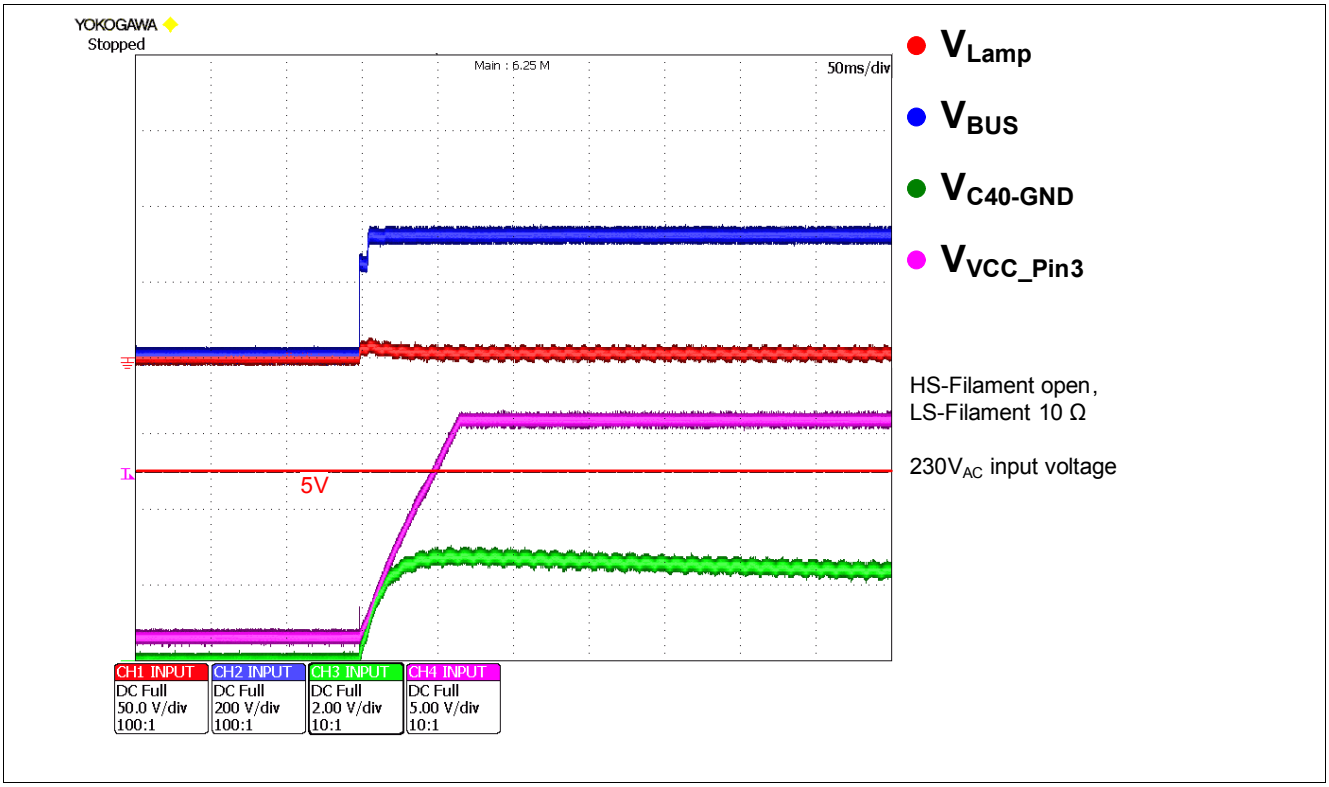


Figure 5-1 Startup without high-side-filament

During Run-mode there is no high-side-filament detection via the LVS-Pin active.

A step by step tutorial for dimensioning of the EOL1 and EOL2 thresholds is given in **Chapter 8.2.1** of this document.

5.2 RES-Pin

For deactivating the filament detection for high-side and low-side-filaments the RES-Pin can be connected directly to GND. As explained in **Chapter 5** this Pin is a current source and detects if the filaments are present via the voltage drop at R_{36}. The current out of the RES-pin is addicted by the LVS-status during Startup and the actual voltage at this Pin. During Run-mode, this Pin detects the low-side-filament. When this filament is broken or removed the voltage will rise up to 5 V. The voltage passes the V_{RES3} threshold for detecting a missing low-side-filament.

For current mode preheating designs an additional series resistor to the RES-Pin (for example 330 Ω) is recommended to avoid destroying the ESD-Structure if the voltage at the RES-Pin rises up to higher levels. This voltage spike can occur in current mode preheating designs at lamp removal and is depending on the resonant circuit and RES-Pin wiring.

For reliable filament detection during Startup the voltage V_{RES} has to reach the filament detection level until the chip supply voltage VCC reaches the turn-on-threshold of V_{VCCOn} (see also **Figure 2-1**).

6 Detection of failures

In this chapter advice and examples for evaluating the failure detection functions are given. Detailed descriptions of the failure conditions can be found in the Datasheet. Chapter 3 and Chapter 4 in the Datasheet show tables and flow charts which protection feature is active in which operating mode and how the IC will react to this failure.

6.1 Surge detection

The ICB2FL03G has implemented a special detection for Surge events. A combined detection of Bus-overvoltage followed by inverter-overcurrent is detected as Surge and leads to a restart without latching this Failure. **Figure 6-1** shows two oscillograms with the signals under Surge condition. For these oscillograms the half-bridge MOSFETs were replaced by 500 V Types to provoke an earlier avalanche breakdown in case of Bus-overvoltage. In the original mounting with 600 V MOSFETs the Surge voltage must be as high that other components can get destroyed before the half-bridge breakdown initiate the Surge detection.

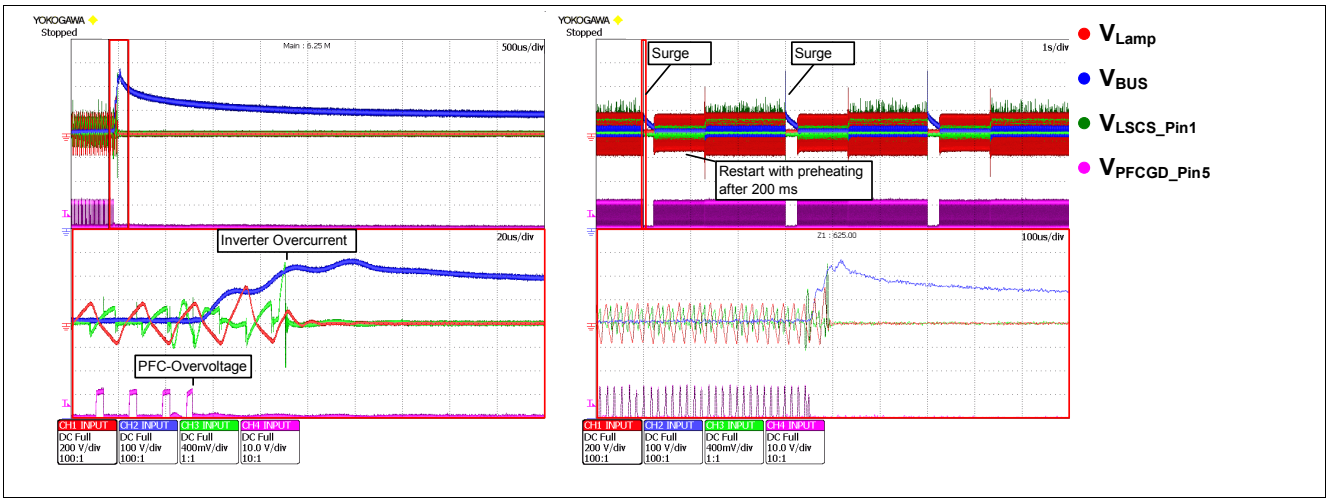


Figure 6-1 Surge detection; Surge Pulse of 1100 V

The left oscillogram shows one single Surge event with a higher resolution and the right one shows three Surge events for explanation of the Flow diagram. Directly after Bus-voltage rising due to the Surge-pulse the PFC-stage detects PFC-overvoltage and stops the PFCGD. At a Bus-voltage of about 620 V the half-bridge MOS-FET breaks down due to the avalanche effect. This results in a high current spike at LSCS-Pin. The IC detects this overcurrent during overvoltage and stops inverter gate drives (see Chapter 3.3 in the Datasheet - “Fault A”). This signal combination doesn’t increment the “Fault Counter” and leads to an IC restart after about 200 ms with preheating. This can be seen in the right oscillogram.

It is important that the time constant of the low pass filter at this the PFCVS-Pin (generated by the voltage divider and C_{11}) is small enough that the voltage can rise fast enough to the 109 % threshold during Surge conditions. Otherwise the Surge condition can’t be clearly detected.

6.2 Inverter-overcurrent protection

The inverter-overcurrent protection via the LVS-Pin detects two different thresholds dependent on the actual operation mode. The first threshold of $V_{LSCSOvC2}$ is only active during Preheat- and Run-mode. In all other modes the detection threshold of $V_{LSCSOvC1}$ is active for inverter-overcurrent protection. Overshooting these thresholds results in a single restart of the IC. After a second detection within 40 s the IC goes into latched fault-mode. This means that an input voltage interruption or a lamp removal is necessary for a new startup of the IC.

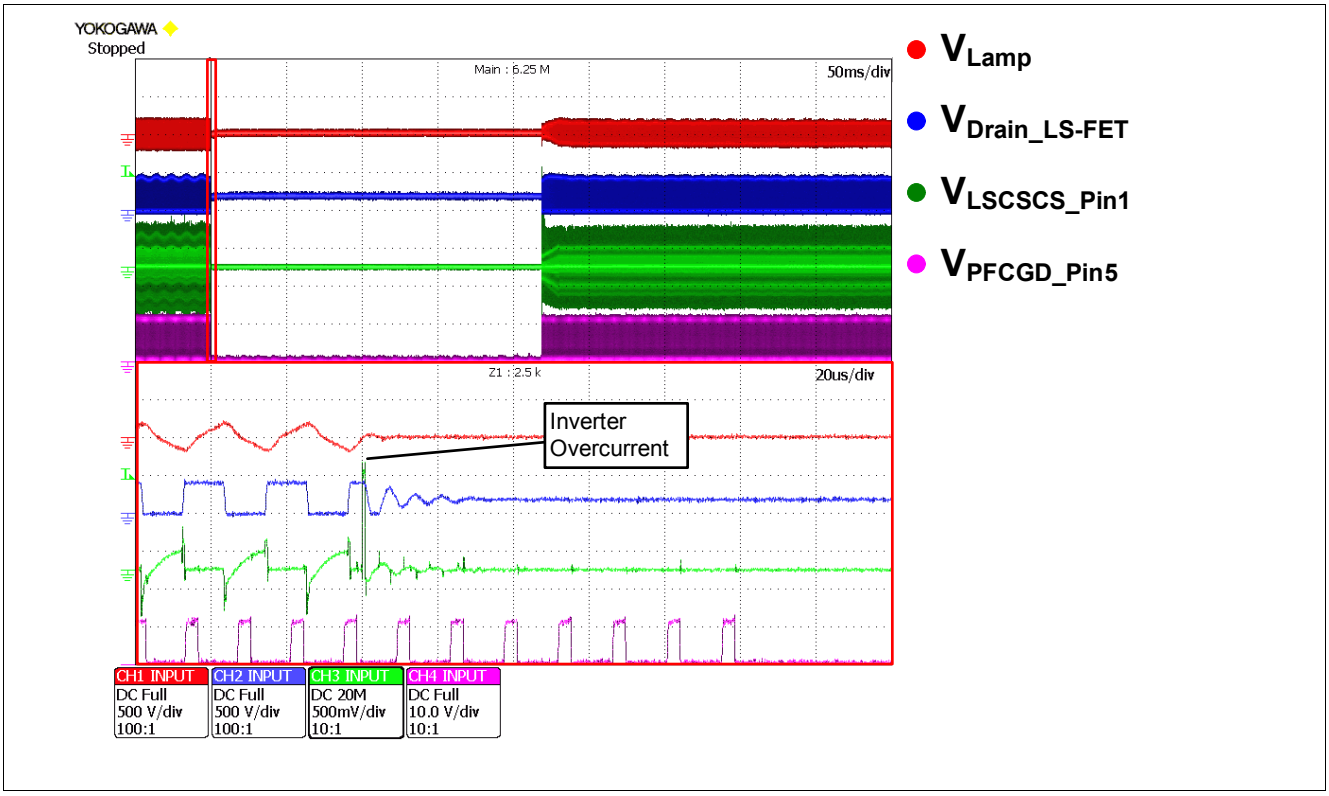


Figure 6-2 Inverter Overcurrent

Figure 6-2 shows an oscillogram with a generated inverter-overcurrent. For this measurement a series resistor of 1 kΩ was inserted in series to the LSCS-Pin. The overcurrent signal is generated by a waveform generator and is overlaid directly to the LSCS-Pin via a diode.

The half-bridge (blue signal) stops immediately after detecting inverter-overcurrent - Fault F. With a short delay of about 100 µs the PFCGD stops working too. This delay is caused by the Digital-Logic. About 200 ms after turning off and incrementing the failure counter, the IC starts another Startup. When there occurs a second inverter-overcurrent or another Fault F failure within 40 s the IC goes into latched fault-mode.

6.3 PFC-overcurrent protection

Figure 6-3 shows an oscillogram of the Demo board Startup. The green waveform shows the voltage at the PFCCS-Pin (across the PFC-Shunt resistor of 1 Ω). In the beginning the PFC starts in a Soft start-mode and a short turn-on-time. The turn-on-time is increased continuously because the Bus-voltage is below the nominal value (red area of the Oscillogram).

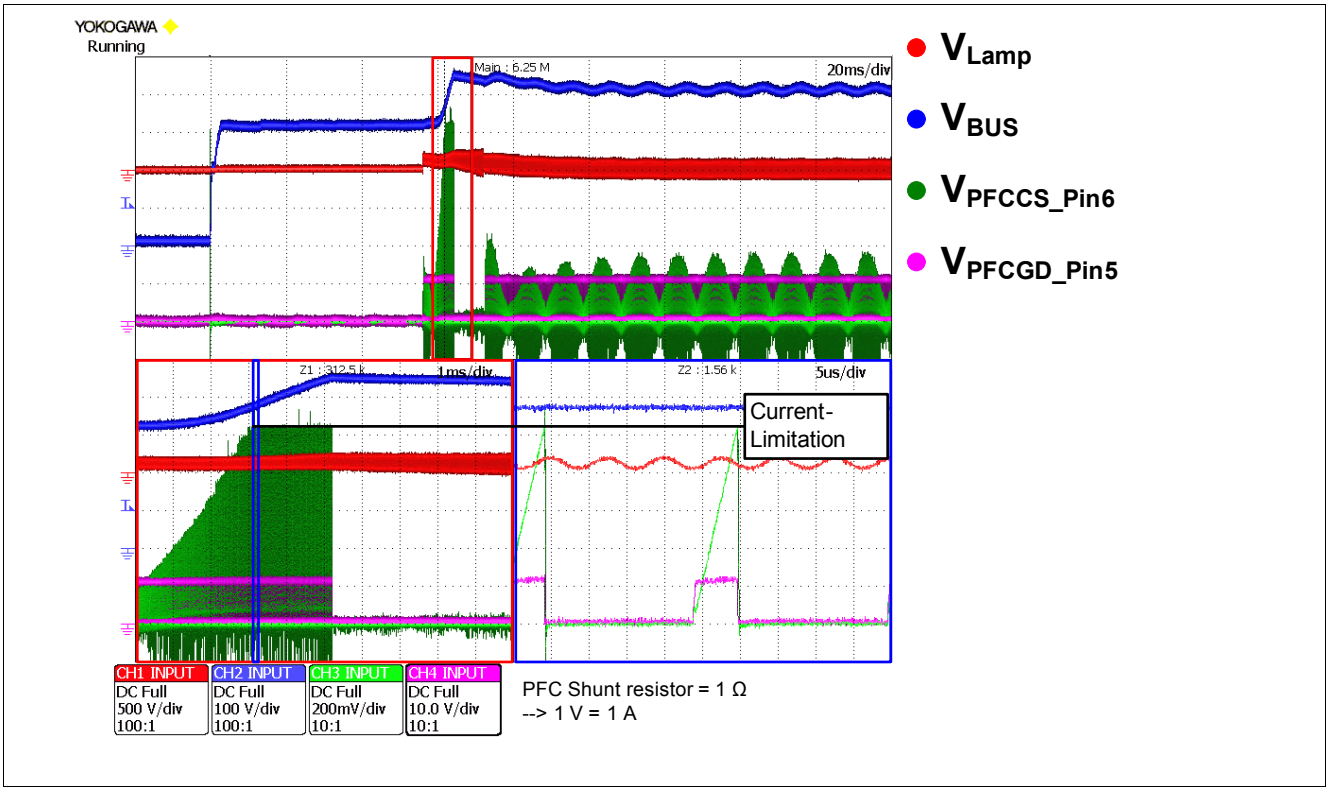


Figure 6-3 PFC-overcurrent

The current through the PFC-inductor increases and after reaching the PFC-overcurrent threshold of $V_{PFCCSOff}$ the PFCGD turns off cycle by cycle. This working point is shown in the blue area of the oscillogram and is not handled as a fault of operation. This feature protects the PFC-stage against overload.

6.4 Bus-overvoltage protection 109% - 105% threshold

Dependent on the input voltage a short Bus-overvoltage can occur during Startup, fully covered by the Bus-overvoltage protection. **Figure 6-4** shows an oscillogram for explaining the functionality of the Bus-overvoltage protection. Start-up activates the inverter gate-drives and the PFC-gate-drive with a short delay. Then the Bus-voltage rises and reaches the 109 % threshold. The PFC-gate-drive stops immediately as long as the Bus-voltage is above the 105 % threshold and the PFC-gate-drive is activated again and the Bus-voltage goes to the nominal value. If the Bus-voltage is > 109% for longer than 625 ms the IC goes into power down and stops working. The IC restarts automatically without preheating when the Bus -voltage is below the 105 % threshold.

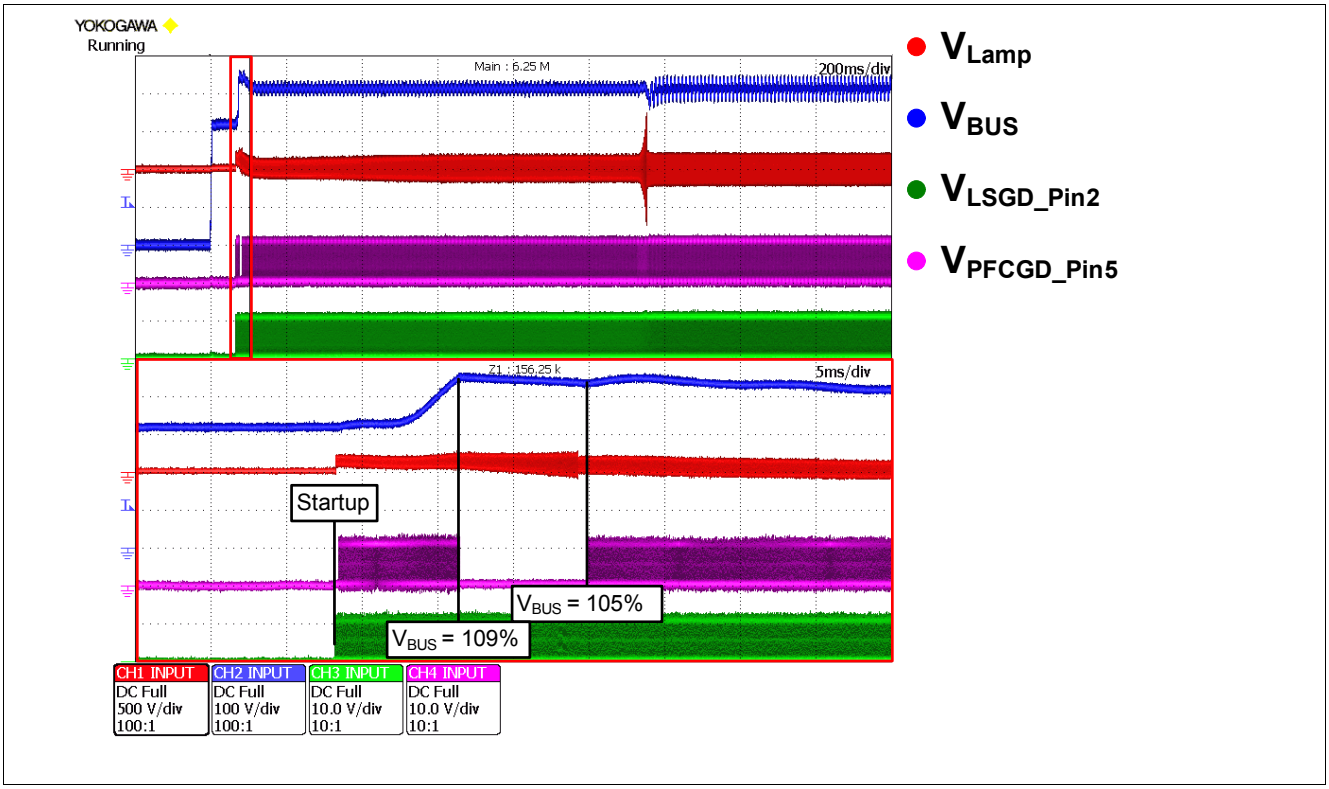


Figure 6-4 Bus-overvoltage hysteresis (Startup)

An additional description of the overvoltage detection in Run-mode can be found in **Chapter 6.1**. The Surge detection described in that chapter is a combined detection of Bus-overvoltage and inverter-overcurrent during PreRun- or Run-Mode.

6.5 Bus-undervoltage protection in Run-Mode 75% threshold

This failure protection is described in **Chapter 6.8** because it is used for the Emergency Lighting feature. Bus-undervoltage can also occur in other operation modes. This results in running with lower Bus-voltage until the IC detects this failure condition after entering Run-mode.

6.6 EOL detection

This chapter gives a short introduction how the EOL (End of Life) tests with high accuracy can be done at our Demo board. More informations and a description of the normative measurement can be found in EN61347-2-3 (VDE 0712-33). The names EOL1 and EOL2 are defined by Infineon Technologies AG. A Lamp overvoltage/overload is called EOL1 and the rectifier effect according to the normative is called EOL2. The normative contains also circuit descriptions, that are necessary for doing the EOL-tests on the ballast. An additional description how this detection works can be found in chapter 2.5 of the Datasheet. The EOL conditions are monitored via the LVS-Pin. A step-by-step guide with a detailed explanation for a basic calculation of the LVS-network is given in **Chapter 8.2.1**. Due to some neglects in the calculations an experimental adjustment in the circuit can be necessary.

For the following measurements the Demo board was supplied with 230 V_{DC} because at DC-supply there is no influence of the AC-ripple to the measurement. When the tests are done with AC supply it is important that the measurement field covers in minimum a full input voltage half wave and an integer multiple of it. Otherwise, due to the AC-Ripple, the measurement isn't reproducible. In this case the resolution of the oscilloscope must be high enough to record the whole high-frequent waveforms with a good accuracy.

6.6.1 EOL1 (Overload)

Figure 6-2 shows an oscillogram after EOL1-detection and an example for the EOL2 test setup.

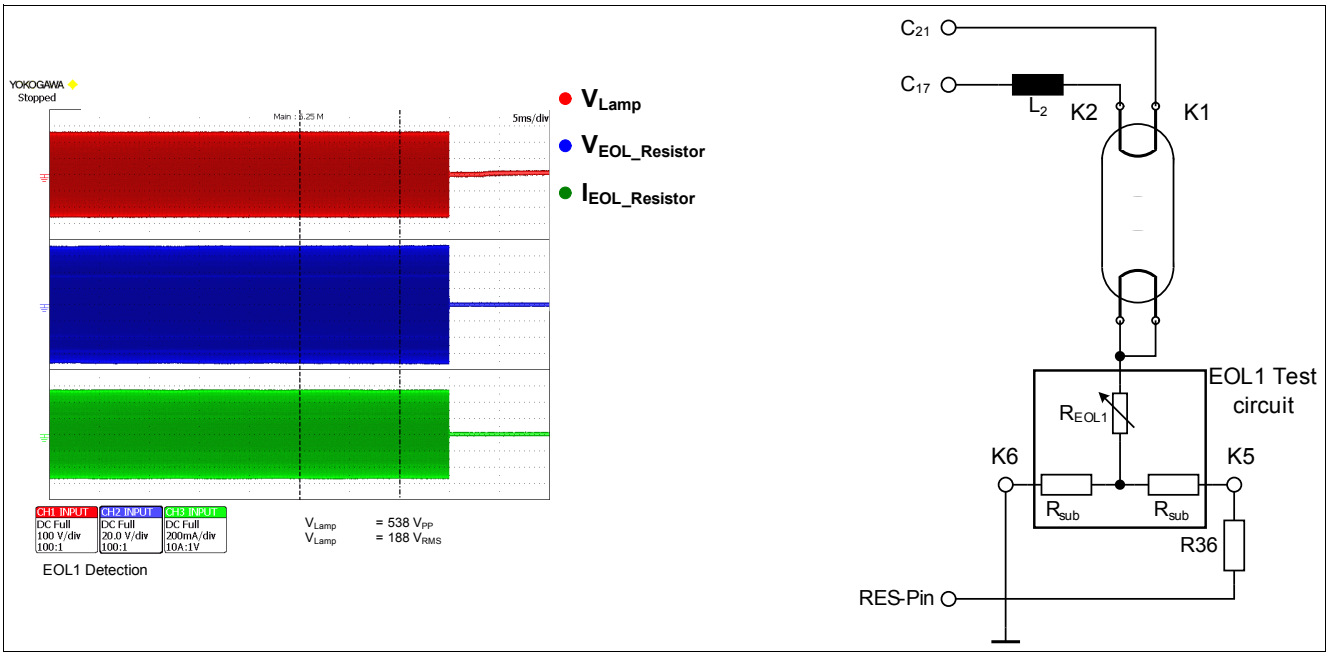


Figure 6-5 EOL1 (Overload) detection; EOL1 test setup

The test was done with a series resistor to the Lamp. The resistance of the series resistor was increased until the IC detects the Lamp-overvoltage and goes into the failure analysis flow. The measured EOL1 shutdown voltage was 538 V_{PP}. This value matches very good with the calculated one (**Chapter 8.2.1**). There is an internal Counter which counts up when the EOL1-event is present and counts down when the EOL1-event isn't detected. When the EOL1-threshold isn't reached in every cycle the time to turn-off the IC can be longer than 620 µs.

6.6.2 EOL2 (Rectifier Effect)

Figure 6-6 shows an example test setup for the EOL2 test. A complete description can be found in the normative EN61347-2-3 (VDE 0712-33). When the current flows via D1, a positive rectifier effect is simulated (EOL2+). current flowing via D2 simulates negative rectifier effect (EOL2-). The level of the positive or negative superimposed lamp-voltage can be adjusted with REOL2. The higher the value of this resistor is, the higher is the EOL2 voltage because the resonant circuit of the Demo board works like a constant current source for the lamp current.

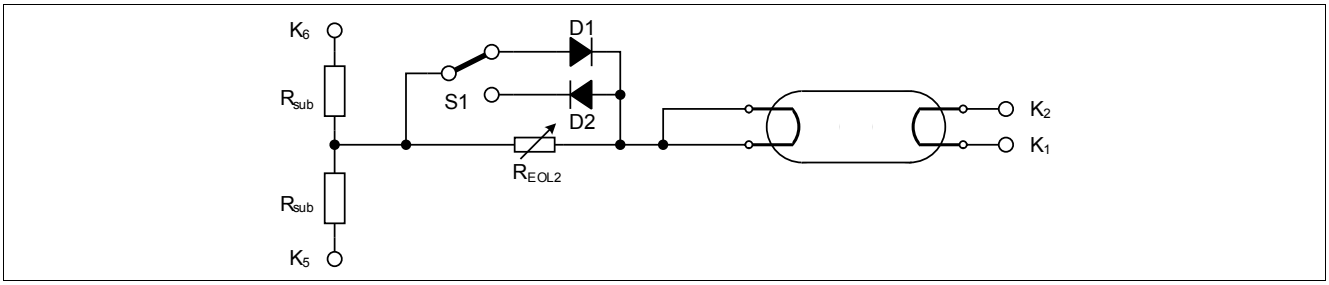


Figure 6-6 EOL2 Test Setup

This failure condition is allowed for a duration 2.5 s, until the IC goes into failure analysis flow. So for the exact measurement of the EOL2 thresholds it is important to increase the value of R_{EOL2} very slow. The EOL2-Power can be calculated by multiplying the RMS-values of the current through R_{EOL2} and the voltage over this resistor. Figure 6-7 shows an example measurement for EOL2+ (left) and EOL2- (right) detection.

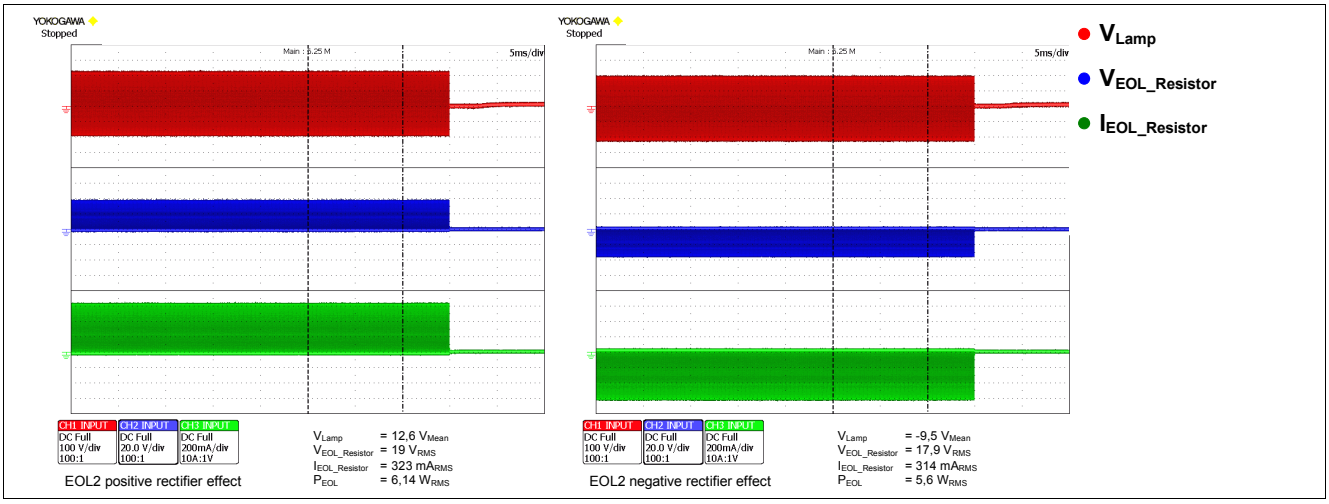


Figure 6-7 EOL2 (Rectifier Effect) detection

The measured values for EOL2-detection are +6.1 W and -5.6 W. The calculated values from **Chapter 8.2.1** are 5.3 W for EOL2+ and 5.3 W for EOL2- and a little bit lower than the measured values. This is founded in some neglects of the calculations and the influence of the voltage drop of the diode (D_1 or D_2 of the test circuit) which generates a higher RMS-value of the voltage via the EOL2-resistor for the measured values. So an experimental adjustment in the circuit can be necessary. Please note, that parasitic inductivity of the resistors have to be low.

The difference between the positive and negative threshold is founded in the internal IC design. There is an internal series resistor of about 5 kΩ to an internal voltage source of about 600 mV at the LVS-Pin (not specified in the datasheet). The internal signal processing of the IC generates an internal potential at the LVS-Pin of about 800 mV at +42 µA and about 400 mV at -42 µA. Due to these differences the positive lamp-voltage shift for EOL2 must be higher than the negative to reach the EOL2 turn-off current in the LVS-Pin. The EOL2 power results of the lamp current multiplied with the EOL2 lamp-voltage shift. Consequently the difference between positive and negative EOL2 rises with the Lamp current because the needed EOL2 lamp-voltage shift for the same EOL2 power is smaller and the influence of the voltage at the LVS-Pin becomes higher. **Figure 6-14** shows an theoretical example of this influence for a designed EOL2 Power of 6 W.

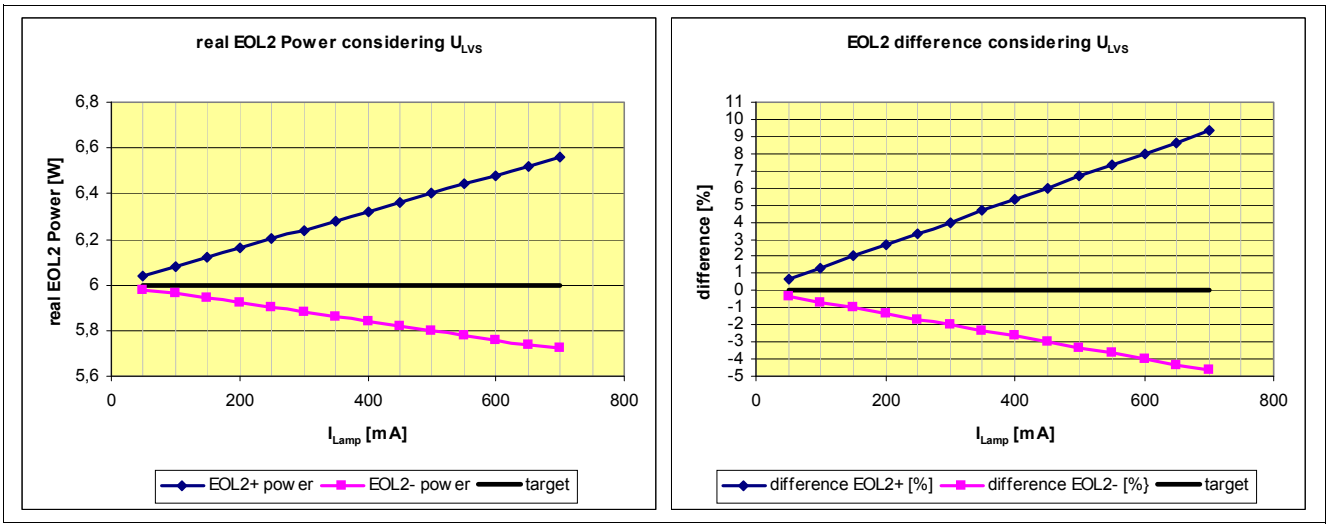


Figure 6-8 EOL2 Power Difference

When the symmetry between the positive and negative EOL2 Power must match as good as possible, an additional compensation circuit can feed an additional current into the LVS-Pin to correct the offset/unsymmetrical

between the positive and negative EOL2 thresholds. **Figure 6-9** shows an example for such a compensation circuit.

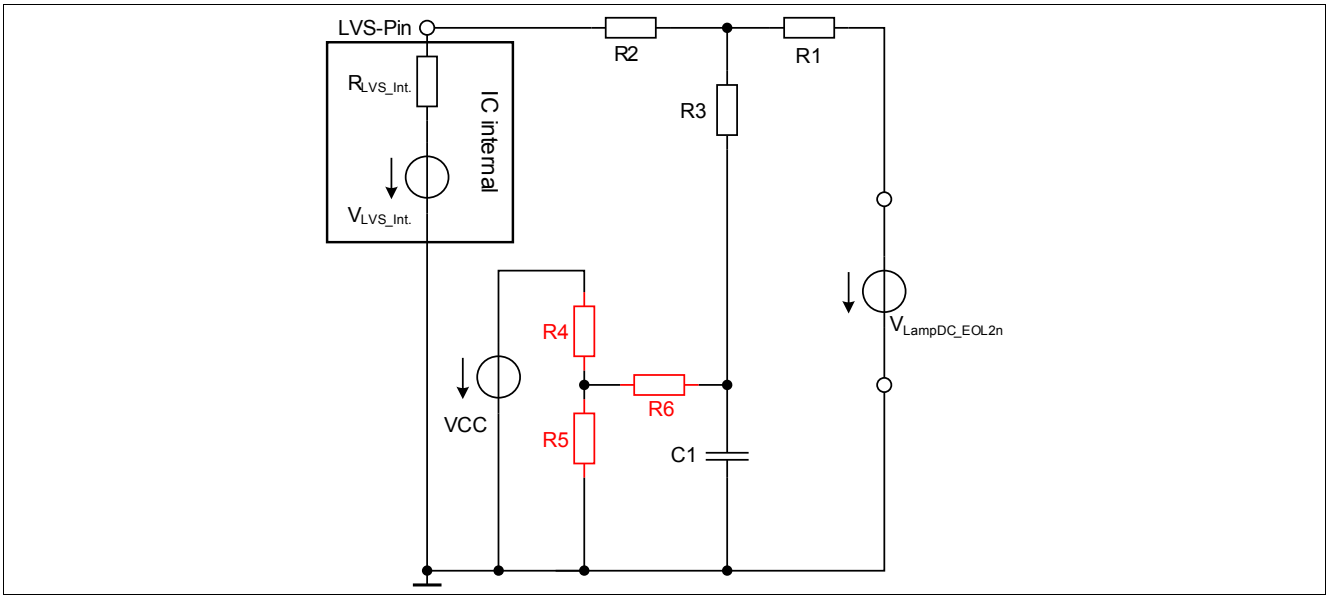


Figure 6-9 Compensation circuit for better EOL2 symmetry @ high lamp currents

The reference names of R_1, R_2, R_3 and C_1 are referenced to the small schematic in **Figure 8-4** and these components are a part of the standard BOM without compensation at LVS-Pin. For the compensation circuit only three resistors connected to the IC supply voltage are necessary (red colored). For this design a good matching between the positive and negative EOL2-threshold can be achieved with R4 = 2.2 MΩ, R5 = 680 kΩ and R6 = 470 kΩ. Due to the high-ohmic values of the resistors there aren't high losses in this compensation circuit. Please note, that this circuit can influence the filament detection via the current into the LVS-Pin before Startup.

6.6.3 Switched-rectifier-effect

Figure 6-10 shows two oscillograms of the IC behavior when the switched-rectifier-effect (according EN61347-2-3; VDE 0712-33) occurs during Run-mode. Applying this test to the ballast leads to an EOL1-detection because the peak Lamp-voltage rises up to the EOL1-detection limit and the duration to turn off is much shorter than for EOL2-detection. There is an internal Counter which counts up when the EOL1 event is present and counts down when the EOL1-event isn't detected. When the EOL1-threshold isn't reached in every cycle the time to turn-off the IC can be longer than 620 µs (e.g. amplitude is close to the detection limits). After detecting EOL1 the IC goes into Power-down-mode with a typical current consumption of IVCCLatch. In this mode, the maximum LVS-current for safe operating area is limited to max. 210 µA. Due to this failure condition the voltage at C40 referred to GND can rise up to high values and a voltage limitation at C40 might be necessary to limit the current flowing into the LVS-Pin.

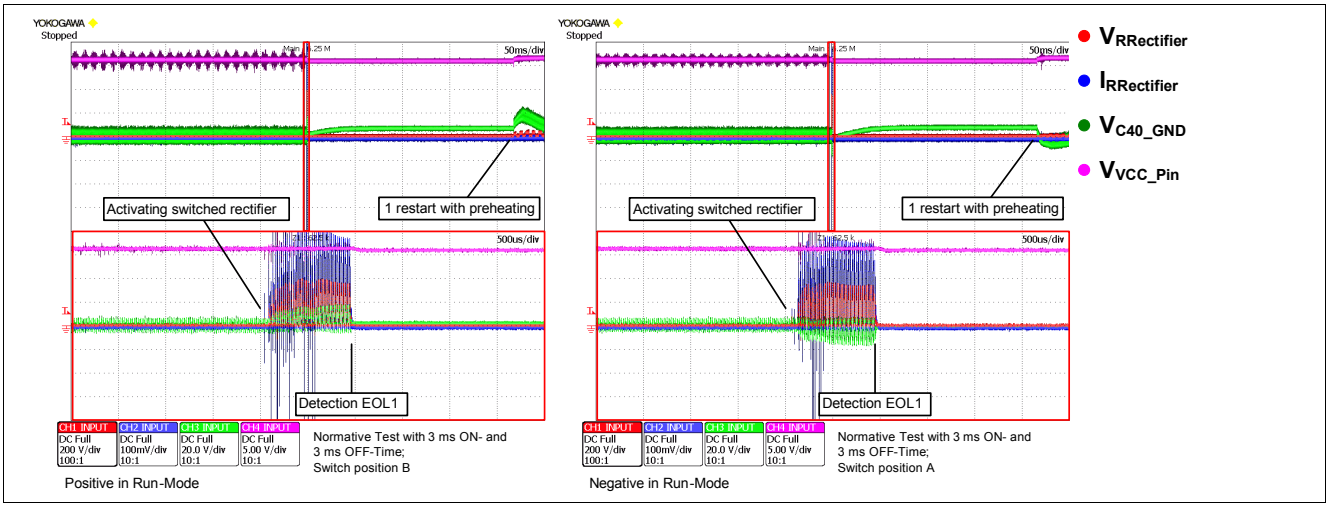


Figure 6-10 Switched-rectifier-effect according EN 61347-2-3 (VDE 0712-33)

The left oscillogram shows the signals when the switched-rectifier-effect is applied in negative direction and the right one shows the behavior at positive switched rectifier effect.

Result: The requirements of the normative are fulfilled.

6.6.4 Hard-rectifier-effect

Figure 6-11 shows two oscillograms with the IC behavior when the hard-rectifier-effect (according EN61347-2-3; VDE 0712-33) occurs during Run-mode.

Applying this test in Run-mode leads to an EOL1-detection due to the same reasons explained in **Chapter 6.6.3**.

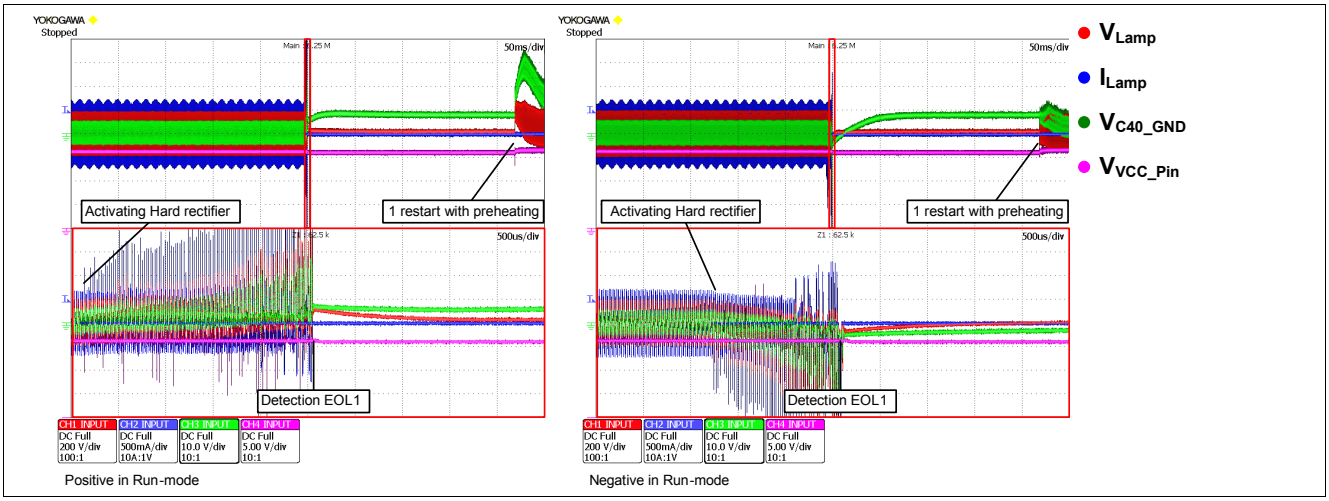


Figure 6-11 Hard-rectifier-effect according EN 61347-2-3 (VDE 0712-33)

The left oscillogram shows the signals when the hard-rectifier-effect is applied in positive direction and on the left side the hard-rectifier-effect is applied in negative direction.

Result: The requirements of the normative are fulfilled.

6.7 Capacitive load (Cap Load)

This chapter should give a good understanding to the effects when the ballast works under cap load conditions. For an explanation, there are two oscillograms which show oscillograms the signals under cap load 1 and cap load 2. Further information to this can be found in the Datasheet, Chapter 2.6.

6.7.1 Cap load 1 (Idling detection / current mode preheating)

This protection feature is only necessary in current mode preheating topologies, where the half-bridge goes into idling operation when the lamp is disconnected during Run-mode. In current mode preheating designs, the resonant capacitor (C_{20}) is connected “behind” the lamp cathodes, so the cathodes are in series with the resonant capacitor. Removing the lamp and the cathodes results in an open load condition with direct charging and discharging of the Snubber C_{16} by the MOSFET and the half-bridge goes over into cap Load 1 operation.

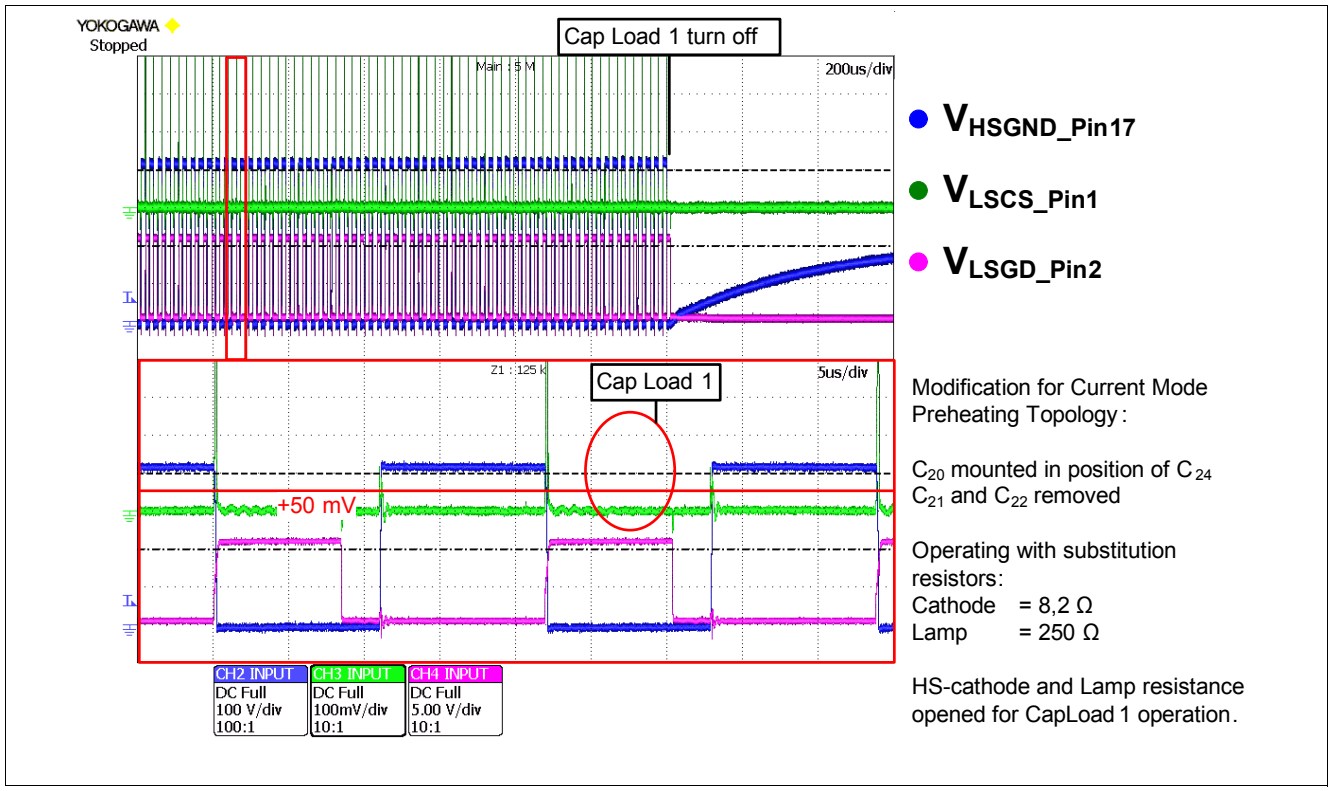


Figure 6-12 Cap load 1 detection in designs with current mode preheating

Figure 6-12 shows an oscillogram in cap load 1 operation with a modified Demo board for current mode preheating topology. The modification to the Demo board is described right beside the oscillogram. The horizontal red line indicates the VLSCSCap1 threshold and the red circle indicates the area, where the Signal of the LSCS-Pin should reach this threshold during normal operation.In this oscillogram is only a high current spike in the moment of turning on the LS-FET present. This leads to a “Fault F” detection after about 2500 ms.

In current mode preheating designs there is a higher probability for Overload detection during ignition mode. In current mode designs the voltage at the RES-Pin can increase to very high levels when removing the lamp during Ignition- and Run-Mode. Please check **Chapter 5.2** for information how the circuit at the RES-Pin can be modified for this ballast topology.

6.7.2 Cap load 2 (Overcurrent / operation below resonance)

Cap load 2 operation can only occur in Designs when the Run-frequency is below the resonance-frequency of the unloaded resonance-circuit. Cap Load 2 operation is detected if the voltage at LSCS-Pin is below $V_{LSCSCap3}$ for longer than $t_{LSCSCap2}$ directly before the HSGD is turned on or exceeds a threshold of $V_{LSCSCap2}$ for longer than $t_{LSCSCap3}$ during On-switching of the HSGD. The duration for detecting this failure is 620 µs.

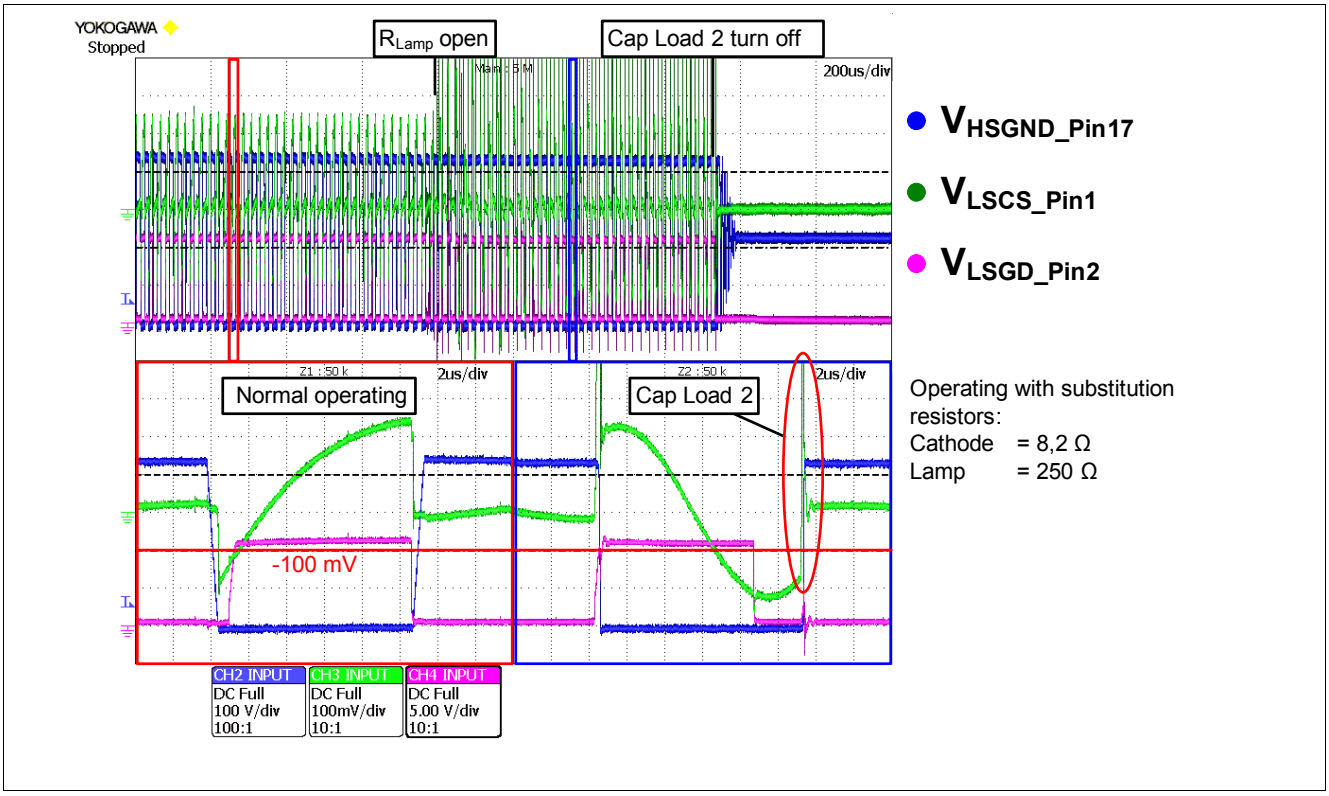


Figure 6-13 Cap load 2 detection

Figure 6-13 shows an Oscillogram under Cap load 2 operation. The red circle shows the relevant area for detecting Cap load 2.

6.8 Emergency detection

The ICB2FL03G supports the Emergency detection requirements (according VDE 0108). For fulfilling this normative it is necessary that the illumination comes back immediately after short input voltage interruptions. The ICB2FL03G detects short interruptions of the input voltage via the LVS-Pin together with the value of the Bus-voltage and restarts in a certain time frame directly with lamp ignition without pervious preheating phase.

Please check the advice in **Chapter 2** and **Chapter 5.1** to design the ballast in that way that the correct function of the Emergency detection is guaranteed. At input voltage interruption the IC-supply has to be connected to the Bus-voltage. **Figure 6-14** shows an oscillogram that demonstrates the functionality for this feature. The oscillogram shows the following sequences: One start from connecting the input voltage to Run-mode followed by input voltage interruption of about 250 ms with directly lamp ignition without preheating and then an input voltage interruption of about 3 s in Run-mode.

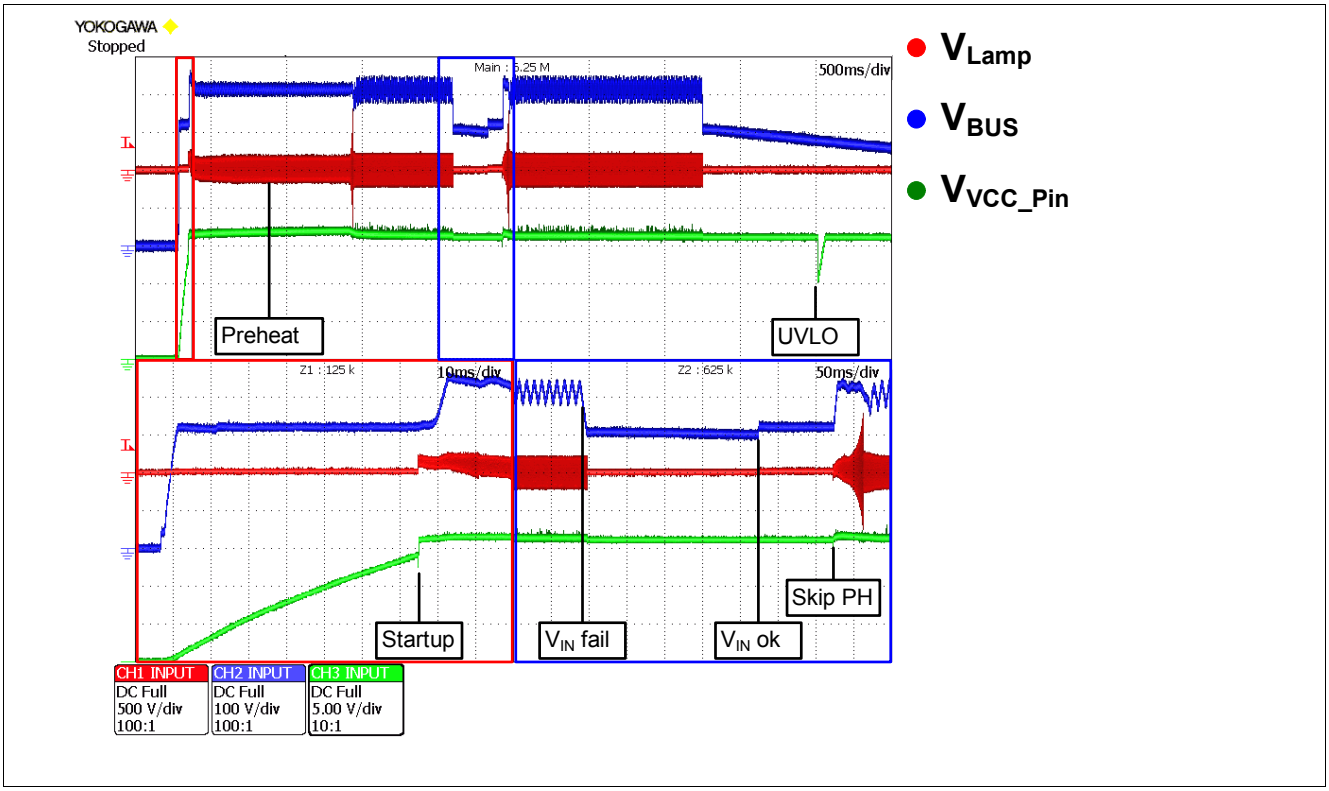


Figure 6-14 Emergency detection

The bottom left of the oscillogram shows the phase from turning on the input voltage into preheating phase. The bottom right of the oscillogram shows input voltage interruption in Run-mode (V_{IN} fail) for about 250 ms. After reaching 75 % of the rated Bus-voltage the IC detects Bus-undervoltage sets the skip preheating flag and stops the inverter. The current consumption goes down to a minimal value and the IC checks the presence of the cathodes 7 times in an interval of t_{TIMER1}. When the input voltage is present again (V_{IN} ok), checked via the current into the LVS-Pin and the counter skip preheating is < 7 the IC restarts without preheating. In the top right of the oscillogram there is second interruption of the input voltage for longer than 700 ms and the IC goes into self generated reset (via UVLO). This resets the skip preheating flag and the IC will start with preheating after a new input voltage detection. For external supply it must be ensured that the IC can perform this UVLO.

7 Advice for Design, Layout and Measurements

This chapter gives some advice for ballast design with the ICB2FL03G. Furthermore some additional technical information to the IC function and advice for measurements are given.

7.1 Deactivation of lamp section

7.1.1 Deactivation of lamp section

For evaluation of the PFC-stage without the lamp section, easy deactivation of lamp circuit is possible. In a first step, the voltage level at LSCS-Pin must be higher than $V_{LSCSCap1}$ to prevent detection of Cap Load 1. A voltage divider from VCC with a Level of about 200 mV at LSCS-Pin is the easiest way for realization this. Without lamp section, the VCC-supply can't be realized via the charge pump so an external supply is necessary (please note the information in the Datasheet, Chapter 3.3 for restrictions at external supply). The LVS- and RES-Pin can be directly connected to GND to deactivate the Lamp protection functions. With this modifications, the Pins and assembly around of HSGD, HSVCC, HSGND and LSGD can stay not connected for full PFC-functionality without lamp section.

7.2 Deactivation of PFC section

For evaluation of the lamp circuit without the PFC-stage, easy deactivation of PFC-stage is possible. To prevent any failure detection of the deactivated PFC-section a voltage level at PFCVS-Pin between $V_{PFCVS95}$ and $V_{PFCVSLOW}$ is necessary. If the voltage at PFCVS is < $V_{PFCVS95}$ the IC restarts 80 ms after activation of the half-bridge and the PFCGD. A level > $V_{PFCVSLOW}$ prevents the IC going into Startup and no Pulse out of the gate drives is visible. The easiest way is to set this voltage with an external DC-supply or a combination of Z-Diode, resistor and voltage divider connected to the VCC-voltage of the IC. With this modification, the Pins and assembly around of AUX, PFCZCD PFCGD and PFCCS can stay not connected for full inverter-functionality without PFC section. If the voltage at PFCCS is between $V_{PFCCSOff}$ and V_{PFCCS_max} (6 V) the PFCGD is inactive and there is no EMI influence of this gate drive.

7.3 RFPH-Pin (Preheating frequency)

The resistor at RFPH-Pin sets the preheating frequency. This Pin is also very helpful for evaluating the device because the voltage level indicates the Status of the Digital-Logic during preheating phase. **Figure 7-1** shows an oscillogram for signal description at this Pin. The voltage at this Pin was filtered by a 16 kHz low-pass-filter in the Oscilloscope. This can be done because there is no interest on fast Signal changes. In the Soft start-phase the voltage at the RFPH-Pin rises up to 2.5 V in 16 Steps and the Inverter frequency is reduced from $F_{StartUp}$ down to the adjusted preheating frequency. Reaching a level of 2.5 V indicates entering the preheating phase. The logic stays in this phase for the time adjusted by the resistance at RTPH-Pin. By reaching the end of the preheating time, the logic enters Ignition-phase and the voltage at RFPH-Pin begins decreasing down to GND-potential in 127 steps within 40 ms while reducing the Inverter frequency down to the Run-frequency adjusted by the resistance at RFRUN-Pin. Decreasing stops when the Ignition control becomes active and goes on when the lamp ignites.

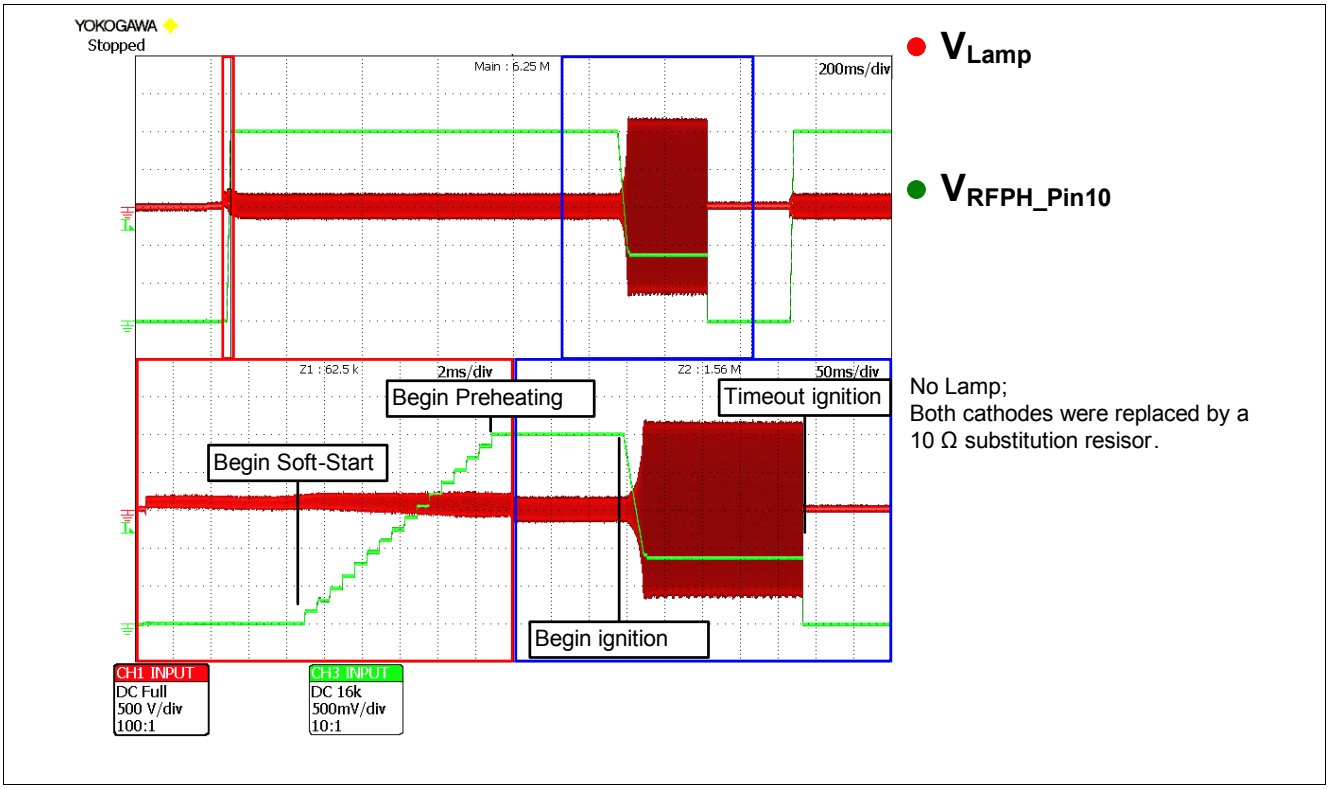


Figure 7-1 Status on RFPH-Pin

This measurement was done only with cathode substitution resistors and no ignition is possible. In this case the Logic detects Ignition Time-out after $t_{NOIgnition}$ and generates on single restart after 200 ms.

7.4 RTPH-Pin (Preheating time)

The preheating time can be adjusted with a resistor between 0Ω and 25 kΩ (equivalent to a preheating time of 0 to 2.5 s) at RTPH-Pin. The voltage at this Pin is also linear to the resistance at RTPH-Pin (0 - 2.5 V). The preheating time t_{RTPH} is divided in 127 counter steps, each with a duration of about 20 ms and an equivalent voltage step at RTPH-Pin of about 20 mV. Dependent on the voltage at the RTPH-Pin the preheating time can fluctuate up to 20 ms when the voltage at this pin is close to these voltage steps.

7.5 PFCVS-Pin

This Pin senses the Bus-voltage and has a protection against operation loop protection when the Bus-voltage falls below 12.5 % of rated level. This protection function can also be used for switching the IC off and on with a microcontroller. When using this Pin for IC Shutdown it is important that the voltage drops very fast below a level of 12.5 % to prevent the PFC-regulation in rising the Bus-voltage to higher levels for compensation. A level higher than 12.5 % leads to a new IC-Startup without preheating for a restart time < t_{TIMER1} and with preheating when the turn-off phase was longer than t_{TIMER1}.

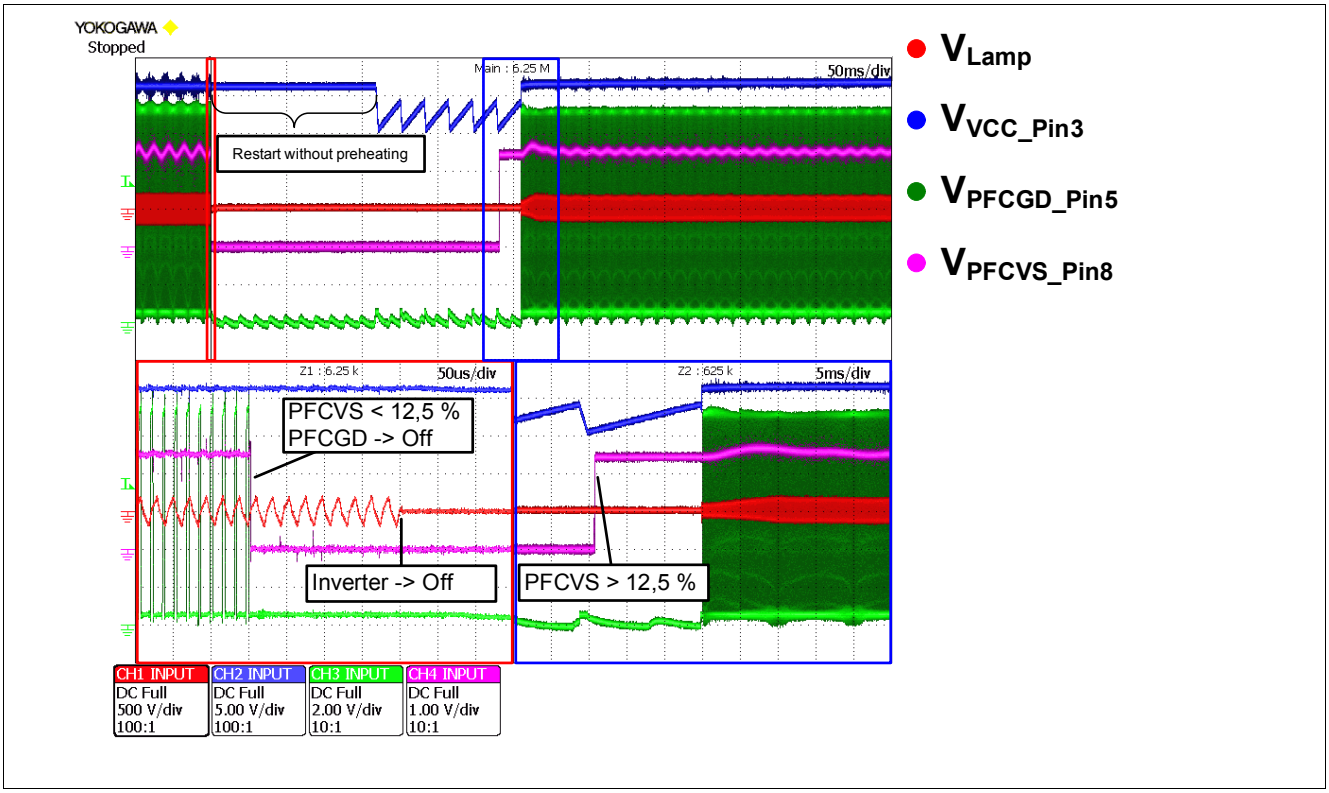


Figure 7-2 IC turn-off and on via PFCVS-Pin

Figure 7-2 shows an example measurement for explaining the logic flow in case of turning off the ballast via PFCVS-Pin. Directly after switching the PFCVS-signal to a level < 12.5 % the PFCGD stops working. With a delay of about 200 µs the inverter stops working too because of reaching the 75 % threshold for Bus-voltage and the IC detects “Fault U - Bus-undervoltage” (see Chapter 3.3 in the Datasheet). Within a time of t_{TIMER1} the IC restarts without preheating when the level at PFCVS-Pin is > 12.5 %. After this time the IC goes into Power-up because the lamp detection is ok and VCC is > VVCCOn. This results in a current consumption of $I_{VCCSupply}$ and due to the level < 12.5 % at PFCVS-Pin the gate drives remains off. This combination generates an UVLO (resets the whole IC) followed by monitoring and a new Power-up. This flow goes on until the voltage at PFCVS-Pin becomes > 12.5 % again and the IC restarts with preheating.

This method for turning off the IC is only suitable when the IC is in Run-mode because in other modes the 75 % threshold for the Bus-voltage isn’t active. A turn-off signal in phases out of the Run-mode, leads to an operation of the IC without PFC-section and to a resulting lower BUS-voltage with a higher ripple until reaching the Run-mode. Then the ballast turns off when activating the 75 % threshold after PreRun-phase.

It is important that the time constant at the PFCVS-Pin (generated by the voltage divider and C_{11}) is small enough that the voltage reaches the 109 % threshold fast enough during Surge conditions. Otherwise the Surge condition can’t be clearly detected.

7.6 RES-Pin

This Pin is needed for filament detection and can be disabled when setting it to GND. When the voltage at this Pin rises higher than V_{RES3} the IC detects operation Filament, handled as “Fault F”. This protection function can also be used for switching the IC off and on with a micro controller. This realization only works in Run-mode and the minimal duration of turn-off should be 400 ms for correct function.

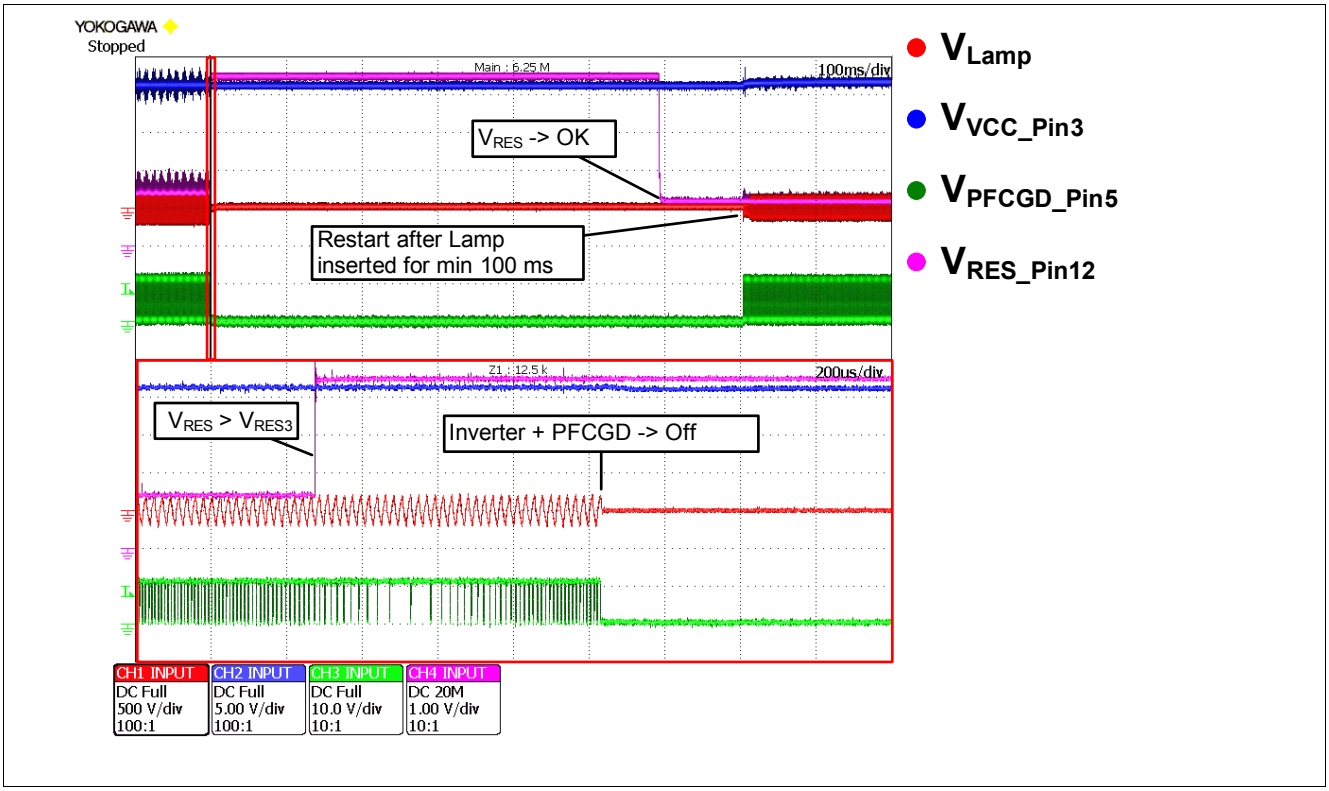


Figure 7-3 IC turn-off and on via RES-Pin

Figure 7-3 shows an example measurement for explaining the logic flow in case of turning off the ballast via RES-Pin. About 700 µs after reaching a level > V_{RES3} at the RES-Pin, the IC detects “Fault F” and the inverter and the PFC stops working. The “Fault Counter” increments by 1 and after a first delay of about 200 ms a decision in addiction to the “Fault Counter” has to be done. This is the reason for the minimal duration of the turn-off time in this solution. Is the “Fault Counter” > 2, for example after a second turn of within 40 s, the logic waits for a lamp removal (V_{RES} > V_{RES3}) of min. 100 ms until a restart can be happen. If the voltage at RES-Pin goes down to a level within the area for correct lamp detection the IC can’t start because the lamp wasn’t removed for longer than 100 ms. So an additional turn-off signal with a minimal turn-off time of 100 ms is necessary for restarting the Ballast. This can be avoided with the minimal turn-off-time of 400 ms mentioned before.

The IC starts with a delay of about 100 ms after reaching the filament detection level at the RES-Pin.

7.7 VCC-Pin

The ICB2FL03G is very robust against EMI and shows best function also under high EMI influence. A ceramic capacitor with a capacity of several 10 nF (10 nF or 47 nF) is recommend to cover the load-jumps for gate driver operation. The signals at this Pin are very suitable for evaluating and distinguishing the states in the State-diagram (see Datasheet Chapter 3.2 and 3.3).

When there are extremely high spikes at the VCC-Pin it might be necessary to modify the capacitance at this pin in order to EMI stability. EMI problems via VCC can be evaluated very easily. For evaluating this topic the signal at VCC-Pin and a signal of the half-bridge (for example HSGND) is necessary. When the half-bridge stops working and immediately after this the voltage at VCC-Pin breaks down to V_{VCCOff} followed by a restart after reaching the V_{VCCON} threshold an EMI-problem at the VCC-Pin can be the reason. All failures covered by the protection functions of the IC which leads to a restart have a minimal duration of t_{TIMER1} until a new restart can be achieved.

For correct Emergency function it is necessary that the IC-supply via the Startup resistors is connected to the Bus-voltage and is designed in that way that the Supply current in latched fault-mode is guaranteed (Please see also **Chapter 2** in this document for more informations)

7.8 LVS-Pin

The LVS-Pin is necessary for high-side-filament detection before startup and for EOL detection in Run-mode. This function can be disabled by connecting the LVS-Pin to GND. This connection should be as short as possible to prevent unintentional reactivation. A reactivation the deactivated LVS-Pin is possible when the voltage at the LVS-Pin reaches a level of $V_{LVSEnable1}$ for a typical duration of 1 µs (not specified in the Datasheet).

7.9 LSCS-Pin

For correct working of the adaptive deadtime the --50 mV threshold must be achieved in all working points (for min. $t_{LSCSCap3}$), otherwise the adaptive deadtime can't be detected properly and wobbling of the deadtime will be the consequence. Also the +50 mV threshold must be reached in normal operation to prevent detecting Cap Load 1 detection.

For some dimming applications it can happen that the +50 mV threshold for Cap Load 1 detection can't be reached at low dimming levels. Infineon Technologies AG provides a special IC (ICB2FL02G) with deactivated Cap load 1 detection, to cover all dimming solutions (Please contact Infineon Technologies AG for further information or visit http://www.infineon.com/smartlighting).

The maximum voltage level at this Pin should not be limited below 1.6 V because an half-bridge shoot through detection and correction is realized at LSCS-Pin.

7.10 Advice for Board Layout

For higher robustness while evaluating on the board, high ohmic resistors (for example 18 kΩ) from MOS-FET Gate to FET Source are suggestive to prevent destroying of the components if there is a broken Gate resistor or broken conductor path on the PCB.

Figure 7-4 shows a simplified circuit diagram with a bold lined power path. This figure helps to differentiate between the Signal- and Power-GND. The blue path is the Signal-GND where the resistors for sensing voltages or adjusting IC-parameters should be connected to. Wires where high current is flowing should be connected to the bold lined GND-potential. If possible connect all Signal-GND lines radiating to the IC GND and all Power-GND lines radiating to the Elko-GND.

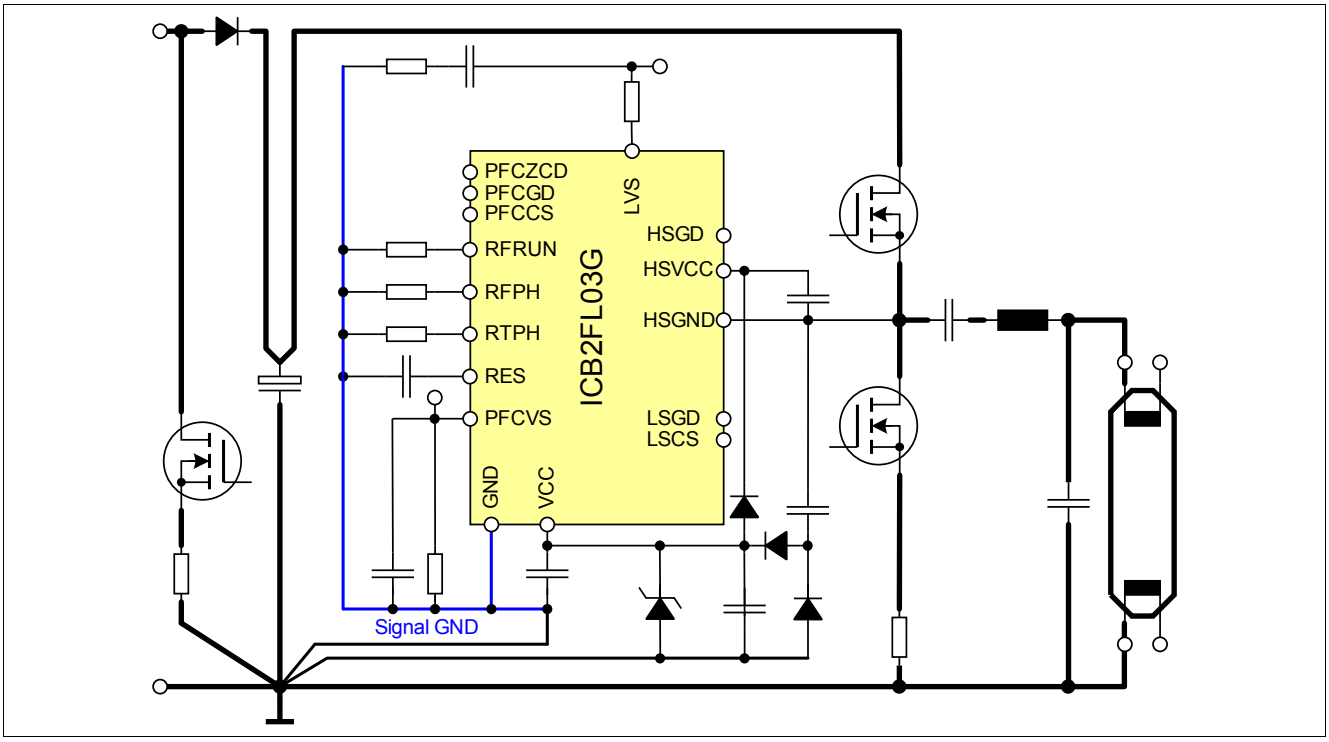


Figure 7-4 Simplified diagram - GND flow

The Demo board provides a good example of effective layout for this circuit.

8 Annex

8.1 Built in Customer Test Mode

The Built in Customer Test Mode is implemented to reduce time for ballast end test dramatically. More informations to this test can be found in the Datasheet in Chapter 2.8.3. There can be also found the requested signal levels and the timing diagram for activating the Test Mode. The following three figures show the benefit in testing time with the accelerated clock. The left oscillograms show the normal sequence without acceleration and the right oscillograms show the accelerated sequences. An additional acceleration can be realized by reducing the preheating time via R_{23} temporally for the ballast end test. An UVLO at VCC resets the Test Mode acceleration.

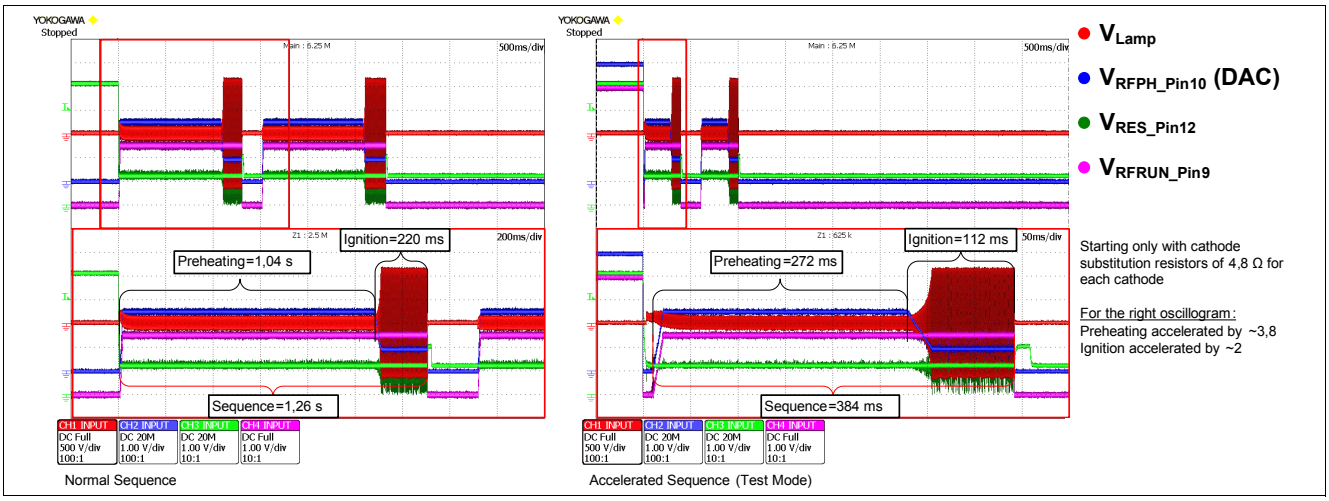


Figure 8-1 Built in Customer Test Mode - Acceleration Preheating & Ignition

Figure 8-1 shows the comparison in the Preheating- and Ignition-phase. An acceleration of about the factor 4 for the Preheating-phase and of about the factor 2 for the time till time-out-ignition can be seen in these oscillograms.

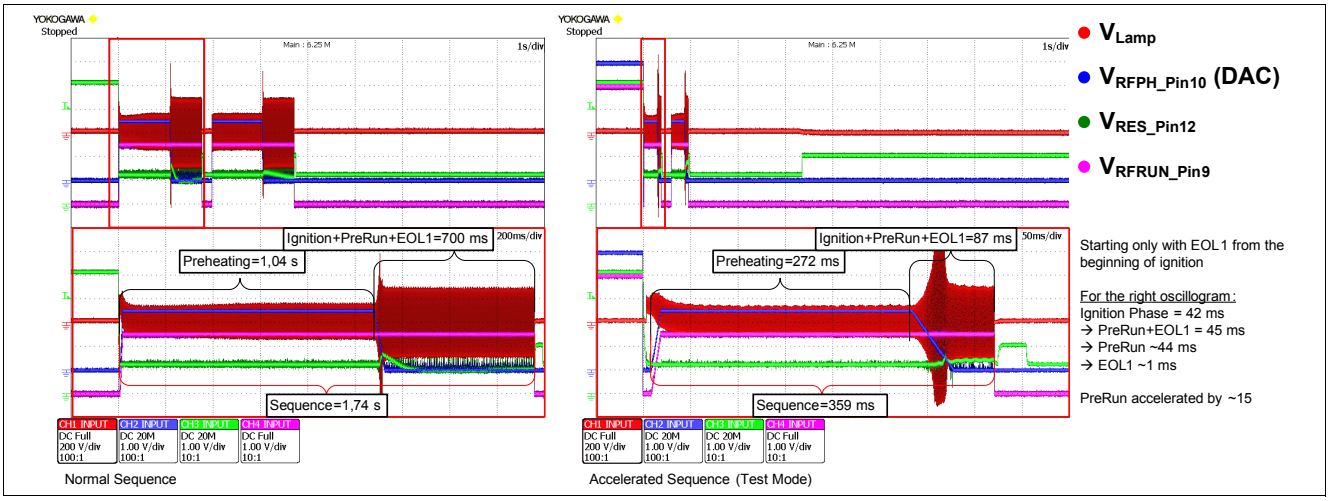


Figure 8-2 Built in Customer Test Mode - Acceleration PreRun

Figure 8-2 shows the acceleration of about the factor 15 for the PreRun-phase. The minimal duration of the Ignition-phase is 42 ms for this IC. This time must be subtracted from the time of Ignition+PreRun+EOL1 because it isn't affected by the acceleration. EOL1 has an duration of 620 µs and has also to be subtracted before calculating the acceleration of PreRun-phase.

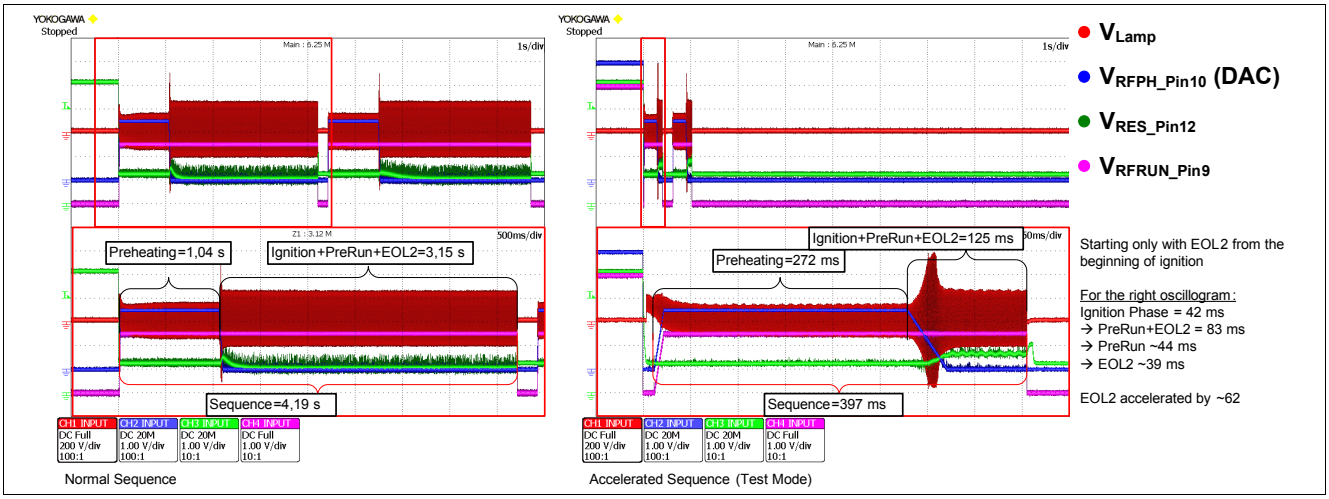


Figure 8-3 Built in Customer Test Mode - Acceleration EOL2

Figure 8-3 shows the acceleration of about 62 for the time till EOL2 detection. With the values of about 700 ms and 86 ms for Ignition- and PreRun-phase out the measurement in Figure 8-2 a normal time of 2450 ms for detecting EOL2 can be calculated. The accelerated time for EOL2 detection is about 39 ms.

8.2 Calculations

The following Chapter describes some necessary calculations for the Demo board design (according to the design used for this Application Note 1 x 54 W T5 with voltage mode preheating).

8.2.1 Example calculation - EOL for 54W T5 Design (Excel)

Figure 8-4 shows a picture of the “EOL calculation Excel-sheet” that supports the design of the EOL-network. Contact us http://www.infineon.com/smartlighting for achieving the tool.

A step by step guide for using this Excel-sheet is given in this chapter. Design relevant data can be entered in the green fields and the orange colored fields indicates that the value will be calculated via implemented formulas. Due to some neglects in the calculations an experimental adjustment in the circuit can be necessary.

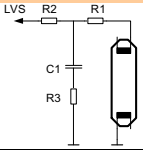
A description of the planned design data can be entered in first green field in the top of the page. After this the nominal values for lamp-voltage and lamp-current can be entered in the parameter section. Also necessary are the inputs for operation frequency, max. allowed EOL-power and the factor for allowed lamp-voltage. After entering these values, the peak-peak lamp-voltage for EOL1- and the DC-offset of the lamp-voltage for EOL2 can be calculated with the currents out of the Datasheet for the EOL1- and EOL2-detection thresholds.

The calculation for the EOL2 resistors R_1 and R_2 can be done under negligence the influence of C_1 and R_3 because C_1 blocks the DC-current in a steady state (Run-mode). The ratio between R_2 and R_1 has an influence to the necessary voltage strength of C_1. For major designs a resistance of about 50 kΩ to 70 kΩ for R_2 is suitable, so a selection of R_1 regarding this resistance is helpful. It can be also helpful to separate the resistance for R_1 into several resistors (in this example 3 x 68 kΩ). This segmenting reduces the voltage drop for each separated resistor of R_1. The selected values for R_1 and R_2 can be entered in the two green fields.

The first field in the EOL1 calculation area calculates the actual max. lamp-voltage for EOL1-detection without C_1 and R_3. This value must be lower than the voltage calculated in the parameter section in the first steps. If this condition is true, R_3 and C_1 are necessary for reducing the amplitude of the AC-current into the LVS-Pin (indication in the result field). The following calculations are necessary for dimensioning these two components, the influence of C_1 for R_3 calculation will be neglected. The voltage across R_2 is calculated with the nominal EOL1-detection current ($I_{LVSSourceAC}$) multiplied with the calculated value of R_2. The voltage across R_1 is the difference between the max. allowed peak-peak lamp-voltage (U_{Lamp_pp}) and the voltage across R_2 (U_{R2pp}). This voltage drop results in a current through R_1 (I_{R1pp}) that is higher than the threshold for EOL1-detection of $I_{LVSSourceSC}$. This current difference

(I_{R3pp}) must be fed via C_1 and R_3 to GND. The field "R_3 calculated" shows the calculated value for the needed resistance. If the selected value for R_3 is higher, the EOL1-detection reacts earlier and if the selected value for R_3 is smaller, the EOL1-detection triggers at a higher lamp-voltage than defined in the parameter section. To reduce the influence of C_1 to the EOL1 threshold the capacitance should be as high as possible and in no case smaller than the calculated value C_{1_min}. After entering the selected value for C_1 in the green field, the values for the resistors and the capacitor in the EOL detection network for this design will be summarized in the top of the page.

EOL: Demoboard 1x54W T5 - VM - 180VAC to 270VAC - ICB2FL03G



This sheet supports designing the EOL circuit with the FL-Controller ICB2FL03G.
Please fill out the green fields top down. The result is listed in the next line.
The design is: R1=204kΩ, R2=68kΩ, R3=6,8kΩ and C1=100nF.
Please note, that it can be necessary to split R1 because of the limited power dissipation.
In this Design the calculated EOL2 Power is about 5,3W+/5,3W- and the calculated EOL1 threshold is about 486Vpp.

Parameter	short	comment	calculation	unit	Values
Lamp voltage (Lamp data)	U_{Lamp}[RMS]			V_{RMS}	118,00
Lamp current (Lamp data)	I_{Lamp}[RMS]			mA_{RMS}	460,00
Operation frequency	f_{RUN}			kHz	45,00
max. allowed EOL Power (DC)	P_{EOLDC_max}			W	5,00
Factor for allowed Lamp Voltage	U_{Lamp_Fact}				1,50
EOL1 threshold (Overvolage)	$I_{LVSSourceAC}$	>620µs (Datasheet)		$µA_{pp}$	210,00
EOL2 threshold (Rectifier)	I_{LVSDC}	>2500ms (Datasheet)		$±µA_{RMS}$	42,00
Lamp voltage (peak-peak)	U_{Lamp_pp}		$U_{Lamp\_pp} = U_{Lamp} \cdot 2 \cdot \sqrt{2} \cdot U_{Lamp\_Fact}$	V_{PP}	500,63
Lamp voltage (DC offset)	U_{Lamp_DC}		$U_{Lamp\_DC} = \frac{P_{EOLDC\_max}}{I_{Lamp}}$	V_{DC}	10,87
EOL2 calculation (Rectifier Effect)					
DC voltage across R_1 and R_2				V_{DC}	10,87
R_1 and R_2 calculated	R_{1calc}+R_{2calc}		$R_{1calc} + R_{2calc} = \frac{U_{Lamp\_DC}}{I_{LVSDC}}$	kΩ	258,80
R_1 selected	R_1	Select R_1 in respect to the voltage strength of C_1. R_1 >> R_2		kΩ	204,00
R2 calculated	R_{2calc}		$R_2 = R_{1calc} + R_{2calc} - R_1$	kΩ	54,80
R_2 selected	R_2			kΩ	68,00
R_1 and R_2 real	R_1+R_2		$R_1 + R_2$	kΩ	272,00
EOL Power (DC) calculated	P_{EOLDC+_calc}		$P_{EOLDC\_max} = (R_1 + R_2) \cdot I_{LVSDC} \cdot I_{Lamp}$	W	5,26
EOL Power (DC) calculated	P_{EOLDC-_calc}		$P_{EOLDC\_max} = (R_1 + R_2) \cdot I_{LVSDC} \cdot I_{Lamp}$	W	5,26
EOL1 calculation (Lamp Overvoltage)					
Actual max voltage	$U_{Lamp\_pp\_EOL1}$		$U_{Lamp\_pp\_EOL2} = I_{LVSSourceAC} \cdot (R_1 + R_2)$	V_{pp}	57,12
Result		ULamp_pp_EOL1 too small, R3 and C1 requiered!			
Voltage across R_2	U_{R2pp}		$U_{R2pp} = I_{LVSSourceAC} \cdot R_2$	V_{pp}	14,28
Voltage across R_1	U_{R1pp}		$U_{R1pp} = U_{Lamp\_pp} - U_{R2pp}$	V_{pp}	486,35
Current through R_1	I_{R1pp}		$I_{R1pp} = \frac{U_{R1pp}}{R_1}$	$µA_{pp}$	2384,08
Current through R_3	I_{R3pp}	C_1 neglected	$I_{R3pp} = I_{R1pp} - I_{LVSSourceAC}$	$µA_{pp}$	2174,08
R_3 calculatet	R_{3calc}		$R_{3calc} = \frac{U_{R2pp}}{I_{R3pp}}$	kΩ	6,57
R_3 selected	R_3			kΩ	6,80
C_1 calculated Select C1 as high as possible in respect of the high side preheating Capacitor!	C_{1_min}	C_1 should affect the current less than 1%	$> \frac{100}{2 \cdot \pi \cdot f_{RUN} \cdot R_3}$	nF	52,01
C_1 selected	C_1	select C_1 as high as possible under consideration of the results of Startup calculation sheet (C40)		nF	100,00
EOL1 max voltage calculated	$U_{Lamp\_pp\_EOL1\_calc.}$		$U_{Lamp\_pp\_EOL2} = \frac{I_{LVSSourceAC} \cdot (R_2 \cdot R_1 + R_3 \cdot R_1 + R_2 \cdot R_3)}{R_3}$	V_{pp}	486

Figure 8-4 Excel based EOL calculation tool

Contact us http://www.infineon.com/smartlighting for achieving the tool.

8.2.2 Example calculation - Startup-network for 54W T5 Design (Excel)

Figure 8-5 shows the calculation example for the Startup-network to the LVS-Pin.

Startup-LVS: Demoboard 1x54W T5 - VM - 180VAC to 270VAC - ICB2FL03G

This sheet supports designing the LVS-startup-circuit with the FL-Controller ICB2FL03G.
Please fill out the green fields top down. The result is listed in the next line.
The design is: R1=470kΩ, R2=470kΩ, DR12=110kΩ, R34=150kΩ, R35=150kΩ and C40=220nF.

Parameter	short	comment	calculation	unit	Values
Minimal Input voltge	V_{IN_min}	DC-voltage or peak-voltage for AC-supply		V_{peak}	176,0
BUS-voltage	V_{BUS}			V_{DC}	410,0
Current for filament detection	$I_{LVSSink}$	max. value from Datasheet		µA	18,0
Internal voltage source LVS	V_{LVS_Int}	typical value, not tested in End-Test		V_{DC}	5,0
R_{41}	R_{41}	R_2 (from EOL-calculation)		kΩ	68,0
R_{42}	R_{42}	R_1 (from EOL-calculation)		kΩ	68,0
R_{43}	R_{43}			kΩ	68,0
R_{44}	R_{44}			kΩ	68,0
R_{45}	R_{45}	R_3 (from EOL-calculation)		kΩ	6,8
with HS-filament inserted, filament must be detected in the whole input voltage range - C40 and R45 neglected					
Resistor EOL-DC-Path@Startup	R_{EOL_DC}		$R_{EOL\_DC} = R_{41} + R_{42} + R_{43} + R_{44}$	kΩ	272,0
Voltage across R_{EOL_DC}	V_{REOL_DC}	for lamp detection	$V_{REOL\_DC} = I_{LVSSink} \cdot R_{EOL\_DC}$	V	4,9
Voltage Ratio	$n_{voltage}$		$n_{voltage} = \frac{V_{BUS}}{V_{IN\_min}}$		2,3
actual V_{DR12} without R_{34}+R_{35}	V_{DR12_1}		$V_{DR12\_1} = V_{LVS\_Int} + V_{REOL\_DC}$	V	9,9
def. V_{DR12} at min. input voltage	$V_{DR12\_min\_def}$	should be about 6V higher than V_{DR12_1}		V	16,0
R_{34} and R_{35} calculated	R_{34_cal}+R_{35_cal}	$R_{34\_cal} + R_{35\_cal} = \frac{V_{DR12\_min\_def} - V_{DR12\_1}}{I_{LVSSink}}$		kΩ	339,1
R_{34} selected	R_{34}			kΩ	150,0
R_{35} selected	R_{35}			kΩ	150,0
R_{34} and R_{35} selected	R_{34}+R_{35}	must be smaller than calculated value		kΩ	300,0
worst case, R_{41} to GND instead of LVS-Pin (for calculation of voltage divider R_1, R_2 and DR_{12} for V_{DR12_min})					
R from DR_{12}-to-LVS-DC@Startup	$R_{Startup\_DC}$		$R_{Startup\_DC} = R_{34} + R_{35} + R_{EOL\_DC}$	kΩ	572,0
Necessary voltage at DR_{12}	V_{DR12_min}	$V_{DR12\_min} = V_{LVS\_Int} + I_{LVSSink} \cdot R_{Startup\_DC}$		V	15,3
Ratio of R_{1+2} to DR_{12}	$n_{R1+2\_to\_DR12}$		$n_{R1+2\_to\_DR12} = \frac{V_{IN\_min}}{V_{DR12\_min}}$		11,5
DR_{12} selected	DR_{12}	take care to R_1 and R_2		kΩ	110,0
parallel circuit DR_{12}, $R_{Startup\_DC}$	$DR_{12+Startup\_DC}$		$DR_{12+Startup\_DC} = \frac{DR_{12} \cdot R_{Startup\_DC}}{DR_{12} + R_{Startup\_DC}}$	kΩ	92,3
Resistor R_1+R_2	R_{1_cal}+R_{2_cal}	$R_{1\_cal} + R_{2\_cal} = R_{3+Startup\_DC} \cdot (n_{R1+2\_to\_DR12} - 1)$		kΩ	969,3
R_1 selected	R_1			kΩ	470,0
R_2 selected	R_2			kΩ	470,0
R_1 and R_2 selected	R_1+R_2	must be smaller than calculated value		kΩ	940,0
UDR12 at minimum input votlage	$V_{DR12\_min\_input}$	$V_{DR12\_min\_input} = \frac{V_{IN\_min} \cdot DR_{12+Startup\_DC}}{R_1 + R_2 + DR_{12+Startup\_DC}}$		V	15,7
UDR12 at maximum input voltage	$V_{DR12\_max\_input}$	$V_{DR12\_max\_input} = \frac{V_{BUS} \cdot DR_{12+Startup\_DC}}{R_1 + R_2 + DR_{12+Startup\_DC}}$		V	36,6
without filament, prevent IC startup worst case, R_{41} open (not connected to LVS-Pin); At maximum input voltage, VC40-to-GND must be < VLVS_Int					
C21 defined	C_{21}			nF	22,0
VDR12_max_input votlage	V_{DR12_temp}			V	43,0
min. value for C_{40}	C_{40_cal}		$C_{40\_cal} = \frac{V_{DR12\_temp} \cdot C_{21}}{V_{LVS\_Int}}$	nF	189,0
selected value for C40	C_{40}	selected value must be higher than calculated value		nF	220,0

Figure 8-5 Excel based Startup-network calculation tool

Contact us http://www.infineon.com/smartlighting for achieving the tool.

8.2.3 Inductor L_1 of the boost converter

The inductivity of the boost inductor typically is designed to operate within a specified voltage range above a minimum frequency in order to get an easier RFI suppression. It is well known, that in critical conduction mode

(CritCM) there is a minimum operating frequency at low input voltages and another minimum at maximum input voltage. In state-of-the-art CritCM PFC controllers the lowest value out of these two criteria is used.

At minimum AC-input voltage (8.1)

$$L_A = \frac{(V_{INACmin} \cdot \sqrt{2})^2 \cdot (V_{BUS} - (V_{INACmin} \cdot \sqrt{2})) \cdot \eta}{4 \cdot f_{min} \cdot P_{OUTPFC} \cdot V_{BUS}}$$

$$L_A = \frac{(180\,V \cdot \sqrt{2})^2 \cdot (410\,V - (180\,V \cdot \sqrt{2})) \cdot 0.95}{4 \cdot 25\,kHz \cdot 60\,W \cdot 410\,V} = 3.89\,mH$$

At maximum AC-input voltage (8.2)

$$L_B = \frac{(V_{INACmax} \cdot \sqrt{2})^2 \cdot (V_{BUS} - (V_{INACmax} \cdot \sqrt{2})) \cdot \eta}{4 \cdot f_{min} \cdot P_{OUTPFC} \cdot V_{BUS}}$$

$$L_B = \frac{(270\,V \cdot \sqrt{2})^2 \cdot (410\,V - (270\,V \cdot \sqrt{2})) \cdot 0.95}{4 \cdot 25\,kHz \cdot 60\,W \cdot 410\,V} = 1.58\,mH$$

With the new control principle for the PFC-preconverter a third criteria that covers the maximum on-time t_{PFCON_max} is necessary.

At maximum on-time (8.3)

$$L_C = \frac{(V_{INACmin} \cdot \sqrt{2})^2 \cdot T_{ONmax} \cdot \eta}{4 \cdot P_{OUTPFC}}$$

$$L_C = \frac{(180\,V \cdot \sqrt{2})^2 \cdot 24.0\,\mu s \cdot \eta}{4 \cdot 60\,W} = 6.16\,mH$$

With the assumed conditions the lowest value out of L_A, L_B, L_C is 1.58 mH

The selected value is: L_1 = 1.58 mH

8.2.4 Shunt resistors for ignition voltage R_{24}, R_{25}

The selected lamp type 54W T5 requires an ignition voltage of V_{IGN} = > 620 V_{RMS}. The Board is designed for an ignition voltage of V_{IGN} = 800 V_{RMS} (1130 V_{peak}). In this application example the resonant inductor is evaluated to L_2 = 1.46 mH and the resonant capacitor to C_{20} = 4.7nF. With this inputs the ignition frequency f_{IGN} can be calculated in a first step:

Calculation of Ignition frequency f_{IGN} (8.4)

$$f_{IGN} = \sqrt{\frac{1 \pm \frac{V_{BUS} \cdot 2}{\pi \cdot V_{IGN}}}{4 \cdot \pi^2 \cdot L_2 \cdot C_{20}}} = \sqrt{\frac{1 \pm \frac{410\,V \cdot 2}{\pi \cdot 1130\,Vpeak}}{4 \cdot \pi^2 \cdot 1.46\,mH \cdot 4.7\,nF}} = 67410\,Hz$$

The second solution of this equation (with the minus sign) leads to a result of 50163 Hz, which is on the capacitive side of the resonant rise. This value is no solution, because the operating frequency approaches from the higher frequency level.

In the next step, the current through the resonant capacitor C_{20} must be calculated when reaching a voltage level of 800 V_{peak}.

Calculation of resonant capacitor current I_{C20} (8.5)

$$I_{C20} = V_{IGN} \cdot 2 \cdot \pi \cdot f_{IGN} \cdot C_{20} = 1130\,V_{peak} \cdot 2 \cdot \pi \cdot 67410\,Hz \cdot 4.7\,\text{nF} = 2.25\,\text{A}$$

Finally the resistors R_{24} and R_{25} can be calculated with I_{C20} and the ignition regulating value at LSCS-Pin of about 0.8 V.

Calculation of R_{24} and R_{25} (8.6)

$$\frac{R_{24} \cdot R_{25}}{R_{24} + R_{25}} = \frac{0.8\,\text{V}}{I_{C20}} = \frac{0.8\,\text{V}}{2.25\,\text{A}} = 0.356\,\Omega$$

The selected values are: $R_{24} = R_{25} = 0.68\Omega$ (= 0.34 Ω)

8.2.5 Ballast parameter

The following formulas give advice for calculating relevant ballast parameters.

Calculation of Startup-resistors R_{11} and R_{12} (8.7)

$$R_{11} + R_{12} = \frac{V_{BUS\ min\ Input}}{I_{VCCLatch} - I_{RES1\ min}} = \frac{254\,\text{V}}{170\,\mu\text{A} + 54.3\,\mu\text{A}} = 1132\,\text{k}\Omega$$

The selected values are: $R_{11} = R_{12} = 470$ kΩ

Calculation of PFCVS-resistor R_{20} (8.8)

$$R_{20} \leqslant \frac{V_{PFCVSREF}}{100 \cdot I_{PFCBIAS}} = \frac{2.5\,\text{V}}{100 \cdot 1.0\,\mu\text{A}} = 25\,\text{k}\Omega$$

The selected value is: $R_{20} = 10$ kΩ

Calculation of PFCVS-resistors R_{14} and R_{15} (8.9)

$$R_{14} + R_{15} = \frac{V_{BUS} - V_{PFCVSREF}}{V_{PFCVSREF}} \cdot R_{20} = \frac{410\,V - 2.5\,V}{2.5\,V} \cdot 10\,\text{k}\Omega = 1630\,\text{k}\Omega$$

The selected values are: $R_{14} = R_{15} = 820$ kΩ

Calculation of low pass capacitor C_{11} (Corner frequency f_{C1} = 10 kHz) (8.10)

$$C_{11} = \frac{1 \cdot (R_{20} + R_{14} + R_{15})}{2 \cdot \pi \cdot f_{C1} \cdot R_{20} \cdot (R_{14} + R_{15})} = \frac{10\,\text{k}\Omega + 820\,\text{k}\Omega + 820\,\text{k}\Omega}{2 \cdot \pi \cdot 10\,\text{kHz} \cdot 10\,\text{k}\Omega \cdot (820\,\text{k}\Omega + 820\,\text{k}\Omega)} = 1.6\,\text{nF}$$

The selected value is: $C_{11} = 2.2$ nF

Calculation of PFC-shunt-resistors R_{18} and R_{19} (8.11)

$$\frac{R_{18} \cdot R_{19}}{R_{18} + R_{19}} = \frac{V_{PFCCSOFF} \cdot \eta \cdot V_{INACMIN} \cdot \sqrt{2}}{4 \cdot P_{OUTPFC}} = \frac{1\,\text{V} \cdot 0.95 \cdot 180\,\text{V} \cdot \sqrt{2}}{4 \cdot 60\,\text{W}} = 1.0\,\Omega$$

The selected values are: R_{18} = 1 Ω and R_{19} = not assembled

Calculation of Run-frequency-resistor R_{21} for f_{RUN} = 45kHz (8.12)

$$R_{21} = R_{FRUN} = \frac{5 \cdot 10^8 \,\Omega \cdot Hz}{f_{RUN}} = \frac{5 \cdot 10^8 \,\Omega \cdot Hz}{45\,kHz} = 11.1\,k\Omega$$

The selected value is: R_{21} = 11 kΩ

Calculation of Preheating-frequency-resistor R_{22} for f_{PH} = 105 kHz (8.13)

$$R_{22} = R_{FPH} = \frac{R_{FRUN}}{\frac{f_{PH} \cdot R_{FRUN}}{5 \cdot 10^8 \cdot \Omega \cdot Hz}} = \frac{11\,k\Omega}{\frac{105\,kHz \cdot 11\,k\Omega}{5 \cdot 10^8 \cdot \Omega \cdot Hz}} = 8.4\,k\Omega$$

The selected value is: R_{22} = 8.2 kΩ

Calculation of Preheating-time-resistor R_{23} for t_{PH} = 1000ms (8.14)

$$R_{23} = R_{TPH} = \frac{t_{PH} \cdot k\Omega}{100\,ms} = \frac{1000\,ms \cdot k\Omega}{100\,ms} = 10\,k\Omega$$

The selected value is: R_{23} = 10 kΩ

The gate-drive-resistors R_{16}, R_{26} and R_{27} are recommended to be equal or higher than 10 Ω (Selected 10 Ω)

Calculation of bootstrap current limitation resistor R_{30} (8.15)

$$R_{30} \geq \frac{2 \cdot V_{VCCON}}{V_{LSCSOVC1}} \cdot \frac{R_{24} \cdot R_{25}}{R_{24} + R_{25}} = \frac{2 \cdot 14.0\,V}{1.6\,V} \cdot \frac{0.68\,\Omega \cdot 0.68\,\Omega}{0.68\,\Omega + 0.68\,\Omega} = 6\,\Omega$$

The factor of 2 is used in order to keep away from limit value.

The selected value is: R_{30} = 33 Ω

Calculation of LS-filament sense resistor R_{36} (8.16)

$$R_{36} < \frac{V_{RES1MIN}}{I_{RES3MIN}} = \frac{1.55\,V}{26.6\,\mu A} = 58.3\,k\Omega$$

$$R_{36} > \frac{V_{RES1MAX}}{I_{RES1MAX}} = \frac{1.65\,V}{32.0\,\mu A} = 51.6\,k\Omega$$

The selected value is: R_{36} = 56 kΩ

Calculation of low pass capacitor C_{19} (8.17)

$$C_{19} = \frac{\sqrt{F_{LP}^2 - 1}}{2 \cdot \pi \cdot f_{RUN} \cdot R_{36}} = \frac{\sqrt{300^2 - 1}}{2 \cdot \pi \cdot 45\,kHz \cdot 56\,k\Omega} = 18.9\,nF$$

The capacitor C_{19} provides a low pass filter together with resistor R_{36} in order to suppress AC voltage drop at the LS-filament. With an estimation of an AC-voltage of about 10 $V_{peak\text{-}to\text{-}peak}$ at LS-filament during Run-mode at f_{RUN} = 45kHz, a suppression by a factor of at least F_{LP} = 300 is necessary.

The selected value is: C_{19} = 22 nF

Please Note: The voltage at RES-Pin must reach the filament detection level until VCC reaches the V_{VCCOn} threshold (see **Chapter 8.3.7**).

8.3 Troubleshooting

This chapter gives some advice for finding typical Startup Problems in designs with the ICB2FL03G. Please check the function in the sequence described in **Chapter 1-4**. When these checks don't solve the problem please have a look at **Chapter 8.3.1**to **Chapter 8.3.10**. When these checks don't solve the Problem, please contact Infineon Technologies AG for furthermore support.

Dependent on the voltage at RES-Pin, the current consumption of the IC can be higher due to I_{RES1} to I_{RES4}.

8.3.1 VCC doesn't reach 10.5 V (V_{VCCOff}) or 14 V (V_{VCCOn})

When VCC doesn't reach the V_{VCCOff} threshold also called UVLO threshold the current consumption of the IC is too high or the current through the VCC Startup-resistors is too low. The minimal needed current, feed via the Start-up resistors is I_{VCCqu1} until reaching V_{VCCOff} and I_{VCCqu2} until reaching V_{VCCOn}. When there is another power consuming device at VCC this can be the reason for preventing VCC rising to V_{VCCOff}.

- Remove any other consumer at VCC.
- Check the Bus-voltage and calculate the minimal current via the Start-up resistors.
- Check if there is a wrong Z-Diode D_9 mounted that limits the voltage at VCC.

8.3.2 VCC hiccup between 14 V (V_{VCCOff}) and 10.5 V (V_{VCCOn})

When VCC reaches the V_{VCCOn} threshold and then goes down to V_{VCCOff} and so on (called hiccup operation) there are the following reasons possible. There can be a problem in detection of the Bus-voltage or in the VCC-supply via the charge pump.

- Is the Bus-voltage in the specified range of 12.5 % and 105 % (~0.39 V and 2.57 V at PFCVS-Pin)?
- Is the voltage divider for Bus-voltage sensing broken?
- Works the LSGD and HSGD during the VCC breakdown? Otherwise check the next two subcategories.
- Are the Diodes of the charge pump correct mounted (D_7 and D_8)?
- Check the Ration of C_{12} and C_{14}
- Is the charge pump design strong enough? Note: Layout and components have to handle the peak currents.

Calculation of charge pump (8.18)

$$I_{CHARGE} = (V_{BUS} - V_{VCC}) \cdot f \cdot C_{16}$$

8.3.3 No LSGD-Pulse

When all Start-up conditions are ok, the first pulse out of the IC is normally visible on LSGD-Pin. When the VCC is above the V_{VCCOn} threshold and the Bus-voltage is in the specified range between 12.5 % and 105 %, a filament detection problem can cause this behavior.

- The Bus-voltage must be smaller than min. value of $V_{PFCVSLow}$ (105 %) before Startup
- Set both LVS-Pins temporally to GND to disable the high-side-filament detection.
- Set the RES-Pin temporally to GND to disable the High- and low-side-filament detection.

When this solves the Problem, for correct function with filament detection a redesigning of the LVS-Path and the resistor R_{36} is necessary (see **Chapter 8.2**).

8.3.4 No HSGD-Pulse

When there is no HSGD-pulse after some first LSGD-Pulses a problem with the HSVCC-supply can be the reason.

- The Bus-voltage must be smaller than min. value of $V_{PFCVSLow}$ (105 %) before Startup
- Check if VCC breaks down to V_{VCCOff} while charging the HSVCC-capacitor C_{14} - a higher capacitance at VCC-Pin might be helpful.
- Check if the HSVCC reaches a level of min. $V_{HSVCCOn}$ (max. value), has C_{14} the right value?

- Check if R_{30} and D_6 are mounted in the right way
- Check if the $V_{LSCSOvC1}$ threshold is reached; Increasing of R_{30} might be helpful

8.3.5 No PFCGD-Pulse

When there is no PFCGD-pulse after 300µs of correct inverter working there can only be a problem in the monitoring of the Bus-voltage or the connecting tracks to MOSFET.

- The Bus-voltage must be smaller than min. value of $V_{PFCVSLow}$ (105 %) before Startup
- The Bus-voltage must be smaller than min. value of $V_{PFCVSRUp}$ (109 %) during Run-mode

There is a Bus-overvoltage hysteresis implemented. When the 109 % threshold is reached in Run-mode the PFCGD turns off immediately and the Bus-voltage must undershoot the 105 % threshold for reactivating the PFCGD.

8.3.6 The IC starts without present high-side-filament

When the IC starts without present high-side-filament a Startup current flows into the LVS-Pin. When there flows a current of min. value of $I_{LVSSINK}$ into the LVS-Pin the IC interprets this as a present high-side-filament. Due to not so good design this current can flow via other components when there is no filament present. When the capacitor in the preheating circuit C_{21} has a high capacitance and C_{40} is relatively low, a transient current flows via C_{21} and L_{21} that is high enough to lead to a high-side-filament detection.

- Measure the peak-voltage between C_{40} and R_{41} referred to GND before VCC reaches V_{VCCOn}, subtract 5 V* and calculate the current flowing into the LVS-Pin with the value of R_{41}. (Further information in **Chapter 5.1**)
- Try a capacitor with a higher capacitance for C_{40}, this reduces the voltage across R_{41} and leads to a lower transient current into the LVS-Pin.

Another reason can be that the VCC-rising is too fast, and the voltage at RES-Pin can't reach the filament detection level until VCC reaches the V_{VCCOn} threshold. Also check the EOL calculation in **Chapter 8.2.1**.

*In the Datasheet there is the voltage $V_{LVSClamp}$ = 6.5 V at I_{LVS} =300 µA specified. For the calculation of the startup current an internal comparator threshold of 5 V (see also **Chapter 5.1**) can be used.

8.3.7 The IC starts without present low-side-filament

When the IC starts without present low-side-filament a component at this pin leads to a limited voltage at this Pin.

- Is the capacitance of C_{19} too high?
- The voltage at RES-Pin must be higher than V_{RES1} before VCC reaches the V_{VCCOn} threshold

Another reason can be that the VCC-rising is too fast and the voltage at RES-Pin can't reach the filament detection level until VCC reaches the V_{VCCOn} threshold (see also **Chapter 8.2**).

8.3.8 The IC stops within t_{PRERUN} after ignition

The Protection Function Matrix in Chapter 4 of the Datasheet shows in which operating mode a special fault detection becomes active. When the IC stops within t_{PRERUN} after ignition, some basic parameters of the circuit aren't in the specified area because in PreRun-mode only a few fault detection functions are active. The following list gives an overview which conditions must be fulfilled for correct IC working.

- Voltage at VCC must be > V_{VCCOff}
- Bus-Voltage must be > 12.5 %
- Voltage at PFCCS-Pin must be < $V_{PFCCSOff}$
- Voltage at RES-Pin must be < V_{RES1}
- Voltage at LSCS-Pin must be < $V_{LSCSOvC1}$

8.3.9 The IC stops about t_{PRERUN} after ignition

When the IC stops about 625 ms after ignition a failure with a short duration of effect (several µs) can be the reason. The following list gives an overview which conditions must be fulfilled for correct IC working.

- Voltage at RES-Pin < V_{RES3}
- Bus-voltage > 75 %
- EOL1 (Overvoltage); Set LVS-Pin temporally to GND to verify if this is the problem
- Cap Load 2; Check Waveform at LSCS-Pin and compare with Chapter 2.6.2 in the Datasheet
- Voltage at LSCS-Pin < $V_{LSCSOvC2}$

8.3.10 The IC stops about 3s after ignition

When the IC stops about 3 s after ignition a failure with a long duration of effect (2500 ms) can be the reason. The following list gives an overview which conditions must be fulfilled for correct IC working.

- EOL2 (Rectifier Effect); Set LVS-Pin temporally to GND to verify if this is the problem
- Cap Load 1; Check the waveform at LSCS-Pin and compare with Chapter 2.6.1 in the Datasheet

8.4 BOM - Schematic - Layout

In this chapter the documentation of the Demo board can be found.

BOM: Demoboard 1x54W T5 - VM - 180VAC to 270VAC - ICB2FL03G

						ICB2FL03G	
	Input voltage = 180VAC to 270VAC					VBUS = 410 VRMS	
				Package			Package
F1	Fuse 1A fast	Wickmann	Typ 370		R1	470kΩ	.1206
					R2	470kΩ	.1206
K1/1	AC Input	WAGO 250-203			R11	470kΩ	.1206
K1/2	AC Input				R12	470kΩ	.1206
K1/3	PE				R13	33kΩ	.1206
K2/1	not connected	WAGO 250-203			R14	820kΩ	.1206
K2/2	High Side Filament				R15	820kΩ	.1206
K2/3	High Side Filament				R16	10Ω	.0805
K3/1	Low Side Filament	WAGO 250-203			R18	1Ω	.1206
K3/2	Low Side Filament				R19	not assembled	.1206
K3/3	not connected				R20	10kΩ	.0805
IC1	ICB2FL03G	Infineon		SO-16	R21	11kΩ	.0805
Q1	IPD60R1k4C6	Infineon		D-Pack	R22	8.2kΩ	.0805
Q2	IPD60R1k4C6	Infineon		D-Pack	R23	10kΩ	.0805
Q3	IPD60R1k4C6	Infineon		D-Pack	R24	0.68Ω	.1206
D1…4	S1M	Fairchild	(1000V/1A/2µs)	DO-214AC	R25	0.68Ω	.1206
D5	MURS160T3	ON Semi	(600V/1A/75ns)	SMB	R26	10Ω	.0805
D6	BYG20J	Philips	(600V/1,5A/75ns)	SOD124	R27	10Ω	.0805
D7	BYG22D	Philips	(200V/1A/25ns)	DO214	R30	33Ω	.1206
D8	BYG22D	Philips	(200V/1A/25ns)	DO214	R34	150kΩ	.1206
D9	BZV55-C16	NXP		SOD-80C	R35	150kΩ	.1206
DR12	110kΩ			.1206	R36	56kΩ	.1206
D82	0Ω			.2512	R41	68kΩ	.0805
					R42	68kΩ	.1206
L101	2x68mH/0.6A	Epcos	B82732F2601B001		R43	68kΩ	.1206
L1 PFC	1.58mH	Epcos	B78326P7373A005	EFD25/13/9	R44	68kΩ	.1206
L 2	1.46mH	Epcos	B78326P7374A005	EFD25/13/9	R45	6,8kΩ	.1206
L 21	100µH/760mA	Epcos	B82144B1104J000	RM5	R61	0Ω	.0805
L 22	100µH/760mA	Epcos	B82144B1104J000	RM5			
C1	220nF/X2/305V	Epcos	B32922C3224M000	RM15			
C2	33nF/630V/MKT	Epcos	B32521N8333K000	RM10			
C3	3,3nF/Y2/300V	Epcos	B32021A3332K000	RM10			
C4	220nF/X2/305V	Epcos	B32922C3224M000	RM15			
C10	10µF/450V	Epcos	B43888C5106M000	single ended			
C11	2,2nF/50V	X7R		.0805			
C12	100nF/50V	X7R		.0805			
C13	1µF/25V	X7R		.1206			
C14	68nF/50V	X7R		.0805			
C15	22nF/630V/MKT	Epcos	B32621A6223K000	RM10			
C16	1nF/630V/MKT	Epcos	B32529C8102K000	RM5			
C17	100nF/630V/MKP	Epcos	B32612A6104K008	RM15			
C19	22nF/50V	X7R		.0805			
C20	4,7nF/1600V/MKP	Epcos	B32612-J1472J008	RM15			
C21	22nF/400V/MKP	Epcos	B32620A4223J000	RM7,5			
C22	22nF/400V/MKP	Epcos	B32620A4223J000	RM7,5			
C23	10nF/50V	X7R		.0805			
C40	220nF/50V	X7R		.0805			

More information:
http://www.infineon.com/smartlighting

http://www.infineon.com/CoolMOS

http://www.epcos.com Email: wolfgang.dreipelcher@epcos.com

Figure 8-6 Bill of Material for Demo Board 1x54W T5 single Lamp with voltage mode preheating

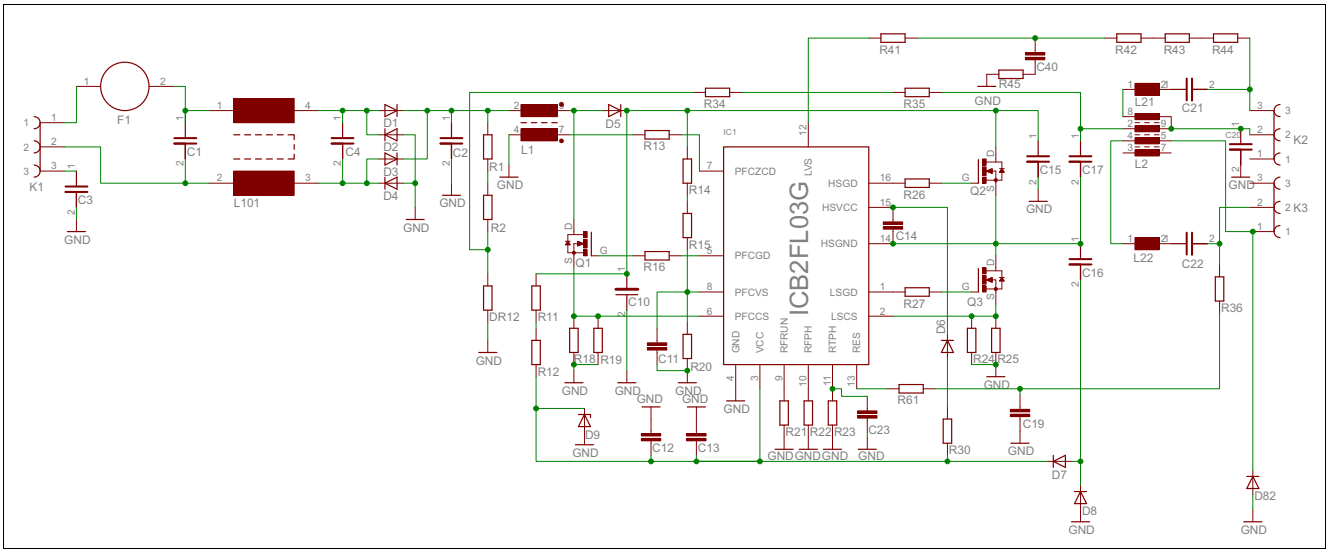


Figure 8-7 Schematic

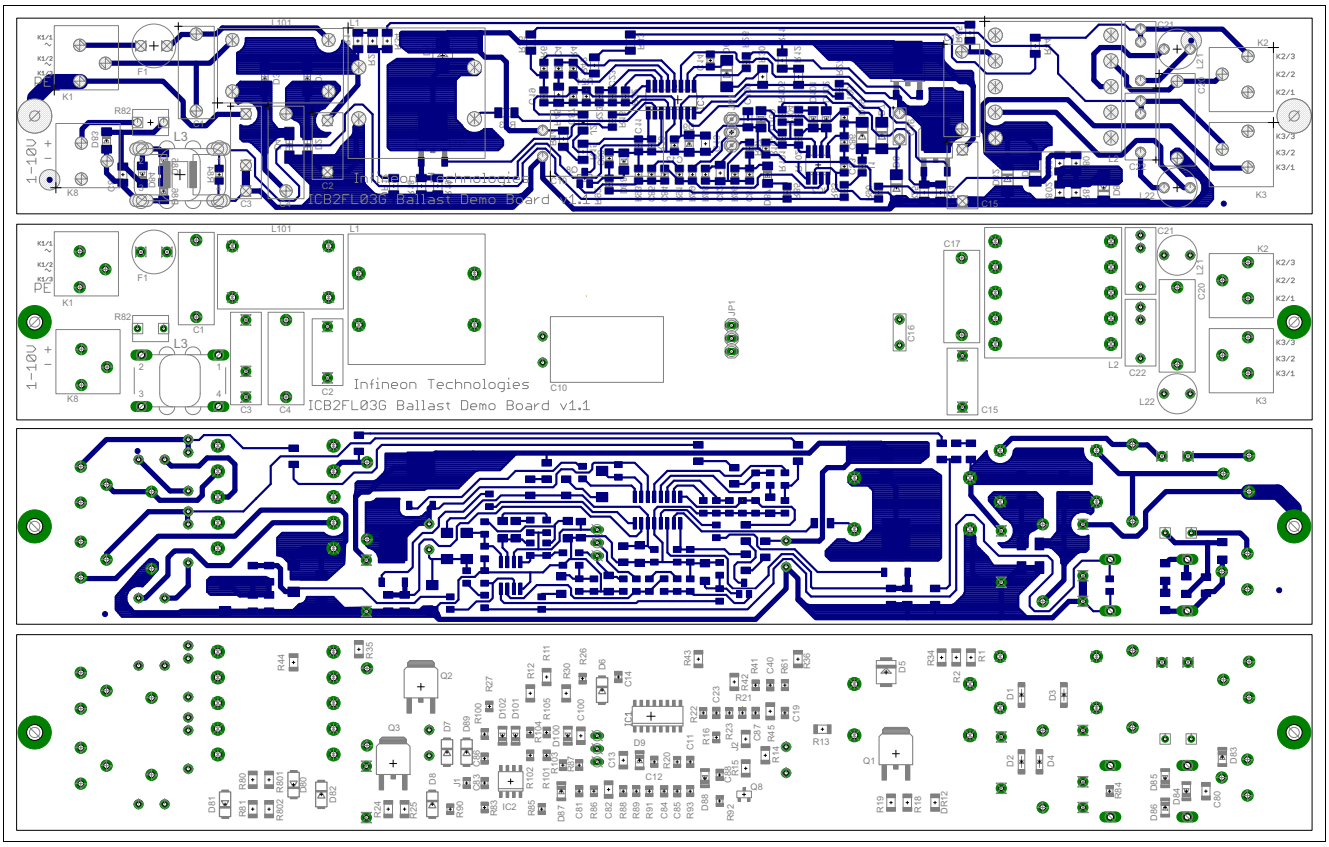


Figure 8-8 Layout

8.5 Burst Measurements according EN 61547

Table 8-1 shows the results of the normative test for the Burst stability.

Table 8-1 Operational characteristics of the Demo board 54W T5

		L	N	PE	L-N	L-PE	N-PE	L-N-PE
U [V]	+	4400	4400	4400	4400	4400	4400	4400
U [V]	-	4400	4400	4400	4400	4400	4400	4400

8.6 Interference Suppression according EN 55015

Figure 8-9 shows the results of the normative test for the Interference Suppression.

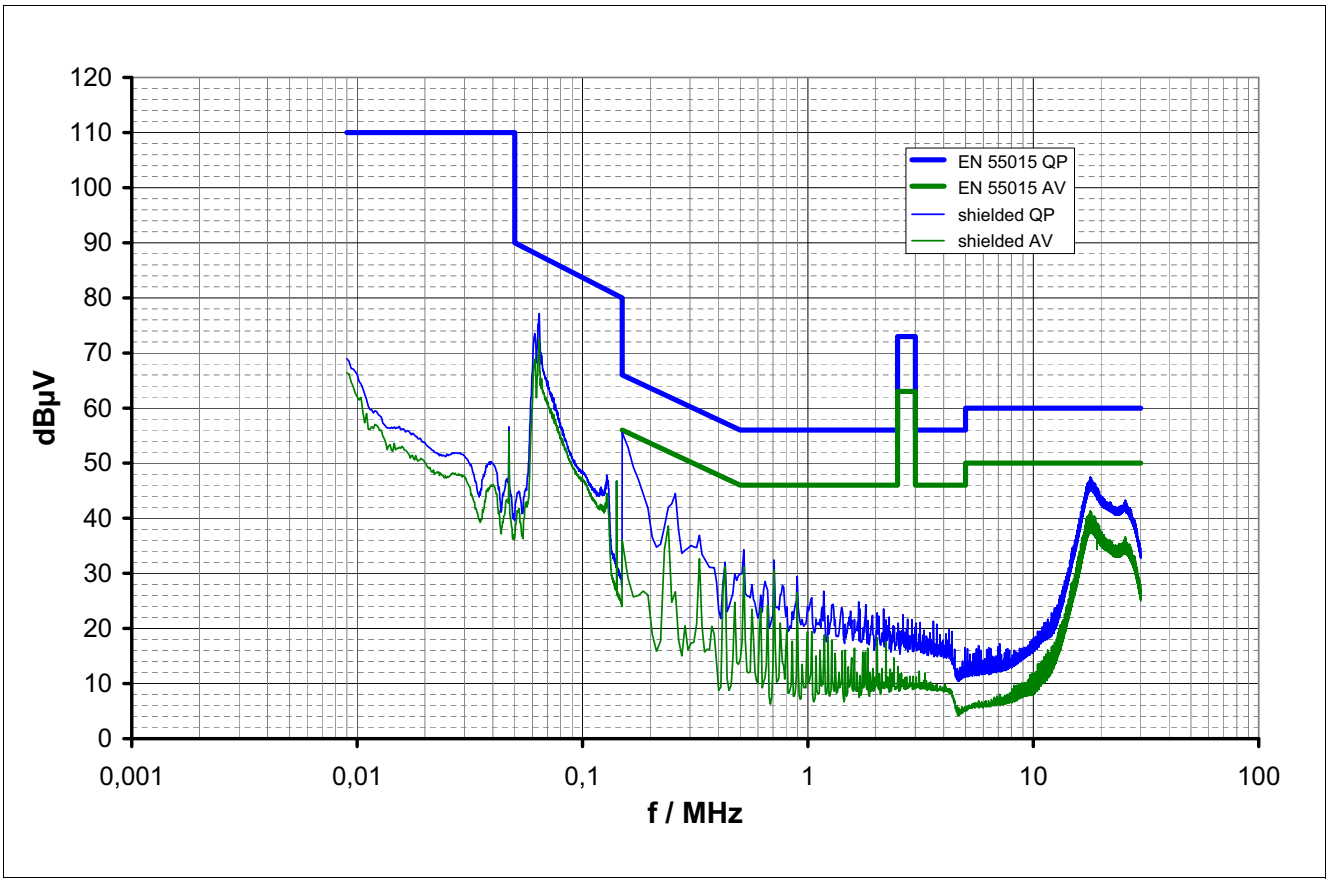


Figure 8-9 Interference Suppression according EN 55015

Terminology

Acronyms	Explanation
A_{THD}	Input current - Total Harmonic Distortion
BOM	Bill of material
CritCM	Critical Conduction Mode
DCM	Discontinuous Conduction Mode
EEI	Energy Efficiency Index
EOL1	End of Life 1 (Inverter Overload)
EOL2	End of Life 2 (Rectifier Effect)
FL	Fluorescent Lamp
f_{PH}	Preheating frequency
F_{RUN}	Run frequency
HSVCC	IC Supply Voltage (High Side)
I_{Lamp}	Lamp current
n	efficiency
PF	Power factor
PFC	Power Factor Correction
THD	Total Harmonic Distortion
t_{PH}	Preheating time
UVLO	Undervoltage Lockout (Restart after VCC hysteresis)
V_{BUS}	Elko voltage
VCC	IC Supply voltage (Low Side)
V_{IGN}	Ignition voltage
V_{IN}	Board Input voltage
V_{Lamp}	Lamp voltage

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