

### FEATURES

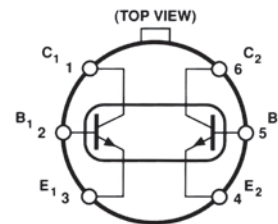
**Low  $V_{OS}$  ( $V_{BE}$  Match):** 40  $\mu\text{V}$  typ, 100  $\mu\text{V}$  max  
**Low  $TCV_{OS}$ :** 0.5  $\mu\text{V}/^\circ\text{C}$  max  
**High  $h_{FE}$ :** 500 min  
**Excellent  $h_{FE}$  Linearity** from 10 nA to 10 mA  
**Low Noise Voltage:** 0.23  $\mu\text{V}$  p-p—0.1 Hz to 10 Hz  
**High Breakdown:** 45 V min

### PRODUCT DESCRIPTION

The MAT01 is a monolithic dual NPN transistor. An exclusive Silicon Nitride "Triple-Passivation" process provides excellent stability of critical parameters over both temperature and time. Matching characteristics include offset voltage of 40  $\mu\text{V}$ , temperature drift of 0.15  $\mu\text{V}/^\circ\text{C}$ , and  $h_{FE}$  matching of 0.7%. Very high  $h_{FE}$  is provided over a six decade range of collector current, including an exceptional  $h_{FE}$  of 590 at a collector current of only 10 nA. The high gain at low collector current makes the MAT01 ideal for use in low power, low level input stages.

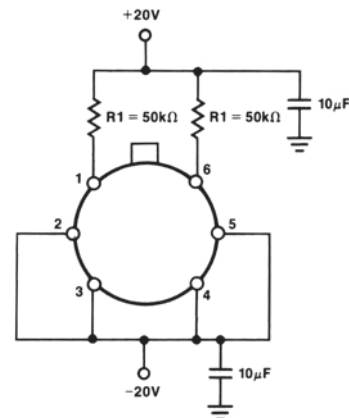
### PIN CONNECTION

TO-78  
 (H Suffix)



NOTE: Substrate is connected to case.

### BURN-IN CIRCUIT



### REV. B

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# MAT01—SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_{CB} = 15\text{ V}$ , $I_C = 10\ \mu\text{A}$ , $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

Parameter	Symbol	Conditions	MAT01AH			MAT01GH			Unit	
			Min	Typ	Max	Min	Typ	Min		
Breakdown Voltage	$BV_{CEO}$	$I_C = 100\ \mu\text{A}$	45			45			V	
Offset Voltage	$V_{OS}$			0.04	0.1		0.10	0.5	mV	
Offset Voltage Stability	$V_{OS}/\text{Time}$	(Note 1)		2.0			2.0		$\mu\text{V}/\text{Mo}$	
First Month			(Note 2)		0.2			0.2		$\mu\text{V}/\text{Mo}$
Long Term					0.1	0.6		0.2	3.2	nA
Offset Current	$I_{OS}$			13	20		18	40	nA	
Bias Current	$I_B$			590			430			
Current Gain	$h_{FE}$	$I_C = 10\ \text{nA}$		500	770		250	560		
		$I_C = 10\ \mu\text{A}$			840			610		
		$I_C = 10\ \text{mA}$			0.7	3.0		1.0	8.0	
Current Gain Match	$\Delta h_{FE}$	$I_C = 10\ \mu\text{A}$			0.8			1.2	%	
		$100\ \text{nA} \leq I_C \leq 10\ \text{mA}$							%	
Low Frequency Noise	$e_n\ \text{p-p}$	0.1 Hz to 10 Hz <sup>3</sup>		0.23	0.4		0.23	0.4	$\mu\text{V}\ \text{p-p}$	
Broadband Noise			$e_n\ \text{rms}$	1 Hz to 10 kHz		0.60			0.60	
Voltage	$e_n$	$f_O = 10\ \text{Hz}^3$				7.0	9.0		7.0	9.0
Noise Voltage					$f_O = 100\ \text{Hz}^3$		6.1	7.6		6.1
Density			$f_O = 1000\ \text{Hz}^3$		6.0	7.5		6.0	7.5	
Offset Voltage Change	$\Delta V_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq 30\ \text{V}$		0.5	3.0		0.8	8.0	$\mu\text{V}/\text{V}$	
Offset Current Change	$\Delta I_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq 30\ \text{V}$		2	15		3	70	$\text{pA}/\text{V}$	
Collector-Base	$I_{CBO}$	$V_{CB} = 30\ \text{V}$ , $I_E = 0^4$		15	50		25	200	pA	
Leakage Current			$I_{CES}$	$V_{CE} = 30\ \text{V}$ , $V_{BE} = 0^{4,5}$		50	200		90	400
Collector-Emitter	$I_{CC}$	$V_{CC} = 30\ \text{V}^5$				20	200		30	400
Leakage Current					$V_{CE(\text{SAT})}$	$I_B = 0.1\ \text{mA}$ , $I_C = 1\ \text{mA}$		0.12	0.20	
Collector-Saturation	$V_{CE(\text{SAT})}$	$I_B = 1\ \text{mA}$ , $I_C = 10\ \text{mA}$		0.8					0.8	
Voltage			$f_T$	$V_{CE} = 10\ \text{V}$ , $I_C = 10\ \text{mA}$		450			450	
Gain-Bandwidth Product	$C_{OB}$	$V_{CB} = 15\ \text{V}$ , $I_E = 0$				2.8			2.8	
Output Capacitance			$C_{CC}$	$V_{CC} = 0$		8.5			8.5	
Collector-Collector										pF
Capacitance									pF	

## ELECTRICAL CHARACTERISTICS (@ $V_{CB} = 15\ \text{V}$ , $I_C = 10\ \mu\text{A}$ , $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , unless otherwise noted.)

Parameter	Symbol	Conditions	MAT01AH			MAT01GH			Unit
			Min	Typ	Max	Min	Typ	Min	
Offset Voltage	$V_{OS}$			0.06	0.15		0.14	0.70	mV
Average Offset	$TCV_{OS}$	(Note 6)		0.15	0.50		0.35	1.8	$\mu\text{V}/^\circ\text{C}$
Voltage Drift			$I_{OS}$		0.9	8.0		1.5	15.0
Offset Current	$TCI_{OS}$	(Note 7)		10	90		15	150	$\text{pA}/^\circ\text{C}$
Average Offset			$I_B$		28	60		36	130
Current Drift	$I_{CBO}$	$T_A = 125^\circ\text{C}$ , $V_{CB} = 30\ \text{V}$ , $I_E = 0^4$		167	400		77	300	
Bias Current			$I_{CES}$	$T_A = 125^\circ\text{C}$ , $V_{CE} = 30\ \text{V}$ , $V_{BE} = 0^{4,6}$		15	80		25
Current Gain	$I_{CC}$	$T_A = 125^\circ\text{C}$ , $V_{CC} = 30\ \text{V}$ , (Note 6)				50	300		90
Collector-Base									
Leakage Current								nA	
Collector-Emitter								nA	
Leakage Current								nA	
Collector-Collector								nA	
Leakage Current								nA	

**TYPICAL ELECTRICAL CHARACTERISTICS** (@  $V_{CB} = 15\text{ V}$  and  $I_C = 10\ \mu\text{A}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

Parameter	Symbol	Conditions	MAT01N Typical	Unit
Average Offset Voltage Drift	$TCV_{OS}$		0.35	$\mu\text{V}/^\circ\text{C}$
Average Offset Current Drift	$TCI_{OS}$		15	$\text{pA}/^\circ\text{C}$
Collector-Emitter-Leakage Current	$I_{CES}$	$V_{CE} = 30\text{ V}, V_{BE} = 0$	90	$\text{pA}$
Collector-Base-Leakage Current	$I_{CBO}$	$V_{CB} = 30\text{ V}, I_E = 0$	25	$\text{pA}$
Gain Bandwidth Product	$f_T$	$V_{CE} = 10\text{ V}, I_C = 10\text{ mA}$	450	$\text{MHz}$
Offset Voltage Stability	$\Delta V_{OS}/T$	First Month (Note 1)	2.0	$\mu\text{V}/\text{Mo}$
		Long-Term (Note 2)	0.2	$\mu\text{V}/\text{Mo}$

## NOTES

<sup>1</sup>Exclude first hour of operation to allow for stabilization.

<sup>2</sup>Parameter describes long-term average drift after first month of operation.

<sup>3</sup>Sample tested.

<sup>4</sup>The collector-base ( $I_{CBO}$ ) and collector-emitter ( $I_{CES}$ ) leakage currents may be reduced by a factor of two to ten times by connecting the substrate (package) to a potential which is lower than either collector voltage.

<sup>5</sup> $I_{CC}$  and  $I_{CES}$  are guaranteed by measurement of  $I_{CBO}$ .

<sup>6</sup>Guaranteed by  $V_{OS}$  test ( $TCV_{OS} \equiv \frac{V_{OS}}{T}$  for  $V_{OS} \ll V_{BE}$ )  $T = 298^\circ\text{K}$  for  $T_A = 25^\circ\text{C}$ .

<sup>7</sup>Guaranteed by  $I_{OS}$  test limits over temperature.

Specifications subject to change without notice.

# MAT01

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

Collector-Base Voltage ( $BV_{CBO}$ )	
MAT01AH, GH	45 V
Collector-Emitter Voltage ( $BV_{CEO}$ )	
MAT01AH, GH	45 V
Collector-Collector Voltage ( $BV_{CC}$ )	
MAT01AH, GH	45 V
Emitter-Emitter Voltage ( $BV_{EE}$ )	
MAT01AH, GH	45 V
Emitter-Base Voltage ( $BV_{EBO}$ ) <sup>2</sup>	5 V
Collector Current ( $I_C$ )	25 mA
Emitter Current ( $I_E$ )	25 mA
Total Power Dissipation	
Case Temperature $\leq 40^\circ\text{C}$ <sup>3</sup>	1.8 W
Ambient Temperature $\leq 70^\circ\text{C}$ <sup>4</sup>	500 mW
Operating Ambient Temperature	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
Operating Junction Temperature	$-55^\circ\text{C}$ to $+150^\circ\text{C}$

Storage Temperature	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	$300^\circ\text{C}$
DICE Junction Temperature	$-65^\circ\text{C}$ to $+150^\circ\text{C}$

## NOTES

- <sup>1</sup>Absolute maximum ratings apply to both DICE and packaged devices.
- <sup>2</sup>Application of reverse bias voltages in excess of rating shown can result in degradation of  $h_{FE}$  and  $h_{FE}$  matching characteristics. Do not attempt to measure  $BV_{EBO}$  greater than the 5 V rating shown.
- <sup>3</sup>Rating applies to applications using heat sinking to control case temperature. Derate linearity at 16.4 mW/ $^\circ\text{C}$  for case temperatures above  $40^\circ\text{C}$ .
- <sup>4</sup>Rating applies to applications not using heat sinking; device in free air only. Derate linearity at 6.3 mW/ $^\circ\text{C}$  for ambient temperatures above  $70^\circ\text{C}$ .

## ORDERING GUIDE<sup>1</sup>

Model	$V_{OS\ max}$ ( $T_A = 25^\circ\text{C}$ )	Temperature Range	Package Option
MAT01AH <sup>2</sup>	0.1 mV	$-55^\circ\text{C}$ to $+125^\circ\text{C}$	TO-78
MAT01GH	0.5 mV	$-55^\circ\text{C}$ to $+125^\circ\text{C}$	TO-78

## NOTES

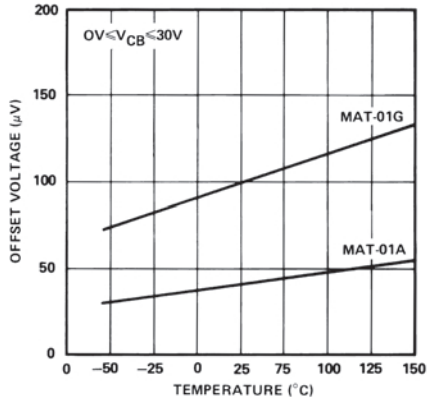
- <sup>1</sup>Burn-in is available on commercial and industrial temperature range parts in TO-can packages.
- <sup>2</sup>For devices processed in total compliance to MIL-STD-883, add/883 after part number. Consult factory for 883 data sheet.

## CAUTION

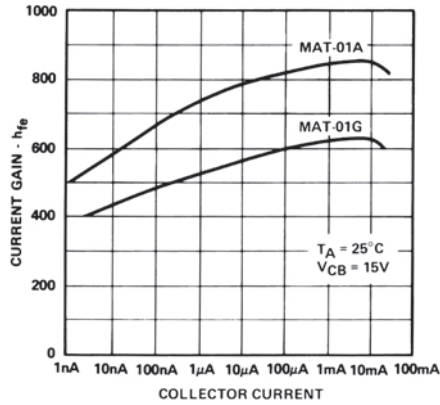
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the MAT01 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



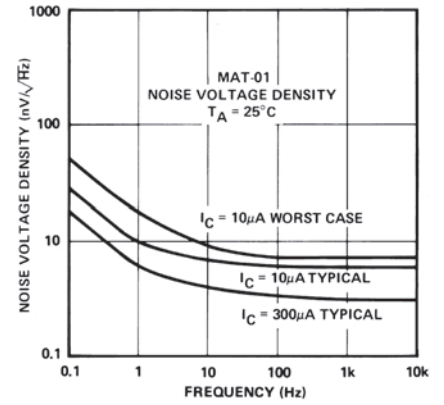
# Typical Performance Characteristics—MAT01



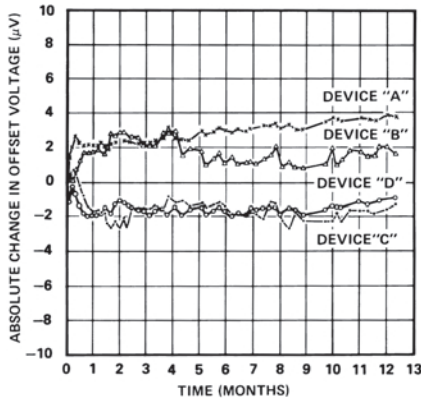
TPC 1. Offset Voltage vs. Temperature



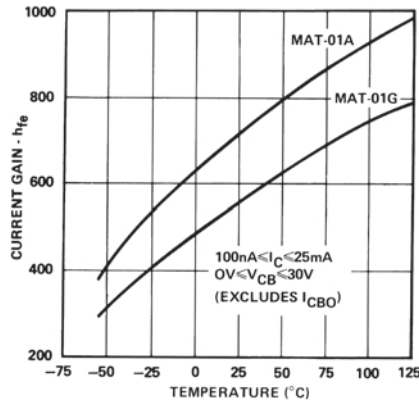
TPC 2. Offset Voltage vs. Time



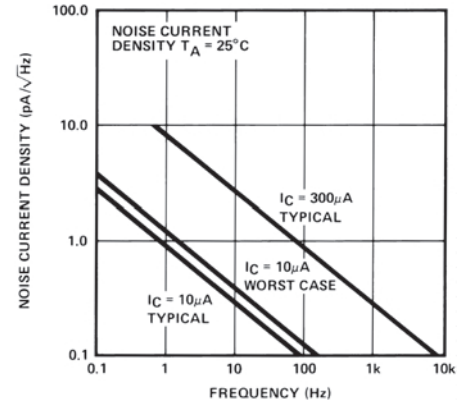
TPC 3. Base-Emitter Voltage vs. Collector Current



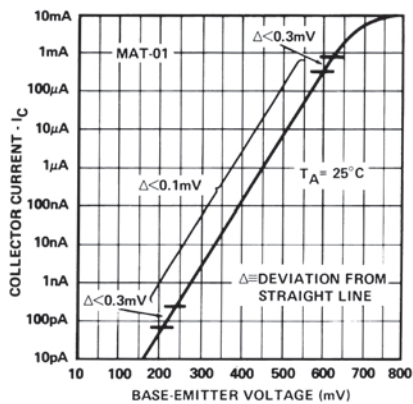
TPC 4. Current Gain vs. Collector Current



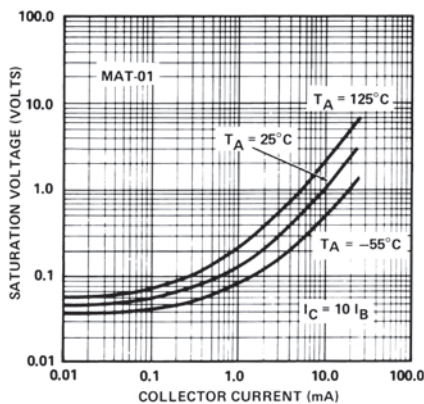
TPC 5. Current Gain vs. Temperature



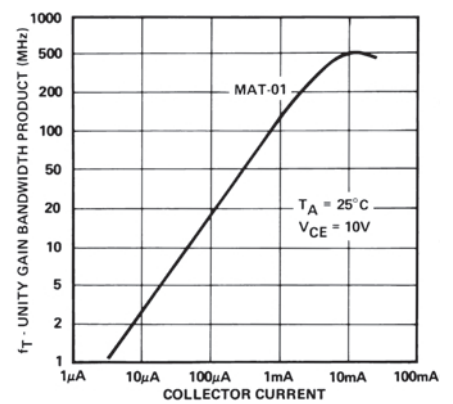
TPC 6. Saturation Voltage vs. Collector Current



TPC 7. Noise Voltage



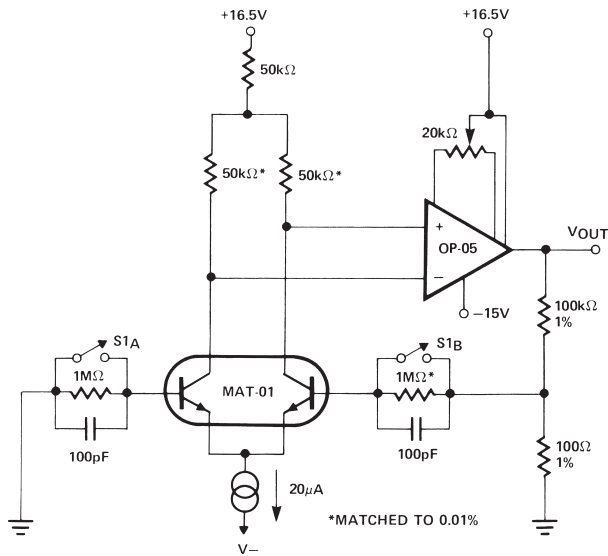
TPC 8. Noise Current Density



TPC 9. Gain-Bandwidth vs. Collector Current

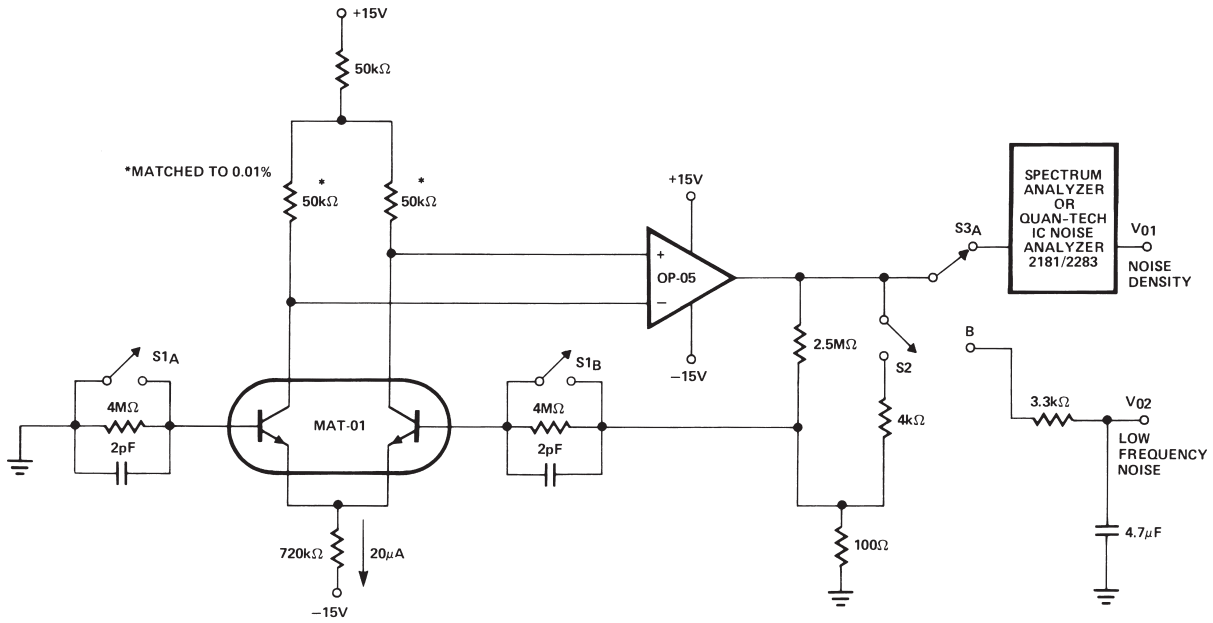
# MAT01

## MAT01 TEST CIRCUITS



TEST	SI <sub>A</sub>	SI <sub>B</sub>	UNITS
V <sub>OS</sub>	X	X	V <sub>OUT1</sub> 1 volt per mV
I <sub>OS</sub>	O	O	V <sub>OUT2</sub> - V <sub>OUT1</sub> 1 volt per nA

Figure 1. MAT01 Matching Measurement Circuit



TEST	SI <sub>A</sub>	SI <sub>B</sub>	S <sub>2</sub>	S <sub>3</sub>	READING
Noise Voltage Density (Per Transistor)	X	X	X	A	$V_{01}/\sqrt{2}$
Noise Current Density (Per Transistor)	O	O	X	A	$V_{01}/(\sqrt{2} \times 4M\Omega)$
Low Frequency Noise (Referred to Input)	X	X	O	B	$\frac{V_{02} \text{ PEAK-TO-PEAK}}{25,000}$

Figure 2. MAT01 Noise Measurement Circuit

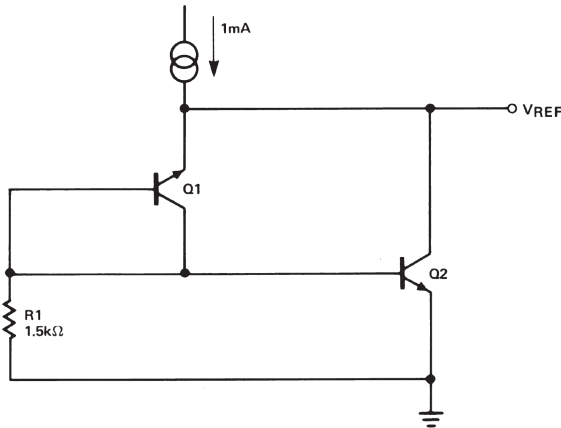
# Typical Performance Characteristics—MAT01

## APPLICATION NOTES

Application of reverse bias voltages to the emitter-base junctions in excess of ratings (5 V) may result in degradation of  $h_{FE}$  and  $h_{FE}$  matching characteristics. Circuit designs should be checked to ensure that reverse bias voltages above 5 V cannot be applied during such transient conditions as at circuit turn-on and turn-off.

Stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the predicted drift performance. Both input terminals should be maintained at the same temperature, preferably close to the temperature of the device's package.

## TYPICAL APPLICATIONS



$V_{REF} \approx 7.0V$   
 $TCV_{REF} \approx 10ppm/^{\circ}C$   
 $R_O \approx 40\Omega$   
 $R_1$  MAY BE ADJUSTED TO MINIMIZE  $TCV_{REF}$ . INCREASING  $R_1$  WILL CAUSE A POSITIVE CHANGE IN  $TCV_{REF}$ .  
 NOTE:  $h_{FE}$  OF Q1 WILL BE REDUCED BY OPERATION OF BREAKDOWN MODE.

Figure 3. Precision Reference

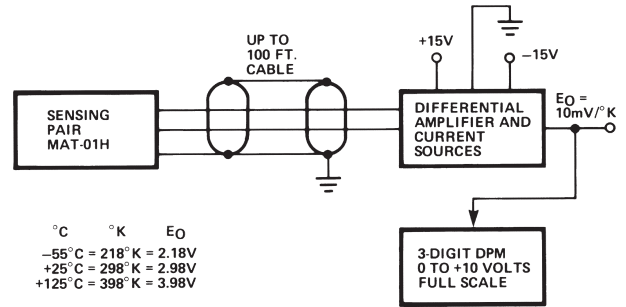


Figure 4. Basic Digital Thermometer Readout in Degrees Kelvin ( $^{\circ}K$ )

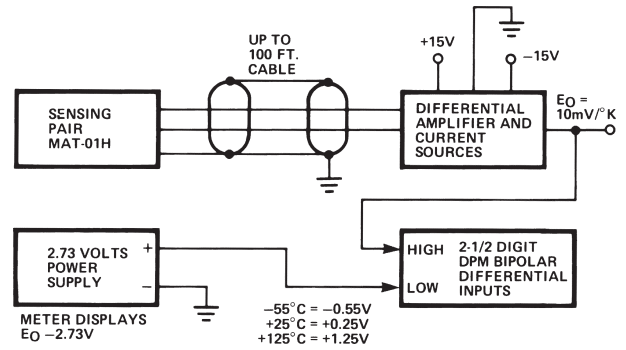
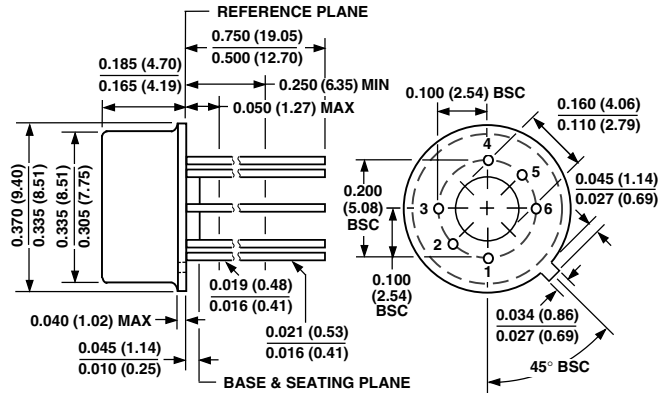


Figure 5. Digital Thermometer with Readout in  $^{\circ}C$

**OUTLINE DIMENSIONS**  
 Dimensions shown in inches and (mm).

**H-06A**  
**6-Lead Metal Can (TO-78)**



C00282-0-2/02(B)

**Revision History**

Location	Page
<b>Data Sheet changed from REV. A to REV. B.</b>	
Edits to FEATURES .....	1
Deleted WAFER TEST LIMITS .....	3
Deleted DICE CHARACTERISTICS .....	3
Edits to Table 5 .....	7

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### Наши контакты:

**Телефон:** +7 812 627 14 35

**Электронная почта:** [sales@st-electron.ru](mailto:sales@st-electron.ru)

**Адрес:** 198099, Санкт-Петербург,  
Промышленная ул, дом № 19, литера Н,  
помещение 100-Н Офис 331