CMOS DDS Modulator

AD7008

FEATURES
Single +5 V Supply
32-Bit Phase Accumulator
On-Chip COSINE and SINE Look-Up Tables
On-Chip 10-Bit DAC
Frequency, Phase and Amplitude Modulation
Parallel and Serial Loading
Software and Hardware Power Down Options
20 MHz and 50 MHz Speed Grades
44-Pin PLCC

APPLICATIONS
Frequency Synthesizers
Frequency, Phase or Amplitude Modulators
DDS Tuning
Digital Modulation

PRODUCT DESCRIPTION

The AD7008 direct digital synthesis chip is a numerically controlled oscillator employing a 32-bit phase accumulator, sine and cosine look-up tables and a 10-bit D/A converter integrated on a single CMOS chip. Modulation capabilities are provided for phase modulation, frequency modulation, and both in-phase and quadrature amplitude modulation suitable for QAM and SSB generation.

Clock rates up to 20 MHz and 50 MHz are supported. Frequency accuracy can be controlled to one part in 4 billion. Modulation may be effected by loading registers either through the parallel microprocessor interface or the serial interface. A frequency-select pin permits selection between two frequencies on a per cycle basis.

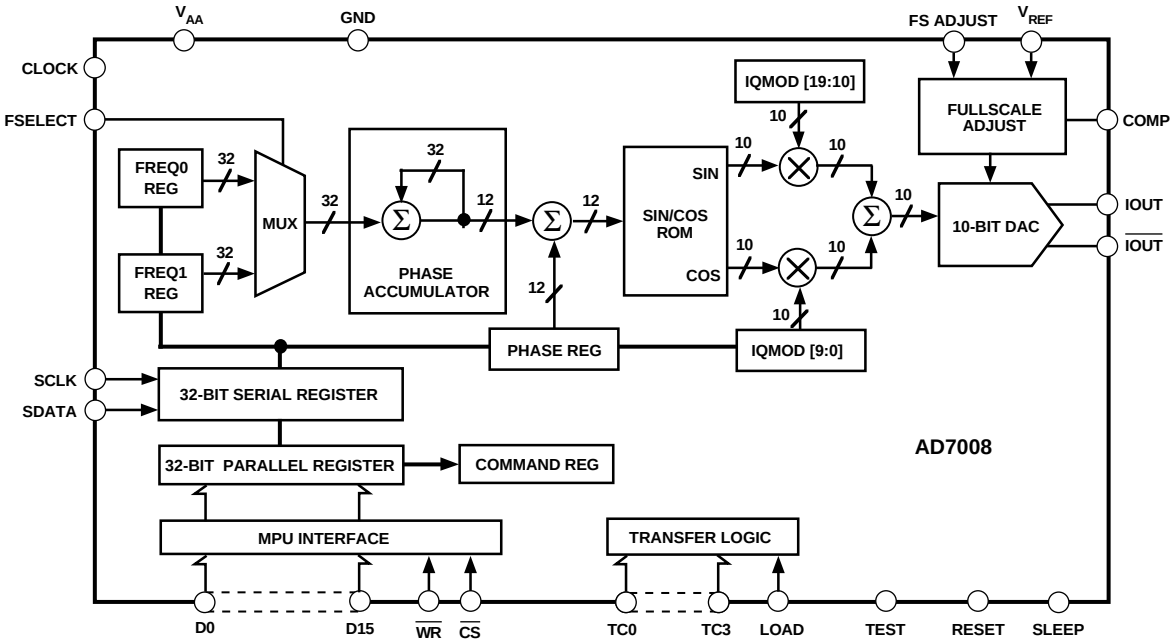
The serial and parallel interfaces may be operated independently and asynchronously from the DDS clock; the transfer control signals are internally synchronized to prevent metastability problems. The synchronizer can be bypassed to reduce the transfer latency in the event that the microprocessor clock is synchronous with the DDS clock.

A power-down pin allows external control of a power-down mode (also accessible through the microprocessor interface) The AD7008 is available in 44-pin PLCC.

PRODUCT HIGHLIGHT

1. Low Power
2. DSP/µP Interface
3. Completely Integrated

FUNCTIONAL BLOCK DIAGRAM



REV. B

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AD7008–SPECIFICATIONS[1] ($V_{AA} = V_{DD} = +5\ V \pm 5\%$; $T_A = T_{MIN}$ to T_{MAX}, $R_{SET} = 390\ \Omega$, $R_{LOAD} = 1\ \Omega$ for IOUT and $\overline{IOUT}$, unless otherwise noted)

Parameter	AD7008AP20 Min	AD7008AP20 Typ	AD7008AP20 Max	AD7008JP50 Min	AD7008JP50 Typ	AD7008JP50 Max	Units	Test Conditions/ Comments
SIGNAL DAC SPECIFICATIONS								
Resolution	10			10			Bits	
Update Rate (f_{MAX})			20			50	MSPS	
IOUT Full Scale		20			20		mA	
Output Compliance			1			1	Volts	
DC Accuracy								
Integral Nonlinearity		±1			±1		LSB	
Differential Nonlinearity		±1			±1		LSB	
DDS SPECIFICATIONS[2]								
Update Rate (f_{MAX})			20			50	MSPS	
Dynamic Specifications								
Signal-to-Noise	50			50			dB	$f_{CLK} = f_{MAX}$, f_{OUT} = 2 MHz
Total Harmonic Distortion	–55			–53			dB	$f_{CLK} = f_{MAX}$, f_{OUT} = 2 MHz
Spurious Free Dynamic Range (SFDR)[3]								
Narrow Band (±50 kHz)	–70			–70			dBc	f_{CLK} = 6.25 MHz, f_{OUT} = 2.11 MHz
Wide Band (±2 MHz)	–55			–55			dBc	
VOLTAGE REFERENCE								
Internal Reference @ +25°C[4]	1.2	1.27	1.35	1.2	1.27	1.35	Volts	
Reference TC		300			300		ppm/°C	
V_{REF} Overdrive[5]	0	2		0	2		V	
LOGIC INPUTS								
V_{INH}, Input High Voltage	V_{DD}–0.9			V_{DD}–0.9			Volts	
V_{INL}, Input Low Voltage			0.9			0.9	Volts	
I_{INH}, Input Current			10			10	µA	
C_{IN}, Input Capacitance			10			10	pF	
POWER SUPPLIES								
V_{DD}	4.75		5.25	4.75		5.25	Volts	
I_{AA}		26			26		mA	$R_{SET} = 390\ \Omega$
I_{DD}		22 + 1.5/MHz			22 + 1.5/MHz		mA	
$I_{AA} + I_{DD}$								
f_{CLK} = Max		80	110		125	160	mA	
Sleep = V_{DD}			10			20	mA	

NOTES

[1]Operating temperature ranges as follows: A Version: –40°C to +85°C; J Version: 0°C to +70°C.

[2]All dynamic specifications are measured using IOUT. 100% Production tested.

[3]f_{CLK} = 6.25 MHz, Frequency Word = 5671C71C HEX, f_{OUT} = 2.11 MHz.

[4]V_{REF} may be externally driven between 0 and V_{DD}.

[5]Do not allow reference current to cause power dissipation beyond the limit of $I_{AA} + I_{DD}$ shown above.

Specifications subject to change without notice.

TIMING CHARACTERISTICS ($V_{AA} = V_{DD}$ +5 V ± 5%; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted)

Parameter	AD7008AP20 Min	Typ	Max	AD7008JP50 Min	Typ	Max	Units	Test Conditions/Comments
t_1	50			20			ns	CLOCK Period
t_2	20			8			ns	CLOCK High Duration
t_3	20			8			ns	CLOCK Low Duration
t_4	5			5			ns	CLOCK to Control Setup Time
t_5	3			3			ns	CLOCK to Control Hold Time
t_6	$4t_1$			$4t_1$			ns	LOAD Period
t_7	$2t_1$			$2t_1$			ns	LOAD High Duration[1]
t_8	5			5			ns	LOAD High to TC0–TC3 Setup Time
t_9	5			5			ns	LOAD High to TC0–TC3 Hold Time
t_{10}	10			10			ns	$\overline{WR}$ Falling to $\overline{CS}$ Low Setup Time
t_{11}	10			10			ns	$\overline{WR}$ Falling to $\overline{CS}$ Low Hold Time
t_{12}	20			20			ns	Minimum $\overline{WR}$ Low Duration
t_{13}	10			10			ns	Minimum $\overline{WR}$ High Duration
t_{14}	3			3			ns	$\overline{WR}$ to D0–D15 Setup Time
t_{15}	3			3			ns	$\overline{WR}$ to D0–D15 Hold Time
t_{16}	20			20			ns	SCLK Period
t_{17}	8			8			ns	SCLK High Duration
t_{18}	8			8			ns	SCLK Low Duration
t_{19}	10			10			ns	SCLK Rising to SDATA Setup Time
t_{20}	10			10			ns	SCLK Rising to SDATA Hold Time

NOTE
[1]May be reduced to $1t_1$ if LOAD is synchronized to CLOCK and Setup (t_4) and Hold (t_5) Times for LOAD to CLOCK are observed.

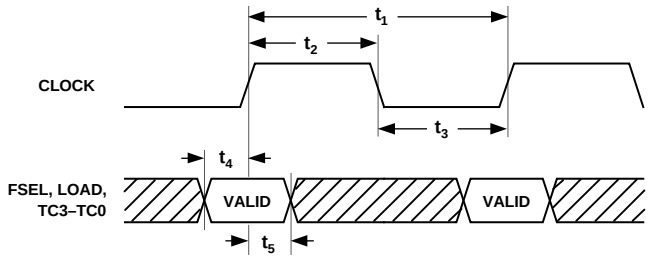


Figure 1. Clock Synchronization Timing

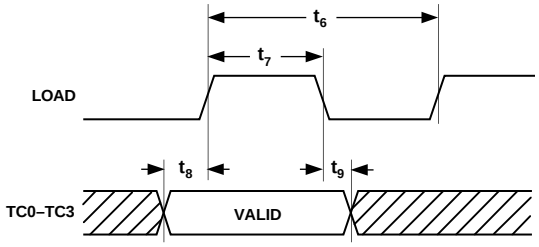


Figure 2. Register Transfer Timing

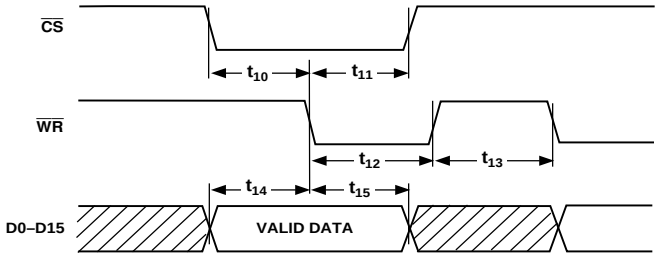


Figure 3. Parallel Port Timing

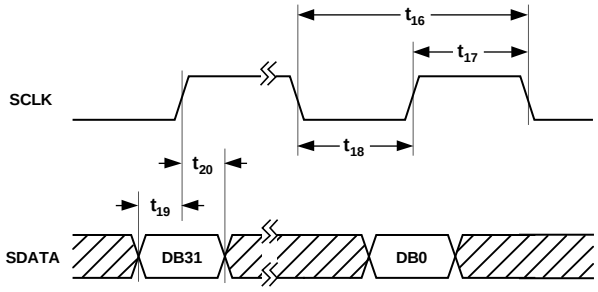


Figure 4. Serial Port Timing

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

V_{AA}, V_{DD} to GND . . . . . –0.3 V to +7 V
AGND to DGND . . . . . –0.3 V to +0.3 V
Digital I/O Voltage to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to AGND . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Industrial (A Version) . . . . . –40°C to +85°C
Commercial (J Version) . . . . . 0°C to +70°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Junction Temperature . . . . . +115°C
PLCC θ_{JA} Thermal Impedance . . . . . +53.8°C/W
θ_{JC} Thermal Impedance . . . . . +24.1°C/W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7008AP20	–40°C to +85°C	44-Pin PLCC	P-44A
AD7008JP50	0°C to +70°C	44-Pin PLCC	P-44A
AD7008/PCB*		1–3.5" Disk	

*AD7008/PCB DDS Evaluation Kit, assembled and tested. Kit includes an AD7008JP50.

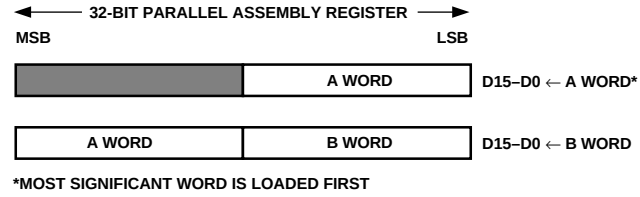


Figure 5. 16-Bit Parallel Port Loading Sequence

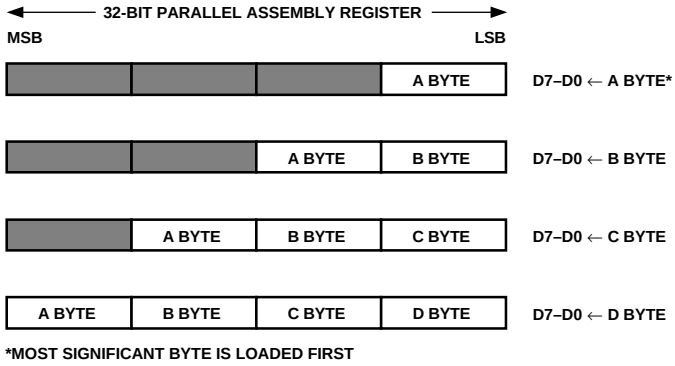


Figure 6. 8-Bit Parallel Port Loading Sequence

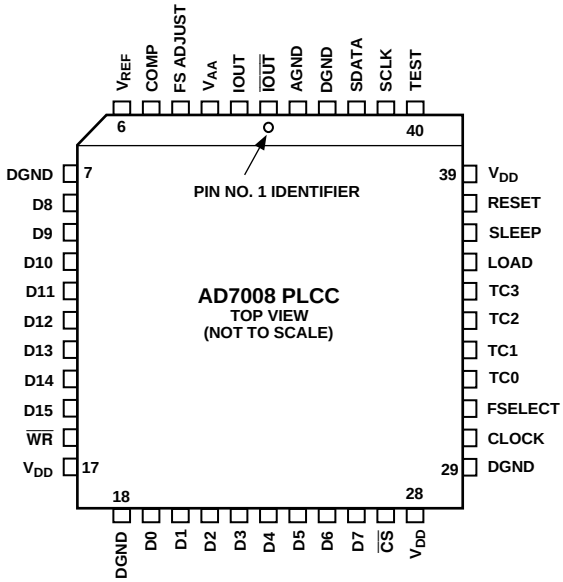
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7008 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION

PLCC



PIN DESCRIPTION

Mnemonic	Function
POWER SUPPLY	
V_{AA}	Positive power supply for the analog section. A 0.1 μF decoupling capacitor should be connected between V_{AA} and AGND. This is +5 V ± 5%.
AGND	Analog Ground.
V_{DD}	Positive power supply for the digital section. A 0.1 μF decoupling capacitor should be connected between V_{DD} and DGND. This is +5 V ± 5%. Both V_{AA} and V_{DD} should be externally tied together.
DGND	Digital Ground; both AGND and DGND should be externally tied together.
ANALOG SIGNAL AND REFERENCE	
IOUT, $\overline{\text{IOUT}}$	Current Output. This is a high impedance current source. A load resistor should be connected between IOUT and AGND. $\overline{\text{IOUT}}$ should be either tied directly to AGND or through an external load resistor to AGND.
FS ADJUST	Full-Scale Adjust Control. A resistor (R_{SET}) is connected between this pin and AGND. This determines the magnitude of the full-scale DAC current. The relationship between R_{SET} and the full-scale current is as follows: $$IOUT_{FULL\text{-}SCALE}\ (mA) = \frac{6233 \times V_{REF}}{R_{SET}} \qquad V_{REF} = 1.27\ V\ nominal\ \ R_{SET} = 390\ \Omega\ typical$$
V_{REF}	Voltage Reference Input. A 0.1 μF decoupling ceramic capacitor should be connected between V_{REF} and V_{AA}. There is an internal 1.27 volt reference which can be overdriven by an external reference if required. See specifications for maximum range.
COMP	Compensation pin. This is a compensation pin for the internal reference amplifier. A 0.1 μF decoupling ceramic capacitor should be connected between COMP and V_{AA}.
DIGITAL INTERFACE AND CONTROL	
CLOCK	Digital Clock Input for DAC and NCO. DDS output frequencies are expressed as a binary fraction of the frequency of this clock. The output frequency accuracy and phase noise is determined by this clock.
FSELECT	Frequency Select Input. FSELECT controls which frequency register, FREQ0 or FREQ1, is used in the phase accumulator. Frequency selection can be done on a cycle-per-cycle basis. See Tables I, II and III.
LOAD	Register load, active high digital Input. This pin, in conjunction with TC3–TC0, control loading of internal registers from either the parallel or serial assembly registers. The load pin must be high at least $1t_1$. See Table II.
TC3–TC0	Transfer Control address bus, digital inputs. This address determines the source and destination registers that are used during a transfer. The source register can either be the parallel assembly register or the serial assembly register. The destination register can be any of the following: COMMAND REG, FREQ0 REG, FREQ1 REG, PHASE REG or IQMOD REG. TC3–TC0 should be valid prior to LOAD rising and should not change until LOAD falls. The Command Register can only be loaded from the parallel assembly register. See Table II.
$\overline{\text{CS}}$	Chip Select, active low digital input. This input in conjunction with $\overline{\text{WR}}$ is used when writing to the parallel assembly register.
$\overline{\text{WR}}$	Write, active low digital input. This input in conjunction with $\overline{\text{CS}}$ is used when writing to the parallel assembly register.
D7–D0	Data Bus, digital inputs. These represent the low byte of the 16-bit data input port used to write to the 32-bit parallel assembly register. The databus can configured for either a 8-bit or 16-bit MPU/DSP ports.
D15–D8	Data Bus, digital inputs. These represent the high byte of the 16-bit data input port used to write to the 32-bit parallel assembly register. The databus can be configured for either a 8-bit or 16-bit MPU/DSP ports. When the databus is configured for 8-bit operation, D8–D15 should be tied to DGND.
SCLK	Serial Clock, digital input. SCLK is used, in conjunction with SDATA, to clock data into the 32-bit serial assembly register.
SDATA	Serial Data, digital input. Serial data is clocked on the rising edge of SCLK, Most Significant Bit (MSB) first.
SLEEP	Low power sleep control, active high digital input. SLEEP puts the AD7008 into a low power sleep mode. Internal clocks are disabled, while also turning off the DAC current sources. A SLEEP bit is also provided in the COMMAND REG to put the AD7008 into a low power sleep mode.
RESET	Register Reset, active high digital input. RESET clears the COMMAND REG and all the modulation registers to zero.
TEST	Test Mode. This is used for factory test only and should be left as a No Connect.

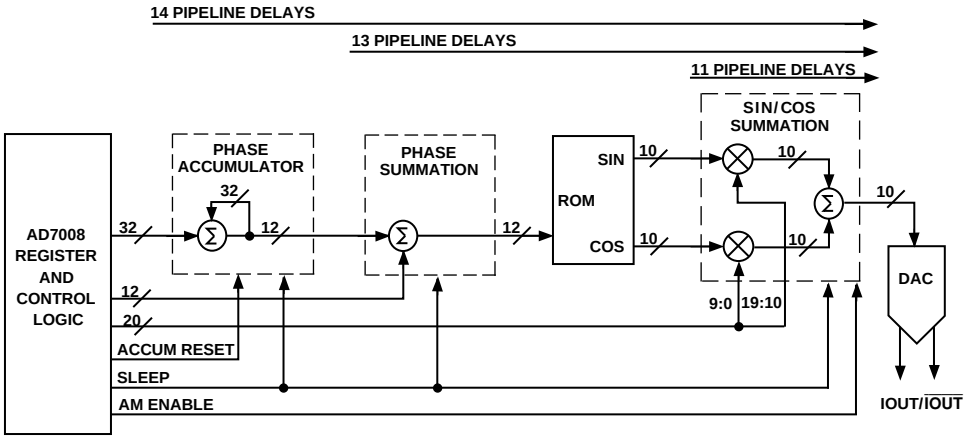


Figure 7. AD7008 CMOS DDS Modulator (See Table I)

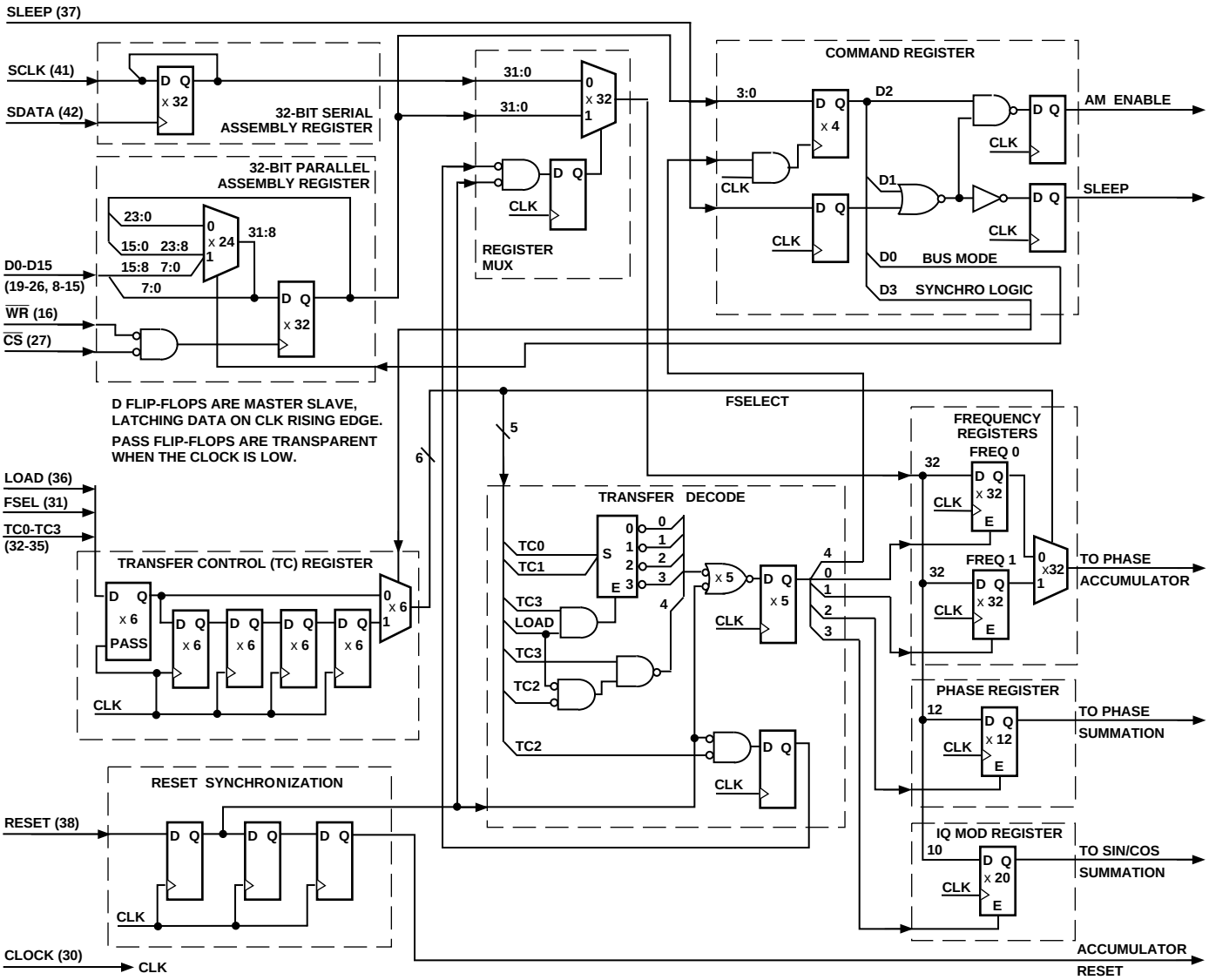


Figure 8. AD7008 Register and Control Logic

Table I. Latency Table

Function	Latency (Synchronizer Enabled CR3 = 0[1])
FSelect	$14t_1$
Phase	$13t_1$
IQ Mod	$11t_1$

NOTE
[1]All latencies are reduced by $4t_1$ when CR3 = 1 (synchronizer disabled). $1t_1$ is equal to one pipeline delay.

Table II. Source and Destination Register

TC3	TC2	TC1	TC0	LOAD	Source Register	Destination Register
X	X	X	X	0	N/A	N/A
0	0	X	X	1	Parallel	COMMAND*
1	0	0	0	1	Parallel	FREQ0
1	0	0	1	1	Parallel	FREQ1
1	0	1	0	1	Parallel	PHASE
1	0	1	1	1	Parallel	IQMOD
1	1	0	0	1	Serial	FREQ0
1	1	0	1	1	Serial	FREQ1
1	1	1	0	1	Serial	PHASE
1	1	1	1	1	Serial	IQMOD

*The Command Register can only be loaded from the parallel assembly registers.

Table III. AD7008 Control Registers

Register	Size	Reset State	Description
COMMAND REG*	4 Bits CR3–CR0	All Zeros	Command Register. This is written to using the parallel assembly register.
FREQ0 REG	32 Bits DB31–DB0	All Zeros	Frequency Register 0. This defines the output frequency, when FSELECT = 0, as a fraction of the CLOCK frequency.
FREQ1 REG	32 Bits DB31–DB0	All Zeros	Frequency Register 1. This defines the output frequency, when FSELECT = 1, as a fraction of the CLOCK frequency.
PHASE REG	12 Bits DB11–DB0	All Zeros	Phase Offset Register. The contents of this register is added to the output of the phase accumulator.
IQMOD REG	20 Bits DB19–DB0	All Zeros	I and Q Amplitude Modulation Register. This defines the amplitude of the I and Q signals as 10-bit twos complement binary fractions. DB[19:10] is multiplied by the Quadrature (sine component and multiplied by the In-Phase (cosine) component.

*On power up, the Command Register should be configured by the user for the desired mode before operation.

Table IV. Command Register Bits*

CR0	= 0	Eight-Bit Databus. Pins D15–D8 are ignored and the parallel assembly register shifts eight places left on each write. Hence four successive writes are required to load the 32-bit parallel assembly register, Figure 6.
	= 1	Sixteen-Bit Databus. The parallel assembly register shifts 16 places left on each write. Hence two successive writes are required to load the 32-bit parallel assembly register, Figure 5.
CR1	= 0	Normal Operation.
	= 1	Low Power Sleep Mode. Internal Clocks and the DAC current sources are turned off.
CR2	= 0	Amplitude Modulation Bypass. The output of the sine LUT is directly sent to the DAC.
	= 1	Amplitude Modulation Enable. IQ modulation is enabled allowing AM or QAM to be performed.
CR3	= 0	Synchronizer Logic Enabled. The FSELECT, LOAD and TC3–TC0 signals are passed through a 4-stage pipeline to synchronize them with the CLOCK, avoiding metastability problems.
	= 1	Synchronizer Logic Disabled. The FSELECT, LOAD and TC3–TC0 signals bypass the synchronization logic. This allows for faster response to the control signals.

*The Command Register can only be loaded from the parallel assembly register.

CIRCUIT DESCRIPTION

The AD7008 provides an exciting new level of integration for the RF/Communications system designer. The AD7008 combines the numerically controlled oscillator (NCO), SINE/COSINE look-up tables, frequency, phase and IQ modulators, and a digital-to-analog converter on a single integrated circuit.

The internal circuitry of the AD7008 consists of four main sections. These are:

Numerically Controlled Oscillator (NCO) + Phase Modulator
SINE and COSINE Look-Up Tables
In Phase and Quadrature Modulators
Digital-to-Analog Converter

The AD7008 is a fully integrated Direct Digital Synthesis (DDS) chip. The chip requires one reference clock, two low-precision resistors and six decoupling capacitors to provide digitally created sine waves up to 25 MHz. In addition to the generation of this RF signal, the chip is fully capable of a broad range of simple and complex modulation schemes. These modulation schemes are fully implemented in the digital domain allowing accurate and simple realization of complex modulation algorithms using DSP techniques.

THEORY OF OPERATION

Sine waves are typically thought of in terms of their amplitude form: $a(t)$ = sin (ωt) or $a(t)$ = cos (ωt). However, these are nonlinear and not easy to generate except through piece wise construction. On the other hand, the angular information is linear in nature. That is, the phase angle rotates though a fixed angle for each unit of time. The angular rate depends on the frequency of the signal by the traditional rate of: $\omega = 2\pi f$.

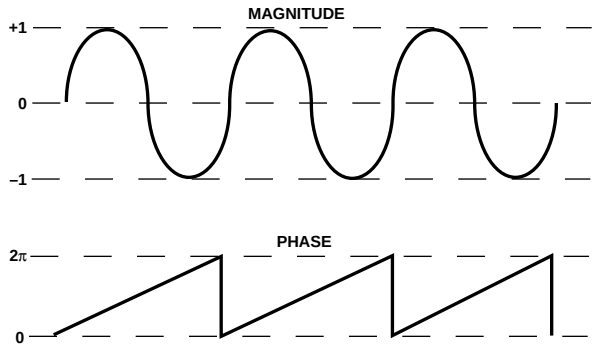


Figure 9.

Knowing that the phase of a sine wave is linear and given a reference interval (clock period), the phase rotation for that period can be determined.

$$\Delta Phase = \omega dt$$

Solving for w:

$$\omega = \frac{\Delta \text{Phase}}{\text{dt}} = 2\,\pi\text{f}$$

Solving for f and substituting the reference clock frequency for the reference period: $\left(\frac{1}{f_{CLOCK}} = dt\right)$:

$$f = \frac{\Delta Phase \times f_{CLOCK}}{2\,\pi}$$

The AD7008 *builds* the output based on this simple equation. A simple DDS chip will implement this equation with 3 major subcircuits. The AD7008 has an extra section for I and Q modulation.

Numerically Controlled Oscillator + Phase Modulator

This consists of two frequency select registers, a phase accumulator and a phase offset register. The main component of the NCO is a 32-bit phase accumulator which assembles the phase component of the output signal. Continuous time signals have a phase range 0 to 2 π. Outside this range of numbers, the sinusoidal functions repeat themselves in a periodic manner. The digital implementation is no different. The accumulator simply scales the range of phase numbers into a multibit digital word. The phase accumulator in the AD7008 is implemented with 32 bits. Therefore in the AD7008, $2\,\pi = 2^{32}$. Likewise, the $\Delta Phase$ term is scaled into this range of numbers $0 \le \Delta Phase \le 2^{32} - 1$. Making these substitutions into the equation above:

$$f = \frac{\Delta Phase \times f_{CLOCK}}{2^{32}} \; where \; 0 \le \Delta Phase < 2^{32}$$

With a clock signal of 50 MHz and a phase word of 051EB852 hex:

$$f = \frac{51EB852 \times 50\ MHz}{2^{32}} = 1.000000000931\ MHz$$

The input to the phase accumulator (i.e., the phase step) can be selected either from the FREQ0 Register or FREQ1 Register, and this is controlled by the FSELECT pin. The phase accumulator in the AD7008 inherently generates a continuous 32-bit phase signal, thus avoiding any output discontinuity when switching between frequencies. This facilitates complex frequency modulation schemes, such as GMSK.

Following the NCO, a phase offset can be added to perform phase modulation using the 12-bit PHASE Register. The contents of this register are added to the most significant bits of the NCO.

Sine and Cosine Look-Up Tables

To make the output useful, the signal must be converted from phase information into a sinusoidal value. Since phase information maps directly into amplitude, a ROM look up table converts the phase information into amplitude. To do this the digital phase information is used to address a Sine/Cosine ROM LUT. Only the most significant 12 bits are used for this purpose. The remaining 20 bits provide frequency resolution and minimize the effects of quantization of the phase to amplitude conversion.

In Phase and Quadrature Modulators

Two 10-bit amplitude multipliers are provided allowing the easy implementation of either Quadrature Amplitude Modulation (QAM) or Amplitude Modulation (AM). The 20-bit IQMOD Register is used to control the amplitude of the I (cos) and Q (sin) signals. IQMOD [9:0] controls the I amplitude and IQMOD [19:10] controls the Q amplitude.

The user should ensure that when summing the I and Q signals the sum should not exceed the value that a 10-bit accumulator can hold. The AD7008 does not clip the digital output; the output will roll over instead of clip.

When amplitude modulation is not required, the IQ multipliers can be bypassed (CR = 2). The sine output is directly sent to the 10-bit DAC.

Digital-to-Analog Converter

The AD7008 includes a high impedance current source 10-bit DAC, capable of driving a wide range of loads at different speeds. Full-scale output current can be adjusted, for optimum power and external load requirements, through the use of a single external resistor (R_{SET}).

The DAC can be configured for single or differential-ended operation. $\overline{IOUT}$ can be tied directly to AGND for single-ended operation or through a load resistor to develop an output voltage. The load resistor can be any value required as long as the full-scale voltage developed across it does not exceed 1 volt. Since full-scale current is controlled by R_{SET}, adjustments to R_{SET} can balance changes made to the load resistor.

DSP and MPU Interfacing

The AD7008 contains a 32-bit parallel assembly register and a 32-bit serial assembly register. Each of the modulation registers can be loaded from either assembly register under control of the LOAD pin and the Transfer-Control (TC) pins (See Table II). The Command register can be loaded only from the parallel assembly register. In practical use, both serial and parallel interfaces can be used simultaneously if the application requires.

TC3–TC0 should be stable before the LOAD signal rises and should not change until after LOAD falls (Figure 2).

The DSP/MPU asserts both $\overline{WR}$ and $\overline{CS}$ to load the parallel assembly register (Figure 3). At the end of each write, the parallel assembly register is shifted left by 8 or 16 bits (Depending on CR0), and the new data is loaded into the low bits. Hence, two 16-bit writes or four 8-bit writes are used to load the parallel assembly register. When loading parallel data, it is only necessary to write as much data as will be used by that register. For instance, the Command Register requires only one write to the parallel assembly register.

Serial data is input to the chip on the rising edge of SCLK, most significant bit first (Figure 4). The data in the assembly registers can be transferred to the modulation registers by means of the transfer control pins.

Maximum Updating of the AD7008

Updating the AD7008 need not take place in a synchronous fashion. However, in asynchronous systems, most of the external clock pulses (LOAD and SCLK) must be high for greater than one system clock period. This insures that at least one CLOCK rising edge will occur successfully completing the latch function (Figure 1).

However, if the AD7008 is run in a synchronous mode with the controlling DSP or microcontroller, the AD7008 may be loaded very rapidly. Optimal speed is attained when operated in the 16-bit load mode; the following discussion will assume that mode is used. Each of the modulation registers require two 16 bit loads. This data is latched into the parallel assembly register on the falling edge of the $\overline{WR}$ command. This strobe is not qualified by the CLOCK pulse but must be held low for a minimum of 20 ns and only need be high for 10 ns. The two 16-bit words may be loaded in succession. While the second 16-bit word is being latched into the parallel assembly register, the Transfer and Control word may be presented to the TC3–TC0 pins. If the designation register is always the same, an external register can be used to store the information on the inputs of TC3–TC0. At some time after the second falling edge of $\overline{WR}$, the LOAD signal may go high. As long as the load signal is high 5 ns (see setup time) before the rising edge of the CLOCK signal, data will be transferred to the destination register.

The limiting factor of this technique is the $\overline{WR}$ period which is 30 ns. Thus the CLOCK may run up to 33 MSPS using this technique and the effective update rate would be one half or 16.5 MHz. See timing Figure 10 for timing details.

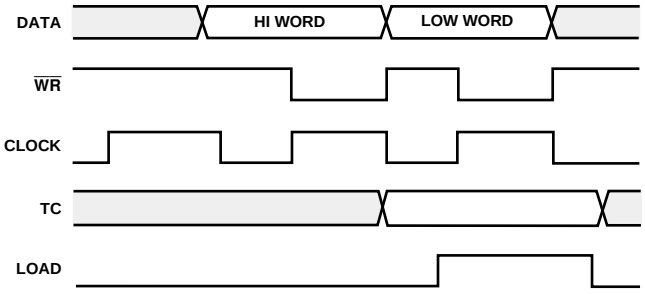


Figure 10. Accelerated Data Load Sequence

APPLICATIONS

Serial Configuration

Data is written to the AD7008 in serial mode using the two signal lines SDATA and SCLK. Data is accumulated in the serial assembly register with the most significant bit loaded first. The data bits are loaded on the rising edge of the serial clock. Once data is loaded in the serial assembly register, it must be transferred to the appropriate register on chip. This is accomplished by setting the TC bits according to Tables II and III. If you want to load the serial assembly register into FREQ1 register, the TC bits should be 1101. When the LOAD pin is raised, data is transferred directly to the FREQ1 register. When operating in serial mode, some functions must still operate in parallel mode such as loading the TC bits and updating the Command register which is accessed only through the parallel assembly register. See Figure 11 for a typical serial mode configuration.

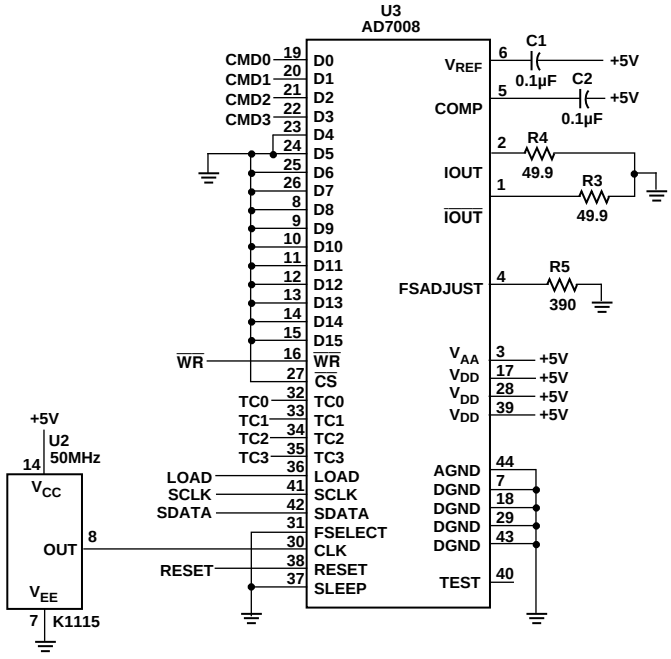


Figure 11. General Purpose Serial Interface

Parallel Configuration

The AD7008 functions fully in the parallel mode. There are two parallel modes of operation. Both are similar but are tailored for different bus widths, 8 and 16 bits. All modes of operation can be controlled by the parallel interface.

On power up and reset, the chip must be configured by instructing the command register how to operate. The command register may be used to set the device up for 8- or 16-bit mode, sleep mode, amplitude control and synchronization logic. At reset, the chip defaults to 8-bit bus, no amplitude control and logic synchronized. The code fragment below indicates how the initialization code for the AD7008 might look using the ADSP-21020.

```
{dds_para is a port define to decode for
the parallel assembly register write pulse.
dds_cont is a port defined to decode for
the TC control Load pin.  The Command reg-
ister must first be loaded with configura-
tion information. In this example, the chip
is set up for 16 bits data. See Table III
for details.}
r4 = 0x00010000;  {16 bits, Normal Op., AM
                   disabled, Synchronizer
                   enabled}
dm(dds_para) = r4; {write data to parallel
                   assembly register}
r4 = 0x00000000;
dm(dds_cont) = r5; {No data written, data is
                   just transferred from
                   parallel assembly
                   register to the command
                   register}
r4 = 0x051E0000;  {1 MHz=051EB852, load high
                   word first}
dm(dds_para) = r4;
r4 = 0xB8520000;  {Now load low word}
dm(dds_para)=r4;
r4 = 0x80000000;  {Transfer data from the
                   parallel assembly
                   register to Freq0}
dm(dds_cont)=r4;
```

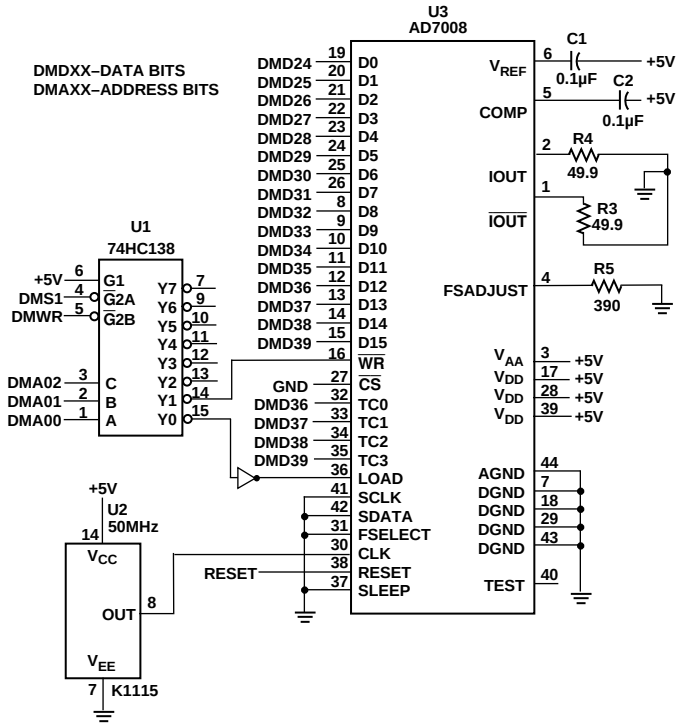


Figure 12. Parallel Interface to a 16- or 32-Bit DSP or Microprocessor

Local Oscillator

The AD7008 is well suited for applications such as local oscillators used in super-heterodyne receivers. Although the AD7008 can be used in a variety of receiver designs, one simple local os-

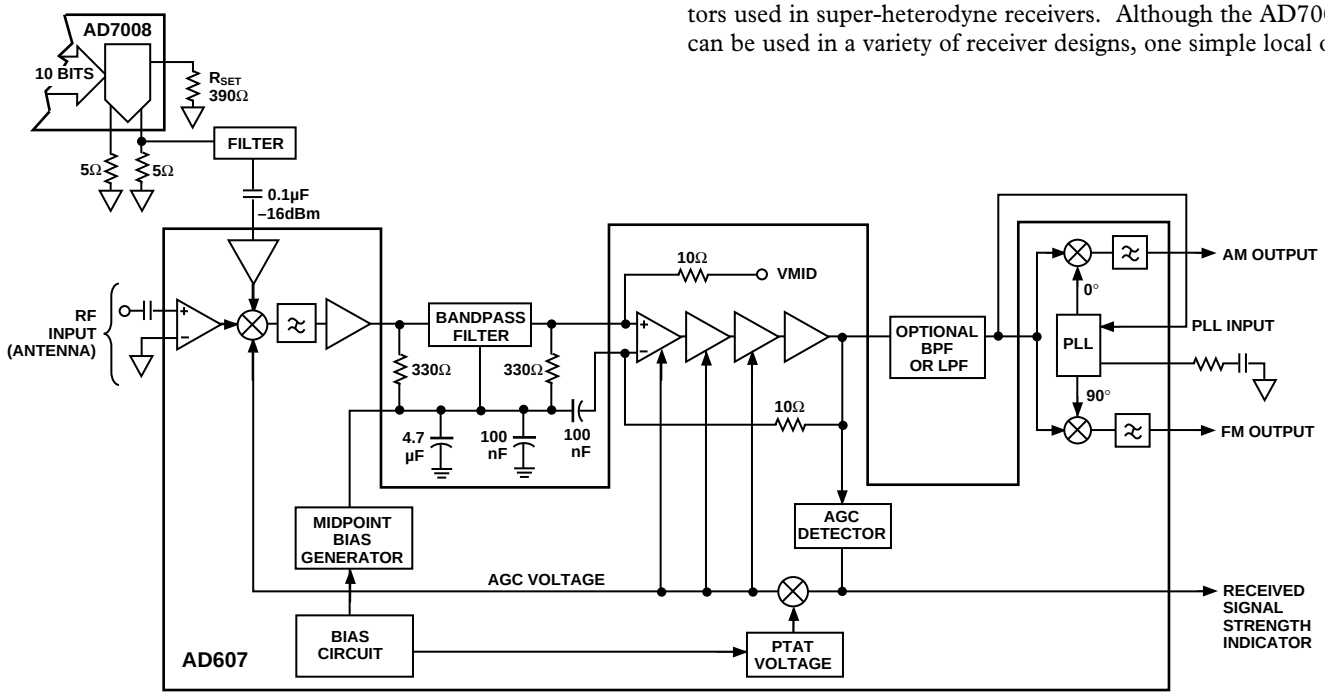


Figure 13. AD7008 and AD607 Receiver Circuit

cillator application is with the AD607 Monoceiver(tm). This unique two chip combination provides a complete receiver subsystem with digital frequency control, RSSI and demodulated outputs for AM, FM and complex I/Q (SSB or QAM). (See Figure 13.)

Direct Digital Modulator

In addition to the basic DDS function provided by the AD7008, the device also offers several modulation capabilities useful in a wide variety of application. The simplest modulation scheme is frequency shift keying or FSK. In this application, each of the two frequency registers is loaded with a different value, one representing the space frequency and the other the mark frequency. The digital data stream is fed to the FSELECT pin causing the AD7008 to modulate the carrier frequency between the two values.

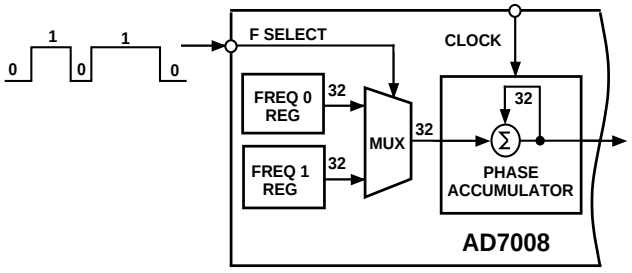


Figure 14. FSK Modulator

The AD7008 has three registers that can be used for modulation. Besides the example of frequency modulation shown above, the frequency registers can be updated dynamically as can the phase register and the IQMOD register. These can be modulated at rates up to 16.5 MHz. The example shown below along with code fragment shows how to implement the AD7008 in an amplitude modulation scheme. Other modulation schemes can be implemented in a similar fashion.

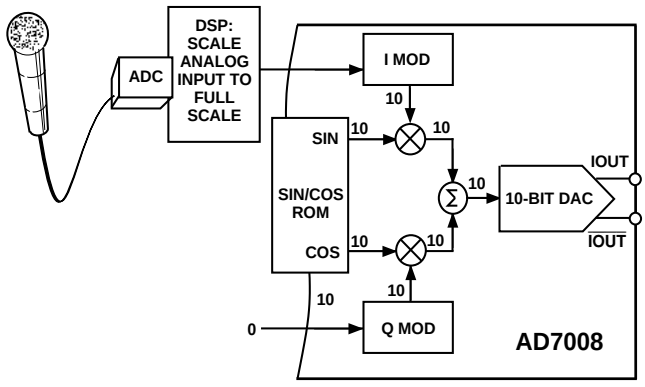


Figure 15. Amplitude Modulation

```
{_____IRQ3 Interrupt Vector_____}
{in_audio is a port used to sample the audio
signal.  This signal is assumed to be twos
complement.  This interrupt should be serviced
at an audio sample rate.  This routine assumes
that the AD7008 has been set up with the Ampli-
tude Modulation Enabled.}
irq3_asserted:
{Get audio sample}
  r6=dm(in_audio);
{This section converts the twos complement au-
dio into offset binary scaled for modulating
the AD7008.  If twos complement is used, the
modulation scheme will instead be double side-
band, suppressed carrier.}
  r5 = 0x80000000;
  r6 = r6 xor r5;
  r6 = lshift r6 by -1;
  r6 = r6 xor r5;
  r4 = lshift r6 by -6;
{Load parallel assembly register with modula-
tion data.  Q portion set to midscale, I
portion with scaled data}
  r5 = 0x00000004;
  dm(dds_para) = r5;
  dm(dds_para) = r4;
{Transfer parallel assembly register to IQMOD
register}
  r4 = 0xb0000000;
  dm(dds_cont) = r4;
  rti;
```

Many applications require precise control of the output amplitude, such as in local oscillators, signal generators and modulators. There are several methods to control signal amplitude. The most direct is to program the amplitude using the IQMOD register on the AD7008. Other methods include selecting the load resistor value or changing the value of R_{SET}. Another option is to place a voltage out DAC on the ground side of R_{SET} as in Figure 16. This allows easy control of the output amplitude without affecting other functions of the AD7008. Any combination of these techniques may be used as long as the full-scale voltage developed across the load does not exceed 1 volt.

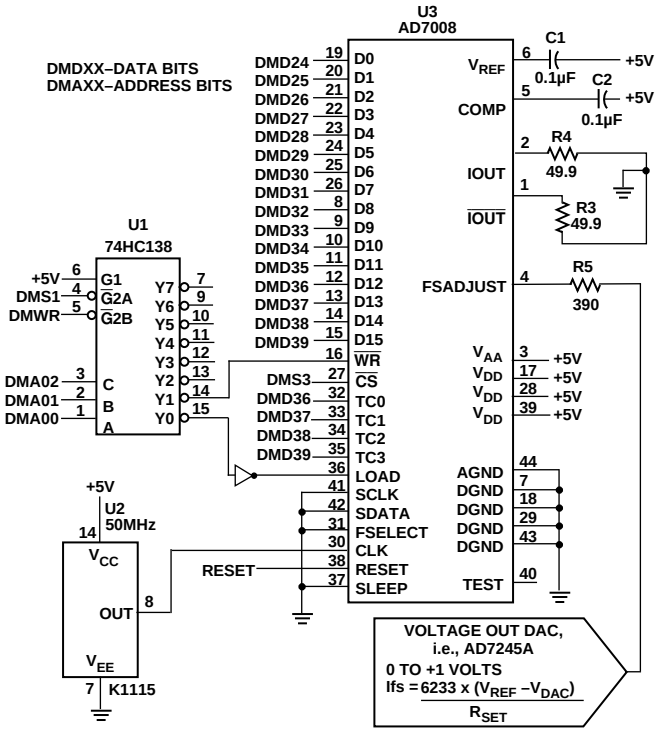


Figure 16. External Gain Adjustment

AD7008–Typical Performance Characteristics

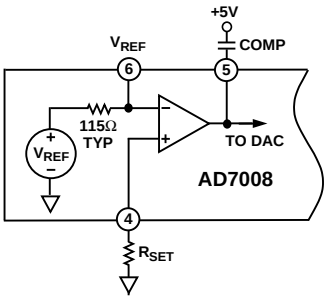


Figure 17. Equivalent Reference Circuit

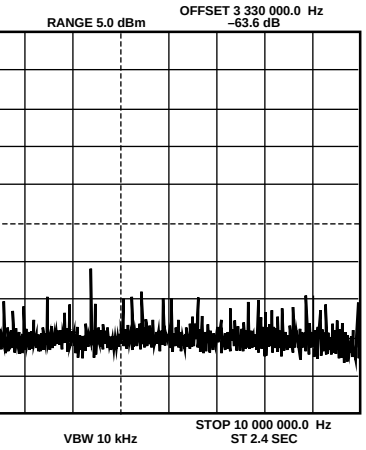


Figure 18. f_{CLK} = 20 MHz, f_{OUT} = 1.1 MHz

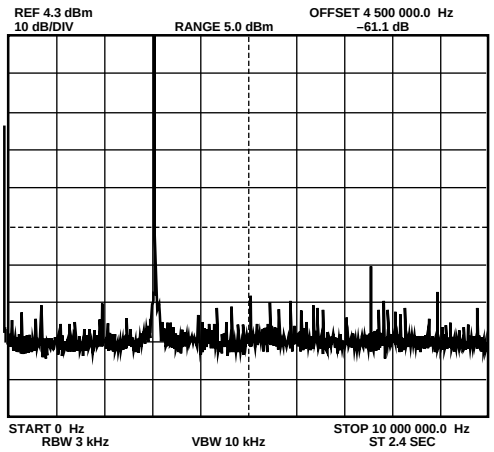


Figure 19. f_{CLK} = 20 MHz, f_{OUT} = 3.1 MHz

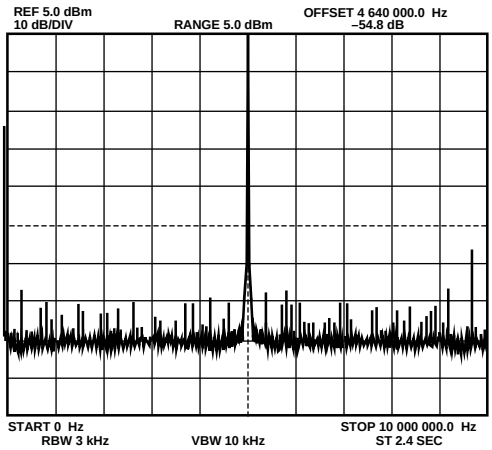


Figure 20. f_{CLK} = 20 MHz, f_{OUT} = 5.1 MHz

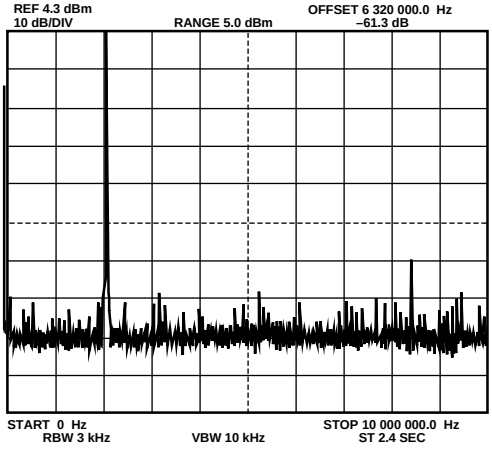


Figure 21. f_{CLK} = 20 MHz, f_{OUT} = 2.1 MHz

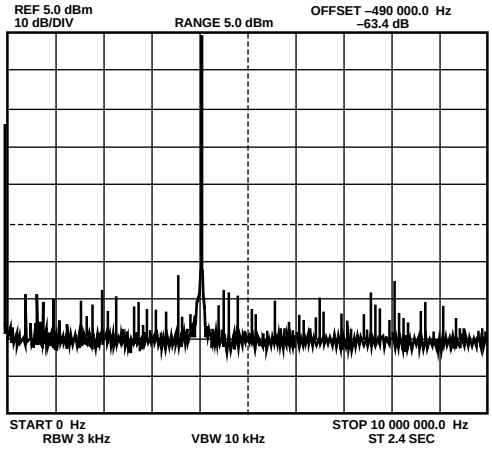


Figure 22. f_{CLK} = 20 MHz, f_{OUT} = 4.1 MHz

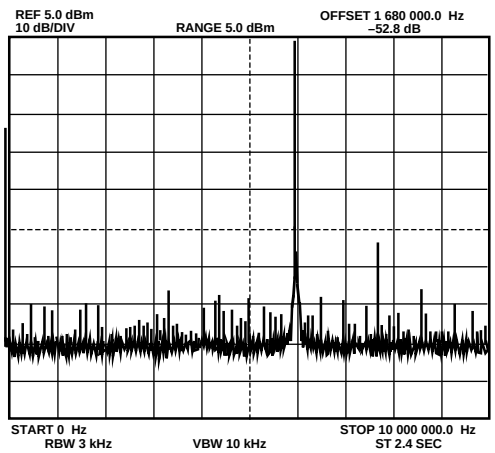


Figure 23. f_{CLK} = 20 MHz, f_{OUT} = 6.1 MHz

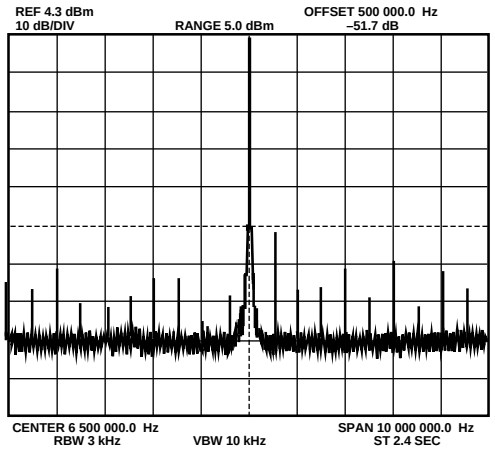


Figure 24. f_{CLK} = 20 MHz, f_{OUT} = 6.5 MHz

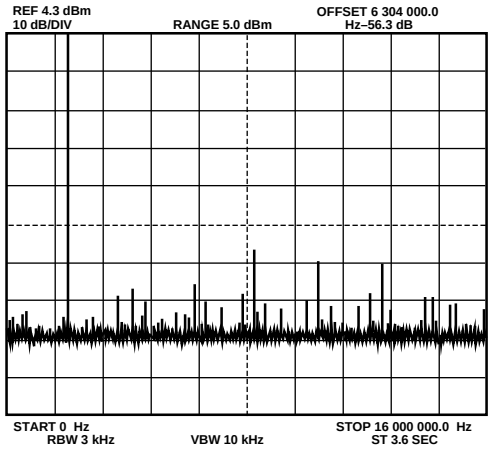


Figure 25. f_{CLK} = 50 MHz, f_{OUT} = 2.1 MHz

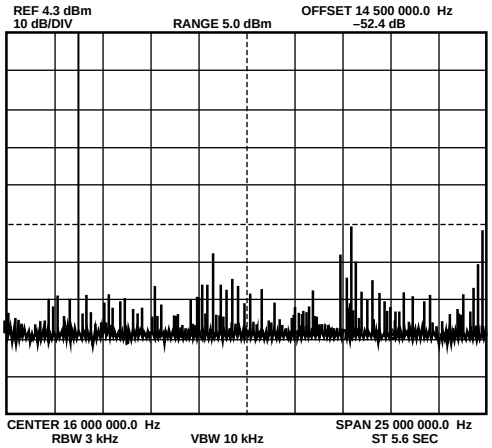


Figure 26. f_{CLK} = 50 MHz, f_{OUT} = 7.1 MHz

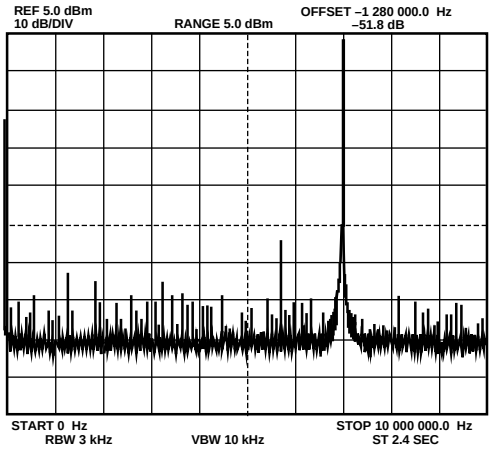


Figure 27. f_{CLK} = 20 MHz, f_{OUT} = 7.1 MHz

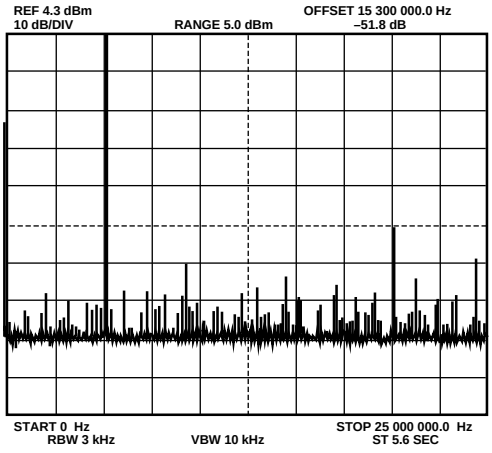


Figure 28. f_{CLK} = 50 MHz, f_{OUT} = 5.1 MHz

AD7008–Typical Performance Characteristics

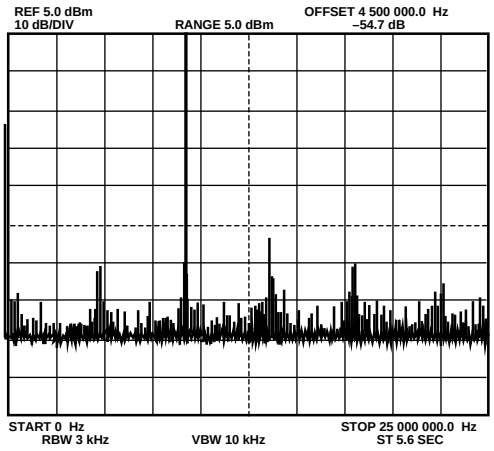


Figure 29. f_{CLK} = 50 MHz, f_{OUT} = 9.1 MHz

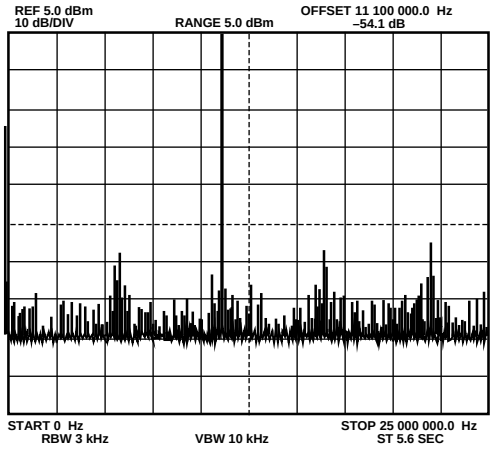


Figure 30. f_{CLK} = 50 MHz, f_{OUT} = 11.1 MHz

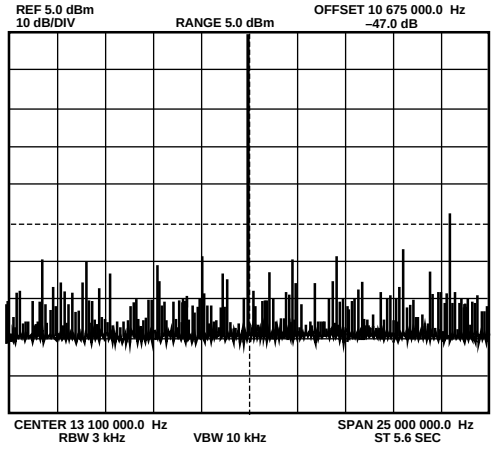


Figure 31. f_{CLK} = 50 MHz, f_{OUT} = 13.1 MHz

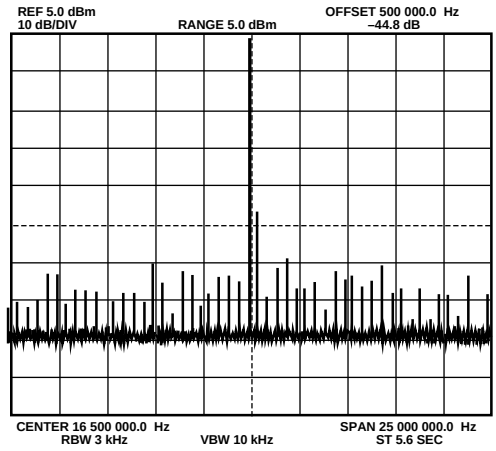


Figure 32. f_{CLK} = 50 MHz, f_{OUT} = 16.5 MHz

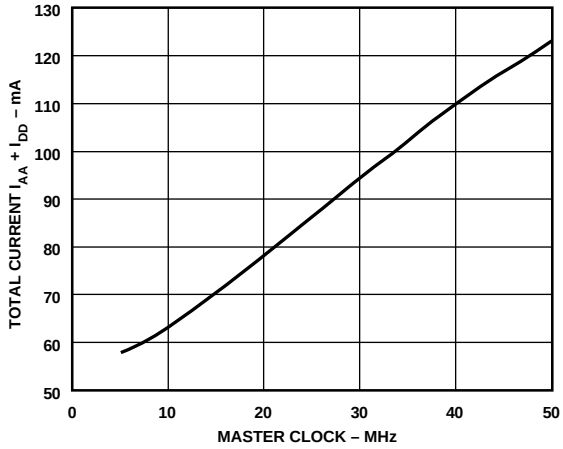


Figure 33. Typical Current Consumption vs. Frequency

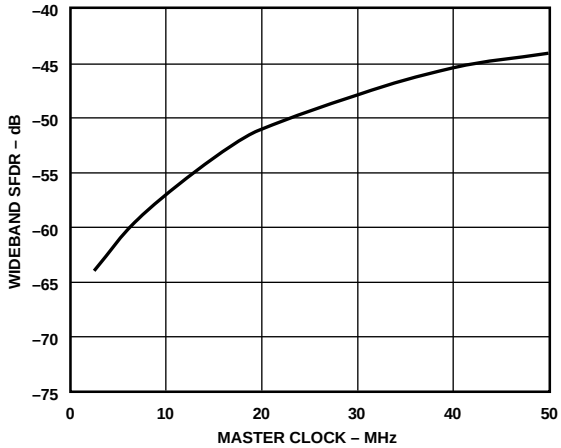


Figure 34. Typical Plot of SFDR vs. Master Clock Frequency When f_{OUT} = 1/3f_{CLK}, Frequency Word = 5671C71C Hex

AD7008/PCB DDS EVALUATION BOARD

The AD7008/PCB DDS Evaluation Board allows designers to evaluate the high performance AD7008 DDS Modulator with a minimum amount of effort.

To prove this DDS will meet the user's waveform synthesis requirements, the only things needed are the AD7008/PCB DDS Evaluation Board, +5 V power supply, an IBM-compatible PC, and a spectrum analyzer. The evaluation setup is shown below.

The DDS evaluation kit includes a populated, tested AD7008/PCB board; software which controls the AD7008 through the parallel printer port in a DOS or Windows environment and an AD7008P.

The AD7008 direct digital synthesis chip is a numerically controlled oscillator employing a 32-bit phase accumulator, sine and cosine look-up tables, and a l0-bit D/A converter integrated on a single CMOS chip. Modulation capabilities are provided for phase modulation, frequency modulation, and both in-phase and quadrature amplitude modulation suitable for SSB generation.

Clock rates up to 20 MHz and 50 MHz are supported. Frequency accuracy can be controlled to one part in four billion.

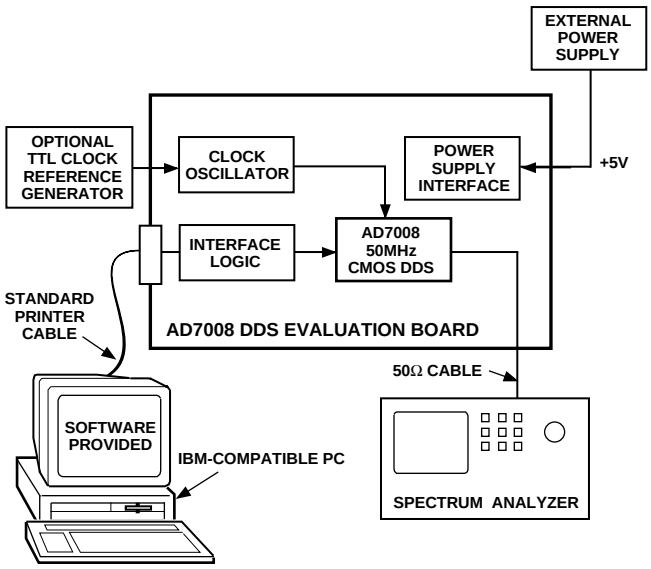


Figure 35. AD7008 DDS Evaluation Board Setup

Table IV. AD7008/PCB Typical Electrical Characteristics (Nominal power supplies, CLK = 50 MHz)

Characteristics	Typical Value	Units
+5.0 V Supply Current	125	mA
AD7008 Output Voltage (Terminated into 50 Ω Externally)	0 to +1.0	V
CMOS clock input HIGH	4.1 to 5	V
CMOS clock input LOW	0.0 to 0.5	V

USING THE AD7008/PCB DDS EVALUATION BOARD

The AD7008/PCB evaluation kit is a test system designed to simplify the evaluation of the AD7008 50 MHz Direct Digital Synthesizer. Provisions to control the AD7008 from the printer port of an IBM-compatible PC are included, along with the necessary software. This data sheet provides information on operating the evaluation board; additional details are available from the ADI technical assistance line 1-800-ANALOGD.

Prototyping Area

An area near one edge of the board is intentionally left void of components to allow the user to add additional circuits to the evaluation test set. Users may want to build custom analog filters for the outputs, or add buffers and operational amplifiers used in the final applications.

XO vs. External Clock

The reference clock of the AD7008/PCB is normally provided by a 50 MHz CMOS oscillator. This oscillator can be removed and an external CMOS clock connected to CLOCK. If an external clock is used, a 50 Ω resistor R6 should be installed.

Power Supply

Power for the AD7008/PCB must be provided externally through the pin connections, as described in the Inputs/Outputs. The power leads should be twisted to reduce ground loops.

AD7008/PCB BILL OF MATERIAL

Quantity	Reference	Description
1	C1	Tag – Tant Cap, 10 µF, 35 V, 20%
8	C2–C9	Cer Chip Cap, 0.1 µF, Murata Grm42
6	CLOCK, FSEL I_{OUT}, I_{OUTN} SCLK, SDATA	SMB – Submin Snap-on (Male) PCB MT Plug
1	FSADJ	RN55 – Res Met Film, 392
1	LK1	HDR SIP 3-Pin Male
1		Shunt 530153-2
1	P1	36-Pin D Conn Rt Ang Pcmt Fem AMP
1	P2	PC Voltage Ter Blk w/Screws Augat RDI
3	R1–R3	RN55 – Res Met Film, 10k
2	R4, R5	RN55 – Res Met Film, 49.9
1	RZ1	10P Bussed Res Ntwk, 10k CSC10A01103G
1	RZ2	6P Bussed Res Ntwk, 4.7k CSC06A01472G
1	U1	AD7008 JP50 CMOS DDS Modulator
1	U2	74HC74 – Dual D-type Pos-Ed-Trigd Flip-Flop
1	V_{REF}	Pin Terminal, Testpoint
1	XTAL	OSC XTAL, Fox F1100H 50 MHz
1		Socket, Methode 213-044-501
4		Support, Nylon
1		PCB, 48295(-)
26		Pin Sockets, Closed End

Controlling the AD7008/PCB

The AD7008/PCB is designed to allow control (frequency specification, reset, etc.) through the parallel printer port of a standard IBM-compatible PC. The user simply disconnects the printer cable from the printer and inserts it into edge connector P1 of the evaluation board.

The printer port provides information to the AD7008/PCB through eight data lines and four control lines. Control signals are latched on the AD7008/PCB to prevent problems with long printer cables.

A 3.5" floppy disk containing software to control the AD7008 is provided with the AD7008/PCB. This software was developed using C. The C source code is provided in a file named A:\AD7008.C, which the user may view, run, or modify.

An executable version of this software is also provided, and can be executed from DOS by typing "A:\AD7008." The software prompts the user to provide the necessary information needed by the program. Additional information is included in a test file named A:\readme.txt.

A windows 3.1 executable called WIN7008 is also included.

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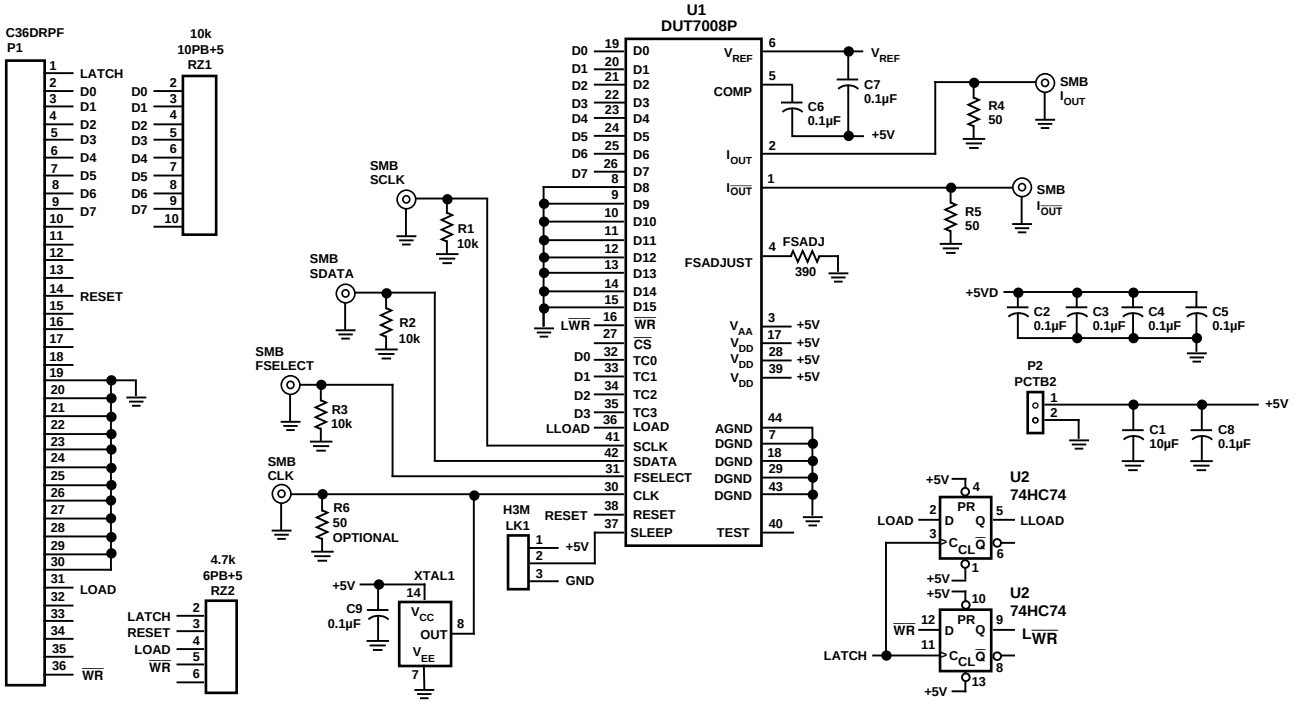


Figure 36.

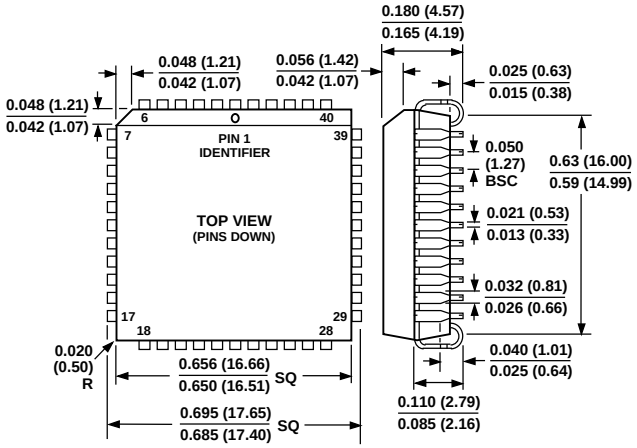
INPUTS/OUTPUTS

Name	Description
P1	36-pin edge connector to connect to parallel port of PC.
CLOCK	CMOS input for clock R6 provides termination.
FSEL	CMOS input to select between Freq 0 and Freq 1. Low selects Freq 0.
SDATA	CMOS input for serial input pin.
SCLK	CMOS input for clocking in SDATA.
I_{OUT}	Analog output.
$I_{OUT}N$	Complementary analog output.
V_{REF}	Test point for V_{REF} pin.
P2	+5 V and ground power connection.
LK1	External sleep command input.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

44-Pin PLCC (P-44A)



PRINTED IN U.S.A.

Стандарт Электрон Связь

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