# High Efficiency Single Synchronous Buck PWM Controller

## General Description

The RT8240A/B/C PWM controller provides high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high voltage batteries to generate low voltage CPU core, I/O, and chipset RAM supplies in notebook computers.

The RT8240A/B/C supports on chip voltage programming function between 1V and 1.05V by controlling G0 digital inputs.

The constant on-time PWM control scheme handles wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients while maintaining a relatively constant switching frequency.

The RT8240A/B/C achieves high efficiency at a reduced cost by eliminating the current sense resistor found in traditional current mode PWMs. Efficiency is further enhanced by its ability to drive very large synchronous rectifier MOSFETs and enter diode emulation mode at light load condition. The buck conversion allows this device to directly step down high voltage batteries at the highest possible efficiency. The RT8240A/B/C is intended for CPU core, chipset, DRAM, or other low voltage supplies as low as 1V. The RT8240A/B/C is available in a WQFN-12L 2x2 package.

## Ordering Information

RT8240A/B/C□□

- Package Type
  QW : WQFN-12L 2x2 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
  Z : ECO (Ecological Element with Halogen Free and Pb free)
- Switching Frequency Operation
  A : 300kHz
  B : 400kHz
  C : 500kHz

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

## Features

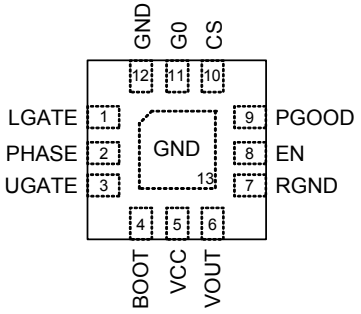
- **Built-in 0.5% Reference Voltage**
- **1 Bit Programmable Output Voltage Between 1V and 1.05V with Integrated Transition Support**
- **Output Voltage Range from 1V to 3.6V**
- **Quick Load-Step Response within 100ns**
- **Support Pure MLCC Output Capacitor**
- **4700ppm/°C Programmable Current Limit by Low Side $R_{DS(ON)}$ Sensing**
- **4.5V to 26V Battery Input Range**
- **Internal Ramp Current Limit Soft-Start Control**
- **Drives Large Synchronous Rectifier FETs**
- **Integrated Boost Switch**
- **Over/Under Voltage Protection**
- **Thermal Shutdown**
- **Power Good Indicator**
- **RoHS Compliant and Halogen Free**

## Applications

- Notebook Computers
- CPU/GPU Core Supply
- Chipset/RAM Supply
- Generic DC/DC Power Regulator

## Pin Configurations

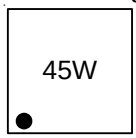
(TOP VIEW)




WQFN-12L 2x2

## Marking Information

RT8240AGQW




45: Product Code
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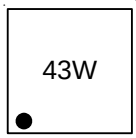
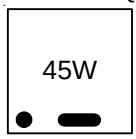
RT8240CGQW




43 : Product Code
YMDNN : Date Code

RT8240AZQW

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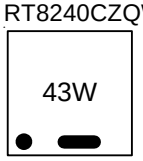
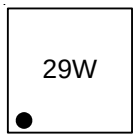
YMDNN : Date Code

RT8240CZQW




43 : Product Code
YMDNN : Date Code

RT8240BGQW

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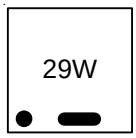
RT8240BZQW

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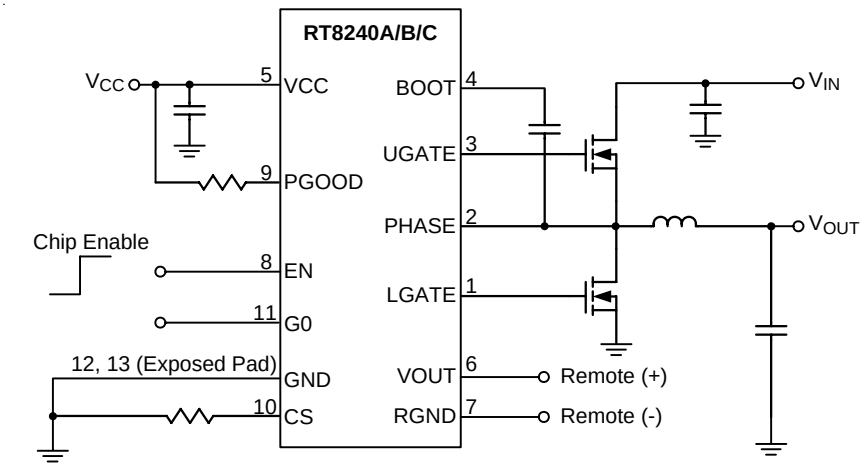
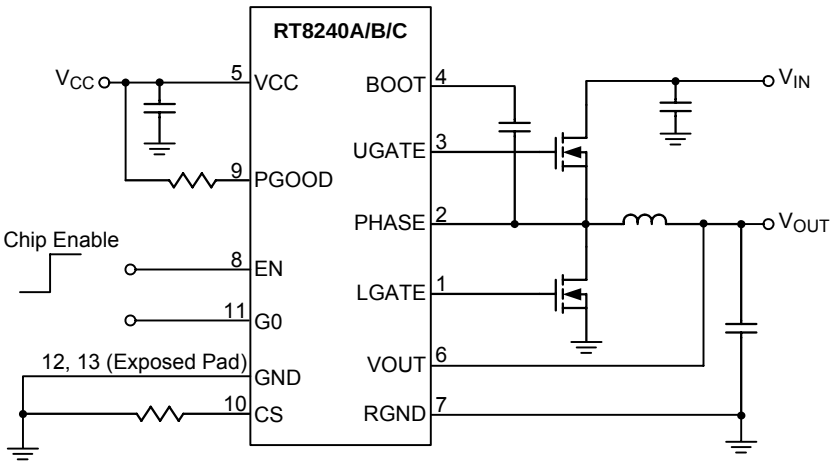
## Typical Application Circuit

### (1) Remote Sense



**(2) Local Sense**



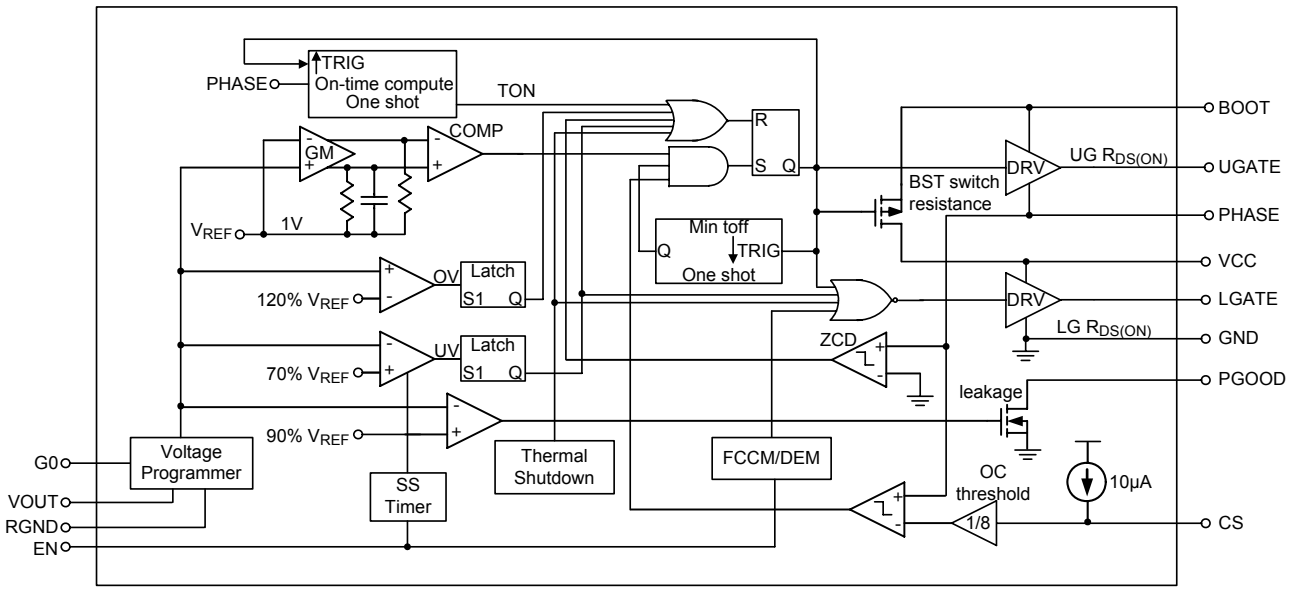

**VID Table**

| G0 | $V_{OUT}$ |
|---|---|
| 0 | 1V |
| 1 | 1.05V |

## Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 1 | LGATE | Gate Drive Output for Low Side External MOSFET. |
| 2 | PHASE | External Inductor Connection Pin for PWM Converter. It behaves as the current sense comparator input for low side MOSFET $R_{DS(ON)}$ sensing and reference voltage for on time generation. |
| 3 | UGATE | Gate Drive Output for the High Side External MOSFET. |
| 4 | BOOT | Supply Input for High Side Driver. Connect a capacitor to the floating node (PHASE) pin. |
| 5 | VCC | Control Voltage Input. Provides the power for the buck controller, the low side driver and the bootstrap circuit for high side driver. Bypass to GND with a 4.7μF ceramic capacitor. |
| 6 | VOUT | Output Voltage Feedback Input. Connect $V_{OUT}$ to converter output node. |
| 7 | RGND | Remote Voltage Sense Ground Pin. |
| 8 | EN | PWM Enable Pin. Pull low to GND to disable the PWM. |
| 9 | PGOOD | Open Drain Power Good Indicator. High impedance indicates power is good. |
| 10 | CS | Current Limit Threshold Setting Input. Connect a setting resistor to GND and the current limit threshold is equal to 1/8 of the voltage at this pin. |
| 11 | G0 | Input Pin for Programming the Output Voltage Between 1V and 1.05V. |
| 12, 13 (Exposed Pad) | GND | Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation. |

## Function Block Diagram



## Absolute Maximum Ratings (Note 1)

- VCC, VOUT, PGOOD, EN, CS, G0 to GND ---------- –0.3V to 6V
- RGND to GND ---------- –0.7V to 0.7V
- PHASE to GND
  - DC ---------- –0.3V to 32V
  - <20ns ---------- –8V to 38V
- BOOT to PHASE ---------- –0.3V to 6V
- UGATE to PHASE
  - DC ---------- –0.3V to 6V
  - <20ns ---------- –5V to 7.5V
- LGATE to GND
  - DC ---------- –0.3V to 6V
  - <20ns ---------- –2.5V to 7.5V
- Power Dissipation, $P_D$ @ $T_A$ = 25°C
  - WQFN-12L 2x2 ---------- 0.606W
- Package Thermal Resistance (Note 2)
  - WQFN-12L 2x2, $\theta_{JA}$ ---------- 165°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

## Recommended Operating Conditions (Note 4)

- Supply Input Voltage, $V_{IN}$ ---------- 4.5V to 26V
- Control Voltage, $V_{CC}$ ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

## Electrical Characteristics

($V_{CC}$ = 5V, $V_{IN}$ = 8V, $V_{EN}$ = 5V, $T_A$ = 25°C, unless otherwise specified)

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **PWM Controller** | | | | | | | |
| $V_{CC}$ Quiescent Supply Current | | $I_Q$ | FB forced above the regulation point, $V_{EN}$ = 5V | -- | 500 | 1250 | μA |
| $V_{CC}$ Shutdown Current | | $I_{SHDN}$ | $V_{CC}$ current, $V_{EN}$ = 0V | -- | -- | 1 | μA |
| CS Shutdown Current | | | CS pull to GND | -- | -- | 1 | μA |
| VOUT Error Comparator Threshold | | | $V_{CC}$ = 4.5 to 5.5V, DEM | –0.5 | 0 | 0.5 | % |
| VOUT Voltage Range | | $V_{OUT}$ | | 1 | -- | 3.6 | V |
| On-Time, Pulse Width | RT8240A | $t_{ON}$ | $f_{SW}$ = 300kHz, $V_{OUT}$ = 1.05V | 371 | 437 | 502 | ns |
| | RT8240B | | $f_{SW}$ = 400kHz, $V_{OUT}$ = 1.05V | 279 | 328 | 377 | |
| | RT8240C | | $f_{SW}$ = 500kHz, $V_{OUT}$ = 1.05V | -- | 262 | -- | |

*To be continued*

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Minimum Off-Time | | $t_{OFF}$ | | 250 | 400 | 550 | ns |
| **Current Sensing** | | | | | | | |
| CS Source Current | | $I_{CS}$ | CS to GND | 9 | 10 | 11 | μA |
| CS Source Current Temperature Coefficient | | | | -- | 4700 | -- | ppm/°C |
| Zero Crossing Threshold | | | | −10 | -- | 5 | mV |
| **Protection Function** | | | | | | | |
| Current Limit | | $I_{LIM}$ | GND − PHASE = $V_{CS}$ / 8 | −20 | 0 | 20 | mV |
| Negative Current Limit | | | PHASE − GND = $V_{CS}$ / 8 | -- | 3 | -- | mV |
| Output Under Voltage Protection Threshold | | $V_{UVP}$ | | 65 | 70 | 75 | % |
| Over Voltage Protection | | $V_{OVP}$ | With respect to error comparator threshold | 115 | 120 | 125 | % |
| OVP Fault Delay | | | VOUT forced above OVP threshold | -- | 5 | -- | μs |
| $V_{CC}$ Under Voltage Lockout (UVLO) Threshold | | $V_{UVLO}$ | Rising edge, PWM disabled below this level | 3.6 | 3.8 | 4 | V |
| $V_{CC}$ UVLO Hysteresis | | $\Delta V_{UVLO}$ | | -- | 100 | -- | mV |
| VOUT Soft-Start | | | From EN = high to $V_{OUT}$ = 95% | -- | 1300 | -- | μs |
| UV Blank Time | | | From EN signal going high | -- | 3 | -- | ms |
| Thermal Shutdown | | $T_{SD}$ | | -- | 150 | -- | °C |
| Thermal Shutdown Hysteresis | | $\Delta T_{SD}$ | | -- | 10 | -- | °C |
| **Driver On Resistance** | | | | | | | |
| UGATE Driver Source | | $R_{UGATEsr}$ | BOOT − PHASE forced to 5V | -- | 1.8 | 3.6 | Ω |
| UGATE Driver Sink | | $R_{UGATEsk}$ | BOOT − PHASE forced to 5V | -- | 1.2 | 2.4 | Ω |
| LGATE Driver Source | | $R_{LGATEsr}$ | LGATE, High State | -- | 1.8 | 3.6 | Ω |
| LGATE Driver Sink | | $R_{LGATEsk}$ | LGATE, Low State | -- | 0.67 | 1.34 | Ω |
| Dead Time | | | LGATE Rising ($V_{PHASE}$ = 1.5V) | -- | 30 | -- | ns |
| | | | UGATE Rising | -- | 30 | -- | |
| Internal Boost Charging Switch On Resistance | | | VCC to BOOT, 10mA | -- | -- | 80 | Ω |
| **EN Threshold** | | | | | | | |
| EN Input Threshold Voltage | Logic-High | | | 1.8 | -- | -- | V |
| | Logic-Low | | | -- | -- | 0.5 | |
| **Voltage Programming Input Threshold** | | | | | | | |
| G0 Input Threshold Voltage | Logic-High | | | 735 | -- | -- | mV |
| | Logic-Low | | | -- | -- | 315 | |
| **PGOOD (upper side threshold determined by OVP threshold)** | | | | | | | |
| Trip Threshold | | | Falling edge, measured at VOUT, with respect to reference, no load. | −19 | −15 | −11 | % |

*To be continued*

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Trip Hysteresis | | | -- | 3 | -- | % |
| Fault Propagation Delay | | Falling edge, VOUT forced below PGOOD trip threshold | -- | 2.5 | -- | μs |
| Output Low Voltage | | $I_{SINK}$ = 1mA | -- | -- | 0.4 | V |
| Leakage Current | | High state, forced to 5V | -- | -- | 1 | μA |

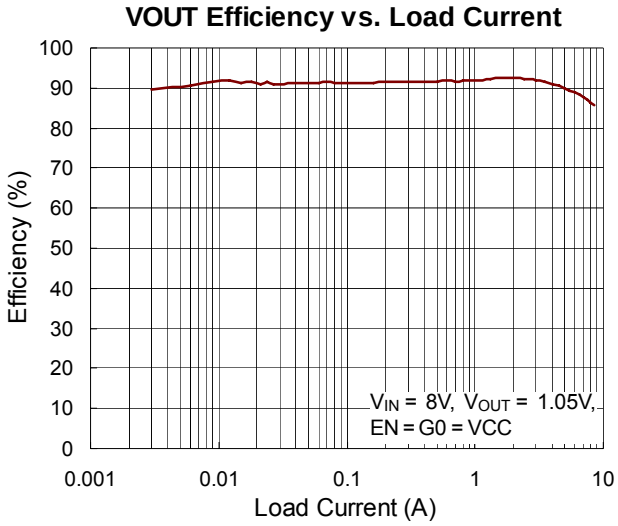
**Note 1.** Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

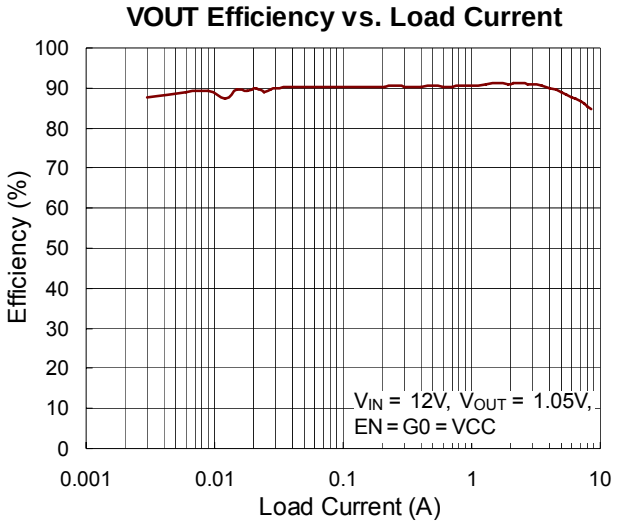
**Note 2.** $\theta_{JA}$ is measured in natural convection at $T_A$ = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

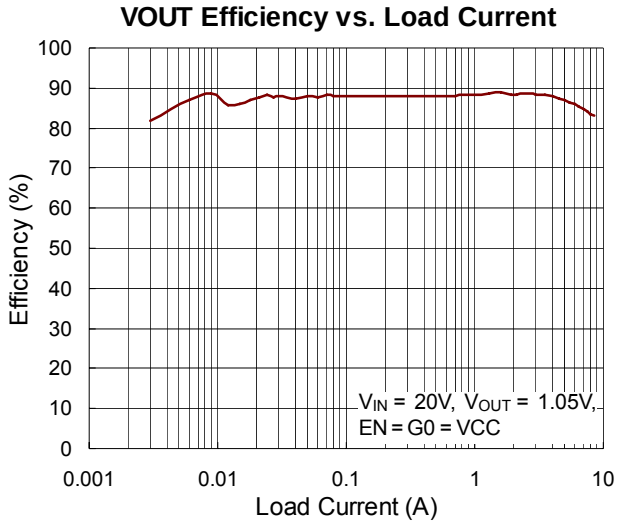
**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

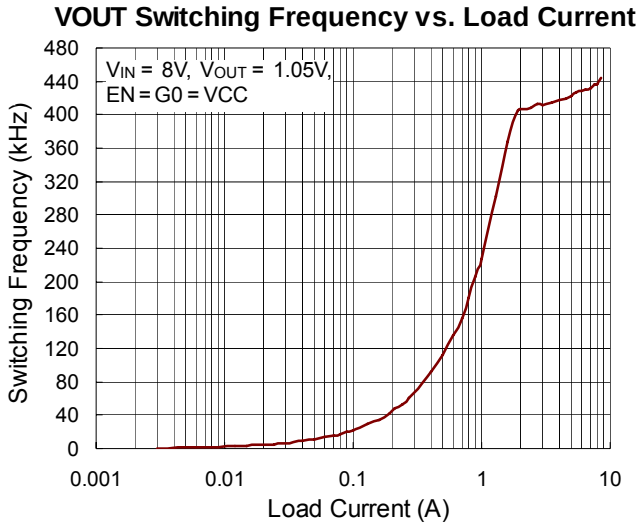
**Note 4.** The device is not guaranteed to function outside its operating conditions.

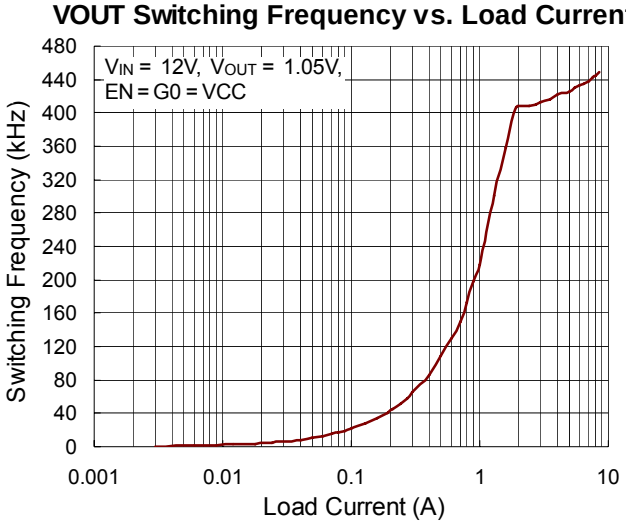
## Typical Operating Characteristics

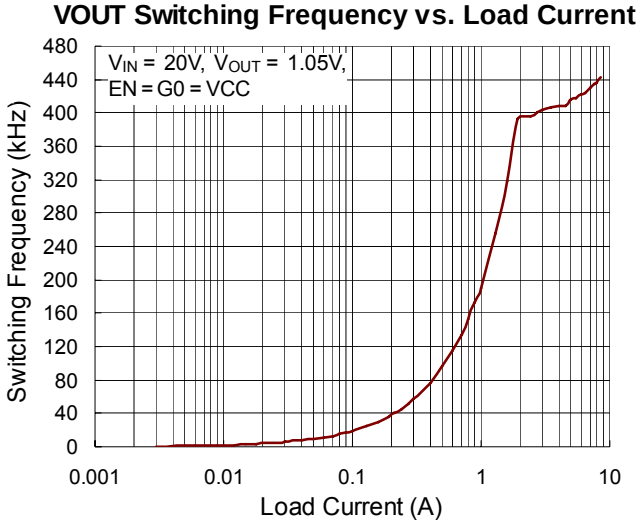


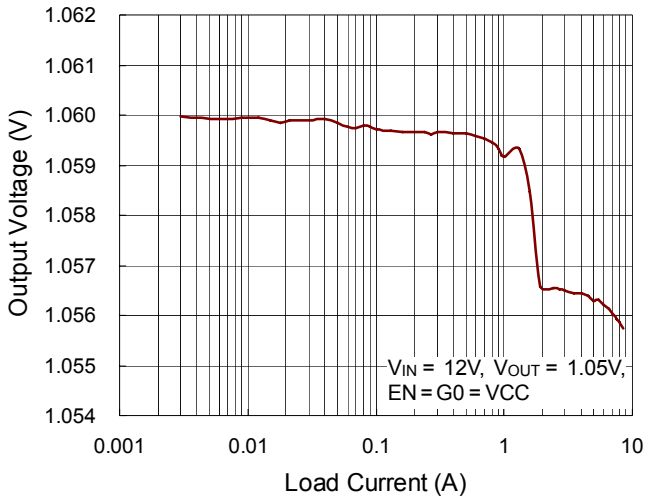



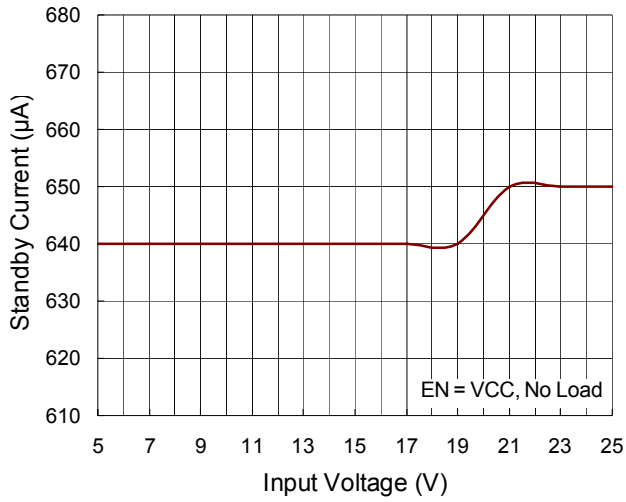



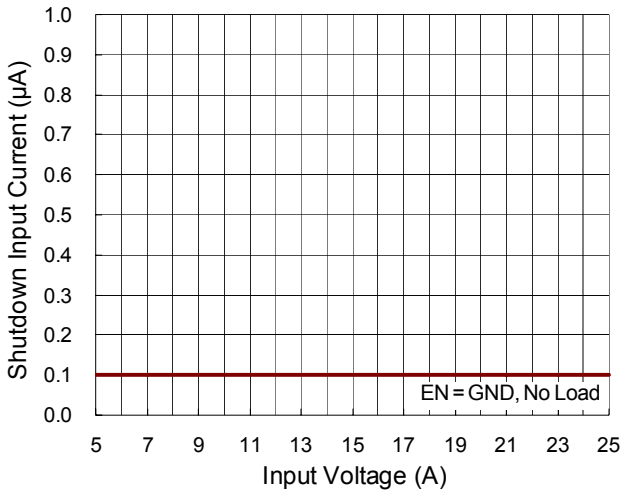
**VOUT Output Voltage vs. Load Current**



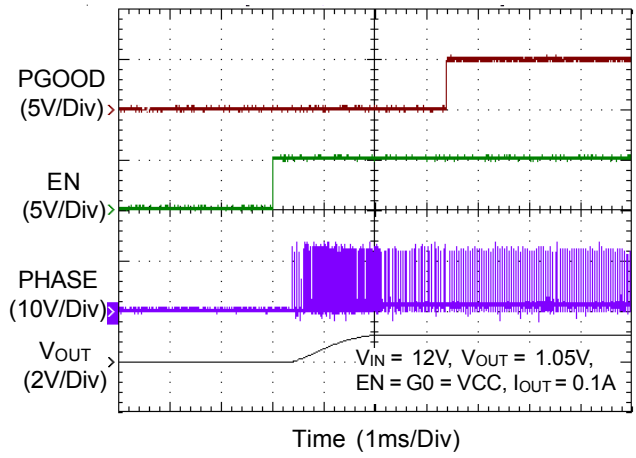

**Standby Current vs. Input Voltage**



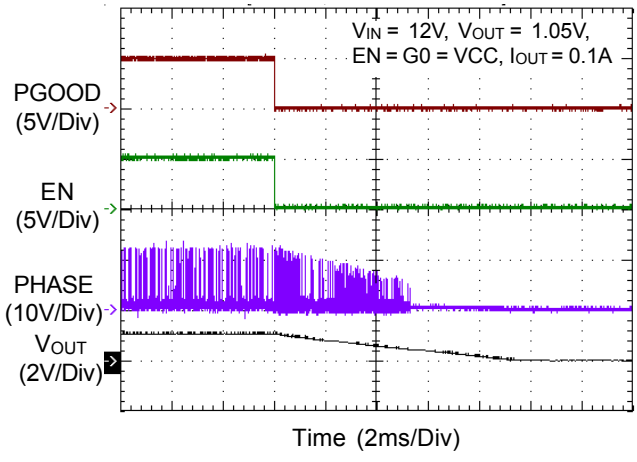

**Shutdown Input Current vs. Input Voltage**



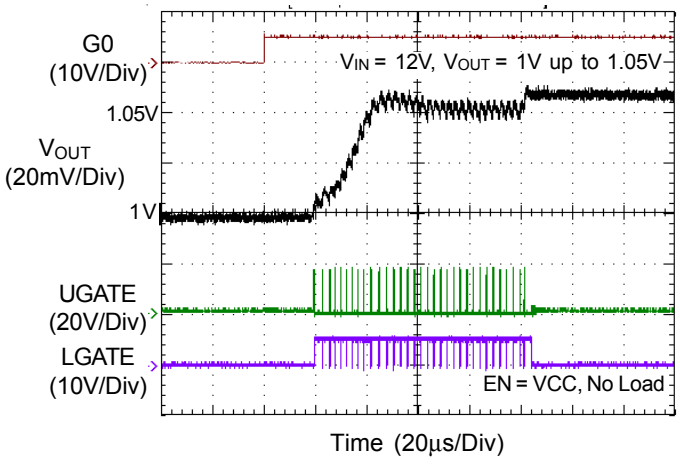

**Power On from EN**



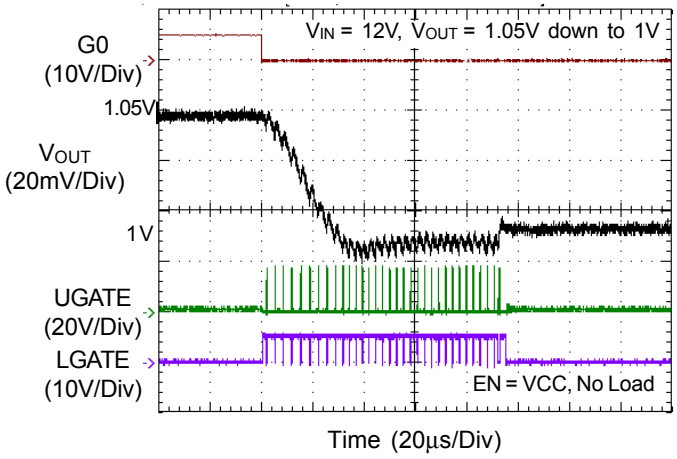

**Power Off from EN**



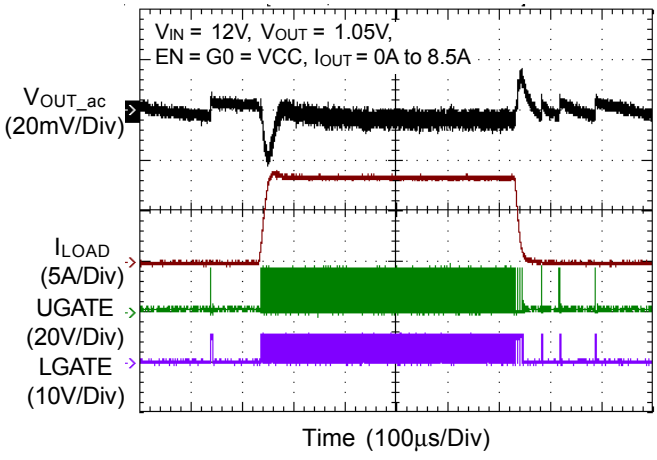

**Dynamic VID Up**



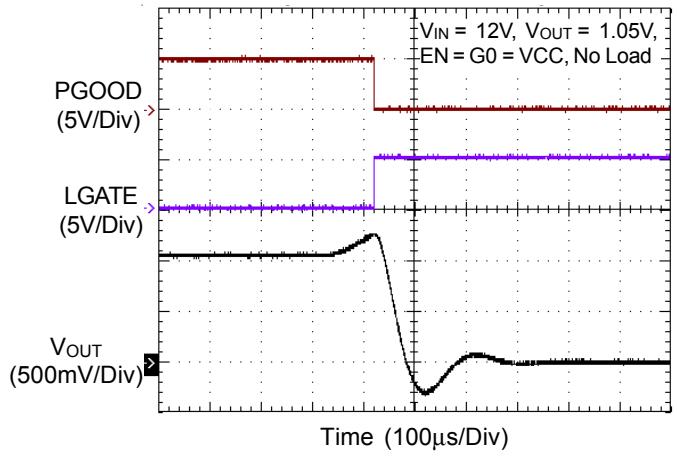
### Dynamic VID Down



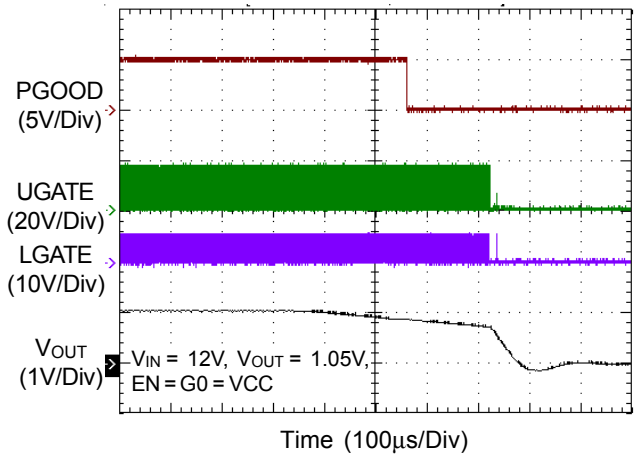

### VOUT DEM-Mode Load Transient Response




### OVP




### UVP



## Application Information

The RT8240A/B/C is a single, Mach Response™ PSR™ mode synchronous buck controller which supports chip voltage programming function between 1V and 1.05V by controlling the G0 digital input. The Richtek's PSR™ technology is specifically designed to support low ESR output capacitor system. The Richtek's Mach Response™ technology provides fast response to load steps. The topology circumvents the poor load transient timing problems of fixed-frequency current mode PWMs while avoiding the problems caused by widely varying switching frequency in conventional constant-on-time and constant-off-time PWM schemes. A special adaptive on-time control trade off the performance and efficiency over wide input voltage range. The PSR™ mode PWM modulator is specifically designed to have better noise immunity for such a single output application.

### PWM Operation

The Mach Response™ PSR™ mode controller internally provides a pseudo ramp signal, so the controller can support low ESR output capacitor to increase the flexibility of output capacitor selection. Refer to the function block diagram of RT8240A/B/C, the synchronous high side MOSFET will be turned on at the beginning of each cycle. After the internal one shot timer expires, the MOSFET will be turned off. The pulse width of this one shot is determined by the converter's input voltage and the output voltage to keep the frequency constant in a specific input voltage range. Another one shot sets a minimum off-time (400ns typ.). The on-time one shot will be triggered if the error comparator is high, the low side switch current is below the current limit threshold, and the minimum off-time one shot has timed out.

### On-Time Control

The on-time one shot comparator has two inputs. One input monitors the output voltage, while the other input samples the input voltage and converts it to a current. This input voltage proportional current is used to charge an internal on-time capacitor. The on-time is the time required for the voltage on this capacitor to charge from zero volts to VOUT, thereby making the on-time of the high side switch directly proportional to output voltage and inversely proportional to input voltage. The implementation results in a nearly constant switching frequency without the need a clock generator.

### Diode Emulation Mode

In diode-emulation mode, the RT8240A/B/C automatically reduces switching frequency at light load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly and without increasing $V_{OUT}$ ripples or load regulation. As the output current decreases from heavy load condition, the inductor current is also reduced, and eventually comes to the point that its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. By emulation the behavior of diodes, the low side MOSFET allows only partial of negative current when the inductor freewheeling current reach negative. As the load current is further decreased, it takes longer and longer to discharge the output capacitor to the level than requires the next "ON" cycle. The on-time is kept the same as that in the heavy load condition. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous condition. The transition load point to the light load operation can be calculated as follows (Figure 1) :

$$I_{LOAD} \approx \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$

where $t_{ON}$ is the on-time.

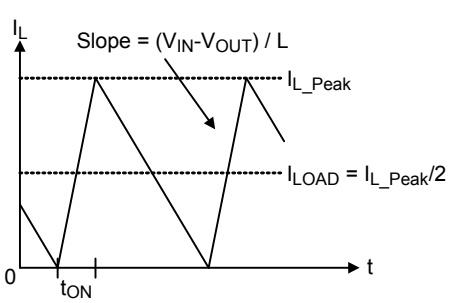



Figure 1. Boundary Condition of CCM/DCM

The switching waveforms may appear noisy and asynchronous when light loading causes diode emulation operation, but this is a normal operating condition that results in high light load efficiency. Trade-offs in DEM noise vs. light load efficiency is made by varying the inductor

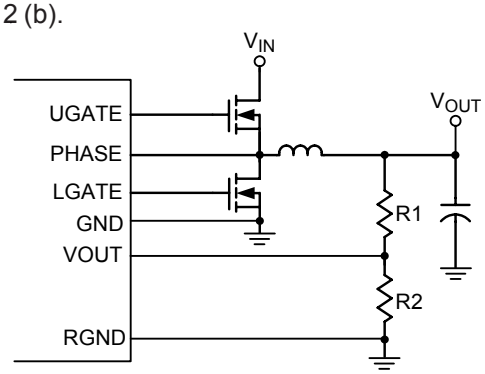
value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. The disadvantages for using higher inductor values include larger physical size and degrade load transient response (especially at low input voltage levels).

### Output Voltage Setting

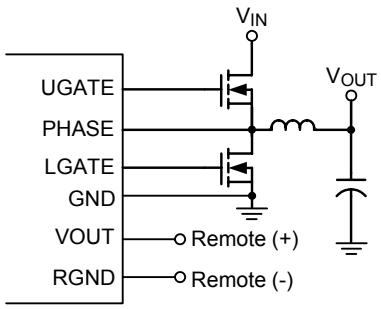
The RT8240A/B/C output voltage can be adjusted from 1V to 3.6V by setting the feedback resistor R1 and R2, see Figure 2 (a). With G0 in low state, the $V_{OUT}$ is at the lowest value (1V). Choose R2 to be approximately 10kΩ, and solve for R1 using the below equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$ where $V_{REF}$ is 1V typically.

The RT8240A/B/C output voltage can also set by differential, remote sense inputs to eliminate the effects of voltage drops along PC board traces. Connect to VOUT to Remote (+) and connect to RGND to Remote (–), see Figure 2 (b).




(a) Resistor Divider




(b) Remote sense

Figure 2. Setting $V_{OUT}$

### Output Voltage Transition Control

The RT8240A/B/C provides one digital input G0 to allow selection among two output voltages. The output voltage is regulated by comparing the VOUT pin to the internal 1V reference. The G0 digital input control the gate of internal MOSFET whose drain is connected to the bottom resistor of the internal resistor divider (Figure 3). A logic high signal on G0 will be selected to the internal resistor divider.

When the G0 input changes state, the change quickly causes three actions :

- Change from uni-feedback to internal resistor divider.
- The PGOOD output is temporarily latched into its present state. This prevents chattering or false tripping while $V_{OUT}$ moves to the new level.
- When G0 changes state whether DEM is set or not, then enter the PWM mode and count 32 clock cycles. For the duration of 32 clock cycles, the RT8240A/B/C will keep to monitor the UVP and OVP function. This behavior allows the output to slew down to the new level with tripping the OVP or UVP function when the G0 change causes a rapid change at VOUT pin.

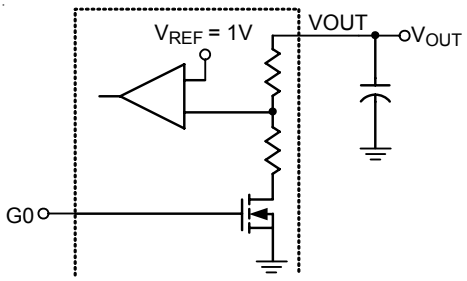



Figure 3. Output Voltage Selection by G0 Input

### Output Voltage Transition Operation

The digital input control pin G0 allows $V_{OUT}$ to transition to both higher and lower values. For a down transition, the rapid change G0 from high to low suddenly will cause $V_{OUT}$ to go above 1V. At this time, the LGATE will drive high to turn on the low side MOSFET and draw current from the output capacitor via the inductor. The LGATE will remain on until $V_{OUT}$ falls to 1V, at which point a normal UGATE switching cycle begins, as shown in Figure 4. For a down transition, the low side MOSFET stays on before $V_{OUT}$ reaches to 1V, thus the negative inductor current will be increased. If the negative current too large to trigger the negative current limit, the low side MOSFET is turned off which can avoid too much negative current to damage component. Refer to the Negative Current Limit section for a full description.

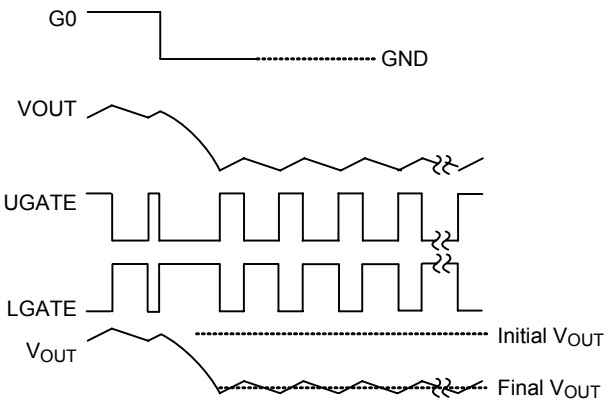



Figure 4. Output Voltage Down Transition

For an up transition (from lower to higher $V_{OUT}$) as shown in Figure 5, the G0 change from low to high and causes $V_{OUT}$ to drop below 1V. This quickly trips the comparator regardless of whether DEM is active or not, generating an UGATE on-time and a subsequent LGATE will be turned on. At the end of the minimum off-time (400ns), if $V_{OUT}$ is still below 1V then another UGATE on-time is started. This sequence continues until the VOUT pin exceeds 1V.

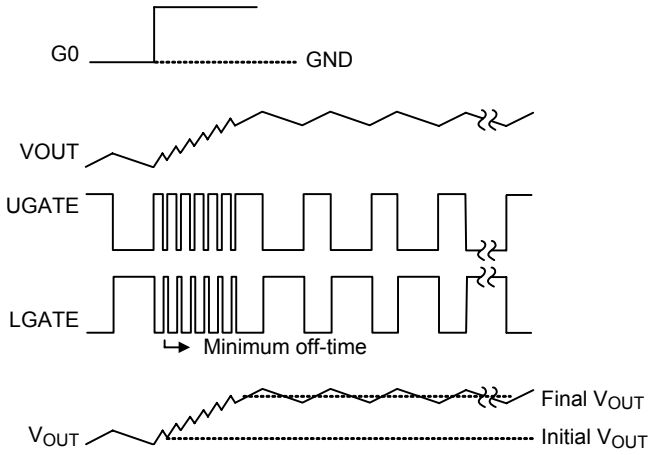



Figure 5. Output Voltage Up Transition

If the $V_{OUT}$ change is significant, there can be several consecutive cycle of UGATE on-time followed by minimum LGATE time. This can cause a rapid increase in inductor current : typically it only takes a few switching cycles for inductor current to rise up to the current limit. At some point the $V_{OUT}$ will rise up to 1V and the UGATE pulses will cease, but the inductor's $LI^2$ energy must then flow into the output capacitor. This can create a significant overshoot, as shown in Figure 6.

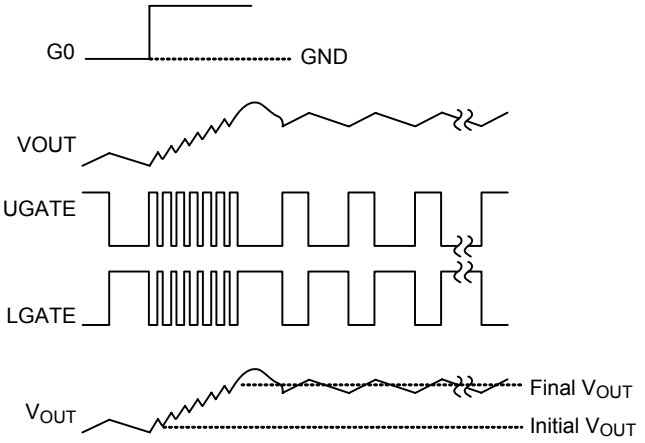



Figure 6. Output Voltage Up Transition with Overshooting

The overshooting can be approximated by the following equation, where $I_{CL}$ is the current limit, $V_{FINAL}$ is the desired set point for the final voltage, L is in μH and $C_{OUT}$ is in μF :

$$V_{MAX} = \sqrt{\left(\frac{I_{CL}^2 \times L}{C_{OUT}}\right) + V_{FINAL}^2}$$

### Current Limit Setting (CS)

The RT8240A/B/C provides cycle-by-cycle current limiting control. The current limit circuit employs a unique "Valley" current sensing algorithm. If the magnitude of the current sense signal at PHASE is above the current limit threshold, the PWM is not allowed to initiate a new cycle (Figure 7). The actual peak current is greater than the current limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current limit characteristic and maximum load capability are a function of the sense resistance, inductor value, and battery and output voltage.

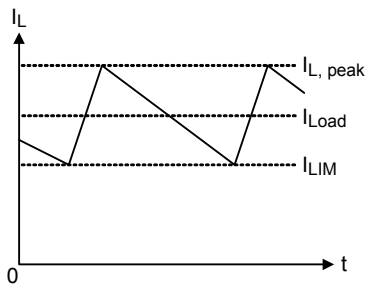



Figure 7. "Valley" Current Limit

The RT8240A/B/C uses the on resistance of the synchronous rectifier as the current sense element and supports temperature compensated MOSFET $R_{DS(ON)}$ sensing The $R_{ILIM}$ setting resistor between CS pin and GND sets the current limit threshold. The CS pin sources $I_{CS}$ current, which is 10μA typically at room temperature and this current has 4700ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(ON)}$. When the voltage drop across low side MOSFET equals the voltage across the $R_{ILIM}$ setting resistor, positive current limit will activate. The high side MOSFET will not be turned on until the voltage drop across the MOSFET falls below the current limit threshold.

Choose a current limit setting resistor by following equation :

$R_{ILIM} = (I_{ILIM} \times R_{DS(ON)}) \times 8 / I_{CS}$

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current sense signal seen by PHASE and GND.

### Negative Over Current Limit (CCM Only)

The RT8240A/B/C also supports cycle-by-cycle negative over current limiting in CCM Mode only. The over current limit is set to be negative but is the same absolute value as the positive over current limit. If output voltage continues to rising, the low side MOSEFT stays on, thus inductor current is reduced and reverses direction after it reaches zero. When there is too much negative current in the inductor, the low side MOSFET is turned off and the current flows to VIN through the body diode of the high side MOSFET. Because this protection limits current to discharge the output capacitor, output voltage tends to rise, eventually hitting the over voltage protection threshold and shutdown. If the device hits the negative over current threshold again before output voltage is discharged to the target level, the low side MOSFET is turned off and process repeats. It ensures maximum allowable discharge capability when output voltage continues to rise. On the other hand, if the output is discharged to the target level before negative current threshold is reached, the low side MOSFET is turned off, the high side MOSFET is then turned on, and the device resumes normal operation.

### MOSFET Gate Driver (UGATE, LGATE)

The high side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET (s). When configured as a floating driver, 5V bias voltage is delivered from VCC supply. The average drive current is proportional to the gate charge at $V_{GS}$ = 5V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between BOOT and PHASE pins. A dead time to prevent shoot through is internally generated between high side MOSFET off to low side MOSFET on, and low side MOSFET off to high side MOSFET on. The low side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET (s). The internal pull-down transistor that drives LGATE low is robust, with a 0.67Ω typical on resistance. A 5V bias voltage is delivered form VCC supply. The instantaneous drive current is supplied by the flying capacitor between VCC and GND.

For high current applications, some combinations of high and low side MOSFETs might be encountered that will cause excessive gate-drain coupling, which can lead to efficiency killing, EMI-producing shoot through currents. This is often remedied by adding a resistor in series with BOOT, which increases the turn-on time of the high side MOSFET without degrading the turn-off time, as shown in Figure 8.

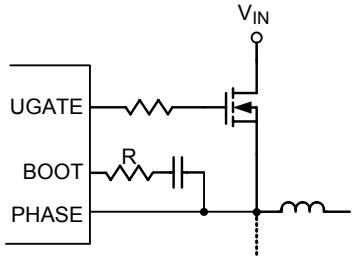



Figure 8. Increasing the UGATE Rise Time

### Power Good Output (PGOOD)

The power good output is an open-drain output and requires a pull-up resistor. When the output voltage is 15% above or 15% below its set voltage, PGOOD gets pulled low. It is held low until the output voltage returns to within these tolerances once more. In soft start, PGOOD is actively held low and is allowed to transition high until soft start is over and the output reaches 88% of its set voltage. There is a 2.5μs delay built into PGOOD circuitry to prevent false transition.

### POR, UVLO and Soft-Start

Power On Reset (POR) occurs when VCC rises above to approximately 4V. After POR is triggered, the RT8240A/B/C will reset the fault latch and prepare the PWM for operation. Below 3.8V (typ.), the VCC Under Voltage Lockout (UVLO) circuitry inhibits switching by keeping UGATE and LGATE low. A built-in soft-start is used to prevent surge current from power supply input after EN is enabled. It clamps the ramping of the internal reference voltage which is compared with FB signal. The typical soft-start duration is 1.3ms.

### Over Voltage Protection (OVP)

The output voltage can be continuously monitored for over voltage. If the output exceeds 20% of its set voltage threshold, over voltage protection is triggered and the LGATE low side gate driver is forced high. This activates the low side MOSFET switch which rapidly discharges the output capacitor and reduces the input voltage. The RT8240A/B/C will be latched once OVP is triggered and only be released by toggling EN or VCC power on reset. There is a 5μs delay built into the OVP circuit to prevent false alarm.

Note that LGATE latching high causes the output voltage to dip slightly negative when energy has been previously stored in the LC tank circuit. For loads that cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse polarity clamp.

If the over voltage condition is caused by a short in high side switch, turning the low side MOSFET on 100% creates an electrical short between the battery and GND, blowing the fuse and disconnecting the battery from the output.

### Under Voltage Protection (UVP)

The output voltage can be continuously monitored for under voltage. When under voltage protection is enabled, if the output is less than 70% of its set voltage threshold, under voltage protection is triggered, then both UGATE and LGATE gate drivers are forced low. In order to remove the residual charge on the output capacitor during the under voltage period, if PHASE is greater than 1V, the LGATE is forced high until PHASE is lower than 1V. During soft-start, the UVP blanking time is 3ms.

### Thermal Protection

The RT8240A/B/C monitors the temperature of itself. If the temperature exceeds the threshold value, 150°C (typ.), all internal circuitry is inactive during thermal shutdown. The RT8240A/B/C is latched once thermal shutdown is triggered and can only be released by toggling EN or VCC power on reset.

### Output Inductor Selection

The switching frequency (on-time) and operating point (% ripple or $L_{IR}$) determine the inductor value as follows :

$$L = \frac{t_{ON} \times (V_{IN} - V_{OUT})}{L_{IR} \times I_{LOAD(MAX)}}$$

where $L_{IR}$ is the ratio of the peak to peak ripple current to the maximum average inductor current.

Find a low loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current ($I_{PEAK}$) :

$$I_{PEAK} = I_{LOAD(MAX)} + \left( \frac{LIR}{2} \times I_{LOAD(MAX)} \right)$$

The calculation above shall serve as a general reference. To further improve transient response, the output inductor could be reduced further. This needs to be considered along with the selection of the output capacitor.

### Output Capacitor Selection

The capacitor value and ESR determines the amount of output voltage ripple and load transient response. So, the capacitor value must be greater than the largest value calculated from below equations.

$$V_{SAG} = \frac{(\Delta I_{LOAD})^2 \times L \times (t_{ON} + t_{OFF(MIN)})}{2 \times C_{OUT} \left[ V_{IN} \times t_{ON} - V_{OUT} \times (t_{ON} + t_{OFF(MIN)}) \right]}$$

$$V_{SOAR} = \frac{(\Delta I_{LOAD})^2 \times L}{2 \times C_{OUT} \times V_{OUT}}$$

$$V_{P-P} = L_{IR} \times I_{LOAD(MAX)} \times \left( ESR + \frac{1}{8 \times C_{OUT} \times f} \right)$$

Where $V_{SAG}$ and $V_{SOAR}$ are the allowable amount of undershoot voltage and overshoot voltage in load transient, $V_{P-P}$ is output ripple voltage, $t_{OFF(MIN)}$ is minimum off-time.

### Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT8240A/B/C, the maximum junction temperature is 125°C and $T_A$ is the ambient temperature. The junction to ambient thermal resistance, $\theta_{JA}$, is layout dependent. For WQFN-12L 2x2 packages, the thermal resistance, $\theta_{JA}$, is 165° C/W on a standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at $T_A$ = 25°C can be calculated by the following formula:

$P_{D(MAX)}$ = (125°C – 25°C) / (165°C/W) = 0.606W for WQFN-12L 2X2 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, $\theta_{JA}$. For the RT8240A/B/C package, the derating curve in Figure 9 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

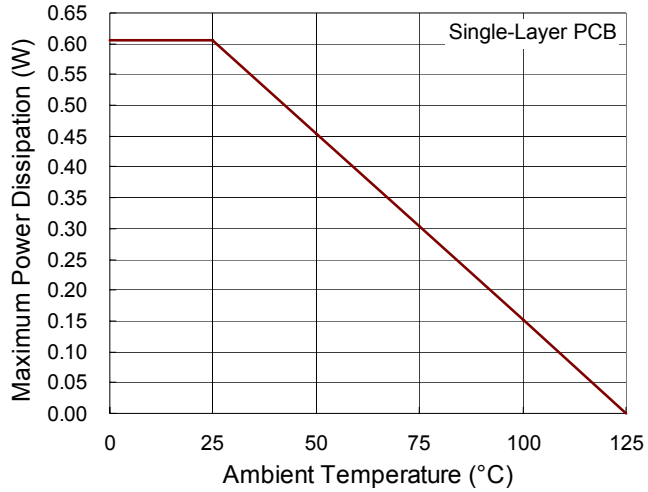



Figure 9. Derating Curves for the RT8240A/B/C Package

### Layout Considerations

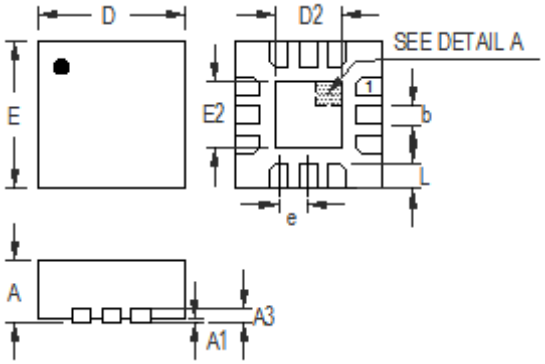
Layout is very important in high frequency switching converter design. If designed improperly, the PCB could radiate excessive noise and contribute to the converter instability.

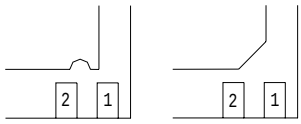
For best performance of the RT8240A/B/C, the following guidelines should be strictly followed.

Connect RC low pass filter from VCC, 1μF and 10Ω are recommended. Place the filter capacitor close to the IC.

- Keep current limit setting network as close as possible to the IC. Routing of the network should be kept away from high voltage switching nodes to prevent it from coupling.
- Connections from the drivers to the respective gate of the high side or the low side MOSFET should be as short as possible to reduce stray inductance.
- All sensitive analog traces and components such as VOUT, RGND, EN, PGOOD, CS, G0 and VCC should be placed away from high voltage switching nodes such as PHASE, LGATE, UGATE, or BOOT nodes to prevent it from coupling. Use internal layer (s) as ground plane (s) and shield the feedback trace from power traces and components.
- Current sense connections must always be made using Kelvin connections to ensure an accurate signal, with the current limit resistor located at the device.
- Power sections should connect directly to ground plane (s) using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed to minimize loops and reduce losses.

## Outline Dimension




**DETAIL A**

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.150 | 0.250 | 0.006 | 0.010 |
| D | 1.900 | 2.100 | 0.075 | 0.083 |
| E | 1.900 | 2.100 | 0.075 | 0.083 |
| e | 0.400 | | 0.016 | |
| D2 | 0.850 | 0.950 | 0.033 | 0.037 |
| E2 | 0.850 | 0.950 | 0.033 | 0.037 |
| L | 0.250 | 0.350 | 0.010 | 0.014 |

**W-Type 12L QFN 2x2 Package**

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