Quad Analog Switch/ Multiplexer/Demultiplexer with Separate Analog and Digital Power Supplies

High-Performance Silicon-Gate CMOS

The MC74VHC4316 utilizes silicon–gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF–channel leakage current. This bilateral switch/multiplexer/demultiplexer controls analog and digital voltages that may vary across the full analog power–supply range (from V_{CC} to V_{EE}).

The VHC4316 is similar in function to the metal–gate CMOS MC14016 and MC14066, and to the High–Speed CMOS HC4066A. Each device has four independent switches. The device control and Enable inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. The device has been designed so that the ON resistances ($R_{\rm ON}$) are much more linear over input voltage than $R_{\rm ON}$ of metal–gate CMOS analog switches. Logic–level translators are provided so that the On/Off Control and Enable logic–level voltages need only be $V_{\rm CC}$ and $V_{\rm CC}$ and $V_{\rm CC}$ while the switch is passing signals ranging between $V_{\rm CC}$ and $V_{\rm CC}$. When the Enable pin (active–low) is high, all four analog switches are turned off.

Features

- Logic-Level Translator for On/Off Control and Enable Inputs
- Fast Switching and Propagation Speeds
- High ON/OFF Output Voltage Ratio
- Diode Protection on All Inputs/Outputs
- Analog Power–Supply Voltage Range ($V_{CC} V_{EE}$) = 2.0 to 12.0 V
- Digital (Control) Power–Supply Voltage Range $(V_{CC} GND) = 2.0 \text{ V}$ to 6.0 V, Independent of V_{EE}
- Improved Linearity of ON Resistance
- Chip Complexity: 66 FETs or 16.5 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant



ON Semiconductor®

http://onsemi.com

MARKING DIAGRAMS



SOIC-16 D SUFFIX CASE 751B





TSSOP-16 DT SUFFIX CASE 948F



A = Assembly Location

WL, L = Wafer Lot Y = Year

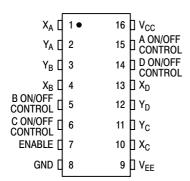
WW, W = Work Week G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74VHC4316DG	SOIC-16 (Pb-Free)	48 Units / Rail
MC74VHC4316DR2G	SOIC-16 (Pb-Free)	2500/Tape&Reel
MC74VHC4316DTG	TSSOP16 (Pb-Free)	96 Units / Rail
MC74VHC4316DTR2G	TSSOP16 (Pb-Free)	2500/Tape&Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



FUNCTION TABLE

Inpu	State of Analog	
Enable	On/Off Control	Switch
L L H	H L X	On Off Off

X = Don't Care.

Figure 1. Pin Assignment

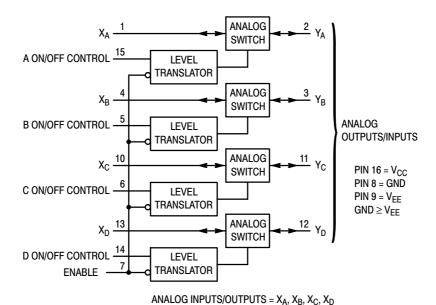


Figure 2. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V _{CC}	11,7	to GND) f. to V _{EE})	- 0.5 to + 7.0 - 0.5 to + 14.0	V
V _{EE}	Negative DC Supply Voltage (Ref. to GND)		- 7.0 to + 0.5	V
V _{IS}	Analog Input Voltage		V _{EE} - 0.5 to V _{CC} + 0.5	V
V _{in}	DC Input Voltage (Ref. to GND)		-0.5 to V_{CC} + 0.5	V
I	DC Current Into or Out of Any Pin		± 25	mA
P _D	•	Package* Package*	500 450	mW
T _{stg}	Storage Temperature		- 65 to + 150	°C
TL		emperature, 1 mm from Case for 10 Seconds (SOIC or TSSOP Package)		

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Positive DC Supply Voltage (Ref. to GND)	2.0	6.0	V
V _{EE}	Negative DC Supply Voltage (Ref. to GND)	- 6.0	GND	V
V _{IS}	Analog Input Voltage	V _{EE}	V _{CC}	V
V _{in}	Digital Input Voltage (Ref. to GND)	GND	V _{CC}	V
V _{IO} *	Static or Dynamic Voltage Across Switch	-	1.2	V
T _A	Operating Temperature, All Package Types	– 55	+ 125	°C
t _r , t _f		0 0 0	1000 600 500 400	ns

^{*}For voltage drops across the switch greater than 1.2 V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND \leq (V_{in} or V_{out}) \leq V_{CC} .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{\rm CC}$). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus.

^{*}Derating - SOIC Package: - 7 mW/°C from 65° to 125°C TSSOP Package: - 6.1 mW/°C from 65° to 125°C

DC ELECTRICAL CHARACTERISTICS Digital Section (Voltages Referenced to GND) V_{EE} = GND Except Where Noted

				Gu	aranteed Li	mit	
Symbol	Parameter	Test Conditions	V _{CC}	– 55 to 25°C	≤ 85°C	≤ 125°C	Unit
V _{IH}	Minimum High-Level Voltage, Control or Enable Inputs	R _{on} = Per Spec	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	٧
V _{IL}	Maximum Low-Level Voltage, Control or Enable Inputs	R _{on} = Per Spec	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	٧
l _{in}	Maximum Input Leakage Current, Control or Enable Inputs	$V_{in} = V_{CC}$ or GND $V_{EE} = -6.0 \text{ V}$	6.0	± 0.1	± 1.0	± 1.0	μΑ
I _{CC}	Maximum Quiescent Supply Current (per Package)	$\label{eq:Vin} \begin{split} V_{in} &= V_{CC} \text{ or GND} \\ V_{IO} &= 0 \text{ V} \\ V_{EE} &= GNE \\ V_{EE} &= -6.6 \end{split}$		2 4	20 40	40 160	μΑ

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

DC ELECTRICAL CHARACTERISTICS Analog Section (Voltages Referenced to V_{EE})

					Gu	aranteed Li	mit	
Symbol	Parameter	Test Conditions	V _{CC}	V _{EE}	– 55 to 25°C	≤ 85 °C	≤ 125°C	Unit
R _{on}	Maximum "ON" Resistance	$\begin{aligned} &V_{in} = V_{IH} \\ &V_{IS} = V_{CC} \text{ to } V_{EE} \\ &I_{S} \leq 2.0 \text{ mA} \end{aligned}$	2.0* 4.5 4.5 6.0	0.0 0.0 - 4.5 - 6.0	- 160 90 90	- 200 110 110	- 240 130 130	Ω
		$\begin{aligned} &V_{in} = V_{IH} \\ &V_{IS} = V_{CC} \text{ or } V_{EE} \text{ (Endpoints)} \\ &I_{S} \leq 2.0 \text{ mA} \end{aligned}$	2.0 4.5 4.5 6.0	0.0 0.0 - 4.5 - 6.0	- 90 70 70	- 115 90 90	- 140 105 105	
ΔR_{on}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$\begin{aligned} &V_{in} = V_{IH} \\ &V_{IS} = 1/2 \; (V_{CC} - V_{EE}) \\ &I_{S} \leq 2.0 \; \text{mA} \end{aligned}$	2.0 4.5 4.5 6.0	0.0 0.0 - 4.5 - 6.0	- 20 15 15	- 25 20 20	- 30 25 25	Ω
I _{off}	Maximum Off-Channel Leakage Current, Any One Channel	$V_{in} = V_{IL}$ $V_{IO} = V_{CC}$ or V_{EE} Switch Off (Figure 3)	6.0	- 6.0	0.1	0.5	1.0	μΑ
I _{on}	Maximum On-Channel Leakage Current, Any One Channel	$V_{in} = V_{IH}$ $V_{IS} = V_{CC}$ or V_{EE} (Figure 4)	6.0	- 6.0	0.1	0.5	1.0	μΑ

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

^{*}At supply voltage (V_{CC} – V_{EE}) approaching 2.0 V the analog switch–on resistance becomes extremely non–linear. Therefore, for low–voltage operation, it is recommended that these devices only be used to control digital signals.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Control or Enable t_r = t_f = 6 ns, V_{EE} = GND)

			Gu	aranteed Li	mit	
Symbol	Parameter	v _{cc} v	– 55 to 25°C	≤ 85 °C	≤ 125°C	Unit
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figures 8 and 9)	2.0 4.5 6.0	40 6 5	50 8 7	60 9 8	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Control or Enable to Analog Output (Figures 10 and 11)	2.0 4.5 6.0	130 40 30	160 50 40	200 60 50	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Control or Enable to Analog Output (Figures 10 and 11)	2.0 4.5 6.0	140 40 30	175 50 40	250 60 50	ns
С	Maximum Capacitance ON/OFF Control and Enable Inputs	_	10	10	10	pF
	Control Input = GND Analog I/O Feedthrough		35 1.0	35 1.0	35 1.0	

^{1.} For propagation delays with loads other than 50 pF, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

^{2.} Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V _{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Switch) (Figure 13)*	15	pF

^{*}Used to determine the no-load dynamic power consumption: $P_D = C_{PD} \ V_{CC}^2 f + I_{CC} \ V_{CC}$. For load considerations, see Chapter 2of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Test Conditions	V _{CC} V	V _{EE} V	Limit* 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 5)	$\begin{array}{ll} f_{in} = 1 \text{ MHz Sine Wave} \\ \text{Adjust } f_{in} \text{ Voltage to Obtain 0 dBm at V}_{OS} \\ \text{Increase } f_{in} \text{ Frequency Until dB Meter} \\ \text{Reads} - 3 \text{ dB} \\ \text{R}_{L} = 50 \Omega, C_{L} = 10 \text{ pF} \end{array}$	2.25 4.50 6.00	- 2.25 - 4.50 - 6.00	150 160 160	MHz
-	Off–Channel Feedthrough Isolation (Figure 6)	$\begin{split} f_{in} &\equiv \text{Sine Wave} \\ \text{Adjust } f_{in} &\text{ Voltage to Obtain 0 dBm at V}_{IS} \\ f_{in} &= 10 \text{ kHz}, \text{ R}_L = 600 \ \Omega, \text{ C}_L = 50 \text{ pF} \\ f_{in} &= 1.0 \text{ MHz}, \text{ R}_L = 50 \ \Omega, \text{ C}_L = 10 \text{ pF} \end{split}$	2.25 4.50 6.00 2.25 4.50 6.00	- 2.25 - 4.50 - 6.00 - 2.25 - 4.50 - 6.00	- 50 - 50 - 50 - 40 - 40 - 40	dΒ
-	Feedthrough Noise, Control to Switch (Figure 7)	$\begin{split} V_{in} &\leq \text{1 MHz Square Wave } (t_r = t_f = 6 \text{ ns}) \\ \text{Adjust } R_L \text{ at Setup so that } I_S = 0 \text{ A} \\ R_L &= 600 \ \Omega, \ C_L = 50 \text{ pF} \\ R_L &= 10 \text{ k}\Omega, \ C_L = 10 \text{ pF} \end{split}$	2.25 4.50 6.00 2.25 4.50 6.00	- 2.25 - 4.50 - 6.00 - 2.25 - 4.50 - 6.00	60 130 200 30 65 100	mV _{PP}
-	Crosstalk Between Any Two Switches (Figure 12)	$\begin{split} f_{in} &\equiv \text{Sine Wave} \\ \text{Adjust } f_{in} &\text{ Voltage to Obtain 0 dBm at V}_{IS} \\ f_{in} &= 10 \text{ kHz}, \text{ R}_{L} = 600 \ \Omega, \text{ C}_{L} = 50 \text{ pF} \\ f_{in} &= 1.0 \text{ MHz}, \text{ R}_{L} = 50 \ \Omega, \text{ C}_{L} = 10 \text{ pF} \end{split}$	2.25 4.50 6.00 2.25 4.50 6.00	- 2.25 - 4.50 - 6.00 - 2.25 - 4.50 - 6.00	- 70 - 70 - 70 - 80 - 80 - 80	dB
THD	Total Harmonic Distortion (Figure 14)	$\begin{split} f_{in} = 1 \text{ kHz, } R_L = 10 \text{ k}\Omega, C_L = 50 \text{ pF} \\ \text{THD} = \text{THD}_{Measured} - \text{THD}_{Source} \\ V_{IS} = 4.0 \text{ Vpp sine wave} \\ V_{IS} = 8.0 \text{ Vpp sine wave} \\ V_{IS} = 11.0 \text{ Vpp sine wave} \end{split}$	2.25 4.50 6.00	- 2.25 - 4.50 - 6.00	0.10 0.06 0.04	%

^{*}Limits not tested. Determined by design and verified by qualification.

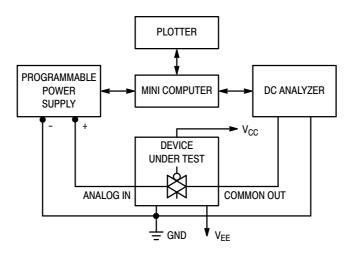


Figure 1. On Resistance Test Set-Up

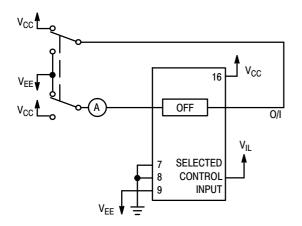


Figure 2. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

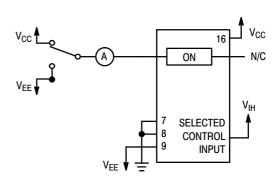
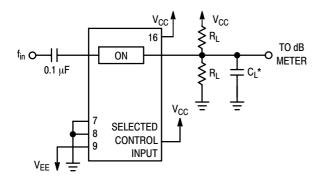
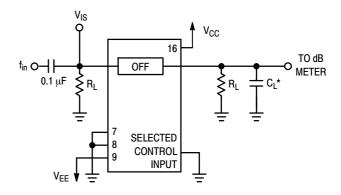


Figure 3. Maximum On Channel Leakage Current, Test Set-Up



^{*}Includes all probe and jig capacitance.

Figure 4. Maximum On-Channel Bandwidth Test Set-Up



*Includes all probe and jig capacitance.

Figure 5. Off-Channel Feedthrough Isolation, Test Set-Up

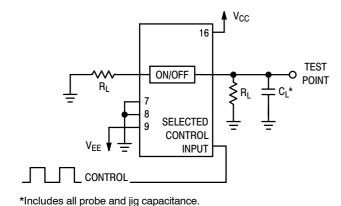


Figure 6. Feedthrough Noise, Control to Analog Out, Test Set-Up

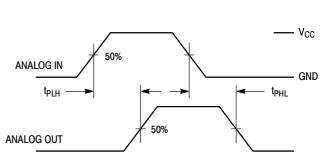
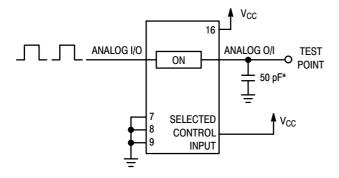
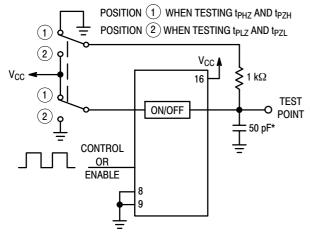


Figure 7. Propagation Delays, Analog In to Analog Out



^{*}Includes all probe and jig capacitance.

Figure 8. Propagation Delay Test Set-Up



^{*}Includes all probe and jig capacitance.

Figure 10. Propagation Delay Test Set-Up

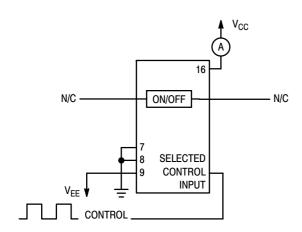


Figure 12. Power Dissipation Capacitance
Test Set-Up

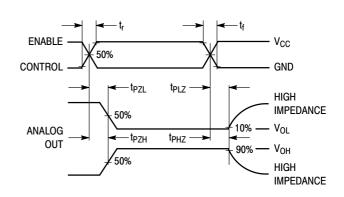
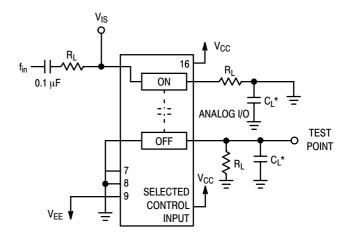
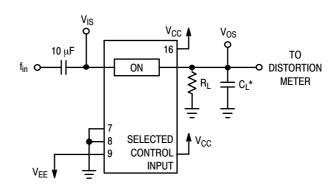


Figure 9. Propagation Delay, ON/OFF Control to Analog Out



^{*}Includes all probe and jig capacitance.

Figure 11. Crosstalk Between Any Two Switches, Test Set-Up (Adjacent Channels Used)



^{*}Includes all probe and jig capacitance.

Figure 13. Total Harmonic Distortion, Test Set-Up

APPLICATIONS INFORMATION

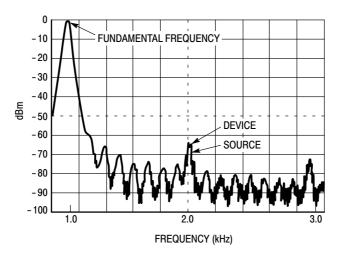


Figure 14. Plot, Harmonic Distortion

The Enable and Control pins should be at V_{CC} or GND logic levels, V_{CC} being recognized as logic high and GND being recognized as a logic low. Unused analog inputs/outputs may be left floating (not connected). However, it is advisable to tie unused analog inputs and outputs to V_{CC} or V_{EE} through a low value resistor. This minimizes crosstalk and feedthrough noise that may be picked up by the unused I/O pins.

The maximum analog voltage swings are determined by the supply voltages V_{CC} and V_{EE} . The positive peak analog voltage should not exceed V_{CC} . Similarly, the negative peak analog voltage should not go below V_{EE} . In the example below, the difference between V_{CC} and V_{EE} is 12 V.

Therefore, using the configuration in Figure 15, a maximum analog signal of twelve volts peak-to-peak can be controlled.

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure 16. These diodes should be small signal, fast turn-on types able to absorb the maximum anticipated current surges during clipping. An alternate method would be to replace the Dx diodes with MOSORBs (MOSORB is an acronym for high current surge protectors). MOSORBs are fast turn-on devices ideally suited for precise dc protection with no inherent wear out mechanism.

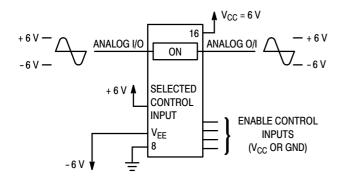


Figure 15.

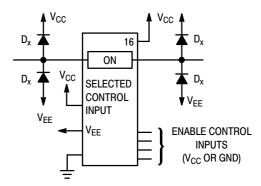


Figure 16. Transient Suppressor Application

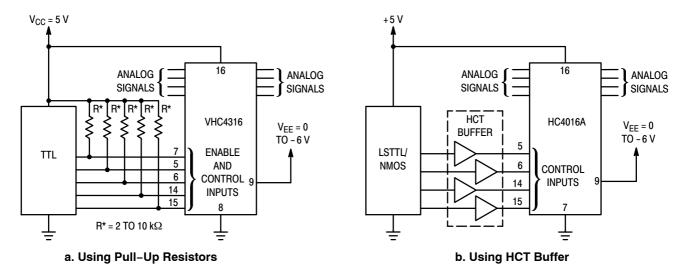


Figure 17. LSTTL/NMOS to HCMOS Interface

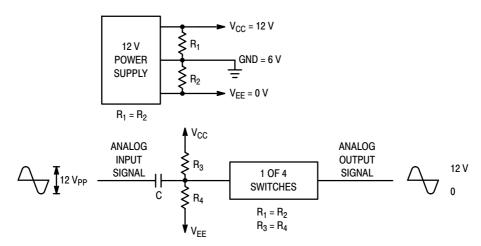


Figure 18. Switching a 0-to-12 V Signal Using a Single Power Supply (GND \neq 0 V)

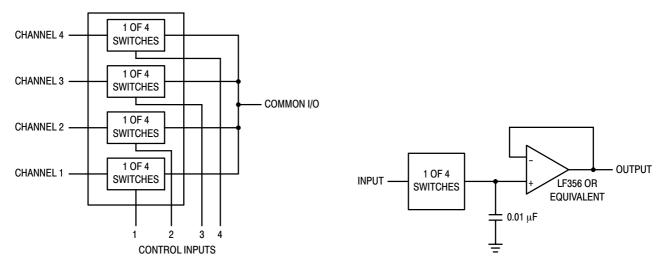
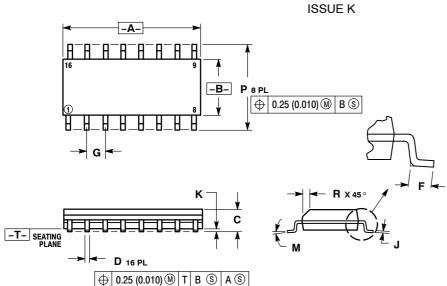


Figure 19. 4-Input Multiplexer

Figure 20. Sample/Hold Amplifier

PACKAGE DIMENSIONS

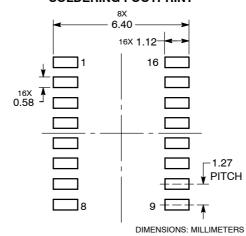
SOIC-16 **D SUFFIX** CASE 751B-05



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. ALLOWABLE DAMBAR
 PROTRUSION. ALLOWABLE DAMBAR
 PROTRUSION SHALL BE 0.127 (0.005) TOTAL
 IN EXCESS OF THE D DIMENSION AT
 MAXIMUM MATERIAL CONDITION.

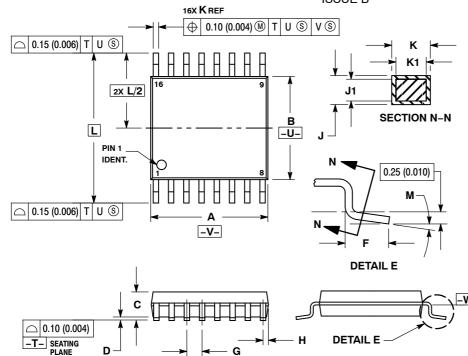
	MILLIMETERS INCHES		HES	
DIM	MIN	MAX	MIN	MAX
Α	9.80	10.00	0.386	0.393
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050	BSC
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
Р	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT



PACKAGE DIMENSIONS

TSSOP-16 **DT SUFFIX** CASE 948F-01 **ISSUE B**



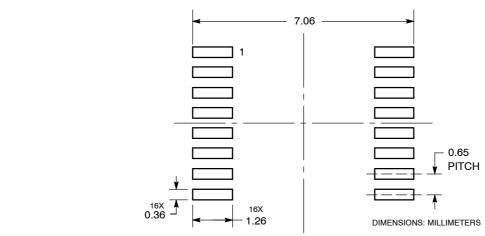
NOTES:

- 1. DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: MILLIMETER. B. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT
- EXCEED 0.15 (0.006) PER SIDE.

 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION. 6. TERMINAL NUMBERS ARE SHOWN FOR
- 6. TERMINAL NUMB REFERENCE ONLY.
- 7. DIMENSION A AND B ARE TO BE

PETE	MILLIN	IETERS	INC	HES .	
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	0.65 BSC		BSC	
Н	0.18	0.28	0.007	0.011	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40		0.252 BSC		
M	0°	8°	0° 8°		

SOLDERING FOOTPRINT



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