CMOS Digital Integrated Circuits Silicon Monolithic

74HC4053D

1. Functional Description

- Triple 2-Channel Analog Multiplexer/Demultiplexer

2. General

The 74HC4053D are high speed CMOS ANALOG MULTIPLEXER/DEMULTIPLEXER fabricated with silicon gate C²MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The 74HC4053D has a 2 channel × 3 configuration.

The digital signal to the control terminal turns "ON" the corresponding switch of each channel a large amplitude signal (V_{CC} - V_{EE}) can then be switched by the small logical amplitude (V_{CC} - GND) control signal.

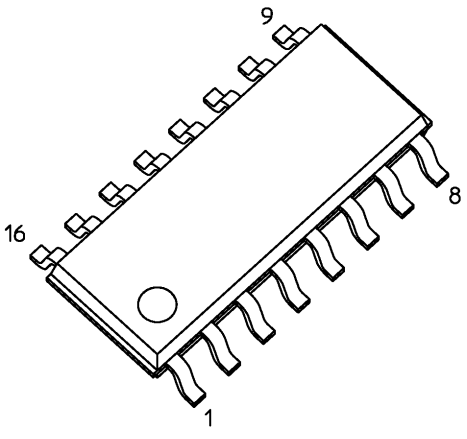
For example, in the case of V_{CC} = 5 V, GND = 0 V, V_{EE} = -5 V, signals between -5 V and +5 V can be switched from the logical circuit with a single power supply of 5 V. As the ON-resistance of each switch is low, they can be connected to circuits with low input impedance.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

3. Features

(1) Low power dissipation: I_{CC} = 4.0 μA (max) (V_{CC} = 6.0 V, V_{EE} = GND, T_a = 25 °C)
(2) High noise immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (min)
(3) Low ON-resistance: R_{ON} = 50 Ω (typ.) at V_{CC} - V_{EE} = 9 V
(4) High noise immunity: THD = 0.020 % (typ.) at V_{CC} - V_{EE} = 9 V
(5) Pin and function compatible with 4053B

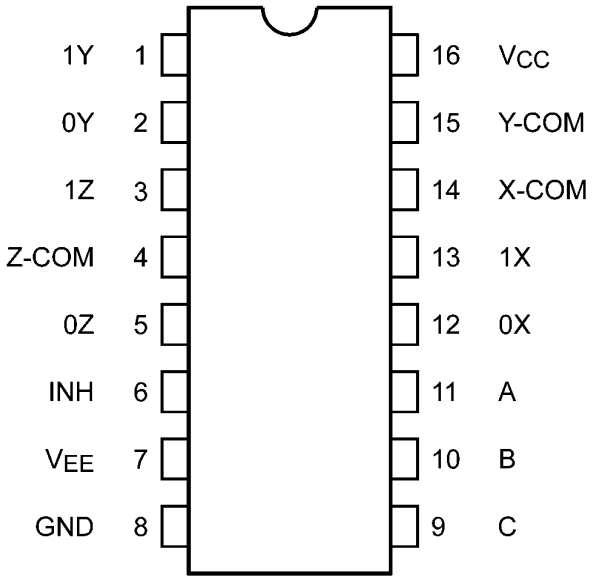
4. Packaging



SOIC16

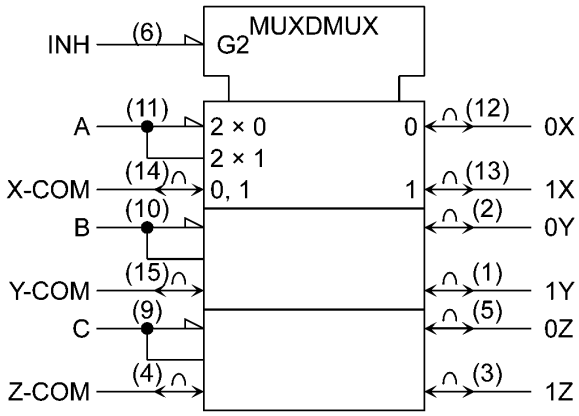
Start of commercial production
2016-08

5. Pin Assignment

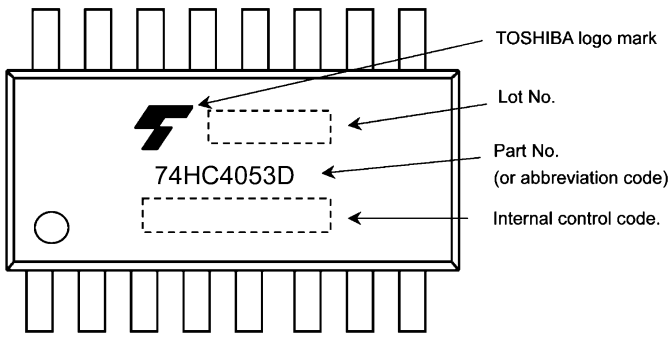


(top view)

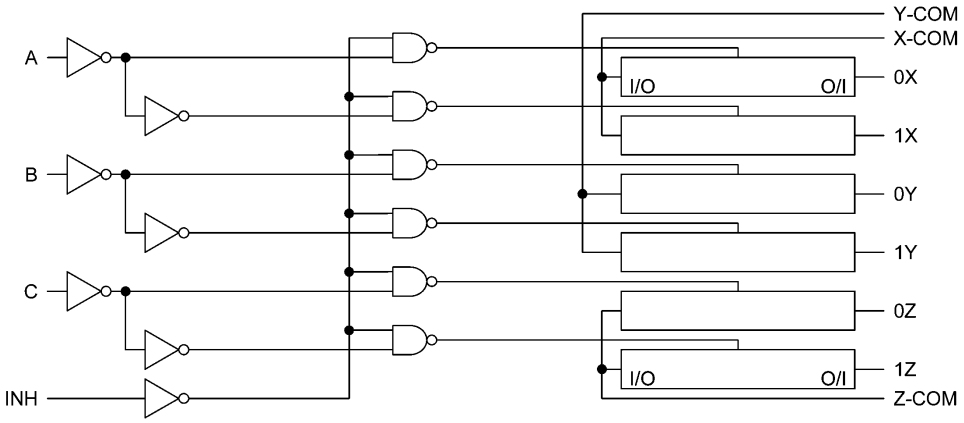
6. IEC Logic Symbol



7. Marking



8. System Diagram



9. Truth Table

Input Inhibit	Input C	Input B	Input A	ON Channel
L	L	L	L	0X, 0Y, 0Z
L	L	L	H	1X, 0Y, 0Z
L	L	H	L	0X, 1Y, 0Z
L	L	H	H	1X, 1Y, 0Z
L	H	L	L	0X, 0Y, 1Z
L	H	L	H	1X, 0Y, 1Z
L	H	H	L	0X, 1Y, 1Z
L	H	H	H	1X, 1Y, 1Z
H	X	X	X	None

X: Don't care

10. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	-0.5 to 7.0	V
	V_{EE}	-7.0 to 0	
	V_{CC}-V_{EE}	-0.5 to 13.0	
Input voltage	V_{IN}	-0.5 to V_{CC} + 0.5	V
Switch I/O voltage	$V_{I/O}$	V_{EE} - 0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
I/O diode current	$I_{I/OK}$	±20	mA
Switch through current	I_T	±25	mA
V_{CC}/ground current	I_{CC}	±50	mA
Power dissipation	P_D	500	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

11. Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 6.0	V
	V_{EE}	-6.0 to 0	
	V_{CC}-V_{EE}	2.0 to 12.0	
Input voltage	V_{IN}	0 to V_{CC}	V
Switch I/O voltage	$V_{I/O}$	V_{EE} to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall times	t_r,t_f	0 to 50	μs

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

12. Electrical Characteristics

12.1. DC Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition	V_{EE} (V)	V_{CC} (V)	Min	Typ.	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	V
				4.5	3.15	—	—	
				6.0	4.20	—	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	V
				4.5	—	—	1.35	
				6.0	—	—	1.80	
ON-resistance	R_{ON}	V_{IN} = V_{IH} or V_{IL} $V_{I/O}$ = V_{CC} to V_{EE} $I_{I/O} \leq$ 2 mA	GND	4.5	—	85	180	Ω
			-4.5	4.5	—	55	120	
			-6.0	6.0	—	50	100	
		V_{IN} = V_{IH} or V_{IL} $V_{I/O}$ = V_{CC} or V_{EE} $I_{I/O} \leq$ 2 mA	GND	2.0	—	150	—	
			GND	4.5	—	70	150	
			-4.5	4.5	—	50	100	
			-6.0	6.0	—	45	80	
Difference of ON-resistance between switches	ΔR_{ON}	V_{IN} = V_{IH} or V_{IL} $V_{I/O}$ = V_{CC} to V_{EE} $I_{I/O} \leq$ 2 mA	GND	4.5	—	10	30	Ω
			-4.5	4.5	—	5	12	
			-6.0	6.0	—	5	10	
Input/Output leakage current (Switch OFF)	I_{OFF}	V_{OS} = V_{CC} or GND V_{IS} = GND or V_{CC} V_{IN} = V_{IH} or V_{IL}	GND	6.0	—	—	±0.06	μA
			-6.0	6.0	—	—	±0.1	
Input/Output leakage current (Switch ON)	$I_{I/O}$	V_{OS} = V_{CC} or GND V_{IN} = V_{IH} or V_{IL}	GND	6.0	—	—	±0.06	μA
			-6.0	6.0	—	—	±0.1	
Control input leakage current	I_{IN}	V_{IN} = V_{CC} or GND	GND	6.0	—	—	±0.1	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND	GND	6.0	—	—	4.0	μA
			-6.0	6.0	—	—	8.0	

12.2. DC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Condition	V_{EE} (V)	V_{CC} (V)	Min	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	V
				4.5	3.15	—	
				6.0	4.20	—	
Low-level input voltage	V_{IL}	—		2.0	—	0.50	V
				4.5	—	1.35	
				6.0	—	1.80	
ON-resistance	R_{ON}	V_{IN} = V_{IH} or V_{IL} $V_{I/O}$ = V_{CC} to V_{EE} $I_{I/O} \leq$ 2 mA	GND	4.5	—	225	Ω
			-4.5	4.5	—	150	
			-6.0	6.0	—	125	
		V_{IN} = V_{IH} or V_{IL} $V_{I/O}$ = V_{CC} or V_{EE} $I_{I/O} \leq$ 2 mA	GND	2.0	—	—	
			GND	4.5	—	190	
			-4.5	4.5	—	125	
			-6.0	6.0	—	100	
Difference of ON-resistance between switches	ΔR_{ON}	V_{IN} = V_{IH} or V_{IL} $V_{I/O}$ = V_{CC} to V_{EE} $I_{I/O} \leq$ 2 mA	GND	4.5	—	35	Ω
			-4.5	4.5	—	15	
			-6.0	6.0	—	12	
Input/Output leakage current (Switch OFF)	I_{OFF}	V_{OS} = V_{CC} or GND V_{IS} = GND or V_{CC} V_{IN} = V_{IH} or V_{IL}	GND	6.0	—	±0.6	μA
			-6.0	6.0	—	±1.0	
Input/Output leakage current (Switch ON)	$I_{I/O}$	V_{OS} = V_{CC} or GND V_{IN} = V_{IH} or V_{IL}	GND	6.0	—	±0.6	μA
			-6.0	6.0	—	±1.0	
Control input leakage current	I_{IN}	V_{IN} = V_{CC} or GND	GND	6.0	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND	GND	6.0	—	40.0	μA
			-6.0	6.0	—	80.0	

12.3. AC Characteristics (Unless otherwise specified, C_L = 50 pF, T_a = 25 °C, Input: t_r = t_f = 6 ns)

Characteristics	Symbol	Test Condition	V_{EE} (V)	V_{CC} (V)	Min	Typ.	Max	Unit
Phase difference between input to output	$\varphi_{I/O}$	—	GND	2.0	—	25	60	ns
			GND	4.5	—	6	12	
			GND	6.0	—	5	10	
			-4.5	4.5	—	4	—	
Output enable time	t_{PZL},t_{PZH}	R_L = 1 kΩ Figure 1	GND	2.0	—	50	225	ns
			GND	4.5	—	14	45	
			GND	6.0	—	12	38	
			-4.5	4.5	—	14	—	
Output disable time	t_{PLZ},t_{PHZ}	R_L = 1 kΩ Figure 1	GND	2.0	—	95	225	ns
			GND	4.5	—	30	45	
			GND	6.0	—	26	38	
			-4.5	4.5	—	26	—	
Control input capacitance	C_{IN}	—	—	—	—	5	10	pF
Common terminal capacitance	C_{IS}	Figure 2	-5.0	5.0	—	11	20	pF
Switch terminal capacitance	C_{OS}	Figure 2	-5.0	5.0	—	7	15	pF
Feedthrough capacitance	C_{IOS}	Figure 2	-5.0	5.0	—	0.75	2	pF
Power dissipation capacitance	C_{PD}	Figure 2 (Note 1)	GND	5.0	—	10	—	pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

12.4. AC Characteristics (Unless otherwise specified, C_L = 50 pF, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 6 ns)

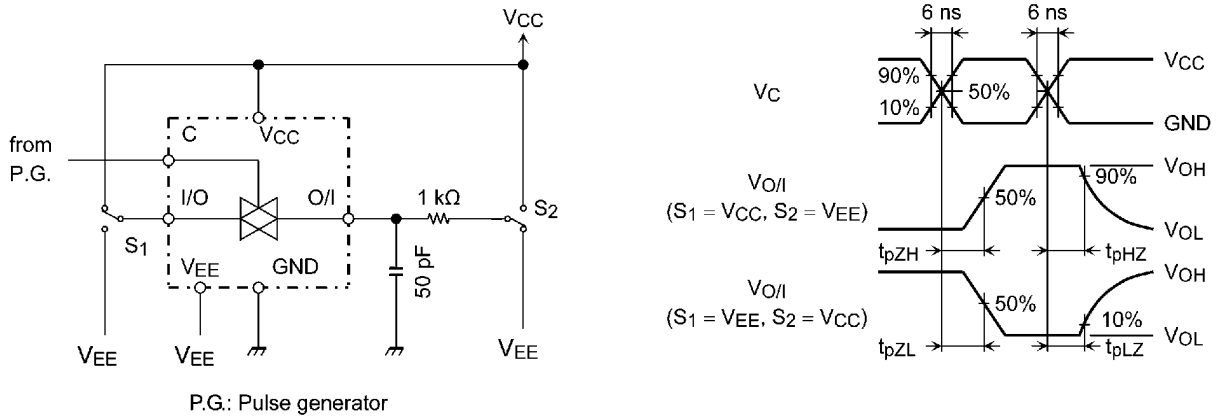
Characteristics	Symbol	Test Condition	V_{EE} (V)	V_{CC} (V)	Min	Max	Unit
Phase difference between input to output	$\varphi_{I/O}$	—	GND	2.0	—	75	ns
			GND	4.5	—	15	
			GND	6.0	—	13	
			-4.5	4.5	—	—	
Output enable time	t_{PZL},t_{PZH}	R_L = 1 kΩ Figure 1	GND	2.0	—	280	ns
			GND	4.5	—	56	
			GND	6.0	—	48	
			-4.5	4.5	—	—	
Output disable time	t_{PLZ},t_{PHZ}	R_L = 1 kΩ Figure 1	GND	2.0	—	280	ns
			GND	4.5	—	56	
			GND	6.0	—	48	
			-4.5	4.5	—	—	
Control input capacitance	C_{IN}	—	—	—	—	10	pF
Common terminal capacitance	C_{IS}	Figure 2	-5.0	5.0	—	20	pF
Switch terminal capacitance	C_{OS}	Figure 2	-5.0	5.0	—	15	pF
Feedthrough capacitance	C_{IOS}	Figure 2	-5.0	5.0	—	2	pF

12.5. Analog Switch Characteristics (T_a = 25 °C) (Note)

Characteristics	Symbol	Test Condition		V_{EE} (V)	V_{CC} (V)	Typ.	Unit
Sine Wave Distortion	THD	R_L = 10 kΩ, C_L = 50 pF, f_{IN} = 1 kHz	V_{IN} = 4.0 V_{p-p}	-2.25	2.25	0.025	%
			V_{IN} = 8.0 V_{p-p}	-4.5	4.5	0.020	
			V_{IN} = 11.0 V_{p-p}	-6.0	6.0	0.018	
Maximum frequency response	$f_{MAX(I/O)}$	Adjust f_{IN} voltage to obtain 0 dBm at V_{OS} Increase f_{IN} frequency until dB meter reads -3 dB R_L = 50 Ω, C_L = 10 pF f_{IN} = 1 MHz, sine wave Figure 3	(Note 1)	-2.25	2.25	120	MHz
			(Note 2)			95	
			(Note 1)	-4.5	4.5	190	
			(Note 2)			150	
			(Note 1)	-6.0	6.0	200	
			(Note 2)			190	
Feed through attenuation (switch OFF)	FTH	V_{IN} is centered at (V_{CC} - V_{EE})/2 Adjust input for 0 dBm. R_L = 600 Ω, C_L = 50 pF, f_{IN} = 1 MHz, sine wave Figure 4		-2.25	2.25	-50	dB
				-4.5	4.5	-50	
				-6.0	6.0	-50	
Crosstalk (control input to signal output)	X_{talk}	R_L = 600 Ω, C_L = 50 pF, f_{IN} = 1 MHz, square wave ($t_r = t_f$ = 6 ns) Figure 5		-2.25	2.25	60	mV
				-4.5	4.5	140	
				-6.0	6.0	200	
Crosstalk (between any switches)	X_{talk}	Adjust V_{IN} to obtain 0 dBm at input. R_L = 600 Ω, C_L = 50 pF, f_{IN} = 1 MHz, sine wave Figure 6		-2.25	2.25	-50	dB
				-4.5	4.5	-50	
				-6.0	6.0	-50	

Note: These characteristics are determined by design of devices.
Note 1: Input COMMON terminal, and measured at SWITCH terminal.
Note 2: Input SWITCH terminal, and measured at COMMON terminal.

13. AC Test Circuit



P.G.: Pulse generator

Figure 1 t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}

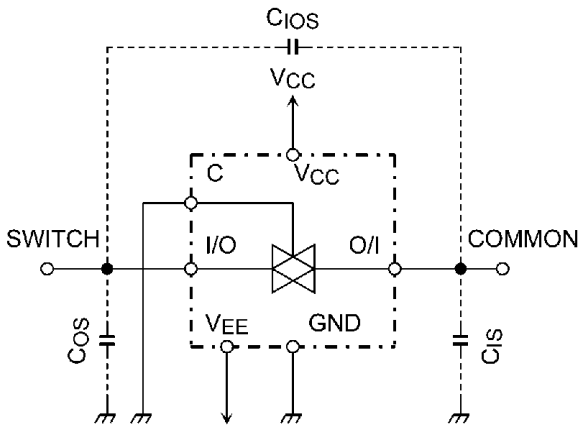


Figure 2 C_{IOS}, C_{IS}, C_{OS}

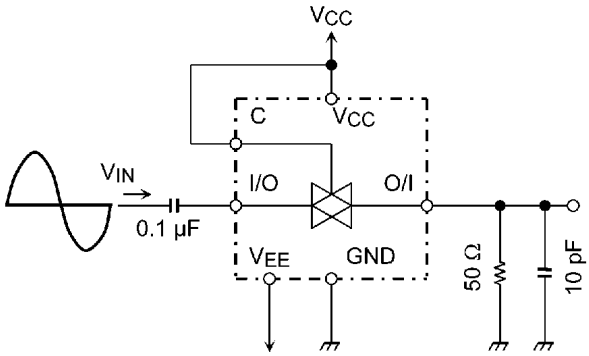


Figure 3 Frequency Response

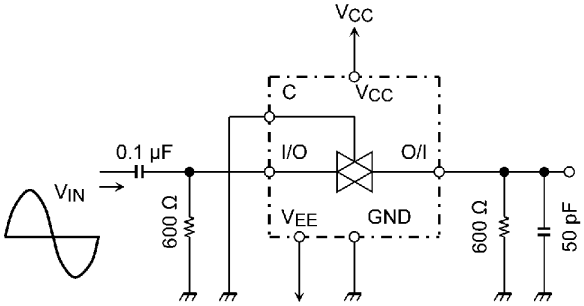
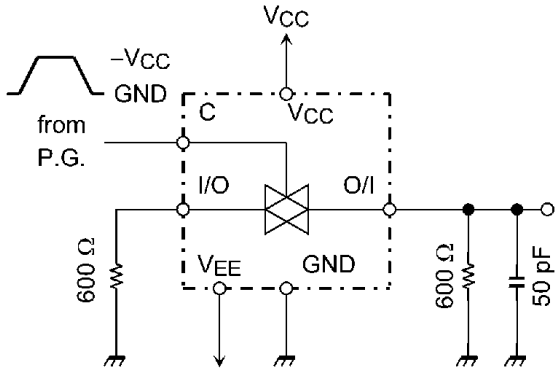


Figure 4 Feedthrough Attenuation



P.G.: Pulse generator

Figure 5 Cross Talk (control input to output signal)

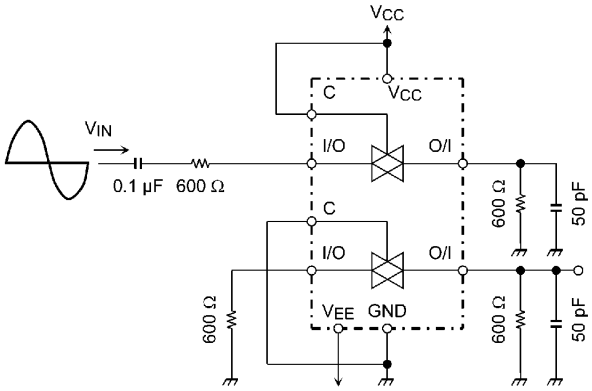
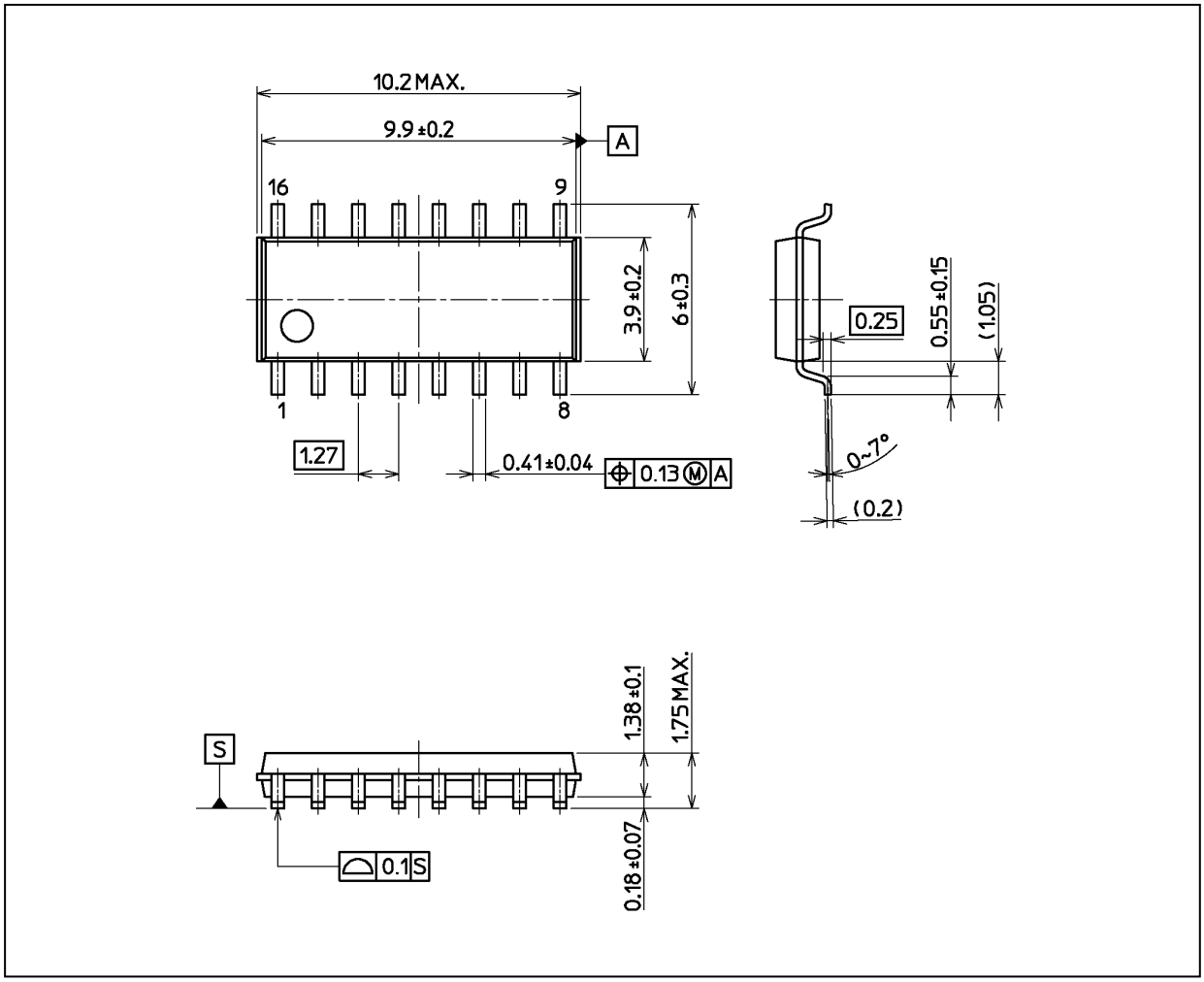


Figure 6 Cross Talk (between any two switches)

Package Dimensions

Unit: mm



Weight: 0.15 g (typ.)

Package Name(s)
Nickname: SOIC16

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