

## REAL-TIME CLOCK (RTC)

Check for Samples: [BQ32002](#)

### FEATURES

- Automatic Switchover to Backup Supply
- I<sup>2</sup>C Interface  
Supports Serial Clock up to 400 kHz
- Uses 32.768-kHz Crystal  
With –63-ppm to +126-ppm Adjustment
- Integrated Oscillator-Fail Detection
- 8-Pin SOIC Package
- –40°C to 85°C Ambient Operating Temperature

### APPLICATIONS

- General consumer electronics

### DESCRIPTION

The BQ32002 device is a compatible replacement for industry standard real-time clocks.

The BQ32002 features an automatic backup supply with integrated trickle charger. The backup supply can be implemented using a capacitor or non-rechargeable battery. The BQ32002 has a programmable calibration adjustment from –63 ppm to +126 ppm. The BQ32002 registers include an OF (oscillator fail) flag indicating the status of the RTC oscillator, as well as a STOP bit that allows the host processor to disable the oscillator. The time registers are normally updated once per second, and all the registers are updated at the same time to prevent a timekeeping glitch. The BQ32002 includes automatic leap-year compensation.

### ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Reel of 2500	BQ32002DR	BQ32002 xx y zzzz <sup>(3)</sup>

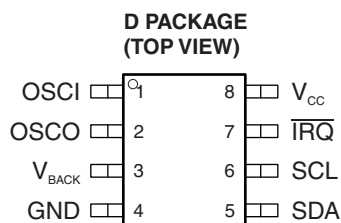
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(3) xx = date code, y = assembly site, zzzz = lot code

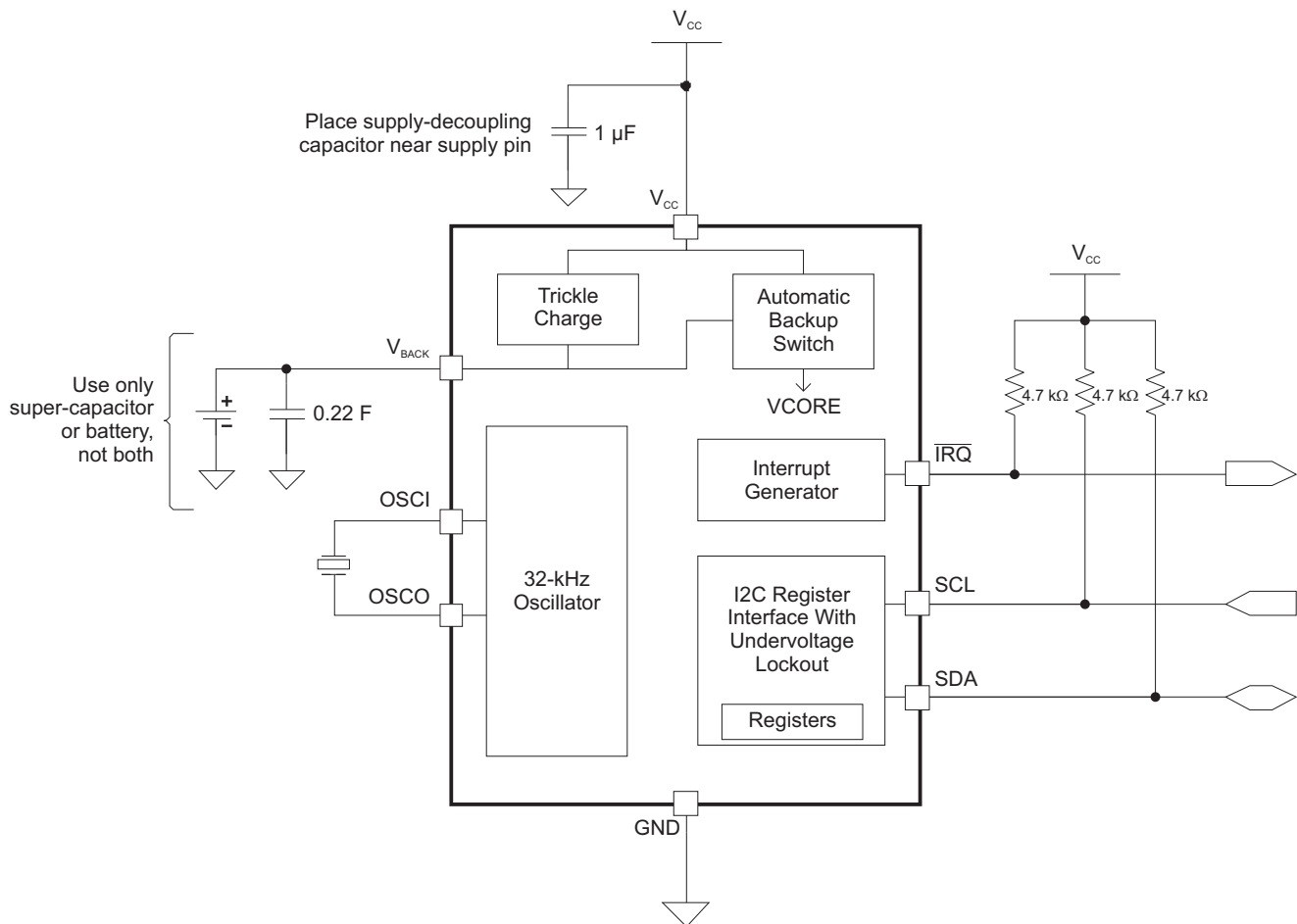


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**TERMINAL FUNCTIONS**

NAME	NO.	TYPE	DESCRIPTION
<b>Power and Ground</b>			
V <sub>CC</sub>	8	-	Main device power
GND	4	-	Ground
V <sub>BACK</sub>	3	-	Backup device power
<b>Serial Interface</b>			
SCL	6	I	I <sup>2</sup> C serial interface clock
SDA	5	I/O	I <sup>2</sup> C serial data
<b>Interrupt</b>			
IRQ	7	O	Configurable interrupt output. Open-drain output.
<b>Oscillator</b>			
OSCI	1	-	Oscillator input
OSCO	2	-	Oscillator output

## FUNCTIONAL BLOCK DIAGRAM AND APPLICATION CIRCUIT



NOTE: All pullup resistors should be connected to V<sub>CC</sub> such that no pullup is applied during backup supply operation.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			LIMIT	UNIT
V <sub>IN</sub>	Input voltage	V <sub>CC</sub> to GND	–0.3 to 4	V
		All other pins to GND	–0.3 to V <sub>CC</sub> + 0.3	V
T <sub>J</sub>	Operating junction temperature		–40 to 150	°C
T <sub>STG</sub>	Storage temperature range after reflow		–60 to 150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V <sub>CC</sub>	Supply voltage, V <sub>CC</sub> to GND	3		3.6	V
T <sub>A</sub>	Operating free-air temperature	–40		85	°C
f <sub>o</sub>	Crystal resonant frequency		32.768		kHz
R <sub>S</sub>	Crystal series resistance			40	kΩ
C <sub>L</sub>	Crystal load capacitance		12		pF

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

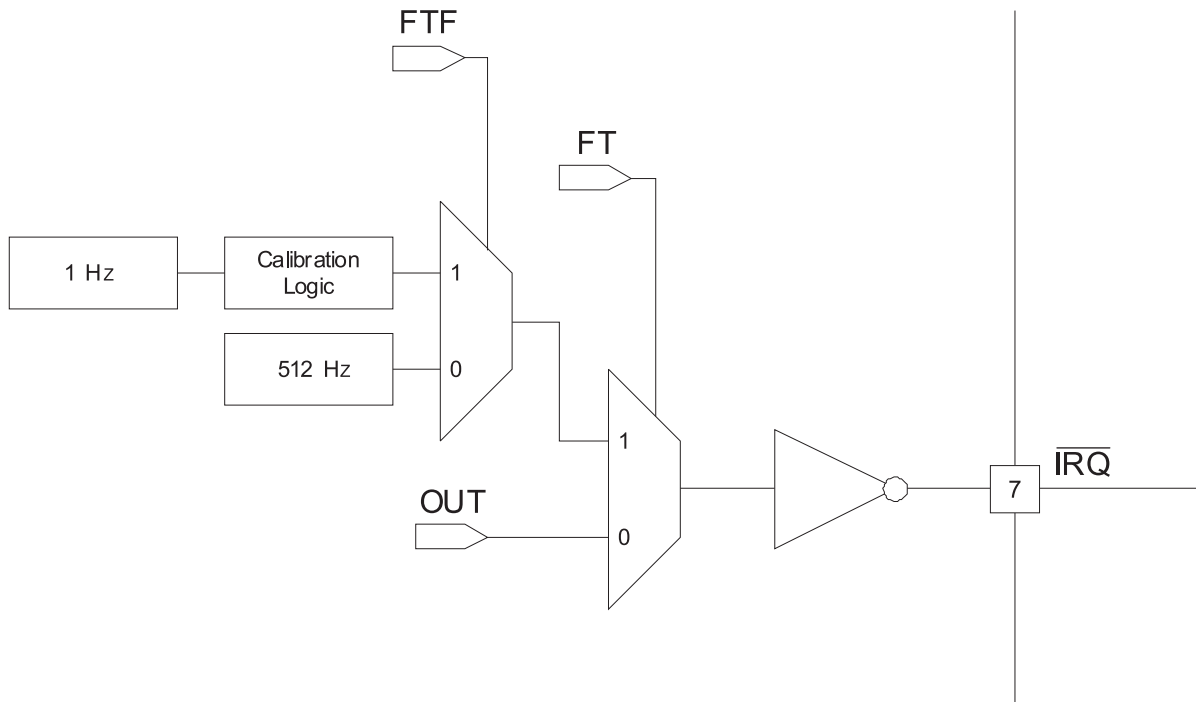
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
I <sub>CC</sub>	V <sub>CC</sub> supply current		65			μA
V <sub>BACK</sub>	Backup supply voltage	Operating	1.4		V <sub>CC</sub>	V
		Switchover	2.0		V <sub>CC</sub>	
I <sub>BACK</sub>	Backup supply current	V <sub>CC</sub> = 0 V, V <sub>BAT</sub> = 3 V, Oscillator on, T <sub>A</sub> = 25°C		0.9	1.5	μA
V <sub>SO</sub>	Switchover voltage	Operating → Backup		1.8		V
		Backup → Operating		2.4		
Logic Level Inputs						
V <sub>IL</sub>	Input low voltage		0.3 V <sub>CC</sub>			V
V <sub>IH</sub>	Input high voltage		0.7 V <sub>CC</sub>			V
I <sub>IN</sub>	Input current	0 V ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>		-1	1	μA
Logic Level Outputs						
V <sub>OL</sub>	Output low voltage	I <sub>OL</sub> = 3 mA			0.4	V
I <sub>L</sub>	Leakage current			-1	1	μA
Real-Time Clock Characteristics						
	Pre-calibration accuracy	V <sub>CC</sub> = 3.3 V, V <sub>BAT</sub> = 3 V, Oscillator on, T <sub>A</sub> = 25°C		±35 <sup>(1)</sup>		ppm

- (1) Typical accuracy is measured using reference board design and KDS DMX-26S surface-mount 32.768-kHz crystal. Variation in board design and crystal section results in different typical accuracy.

## DEVICE INFORMATION

### $\overline{\text{IRQ}}$ Function

The  $\overline{\text{IRQ}}$  pin of the BQ32002 functions as a general-purpose output or a frequency test output. The function of  $\overline{\text{IRQ}}$  is configurable in the device register space by setting the FT, FTF, and OUT bits. On initial power cycles, the OUT bit is set to one, and the FTF and FT bits are set to zero. On subsequent power-ups, with backup supply present, the OUT bit remains unchanged, and the FTF and FT bits are set to zero. When operating on backup supply, the  $\overline{\text{IRQ}}$  pin function is unused.  $\overline{\text{IRQ}}$  pullup resistor should be tied to  $V_{CC}$  to prevent  $\overline{\text{IRQ}}$  operation when operating on backup supply. The effect of the calibration logic is not normally observable when  $\overline{\text{IRQ}}$  is configured to output 1 Hz. The calibration logic functions by periodically adjusting the width of the 1-Hz clock. The calibration effect is observable only every eight or sixteen minutes, depending on the sign of the calibration.



**Figure 1.  $\overline{\text{IRQ}}$  Pin Functional Diagram**

**Table 1.  $\overline{\text{IRQ}}$  Function**

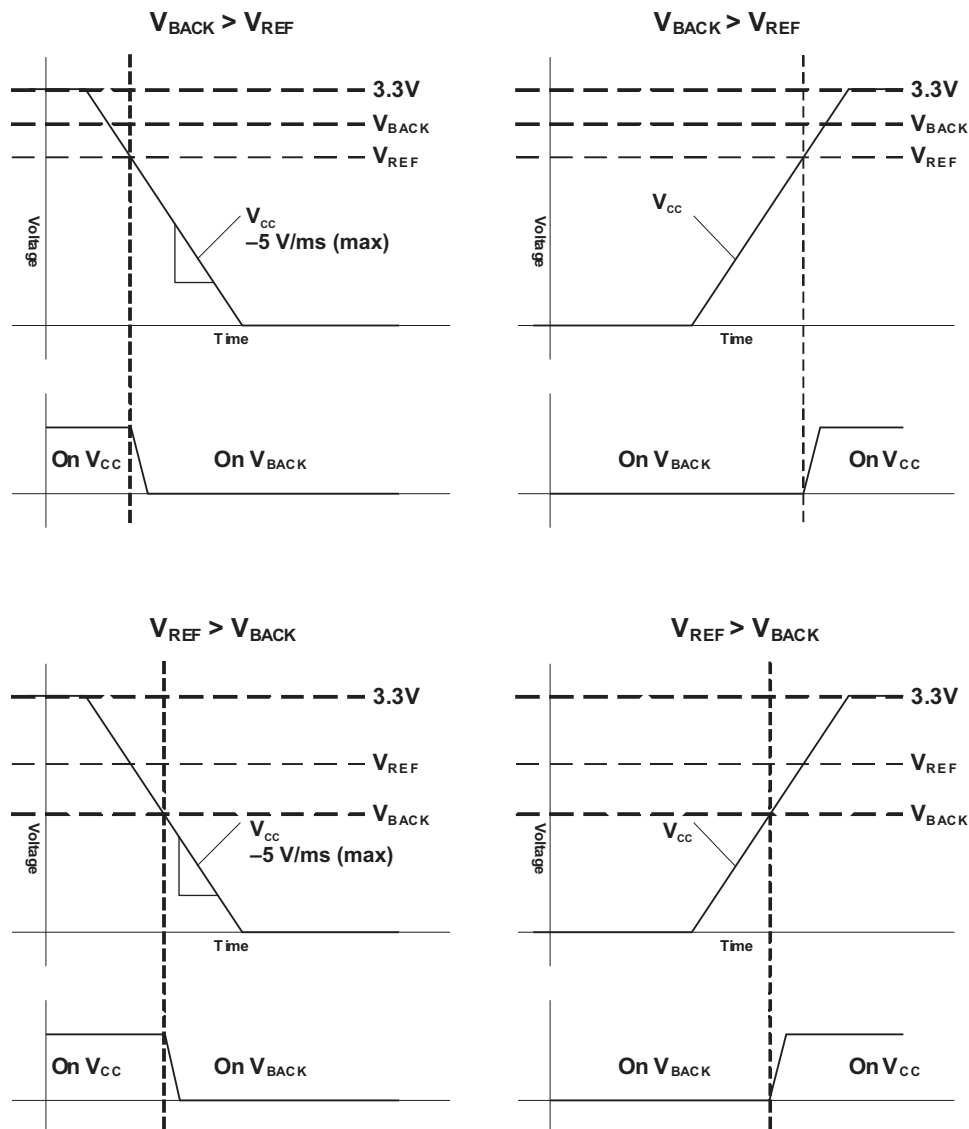
FT	OUT	FTF	$\overline{\text{IRQ}}$ STATE
1	X	1	1 Hz
1	X	0	512 Hz
0	1	X	1
0	0	X	0

## $V_{BACK}$ Switchover

The BQ32002 has an internal switchover circuit that causes the device to switch from main power supply to backup power supply when the voltage of the main supply pin  $V_{CC}$  drops below a minimum threshold. The  $V_{BACK}$  switchover circuit uses an internal reference voltage  $V_{REF}$  derived from the on-chip bandgap reference;  $V_{REF}$  is approximately 1.8 V. The device switches to the  $V_{BACK}$  supply when  $V_{CC}$  is less than the lesser of  $V_{BACK}$  or  $V_{REF}$ . Similarly, the device switches to the  $V_{CC}$  supply when  $V_{CC}$  is greater than either  $V_{BACK}$  or  $V_{REF}$ .

Some registers are reset to default values when the RTC switches from main power supply to backup power supply. Please see the register definitions to determine what register bits are effected by a backup switchover (effected bits have thier reset value (1/0) shown for 'Cycle', bits that are unchanged by backup are made 'UC').

The time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.



**Figure 2. Switchover Diagram**

## I<sup>2</sup>C Serial Interface

The I<sup>2</sup>C interface allows control and monitoring of the RTC by a microcontroller. I<sup>2</sup>C is a two-wire serial interface developed by Philips Semiconductor (see I<sup>2</sup>C-Bus Specification, Version 2.1, January 2000).

The bus consists of a data line (SDA) and a clock line (SCL) with off-chip pullup resistors. When the bus is idle, both SDA and SCL lines are pulled high.

A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer.

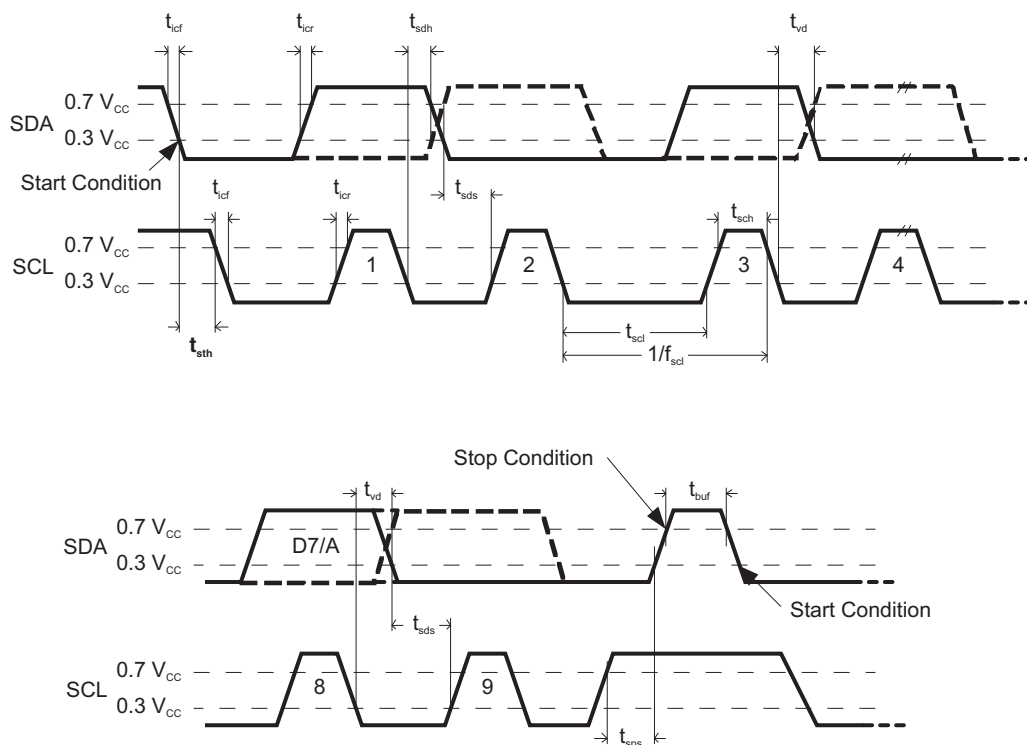
A slave device receives and/or transmits data on the bus under control of the master device. This device operates only as a slave device.

I<sup>2</sup>C communication is initiated by a master sending a start condition, a high-to-low transition on the SDA I/O while SCL is held high. After the start condition, the device address byte is sent, most-significant bit (MSB) first, including the data direction bit (R/W). After receiving a valid address byte, this device responds with an acknowledge, a low on the SDA I/O during the high of the acknowledge-related clock pulse. This device responds to the I<sup>2</sup>C slave address 11010000b for write commands and slave address 11010001b for read commands.

This device does not respond to the general call address.

A data byte follows the address acknowledge. If the R/W bit is low, the data is written from the master. If the R/W bit is high, the data from this device are the values read from the register previously selected by a write to the subaddress register. The data byte is followed by an acknowledge sent from this device. Data is output only if complete bytes are received and acknowledged.

A stop condition, which is a low-to-high transition on the SDA I/O while the SCL input is high, is sent by the master to terminate the transfer. A master device must wait at least 60  $\mu$ s after the RTC exits backup mode to generate a START condition.

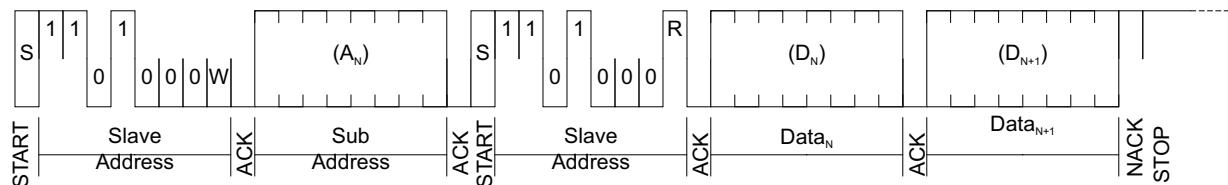
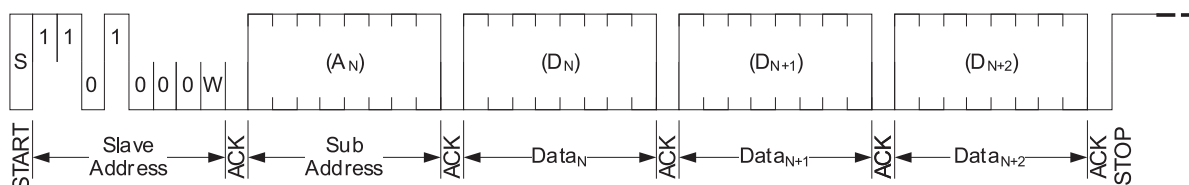


**Figure 3. I<sup>2</sup>C Timing Diagram**

**Table 2. I<sup>2</sup>C Timing**

PARAMETER	STANDARD MODE			FAST MODE			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
$f_{scl}$ I <sup>2</sup> C clock frequency	0		100	0		400	kHz
$t_{sch}$ I <sup>2</sup> C clock high time	4			0.6			μs
$t_{scl}$ I <sup>2</sup> C clock low time	4.7			1.3			μs
$t_{sp}$ I <sup>2</sup> C spike time	0		50	0		50	ns
$t_{sds}$ I <sup>2</sup> C serial data setup time	250			100			ns
$t_{sdh}$ I <sup>2</sup> C serial data hold time	0			0			ns
$t_{icr}$ I <sup>2</sup> C input rise time			1000	$20 + 0.1C_b^{(1)}$		300	ns
$t_{icf}$ I <sup>2</sup> C input fall time			300	$20 + 0.1C_b^{(1)}$		300	ns
$t_{ocf}$ I <sup>2</sup> C output fall time			300	$20 + 0.1C_b^{(1)}$		300	μs
$t_{buf}$ I <sup>2</sup> C bus free time	4.7			1.3			μs
$t_{sts}$ I <sup>2</sup> C Start setup time	4.7			0.6			μs
$t_{sth}$ I <sup>2</sup> C Start hold time	4			0.6			μs
$t_{sps}$ I <sup>2</sup> C Stop setup time	4			0.6			μs
$t_{vd (data)}$ Valid data time (SCL low to SDA valid)			1			1	μs
$t_{vd (ack)}$ Valid data time of ACK (ACK signal from SCL low to SDA low)			1			1	μs

(1)  $C_b$  = total capacitance of one bus line in pF

**Figure 4. I<sup>2</sup>C Read Mode****Figure 5. I<sup>2</sup>C Write Mode**



## Register Maps

**Table 3. Normal Registers**

REGISTER	ADDRESS (HEX)	REGISTER NAME	DESCRIPTION
0	0x00	SECONDS	Clock seconds and STOP bit
1	0x01	MINUTES	Clock minutes
2	0x02	CENT_HOURS	Clock hours, century, and CENT_EN bit
3	0x03	DAY	Clock day
4	0x04	DATE	Clock date
5	0x05	MONTH	Clock month
6	0x06	YEARS	Clock years
7	0x07	CAL_CFG1	Calibration and configuration
9	0x09	CFG2	Configuration 2

**Table 4. Special Function Registers**

REGISTER	ADDRESS (HEX)	REGISTER NAME	DESCRIPTION
32	0x20	SF KEY 1	Special function key 1
33	0x21	SF KEY 2	Special function key 2
34	0x22	SFR	Special function register

## Normal Register Descriptions

**Table 5. SECONDS Register**

**Address** 0x00  
**Name** SECONDS  
**Initial Value** 0XXXXXXb  
**Description** Clock seconds and STOP bit

D7	D6	D5	D4	D3	D2	D1	D0	BIT(S)
STOP	10_SECOND			1_SECOND				Name
r/w	r/w			r/w				Read/Write
0	X	X	X	X	X	X	X	Initial
UC	UC	UC	UC	UC	UC	UC	UC	Cycle

**STOP** Oscillator stop. The STOP bit is used to force the oscillator to stop oscillating. STOP is set to 0 on initial application of power, on all subsequent power cycles STOP remains unchanged. On initial power application STOP can be written to 1 and then written to 0 to force start the oscillator.

0 Normal  
 1 Stop

**10\_SECOND** BCD of tens of seconds. The 10\_SECOND bits are the BCD representation of the number of tens of seconds on the clock. Valid values are 0 to 5. If invalid data is written to 10\_SECOND, the clock will update with invalid data in 10\_SECOND until the counter rolls over; thereafter, the data in 10\_SECOND is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

**1\_SECOND** BCD of seconds. The 1\_SECOND bits are the BCD representation of the number of seconds on the clock. Valid values are 0 to 9. If invalid data is written to 1\_SECOND, the clock will update with invalid data in 1\_SECOND until the counter rolls over; thereafter, the data in 1\_SECOND is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

**Table 6. MINUTES Register**

**Address** 0x01  
**Name** MINUTES  
**Initial Value** 1XXXXXXb  
**Description** Clock minutes

D7	D6	D5	D4	D3	D2	D1	D0	BIT(S)
OF	10_MINUTE			1_MINUTE				Name
r/w	r/w			r/w				Read/Write
1	X	X	X	X	X	X	X	Initial
0	UC	UC	UC	UC	UC	UC	UC	Cycle

**OF** Oscillator fail flag. The OF bit is a latched flag indicating when the 32.768-kHz oscillator has dropped at least four consecutive pulses. The OF flag is always set on initial power-up, and it can be cleared through the serial interface. When OF is 0, no oscillator failure has been detected. When OF is 1, the oscillator fail detect circuit has detected at least four consecutive dropped pulses.

0 No failure detected  
 1 Failure detected

**10\_MINUTE** BCD of tens of minutes. The 10\_MINUTE bits are the BCD representation of the number of tens of minutes on the clock. Valid values are 0 to 5. If invalid data is written to 10\_MINUTE, the clock will update with invalid data in 10\_MINUTE until the counter rolls over; thereafter, the data in 10\_MINUTE is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

**1\_MINUTE** BCD of minutes. The 1\_MINUTE bits are the BCD representation of the number of minutes on the clock. Valid values are 0 to 9. If invalid data is written to 1\_MINUTE, the clock will update with invalid data in 1\_MINUTE until the counter rolls over; thereafter, the data in 1\_MINUTE is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

**Table 7. CENT\_HOURS Register**

**Address** 0x02  
**Name** CENT\_HOURS  
**Initial Value** XXXXXXXXb  
**Description** Clock hours, century, and CENT\_EN bit

D7	D6	D5	D4	D3	D2	D1	D0	BIT(S)
CENT_EN	CENT	10_HOUR		1_HOUR				Name
r/w	r/w	r/w		r/w				Read/Write
X	X	X	X	X	X	X	X	Initial
UC	UC	UC	UC	UC	UC	UC	UC	Cycle

**CENT\_EN** Century enable. The CENT\_EN bit enables the century timekeeping feature. If CENT\_EN is set to 1, then the clock tracks the century using the CENT bit. If CENT\_EN is set to 0, the clock ignores the CENT bit.

0 Century disabled  
 1 Century enabled

**CENT** Century. The CENT bit tracks the century when century timekeeping is enabled. The clock toggles the CENT bit when the year count rolls from 99 to 00. Because the clock compliments the CENT bit, the user can define the meaning of CENT (1 for current century and 0 for next century, or 0 for current century and 1 for next century).

**10\_HOUR** BCD of tens of hours (24-hour format). The 10\_HOUR bits are the BCD representation of the number of tens of hours on the clock, in 24-hour format. Valid values are 0 to 2. If invalid data is written to 10\_HOUR, the clock will update with invalid data in 10\_HOUR until the counter rolls over; thereafter, the data in 10\_HOUR is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

**1\_HOUR** BCD of hours (24-hour format). The 1\_HOUR bits are the BCD representation of the number of hours on the clock, in 24-hour format. Valid values are 0 to 9. If invalid data is written to 1\_HOUR, the clock will update with invalid data in 1\_HOUR until the counter rolls over; thereafter, the data in 1\_HOUR is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

**Table 8. DAY Register**

**Address** 0x03  
**Name** DAY  
**Initial Value** 00000XXXb  
**Description** Clock day

D7	D6	D5	D4	D3	D2	D1	D0	BIT(S)
RSVD					DAY			Name
r/w					r/w			Read/Write
0	0	0	0	0	X	X	X	Initial
0	0	0	0	0	UC	UC	UC	Cycle

**RSVD** Reserved. The RSVD bits should always be written as 0.

**DAY** BCD of the day of the week. The DAY bits are the BCD representation of the day of the week. Valid values are 1 to 7 and represent the days from Sunday to Saturday. DAY updates if set to 0 until the counter rolls over; thereafter, the data in DAY is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

1 Sunday  
 2 Monday  
 3 Tuesday  
 4 Wednesday  
 5 Thursday  
 6 Friday  
 7 Saturday

**Table 9. DATE Register**

**Address** 0x04  
**Name** DATE  
**Initial Value** 00XXXXXXb  
**Description** Clock date

D7	D6	D5	D4	D3	D2	D1	D0	BIT(S)
RSVD		10_DATE		1_DATE				Name
r/w		r/w		r/w				Read/Write
0	0	X	X	X	X	X	X	Initial
0	0	UC	UC	UC	UC	UC	UC	Cycle

RSVD Reserved. The RSVD bits should always be written as 0.

10\_DATE BCD of tens of date. The 10\_DATE bits are the BCD representation of the tens of date on the clock. Valid values are 0 to 3<sup>(1)</sup>. If invalid data is written to 10\_DATE, the clock will update with invalid data in 10\_DATE until the counter rolls over; thereafter, the data in 10\_DATE is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

1\_DATE BCD of date. The 1\_DATE bits are the BCD representation of the date on the clock. Valid values are 0 to 9<sup>(1)</sup>. If invalid data is written to 1\_DATE, the clock will update with invalid data in 1\_DATE until the counter rolls over; thereafter, the data in 1\_DATE is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

(1) 10\_DATE and 1\_DATE must form a valid date, 01 to 31, dependent on month and year.

**Table 10. MONTH Register**

**Address** 0x05  
**Name** MONTH  
**Initial Value** 000XXXXXb  
**Description** Clock month

D7	D6	D5	D4	D3	D2	D1	D0	BIT(S)
RSVD			10_MONTH	1_MONTH				Name
r/w			r/w	r/w				Read/Write
0	0	0	X	X	X	X	X	Initial
0	0	0	UC	UC	UC	UC	UC	Cycle

RSVD Reserved. The RSVD bits should always be written as 0.

10\_MONTH BCD of tens of month. The 10\_MONTH bits are the BCD representation of the tens of month on the clock. Valid values are 0 to 1<sup>(1)</sup>. If invalid data is written to 10\_MONTH, the clock will update with invalid data in 10\_MONTH until the counter rolls over; thereafter, the data in 10\_MONTH is valid.

1\_MONTH BCD of month. The 1\_MONTH bits are the BCD representation of the month on the clock. Valid values are 0 to 9<sup>(1)</sup>. If invalid data is written to 1\_MONTH, the clock will update with invalid data in 1\_MONTH until the counter rolls over; thereafter, the data in 1\_MONTH is valid.

(1) 10\_MONTH and 1\_MONTH must form a valid date, 01 to 12.

**Table 11. YEARS Register**

**Address** 0x06  
**Name** YEARS  
**Initial Value** XXXXXXXXb  
**Description** Clock year

D7	D6	D5	D4	D3	D2	D1	D0	BIT(S)
10_YEAR				1_YEAR				Name
r/w				r/w				Read/Write
X	X	X	X	X	X	X	X	Initial
UC	UC	UC	UC	UC	UC	UC	UC	Cycle

**10\_YEAR** BCD of tens of years. The 10\_YEAR bits are the BCD representation of the tens of years on the clock. Valid values are 0 to 9. If invalid data is written to 10\_YEAR, the clock will update with invalid data in 10\_YEAR until the counter rolls over; thereafter, the data in 10\_YEAR is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

**1\_YEAR** BCD of year. The 1\_YEAR bits are the BCD representation of the years on the clock. Valid values are 0 to 9. If invalid data is written to 1\_YEAR, the clock will update with invalid data in 1\_YEAR until the counter rolls over; thereafter, the data in 1\_YEAR is valid. Time keeping registers can take up to 1 second to update after the RTC switches from backup power supply to main power supply.

**Table 12. CAL\_CFG1 Register**

**Address** 0x07  
**Name** CAL\_CFG1  
**Initial Value** 10000000b  
**Description** Calibration and control

D7	D6	D5	D4	D3	D2	D1	D0	BIT(S)
OUT	FT	S	CAL					Name
r/w	r/w	r/w	r/w					Read/Write
1	0	0	0	0	0	0	0	Initial
UC	UC	UC	UC	UC	UC	UC	UC	Cycle

**OUT** Logic output, when FT = 0. When FT is zero, the logic output of  $\overline{\text{IRQ}}$  pin reflects the value of OUT.

0  $\overline{\text{IRQ}}$  is logic 0

1  $\overline{\text{IRQ}}$  is logic 1

**FT** Frequency test. The FT bit is used to enable the frequency test signal on the  $\overline{\text{IRQ}}$  pin. When FT is 1, a square wave is produced on the  $\overline{\text{IRQ}}$  pin. The FTF bit in the SFR register determines the frequency of the test signal.

0 Disable

1 Enable

**S** Calibration sign. The S bit determines the polarity of the calibration applied to the oscillator. If S is 0, then the calibration slows the RTC. If S is 1, then the calibration speeds the RTC.

0 Slowing (+)

1 Speeding (–)

**CAL** Calibration. The CAL bits along with S determine the calibration amount as shown in [Table 13](#).

**Table 13. Calibration**

CAL (DEC)	S = 0	S = 1
0	+0 ppm	–0 ppm
1	+2 ppm	–4 ppm
N	+N / 491520 (per minute)	–N / 245760 (per minute)
30	+61 ppm	–122 ppm
31	+63 ppm	–126 ppm

**Table 14. CFG2 Register**

**Address** 0x09  
**Name** CFG2  
**Initial Value** 10101010b  
**Description** Configuration 2

D7	D6	D5	D4	D3	D2	D1	D0	BIT(S)
RSVD	RSVD	RSVD		RSVD				Name
r/w	r/w	r/w		r/w				Read/Write
1	0	1	0	1	0	1	0	Initial
1	0	UC	UC	1	0	1	0	Cycle

RSVD Reserved. The RSVD bits should always be written as 0.

## Special Function Registers

**Table 15. SF KEY 1 Register**

**Address** 0x20  
**Name** SF KEY 1  
**Initial Value** 00000000b  
**Description** Special function key 1

D7	D6	D5	D4	D3	D2	D1	D0	BIT(S)
SF KEY B1								Name
r/w								Read/Write
0	0	0	0	0	0	0	0	Initial
0	0	0	0	0	0	0	0	Cycle

SF KEY B1 Special function access key byte 1. Reads as 0x00, and key is 0x5E.

The SF KEY 1 and SF KEY 2 registers are used to enable access to the main special function register (SFR). Access to SFR is granted only after the special function keys are written sequentially to SF KEY 1 and SF KEY 2. Each write to the SFR must be preceded by writing the SF keys to the SF key registers, in order, SF KEY 1 then SF KEY 2.

**Table 16. SF KEY 2 Register**

**Address** 0x21  
**Name** SF KEY 2  
**Initial Value** 00000000b  
**Description** Special function key 2

D7	D6	D5	D4	D3	D2	D1	D0	BIT(S)
SF KEY 2								Name
r/w								Read/Write
0	0	0	0	0	0	0	0	Initial
0	0	0	0	0	0	0	0	Cycle

SF KEY 2 Special function access key byte 2. Reads as 0x00, and key is 0xC7.

The SF KEY 1 and SF KEY 2 registers are used to enable access to the main special function register (SFR). Access to SFR is granted only after the special function keys are written sequentially to SF KEY 1 and SF KEY 2. Each write to the SFR must be preceded by writing the SF keys to the SF key registers, in order, SF KEY 1 then SF KEY 2.

**Table 17. SFR Register**

**Address** 0x22  
**Name** SFR  
**Initial Value** 00000000b  
**Description** Special function register 1

D7	D6	D5	D4	D3	D2	D1	D0	BIT(S)
RSVD							FTF	Name
r/w							r/w	Read/Write
0	0	0	0	0	0	0	0	Initial
0	0	0	0	0	0	0	0	Cycle

RSVD Reserved. The RSVD bits should always be written as 0.

FTF Force calibration to 1 Hz. FTF allows the frequency of the calibration output to be changed from 512 Hz to 1 Hz. By default, FTF is cleared, and the RTC outputs a 512-Hz calibration signal. Setting FTF forces the calibration signal to 1 Hz, and the calibration tracks the internal ppm adjustment. Note: The default 512-Hz calibration signal does not include the effect of the ppm adjustment.

0 Normal 512-Hz calibration  
 1 1-Hz calibration

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ32002D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	32002	<a href="#">Samples</a>
BQ32002DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		32002	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ32002DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ32002DR	SOIC	D	8	2500	367.0	367.0	35.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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