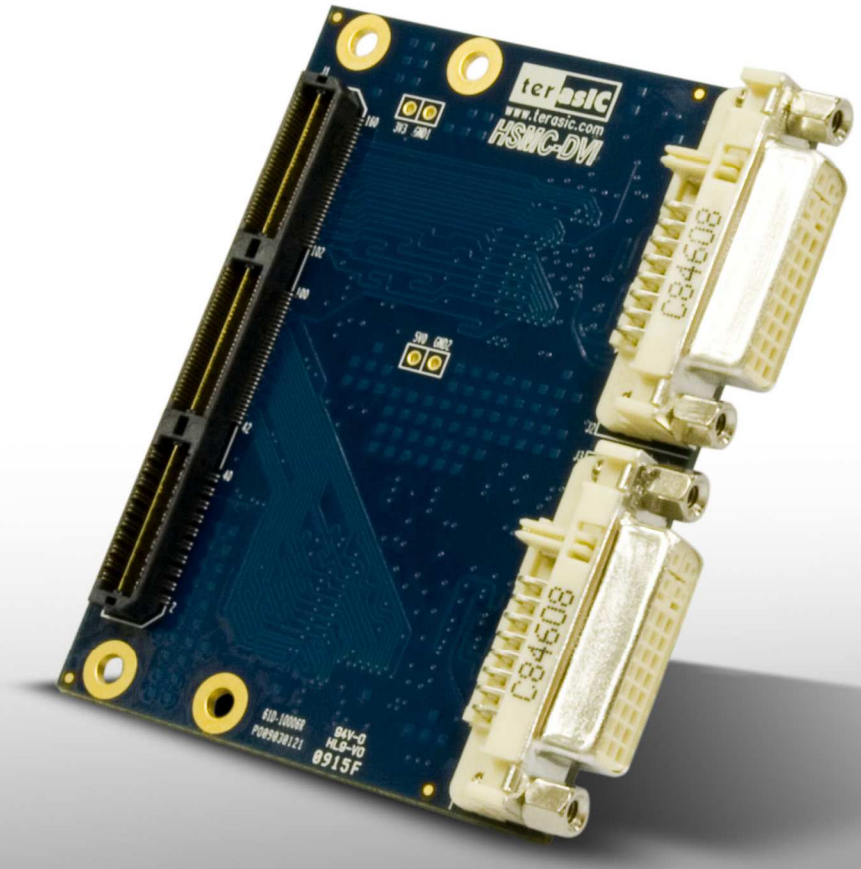
HSMC-DVI

Terasic HSMC-DVI Daughter Board

User Manual



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CHAPTER 1 Introduction

The Terasic HSMC-DVI is a DVI transmitter/receiver board with a High Speed Mezzanine Connector (HSMC) interface. It is designed to allow developers to access high quality and high resolution video signals in their FPGA. It gives the flexibility required in high resolution image processing systems by combining both the DVI transmitter and receiver onto the same card. Lastly, the HSMC-DVI daughter board can be connected to any HSMC/HSTC interface host boards.

1.1 Features

Figure 1.1 shows the photo of the HSMC-DVI board. The important features are listed below:

Digital Transmitter

- One DVI transmitter with single transmitting port
- Digital Visual Interface (DVI) Compliant
- Supports resolutions from VGA to UXGA (25 MHz – 165 MHz Pixel Rates)
- Universal Graphics Controller Interface
  - ✓ 12-Bit, Dual-Edge and 24-Bit, Single-Edge Input Modes
  - ✓ Adjustable 1.1 V to 1.8 V and Standard 3.3 V CMOS Input Signal Levels
  - ✓ Fully Differential and Single-Ended Input Clocking Modes
  - ✓ Standard Intel 12-Bit Digital Video Port Compatible as on Intel™ 81x Chipsets
- Enhanced PLL Noise Immunity
  - ✓ On-Chip Regulators and Bypass Capacitors for Reducing System Costs
- Enhanced Jitter Performance
  - ✓ No HSYNC Jitter Anomaly
  - ✓ Negligible Data-Dependent Jitter
- Programmable Using I²C Serial Interface
- Single 3.3-V Supply Operation

Digital Receiver

- One DVI receiver with single receiving port
- Supports UXGA Resolution (Output Pixel Rates Up to 165 MHz)
- Digital Visual Interface (DVI) Specification Compliant
- True-Color, 24 Bit/Pixel, 16.7M Colors at 1 or 2-Pixels Per Clock
- Laser Trimmed Internal termination Resistors for Optimum Fixed Impedance Matching
- 4x Over-Sampling
- Reduced Ground Bounce Using Time Staggered Pixel Outputs
- Lowest Noise and Best Power Dissipation Using TI PowerPAD™ Packaging

Figure 1.1. The HSMC-DVI board

1.2 About the KIT

This section describes the package content

- HSMC-DVI board x 1
- System CD-ROM x 1

The CD contains technical documents of the HSMC-DVI, and one reference design along with the source code.

Figure 1.2 HSMC-DVI Package

The source code of reference design are available for the following FPGA main board:

- DE3

Figure 1.2.1 The HSMC-DVI board connects with DE3

- Cyclone III Starter Board

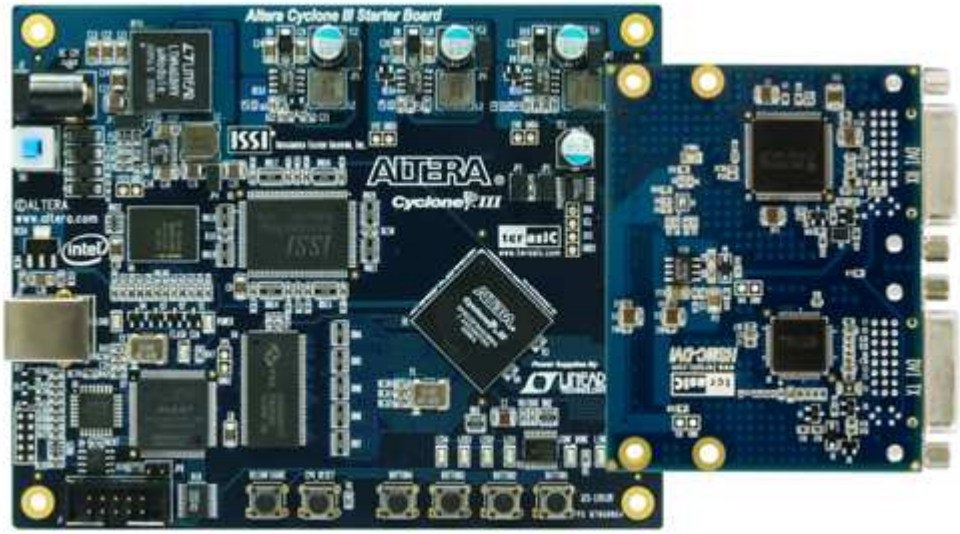


Figure 1.2.2. The HSMC-DVI board connects with Cyclone III Starter Board

- Cyclone III FPGA Development Kit

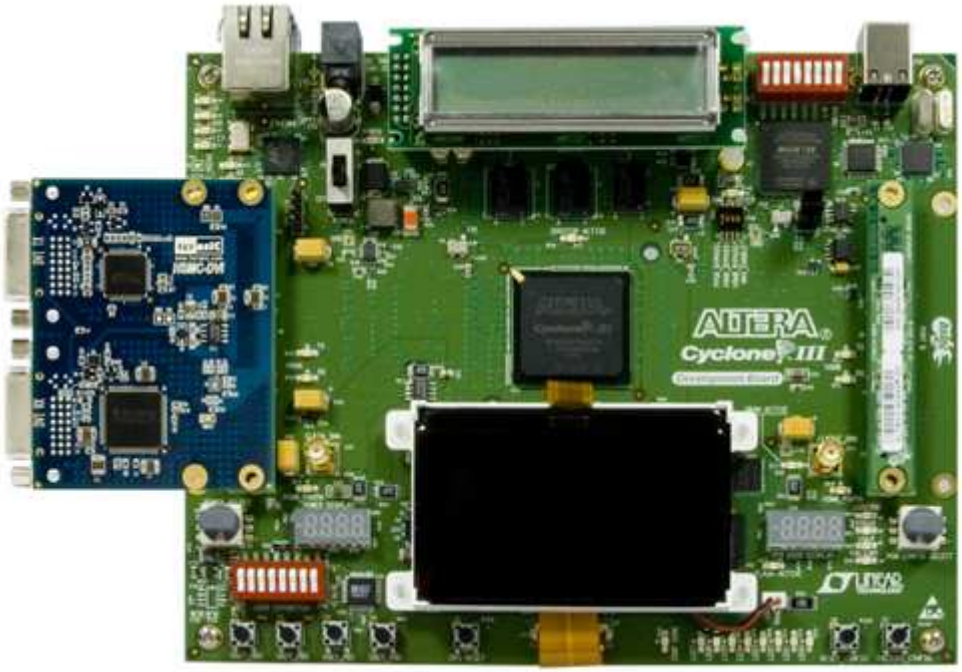


Figure 1.2.3 The HSMC-DVI board connects with Cyclone III Development Board

- Stratix III FPGA Development Kit

Figure 1.2.4. The HSMC-DVI board connects with Stratix III Development Board

1.3 Assemble the HSMC-DVI Board

This section describes how to connect the HSMC-DVI daughter board to a main board, and using DE3 as an example.

The HSMC-DVI daughter board connects to the main boards through the HSTC interface. For the DE3, the HSMC-DVI can be connected to any DE3's four HSTC connectors using a THCB-HFF adapter card (Figure 1.3.1) which can be found in the DE3 package.

Figure 1.3.1 THCB-HFF adapter card

Figure 1.3.2 The HSMC-DVI board connects with DE3

Note. Do not attempt to connect/remove the HSMC-DVI daughter board to/from the main the main board when the power is on, or else the hardware could be damaged.

1.4 Getting Help

Here are some places to get help if you encounter any problem:

- ✓ Email to support@terasic.com
- ✓ Taiwan & China: +886-3-550-8800
- ✓ Korea : +82-2-512-7661
- ✓ Japan: +81-428-77-7000

CHAPTER 2 Architecture

This Chapter covers the architecture of the HSMC-DVI board including its PCB and block diagram.

2.1 Layout and Componets

The picture of the HSMC-DVI board is shown in Figure 2.1.1 and Figure 2.1.2 It depicts the layout of the board and indicates the location of the connectors and key components.

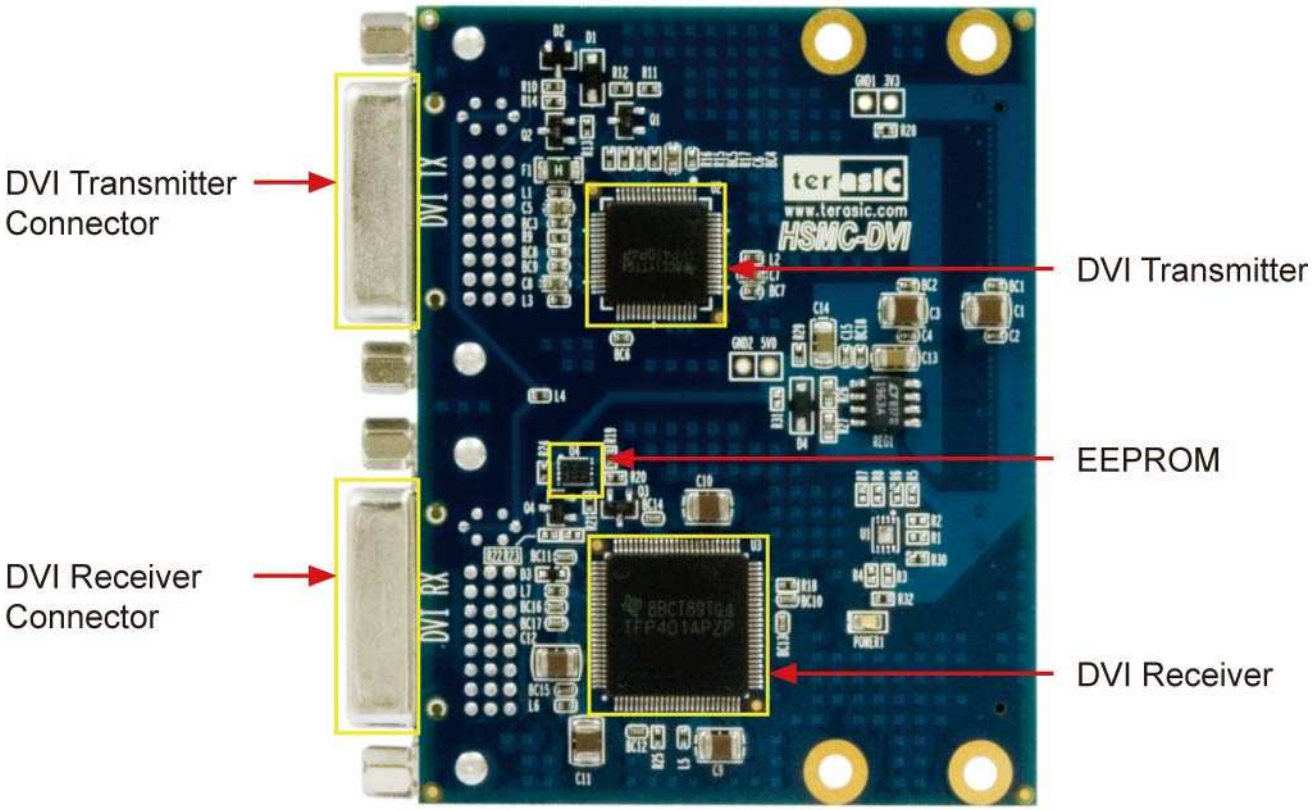


Figure 2.1.1 The HSMC-DVI PCB and component diagram

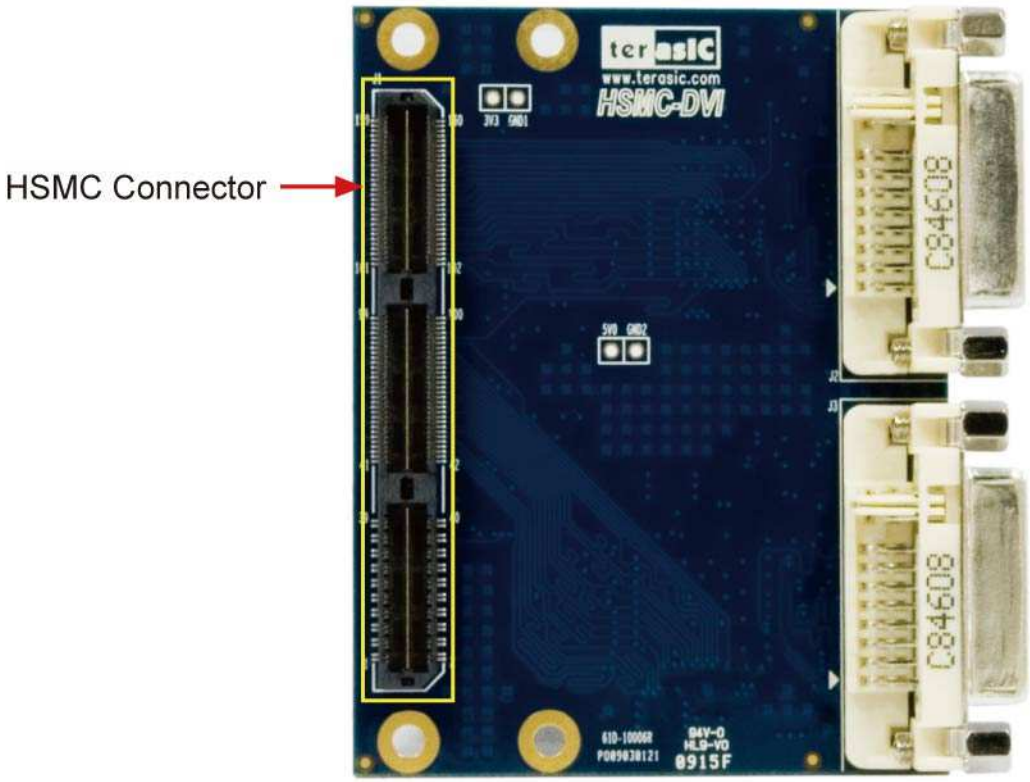


Figure 2.1.2 The HSMC-DVI Back side – HSMC connector view

The following components are provided on the HSMC-DVI board :

- DVI Transmitter (U2)
- DVI Receiver (U3)
- I2C EEPROM (U4)
- DVI Transmitter Connector (J2)
- DVI Receiver Connector (J3)
- HSMC Connector (J1)

2.2 Block Diagram

Figure 2.2.1 shows the block diagram of the HSMC-DVI board

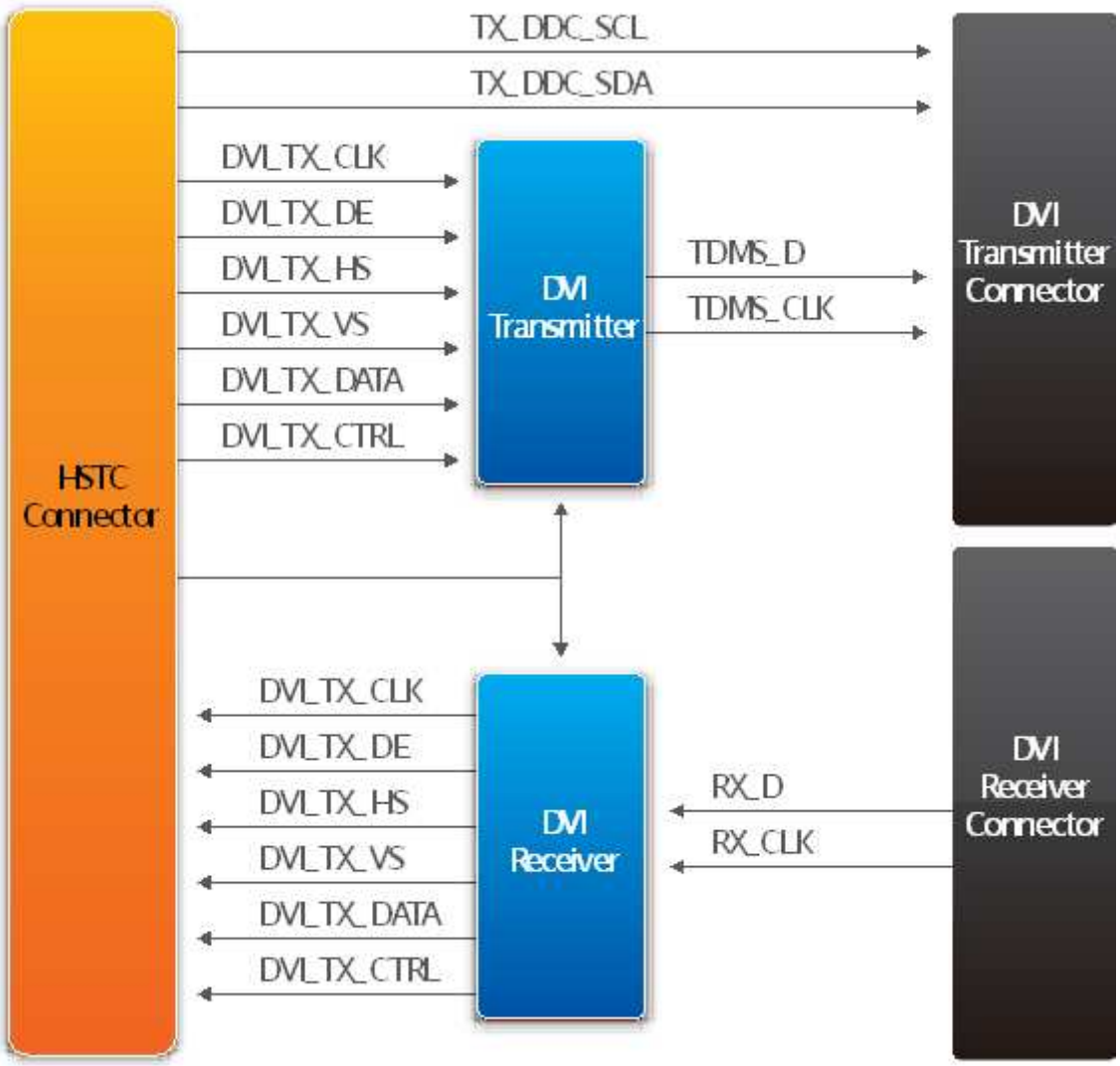


Figure 2.2.1 The block diagram of the HSMC-DVI board

CHAPTER 3 Board Components

This section illustrates the detailed information of the components, connector interfaces, and the pin mapping tables of the HSMC-DVI board

3.1 The HSMC-DVI Connector

This section describes pin definition of the HSMC-DVI interface onboard

All the control and data signals of the DVI transmitter and receiver are connected to the HSMC connector, so users can fully control the HSMC-DVI daughter board through the HSMC interface. Power is derived from 3.3V and 12V of the HSMC connector.

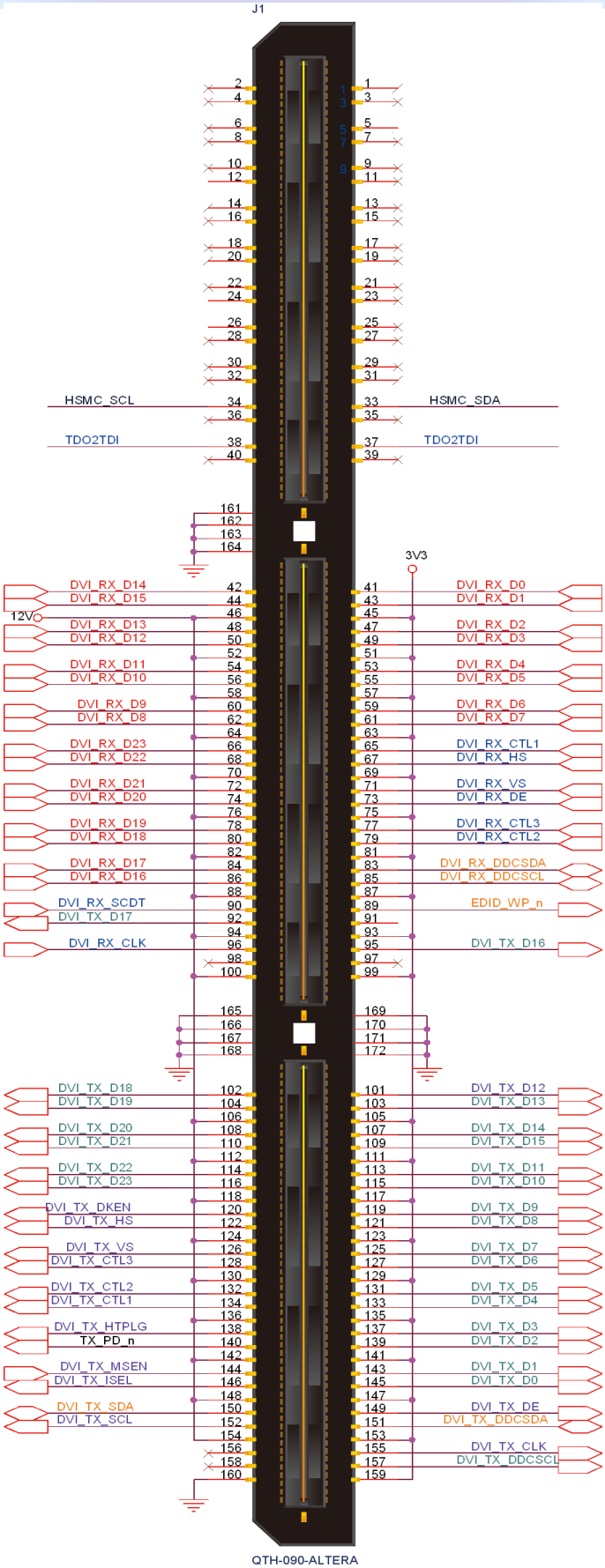


Figure 3.1. The pin-outs on the HSMC connector

The table 3.1 below lists the HSMC signal direction and description.

Note. The power pins are not shown in the table

Table 3.1

Pin Numbers	Name	Direction	Description
1	N.C.	N/A	Not Connect
2	N.C.	N/A	Not Connect
3	N.C.	N/A	Not Connect
4	N.C.	N/A	Not Connect
5	N.C.	N/A	Not Connect
6	N.C.	N/A	Not Connect
7	N.C.	N/A	Not Connect
8	N.C.	N/A	Not Connect
9	N.C.	N/A	Not Connect
10	N.C.	N/A	Not Connect
11	N.C.	N/A	Not Connect
12	N.C.	N/A	Not Connect
13	N.C.	N/A	Not Connect
14	N.C.	N/A	Not Connect
15	N.C.	N/A	Not Connect
16	N.C.	N/A	Not Connect
17	N.C.	N/A	Not Connect
18	N.C.	N/A	Not Connect
19	N.C.	N/A	Not Connect
20	N.C.	N/A	Not Connect
21	N.C.	N/A	Not Connect
22	N.C.	N/A	Not Connect
23	N.C.	N/A	Not Connect
24	N.C.	N/A	Not Connect
25	N.C.	N/A	Not Connect
26	N.C.	N/A	Not Connect
27	N.C.	N/A	Not Connect
28	N.C.	N/A	Not Connect
29	N.C.	N/A	Not Connect
30	N.C.	N/A	Not Connect
31	N.C.	N/A	Not Connect
32	N.C.	N/A	Not Connect
33	HSMC_SDA	Inout	I²C data

34	HSMC_SCL	Output	I²C clock
35	N.C.	N/A	Not Connect
36	N.C.	N/A	Not Connect
39	N.C.	N/A	Not Connect
40	N.C.	N/A	Not Connect
41	DVI_RX_D0	Input	DVI receiver pixel data
42	DVI_RX_D14	Input	DVI receiver pixel data
43	DVI_RX_D1	Input	DVI receiver pixel data
44	DVI_RX_D15	Input	DVI receiver pixel data
45	3V3	Power	Power 3.3V
46	12V	Power	Power 12V
47	DVI_RX_D2	Input	DVI receiver pixel data
48	DVI_RX_D13	Input	DVI receiver pixel data
49	DVI_RX_D3	Input	DVI receiver pixel data
50	DVI_RX_D12	Input	DVI receiver pixel data
51	3V3	Power	Power 3.3V
52	12V	Power	Power 12V
53	DVI_RX_D4	Input	DVI receiver pixel data
54	DVI_RX_D11	Input	DVI receiver pixel data
55	DVI_RX_D5	Input	DVI receiver pixel data
56	DVI_RX_D10	Input	DVI receiver pixel data
57	3V3	Power	Power 3.3V
58	12V	Power	Power 12V
59	DVI_RX_D6	Input	DVI receiver pixel data
60	DVI_RX_D9	Input	DVI receiver pixel data
61	DVI_RX_D7	Input	DVI receiver pixel data
62	DVI_RX_D8	Input	DVI receiver pixel data
63	3V3	Power	Power 3.3V
64	12V	Power	Power 12V
65	DVI_RX_CTL1	Input	Control signal
66	DVI_RX_D23	Input	DVI receiver pixel data
67	DVI_RX_HS	Input	DVI receiver horizontal sync
68	DVI_RX_D6	Input	DVI receiver pixel data
69	3V3	Power	Power 3.3V
70	12V	Power	Power 12V
71	DVI_RX_VS	Input	DVI receiver vertical sync
72	DVI_RX_D5	Input	DVI receiver pixel data
73	DVI_RX_DE	Input	DVI receiver pixel data

74	DVI_RX_D4	Input	DVI receiver pixel data
75	3V3	Power	Power 3.3V
76	12V	Power	Power 12V
77	DVI_RX_CTL3	Input	Control signal
78	DVI_RX_D3	Input	DVI receiver pixel data
79	DVI_RX_CTL2	Input	Control signal
80	DVI_RX_D2	Input	DVI receiver pixel data
81	3V3	Power	Power 3.3V
82	12V	Power	Power 12V
83	DVI_RX_DDCSDA	Inout	DDC I²C data
84	DVI_RX_D1	Input	DVI receiver pixel data
85	DVI_RX_DDSCL	Inout	DDC I²C clock
86	DVI_RX_D16	Input	DVI receiver pixel data
87	3V3	Power	Power 3.3V
88	12V	Power	Power 12V
89	EDID_WP_n	Output	I²C write protect enable
90	DVI_RX_SCDT	Input	Receiver sync detect
91	N.C.	N/A	Not Connect
92	DVI_TX_D17	Output	DVI transmitter data bus
93	3V3	Power	Power 3.3V
94	12V	Power	Power 12V
95	DVI_TX_D16	Output	DVI transmitter data bus
96	DVI_RX_CLK	Input	DVI receiver clock
97	N.C.	N/A	Not Connect
98	N.C.	N/A	Not Connect
99	3V3	Power	Power 3.3V
100	12V	Power	Power 12V
101	DVI_TX_D12	Output	DVI transmitter data bus
102	DVI_TX_D18	Output	DVI transmitter data bus
103	DVI_TX_D13	Output	DVI transmitter data bus
104	DVI_TX_D19	Output	DVI transmitter data bus
105	3V3	Power	Power 3.3V
106	12V	Power	Power 12V
107	DVI_TX_D14	Output	DVI transmitter data bus
108	DVI_TX_D20	Output	DVI transmitter data bus
109	DVI_TX_D15	Output	DVI transmitter data bus
110	DVI_TX_D21	Output	DVI transmitter data bus
111	3V3	Power	Power 3.3V

112	12V	Power	Power 12V
113	DVI_TX_D11	Output	DVI transmitter data bus
114	DVI_TX_D22	Output	DVI transmitter data bus
115	DVI_TX_D10	Output	DVI transmitter data bus
116	DVI_TX_D23	Output	DVI transmitter data bus
117	3V3	Power	Power 3.3V
118	12V	Power	Power 12V
119	DVI_TX_D9	Output	DVI transmitter data bus
120	DVI_TX_DKEN	Output	Data de-skew enable
121	DVI_TX_D8	Output	DVI transmitter data bus
122	DVI_TX_HS	Output	DVI transmitter Horizontal sync
123	3V3	Power	Power 3.3V
124	12V	Power	Power 12V
125	DVI_TX_D7	Output	DVI transmitter data bus
126	DVI_TX_VS	Output	DVI transmitter vertical sync
127	DVI_TX_D6	Output	DVI transmitter data bus
128	DVI_TX_CTL3	Output	Multifunction
129	3V3	Power	Power 3.3V
130	12V	Power	Power 12V
131	DVI_TX_D5	Output	DVI transmitter data bus
132	DVI_TX_CTL2	Output	Multifunction
133	DVI_TX_D4	Output	DVI transmitter data bus
134	DVI_TX_CTL1	Output	Multifunction
135	3V3	Power	Power 3.3V
136	12V	Power	Power 12V
137	DVI_TX_D3	Output	DVI transmitter data bus
138	DVI_TX_HTPLG	Output	Edge select/hot plug input
139	DVI_TX_D2	Output	DVI transmitter data bus
140	TX_PD_n	Output	Power down (active low)
141	3V3	Power	Power 3.3V
142	12V	Power	Power 12V
143	DVI_TX_D1	Output	DVI transmitter data bus
144	DVI_TX_MSEN	Input	Monitor sense/programmable output
145	DVI_TX_D0	Output	DVI transmitter data bus
146	DVI_TX_ISEL	Output	I²C interface select/I²C reset
147	3V3	Power	Power 3.3V
148	12V	Power	Power 12V
149	DVI_TX_DE	Output	DVI data enable

150	DVI_TX_SDA	I/O	DSEL/I²C data
151	DVI_TX_DDCSDA	I/O	DDC I²C data
152	DVI_TX_SCL	Output	Input bus select/I²C clock
153	3V3	Power	Power 3.3V
154	12V	Power	Power 12V
155	DVI_TX_CLK	Output	DVI transmitter clock
156	N.C.	N/A	Not Connect
157	DVI_TX_DDCSCL	Output	DDC I²C clock
158	N.C.	N/A	Not Connect
159	3V3	Power	Power 3.3V
160	GND	Power	Power Ground
161	GND	Power	Power Ground
162	GND	Power	Power Ground
163	GND	Power	Power Ground
164	GND	Power	Power Ground
165	GND	Power	Power Ground
166	GND	Power	Power Ground
167	GND	Power	Power Ground
168	GND	Power	Power Ground
169	GND	Power	Power Ground
170	GND	Power	Power Ground
171	GND	Power	Power Ground
172	GND	Power	Power Ground

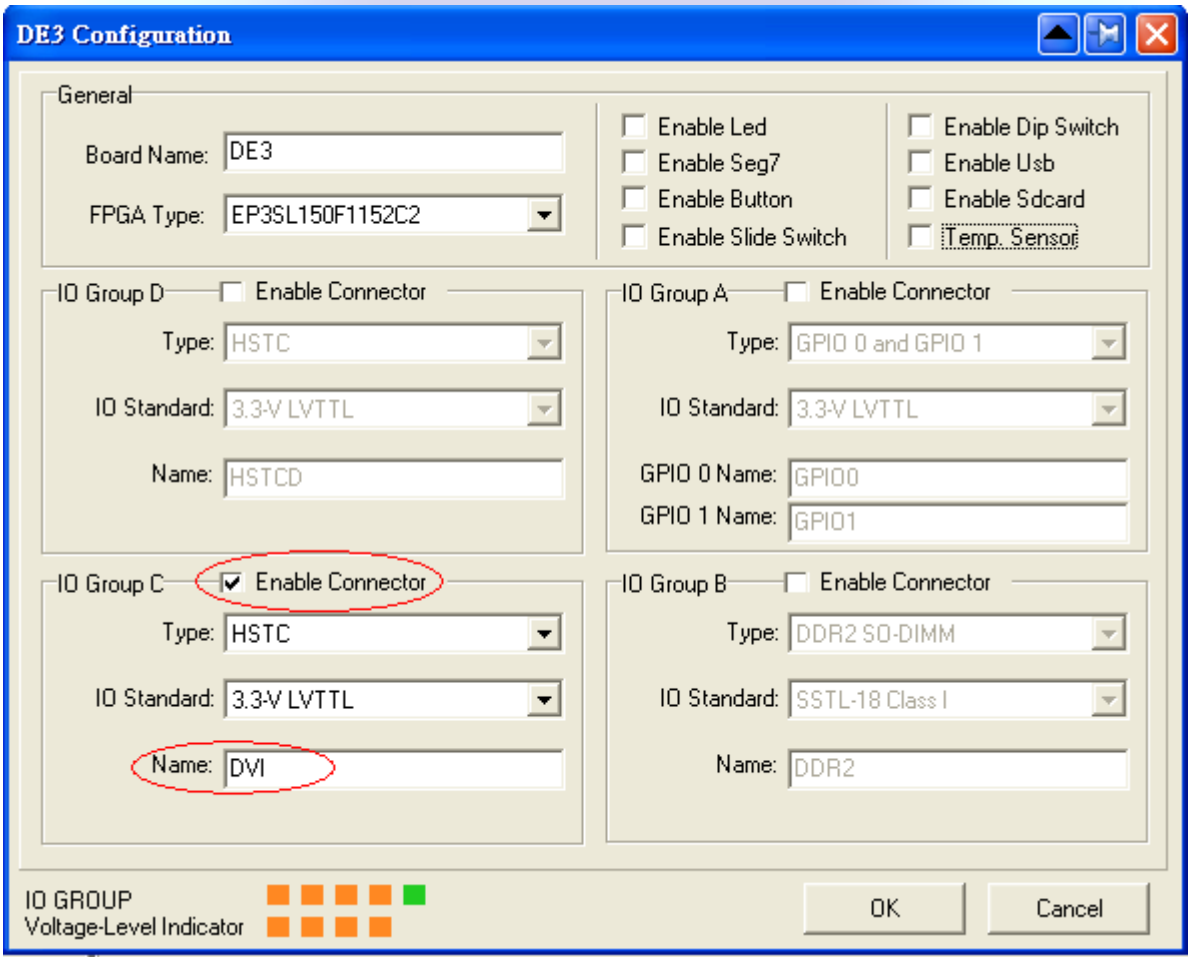
3.2 Generate Pin Assignments

This section describes how to automatically generate a top-level project, including DVI pin assignments

For the DE3 main board:

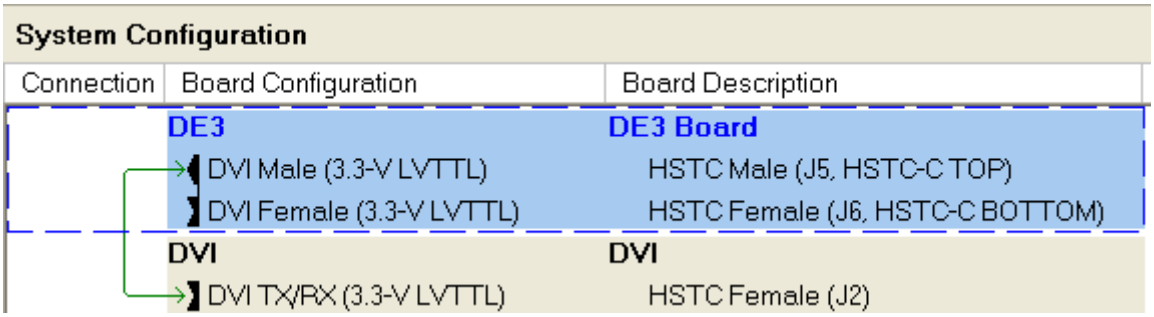
Users can easily create the HSMC-DVI board pin assignments by utilizing the DE3_System Builder V 1.4.3 or later (DE3_System Builder is available on the DE3 System CD or can be downloaded from the website http://de3.terasic.com). Here are the procedures to generate a top-level project for HSMC-DVI.

1) Launch DE3-System Builder
2) Add a DE3 board. Enable the HSTC-C connector and type desired pin pre-fix name in the dialog of DE3 Configuration.



3) Add HSMC-DVI Board.

4) Connect DE3 and HSMC-DVI Board by drag-and-drop the mouse

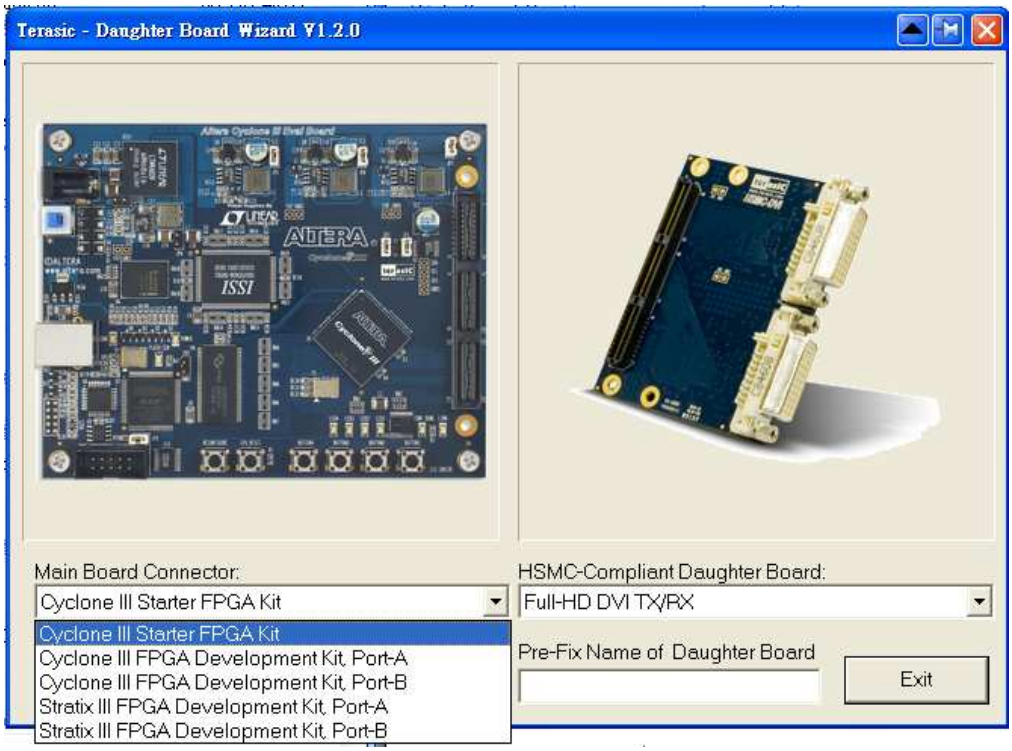


5) Click “Generate” to generate the desired top-level and pin assignments for the HSMC-DVI project.

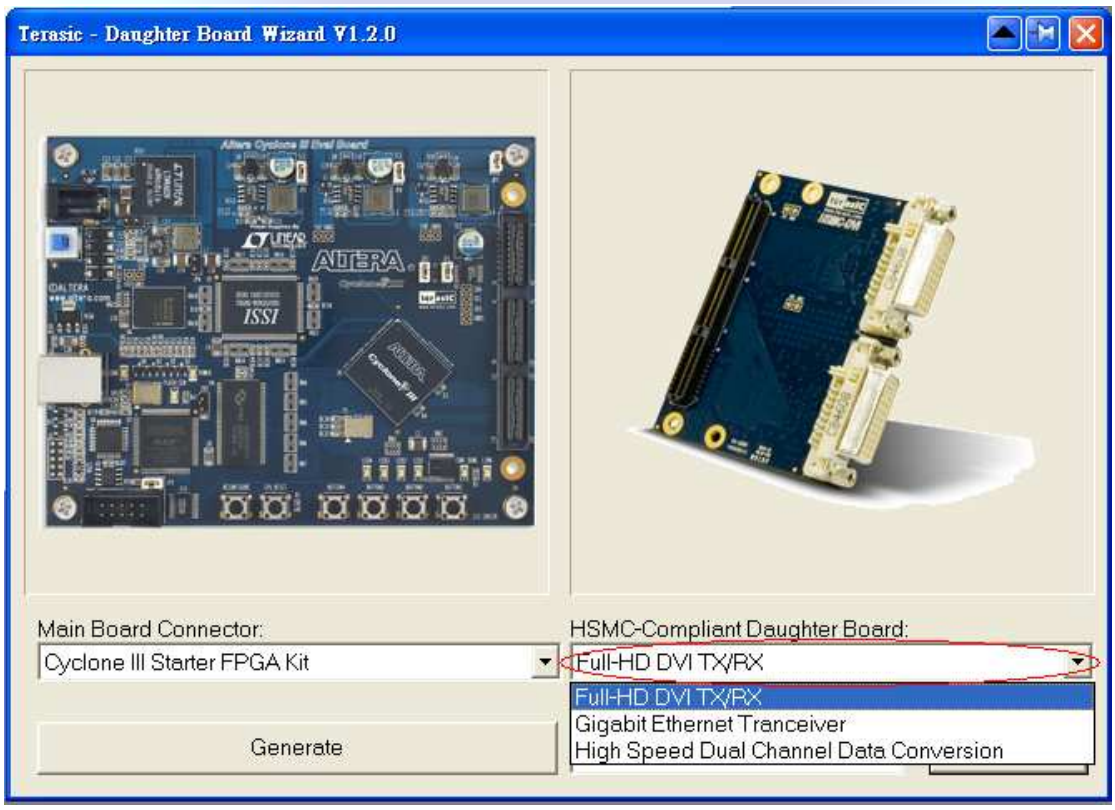
For the Cyclone III starter board, Cyclone III development board, and Stratix III development board:
Users can easily generate HSMC-DVI pin assignments onto their main board by utilizing the Daughter Board Wizard V1.2.0 or later (Daughter Board Wizard is available on the DVI CD-ROM located in the “Tool” folder). Here are the procedures to generate a top-level project for HSMC-DVI.

1) Launch Daughter Board Wizard.

2) Select the Main Board Connector



3) Select the HSMC-Compliant Daughter Board



4) Enter the signal Pre-fix name of Daughter Board and Click ‘Generate’ to generate the desired top-level and pin assignments for the HSMC-DVI project.

CHAPTER 4 Demonstration

This Chapter illustrates the reference design for the HSMC-DVI board

4.1 Introduction

This section describes the functionality of the demonstration briefly.

The demonstration shows how to use DE3 to controls the HSMC-DVI board. The demonstration includes two parts:

Transmission Demo:

The reference design can generate various video format signal for transmit. The supported format includes:

Pattern ID	Video Format	PCLK (MHZ)
0	640x480@60P	25
1	720x480@60P	27
2	1024x768@60P	65
3	1280x1024@60P	108
4	1920x1080@60P	148.5
5	1600x1200@60P	162

Loopback Demo:

Loopback (Internal bypass) the DVI video signals within the FPGA board. The video output pins of the receiver are directly connected to the input video pins of the transmitter.

4.2 System Requirements

The following items are required for the HSMC-DVI Server demonstration.

- HSMC-DVI x 1
- DE3 Board x 1
- LCD monitor with at least one DVI input x 1
- DVI Video source x 1
- DVI Cable x 2

4.3 Hardware Setup

Figure 4.3.1 shows how to setup hardware for the HSMC-DVI demonstration.

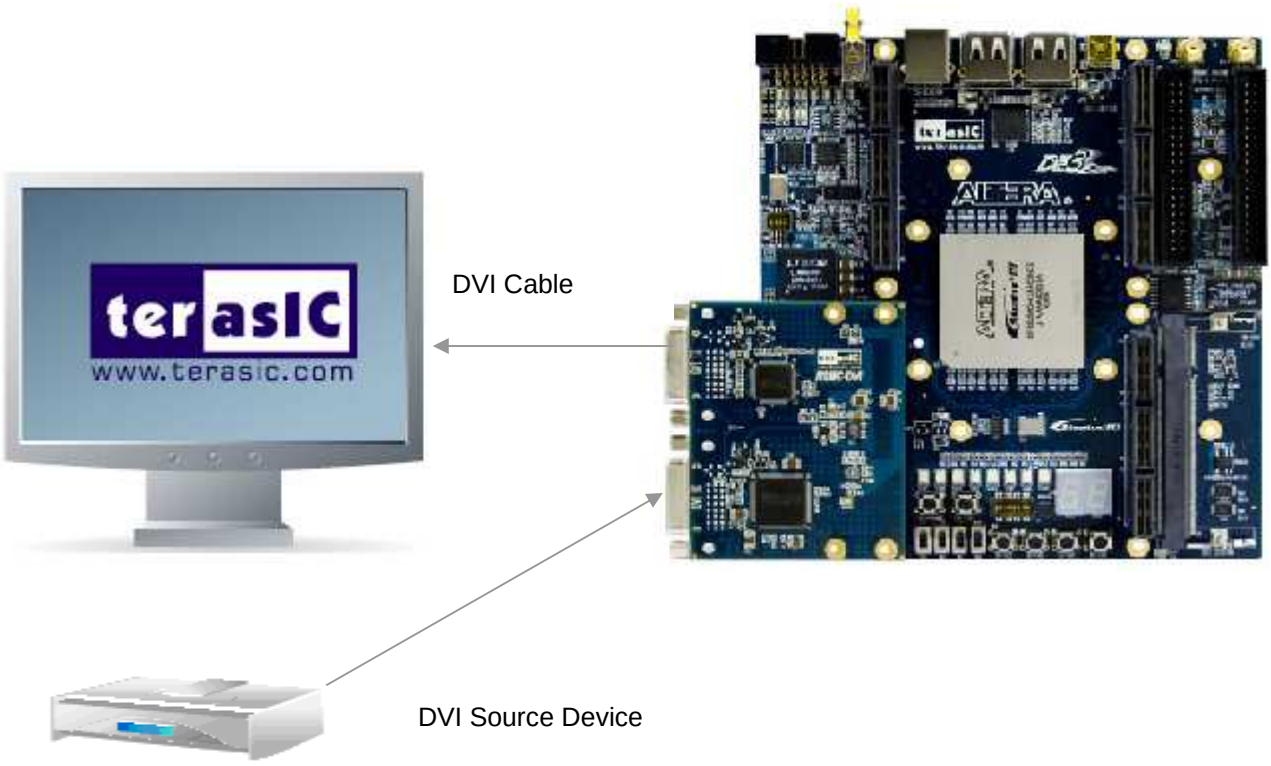


Figure 4.3.1

Note: It is important to connect the DVI daughter board to Port C of the DE3 board.

A THCB-HFF adapter card is used to establish connection with DE3 and HSMC-DVI daughter board.

4.4 Configure FPGA

This section describes the procedures of configure the FPGA.

Please follow the procedure below to configure FPGA:

- Connect DE3 to your PC by an usb cable.
- Power on DE3
- Project directory: DVI_Demo_DE3_150_PortC (Note: Project folder may vary depending on the DE3 device you are using and the corresponding port. As for this demonstration, we are using Port C on the DE3 FPGA)
- Configure FPGA by the Bit Stream File: DVI_Demo.sof

4.4 Demo Operation

This section describes the procedures of operation the demonstration.

DVI Transmission Demo:

For transmission demo, please attach a LCD to DVI-TX port with a DVI cable.

By pressing Button[2] you can toggle between the transmission Demo and Loopback Demo. When transmission demo is active, LED[3] is Off.

Click Button[3] can change active transmission pattern. The associated pattern ID is indicated by LED[2:0]. LED[2]Off -- LED[1]Off -- LED[0]Off means pattern ID zero.

DVI Loopback Demo:

For loopback demo, please attach a LCD to DVI-TX port and attach a DVI-Video source to DVI-RX port with DVI cables, in respectively.

By pressing Button[2] you can toggle the transmission Demo and Loopback Demo. When loopback demo is active, LED[3:0] are on.

The loopback demonstration uses the EDID information which is stored in EEPROM on the DVI-RX. The EDID is already initiated with the DVI board. However, if the EDID is erased or modified by users, please remember to initialize EDID.

By pressing Button[1], the EDID initialization process is started. The LED[3:0] starts to blink when EDID initialization is in process. When EDID is initialized successfully, the LED[3:0] stops blinking. If EDID initialization fails, please try to remove the cable attached to DVI_RX port and press Button[1] to try again.

4.5 Design Concept

This section describes the design concepts for the HSMC-DVI demonstration.

System Block Diagram:

Figure 4.5.1 show the block diagram of the demonstration.

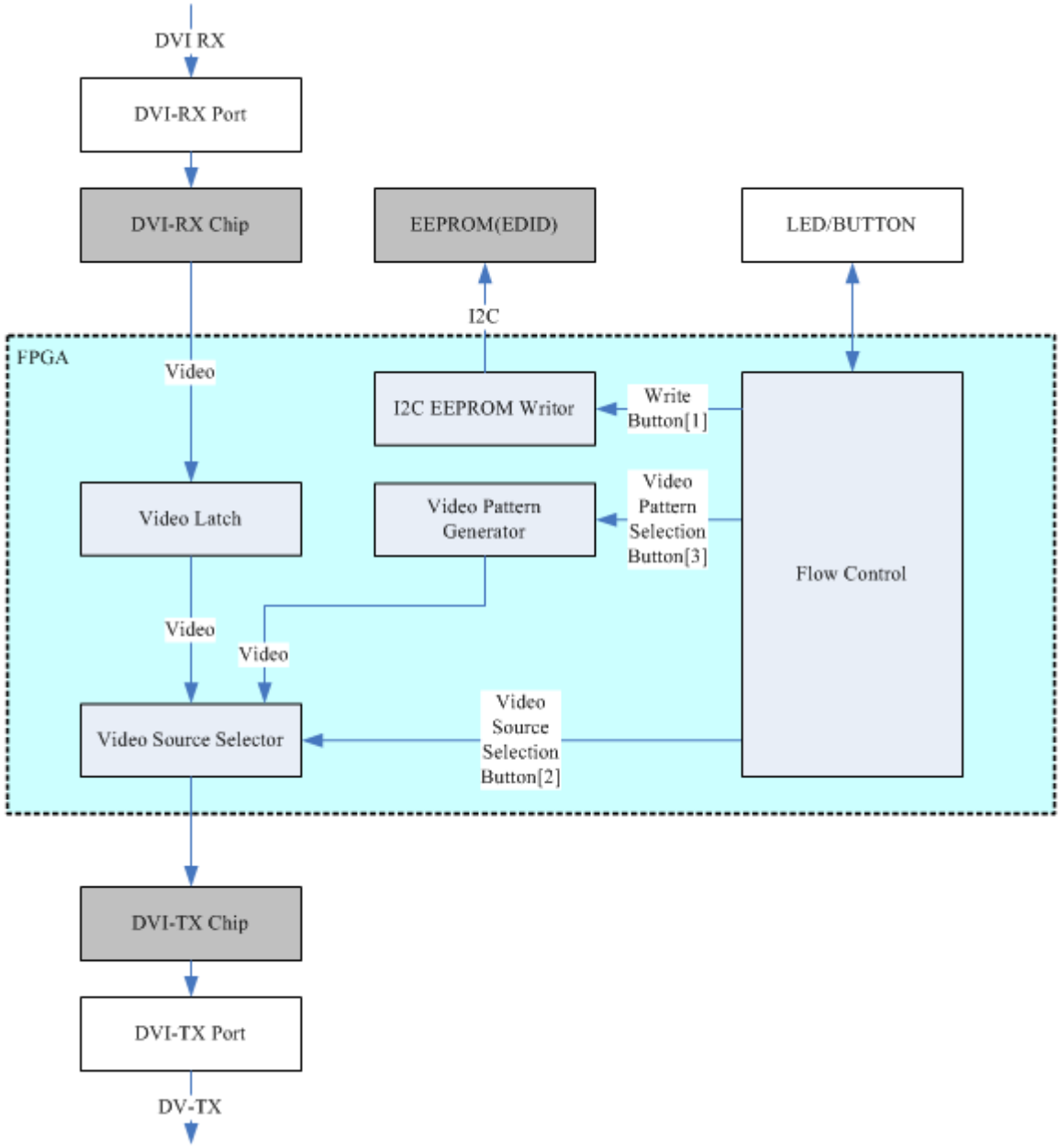


Figure 4.5.1 Block diagram

The “Video Pattern Generator” module corresponds to the generated test patterns for transmission demo. The test patterns includes:

Pattern ID	Video Format	PCLK (MHZ)
0	640x480@60P	25
1	720x480@60P	27
2	1024x768@60P	65
3	1280x1024@60P	108
4	1920x1080@60P	148.5
5	1600x1200@60P	162

The display resolution and pixel rate will change when the mode changes. In this module, the ALTERA PLL-RECONFIG controller is used to generate various pixel rates. The RECONFIG data for various clocks are stored on the ROM. The module source code is located in “vpg” sub-folder. For more information about Stratix III re-configuration PLL, please refer to www.altera.com/literature/an/an454.pdf

The “Video Latch” module is used to latch DVI-RX video for high-speed video streaming.

The “Video Source Selector” module corresponds to the selected desired video source for final video display. Altera LPM_MUX controller is used to achieve high-speed video streaming selection.

The “I2C EEPROM Write” module corresponds to writing aspects of the EDID content to EDID. For writing custom EDID data, users can change this module.

4.6 Source Code Location

Table 4.6 shows the source code location for the DVI reference design for various FPGA main boards.

Table 4.6

FPGA Main Boards	Reference design location
DE3-340 Device (Port C)	\Examples\DVI_Demo_DE3_340_PortC
DE3-150 Device (Port C)	\Examples\DVI_Demo_DE3_150_PortC
Cyclone III Starter Board	\Examples\DVI_Demo_QB3
Cyclone III Development Board (Port B)	\Examples\DVI_Demo_C3H_PortB
Stratix III Development Board (Port B)	\Examples\DVI_Demo_S3H_PortB

CHAPTER 5

Appendix

5.1 Revision History

Date	Change Log
June 25, 2009	Initial Version
March 15, 2010	Table 3.1 Pin assignments corrected

5.2 Always Visit HSMC-DVI Webpage for New Main board

We will be continuing providing interesting examples and labs on our HSMC-DVI

webpage. Please visit www.altera.com or hsmcdvi.terasic.com for more information.

Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

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Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург, Промышленная ул, дом № 19, литера Н, помещение 100-Н Офис 331