零 部 件 规 格 书

生效日期：2007.11.26

编号：

分发单位	份数	零部件名称	G-IC-LEDDR-351-HSOP28-BD9261FP				
		专 用 号	0324402636	本体描述	BD9261FP	版本	A
青岛 IQC/JIT	1	生产厂家		厂家型号		页码	
黄岛 IQC/JIT	1	ROHM		BD9261FP		P1-P25	
顺德 IQC/JIT	1	以下空白					
重庆 IQC/JIT	1						
物流 JIT/IPC	1						

确认参数(T=25℃)

参数	数值	单位	参数	数值	单位
输入电压范围	9～35	V			
LED 最大驱动电流	350	mA			
结温	150	℃			
封装	HSOP28	/			
LED 通道数量	4	/			
以下空白					

更改履历

序号	更改内容	更改人	更改时间	版本
1	以下空白			
2				
3				
4				
5				
6				
7				
8				
9				
10				

备注:

1. 上表要保留此专用号的所有更改记录，便于查询；更改时要把需要更改的内容填完整。
2. 此文件的所有技术规范均应符合海尔集团的最新技术标准要求；如有抵触，以集团标准为准。

编制	审 核	标准化	会签	批 准
徐艳艳	张永玲	孙佟佟	/	万秀水

以上所填、所签均经过确认，并明确表达了技术意图，不会造成歧义，并承担由此造成的损失！

BD9261EFV・BD9261FP Technical Note (VER. 2.0)

Contents

PATENT

US7235954

EP1499165

We applied to other pluel patent, now.

ROHM Co., Ltd.

Power Management team / Inverter Group

Table of Contents

1. Specification for BD9261EFV/BD9261FP

1.1 Features

1. 4ch_LED constant current driver is equipped.
2. Maximum LED output current: 200 mA(peak Current:400mA MAX)
3. External setting of LED voltage by LED_LV terminal is enabled.
4. DC/DC converter is equipped.
5. Both PWM and analog dimming are enabled.
6. LED abnormality detection circuit (OPEN protection, short circuit protection) is equipped.
7. Short circuit protection voltage is adjustable.
8. Short circuit protection detection CH is individually detected and extinguished.
9. Under voltage lock out (UVLO) circuit and over voltage protection (OVP) circuit are equipped.
10. FAIL function is equipped.
11. Packages provided with high heat radiation TSSOP-B28・HSOP28 are adopted.

Parameter	Symbol	Rating	Unit
Operation temperature range	Ta(opr)	-40 to +85	°C
Storage temperature range	Tstg	-55 to +150	°C
Junction temperature	Tjmax	150	°C
Allowable loss 1 (HTSSOP-B28)*1	Pd	4700	mW
Allowable loss 2 (HSOP28)*2	Pd	4700	mW

*1 When Ta = 25°C or higher, derating is done with HTSSOP-B28:-37.6mW/°C (when a 4-layer 70.0mm x 70.0mm x 1.6mm board is mounted).

*2 When Ta = 25°C or higher, derating is done with HSOP28:-37.6mW/°C (when a 4-layer 70.0mm x 70.0mm x 1.6mm board is mounted).

1.2 Absolute maximum rating (Ta = 25°C)

BD9261EFV						BD9261FP					
No.	Terminal	Rating [V]	No.	Terminal	Rating [V]	No.	Terminal	Rating [V]	No.	Terminal	Rating [V]
1	VREF5V	-0.3 to 7	28	VCC	-0.3 to 36	1	OVP	-0.3 to 7	28	FB	-0.3 to 7
2	N	-0.3 to 7	27	STB	-0.3 to VCC	2	LED_LV	-0.3 to 7	27	SS	-0.3 to 7
3	DCDC_GND	-	26	UVLO	-0.3 to 7	3	LED1	-0.3 to 40	26	CP	-0.3 to 7
4	CS	-0.3 to 7	25	FAIL	-0.3 to VCC	4	LED2	-0.3 to 40	25	CS	-0.3 to 7
5	CP	-0.3 to 7	24	SLOPE	-0.3 to 7	5	PWM1	-0.3 to 7	24	DCDC_GND	-
6	SS	-0.3 to 7	23	RT	-0.3 to 7	6	PWM2	-0.3 to 7	23	N	-0.3 to 7
7	FB	-0.3 to 7	22	AGND	-	7	LSP	-0.3 to 7	22	VREF5V	-0.3 to 7
8	OVP	-0.3 to 7	21	ISET	-0.3 to 7	8	LED_GND	-	21	VCC	-0.3 to 36
9	LED_LV	-0.3 to 7	20	VREF	-0.3 to 7	9	PWM3	-0.3 to 7	20	STB	-0.3 to VCC
10	LED1	-0.3 to 40	19	LED4	-0.3 to 40	10	PWM4	-0.3 to 7	19	UVLO	-0.3 to 7
11	LED2	-0.3 to 40	18	LED3	-0.3 to 40	11	LED3	-0.3 to 40	18	FAIL	-0.3 to VCC
12	PWM1	-0.3 to 7	17	PWM4	-0.3 to 7	12	LED4	-0.3 to 40	17	SLOPE	-0.3 to 7
13	PWM2	-0.3 to 7	16	PWM3	-0.3 to 7	13	VREF	-0.3 to 7	16	RT	-0.3 to 7
14	LSP	-0.3 to 7	15	LED_GND	-	14	ISET	-0.3 to 7	15	AGND	-

1.3 Electrical characteristics (unless otherwise specified, Ta = 25°C, VCC = 24V)

BD9261EFV/FP (1/2)						
Item	Symbol	Standard value			Unit	Condition
		Minimum	Standard	Maximum		
[Whole device]						
Operating circuit current	Icc	—	6	12	mA	VCC=24V, STB=3V, LED1-4 OFF
Stand-by circuit current	IST	—	15	30	μA	VCC=24V STB=0V
[VREF5V block]						
VREF5V output voltage	VREF5	4.95	5.0	5.05	V	IO=0mA
VREF5V Maximum output current	IREF5	15	—	-	mA	
[Switching block]						
N terminal source resistance	RONH	0.5	1.0	2.0	μΩ	ION=-10mA
N terminal sink resistance	RONL	0.5	1.0	2.0	Ω	ION=10mA
[Over current protection (OCP) block]						
Over current detection voltage	VOCP	350	400	450	mV	
[Soft-start block]						
SS terminal source current	ISS	-4	-2	-1	μA	
SS terminal release voltage	VSS	2.7	3.0	3.3	V	SS=SWEEP UP
[Error amplifier block]						
LED control voltage	VLED	0.55	0.6	0.65	V	LED_VL=OPEN
OVP control voltage	OVP_FB	1.1	1.2	1.3	V	LED_VL=OPEN,SS<2.7V
FB sink current	IFBSINK	40	100	200	μA	VLED=1.2V, VFB=1.0V CP=GND
FB source current	IFBSOURCE	-200	-100	-40	μA	VLED=0V, VFB=1.0V CP=GND
Upper resistance of divided LED_LV terminal resistance	RupLED_LV	72	120	216	kΩ	LED_LV=0V
Lower resistance of dividedLED_LV terminal resistance	RdownLED_LV	18	30	54	kΩ	LED_LV=3V
[CT oscillator block]						
Oscillation frequency	FCT	558	600	642	KHz	RT=100kΩ
N terminal MAX DUTY output	NMAX_DUTY	78	85	95	%	RT=100kΩ
RT terminal output voltage	VRT	1.05	1.5	1.95	V	RT=100kΩ
SLOPE terminal output voltage	VSLOPE	1.05	1.5	1.95	V	SLOPE=100kΩ
[Over voltage protection (OVP) block						
Over voltage protection detection voltage	VOVP	1.43	1.63	1.83	V	VOVP SWEEP UP, LED_LV=OPEN
OVP sink current	I_OVP	1.5	3.0	6.0	μA	OVP=2.0V
[Short circuit protection (SCP) block]						
Short circuit protection detection voltage	VSCP	0.04	0.10	0.25	V	VOVP SWEEP DOWN
[UVLO block]						
Operation power source voltage (VCC)	VUVLO_VCC	6.0	7.0	8.0	V	VCC=SWEEP UP
VCC_UVLO hysteresis voltage	VUHYS_VCC	150	300	600	mV	VCC=SWEEP DOWN
UVLO terminal Pull-Down resistance	R_UVLO	375	625	1125	kΩ	UVLO=3V
UVLO Release voltage	VUVLO_U	2.4	2.55	2.7	V	VUVLO=SWEEP UP
UVLO Hysteresis voltage	VUHYS_U	50	100	200	mV	VUVLO=SWEEP DOWN

1.3 Electric properties (unless otherwise specified, Ta = 25°C, VCC = 24V)

BD9261EFV/FP (2/2)

Item	Symbol	Standard value			Unit	Condition
		Minimum	Standard	Maximum		
[Filter block]						
CP detection voltage	VCP	1.8	2	2.2	V	CP=SWEEP UP
CP source current	ICP	-4	-2	-1	μA	VCP=0V
[LED driver block]						
LED terminal current accuracy	⊿ILED	-1.5	-	1.5	%	ILED=100mA,
OPEN detection voltage	VOPEN	0.05	0.2	0.35	V	VLED=SWEEP DOWN
SHORT detection voltage	VSHORT	8.5	9	9.5	V	VLED=SWEEP UP
Upper resistance of divided LSP terminal resistance	RupLSP	1260	2100	3180	kΩ	LSP=0V
Lower resistance of divided LSP terminal resistance	RdownLSP	540	900	1620	kΩ	LSP=3V
[STB block]						
STB terminal HIGH voltage	STBH	2.0	-	VCC	V	
STB terminal LOW voltage	STBL	-0.3	-	0.8	V	
STB terminal Pull Down resistance	REN	600	1000	1800	kΩ	VSTB=3.0V
[PWM1,PWM2,PWM3,PWM4 block]						
PWM terminal HIGH voltage	PWMH	2.3	-	5.0	V	
PWM terminal LOW voltage	PWML	-0.3	-	0.8	V	
PWM terminal Pull Down resistance	RPWM	1200	2000	3600	kΩ	PWM1-4=3.0V
[FAIL block (OPEN DRAIN)						
FAIL LOW sink current	VOL	1.0	2.0	4.0	mA	VFAIL=1.0V
[ISET block]						
ISET terminal voltage	VISET	1.3	1.5	1.7	V	
Upper resistance of divided VREF terminal resistance	upRVREF	1200	2000	3600	kΩ	
Lower resistance of divided VREF terminal	downRVREF	1200	2000	3600	kΩ	

(This product is not designed to resist radioactive rays.)

1.4 Operation range

Parameter	Symbol	Range	Unit
Power source voltage	VCC	9.0 to 35.0	V
Minimum output current of LED1-4 terminals	ILED_MIN	15	mA*2
Maximum output current of LED1-4 terminals (AVERAGE)	ILED_MAX1	200	mA*1*2
Maximum output current of LED1-4 terminals (PEAK)	ILED_MAX2	400	mA*1*2*4
LED_LV set voltage range	VLED_LV	0.4 to 1.8	V*3
LSP set voltage range	VLSP	0.3 to 3.5	V
DC/DC oscillation frequency	fsw	100 to 1000	kHz
PWM dimming minimum ON_DUTY time (at I_LED=100mA/1ch)	PWM_MIN	5	uS
Range of voltage applied on VREF terminal	VREF	0.3 to 1.5	V

*1 Wide variation of LED VF increases loss at the driver, which results in high package temperature. Therefore the board needs to be designed with attention paid to heat radiation..

*2 Current amount per 1ch

*3 Larger set values increase thermal loss, resulting in high package temperature. Therefore pay attention to heat radiation when setting.

*4 Peak current: Avoid such use as 400 mA keeps on flowing at PWM DUTY of 100%. Average current needs to not exceed 200mA.

- For the function of increasing current, see the explanation of LED_LV terminal.

1.5 Operation condition of external part

Parameter	Symbol	Range	Unit
Soft-start set capacitance	SS	100p to 1.0μ	μF
Timer latch set capacitance	CP	100p to 1.0μ	F
DC/DC frequency set resistance	RT	60 to 600	kΩ
VREF5V terminal connection capacitance	C_VREF	1.0 to 10	μF
SLOPE terminal connection resistance	R_SLOPE	60 to 1000	kΩ
ISET terminal connection resistance	R_ISET	7.5 to 200	kΩ

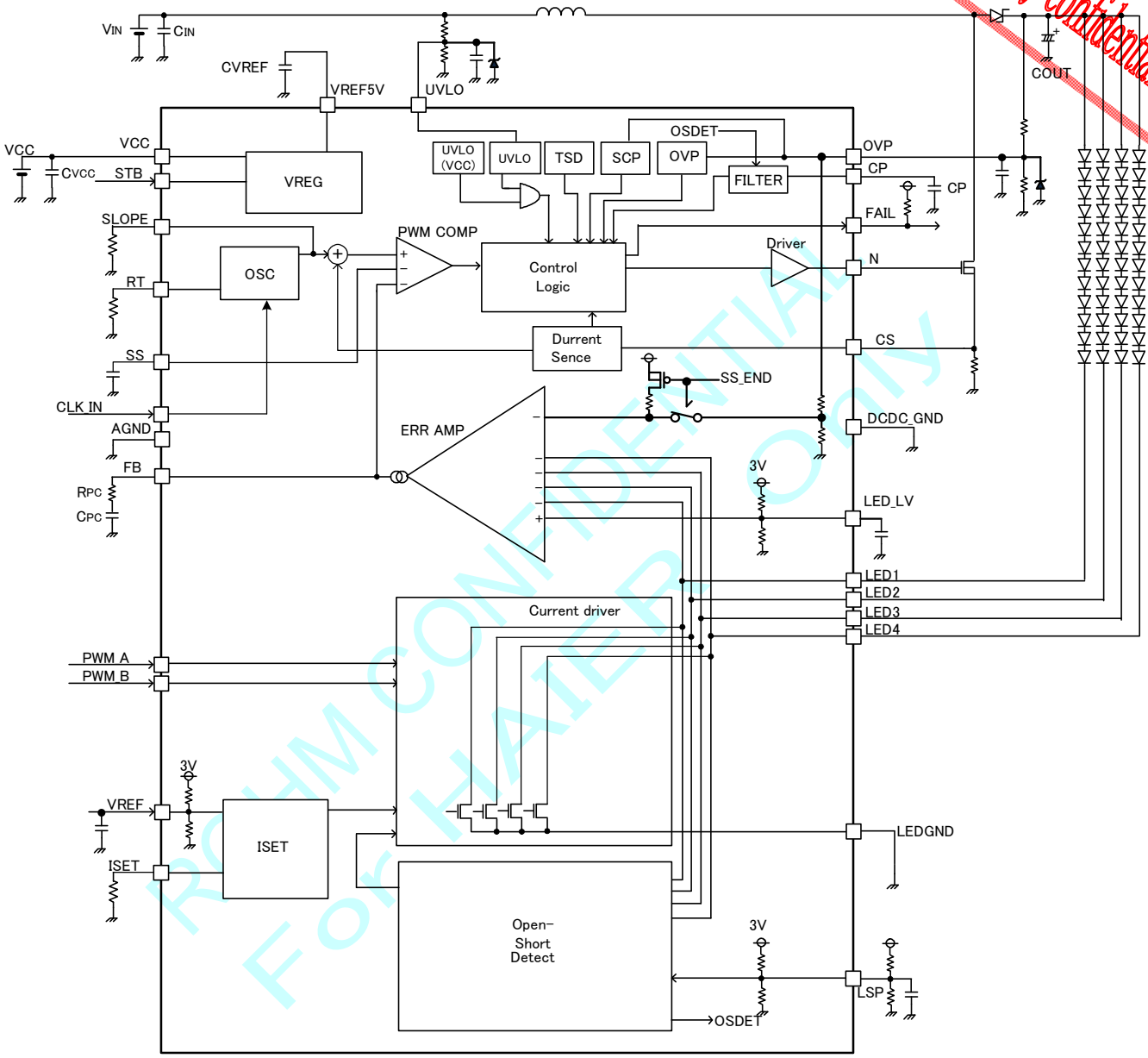
The operation conditions described above are constants for a single IC. Adequate attention must be paid to setting of a constant for an actual set of parts.

1.6 Terminal No., name, and function

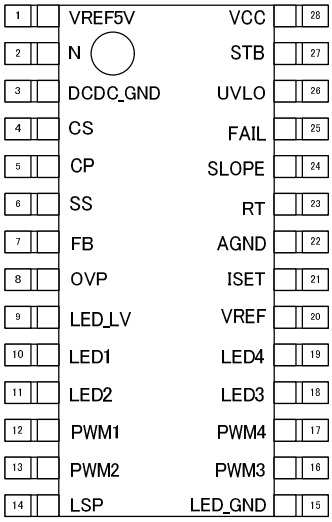
BD9261EFV					
No.	Terminal	Function	No.	Terminal	Function
1	VREF5V	5V regulator output terminal	28	VCC	Power source terminal
2	N	DC/DC switching output terminal	27	STB	Enable terminal
3	DCDC_GND	GND terminal for DCDC converter	26	UVLO	Low voltage malfunction prevention detection terminal
4	CS	DC/DC output current detection terminal	25	FAIL	Abnormality detection output terminal
5	CP	Connecting terminal for filter setting capacitor	24	SLOPE	Connecting terminal for phase compensation resistance
6	SS	Connecting terminal for soft-start time setting capacitor	23	RT	Connecting terminal for DC/DC switching frequency setting resistance
7	FB	Error amplifier output terminal	22	AGND	GND terminal for analog part
8	OVP	Over voltage protection detection terminal	21	ISET	Connecting terminal for LED constant current setting resistance
9	LED_LV	LED feedback voltage setting terminal	20	VREF	Analog dimming DC voltage input terminal
10	LED1	LED output 1	19	LED4	LED output 4
11	LED2	LED output 2	18	LED3	LED output 3
12	PWM1	External PWM dimming signal input terminal (LED1)	17	PWM4	External PWM dimming signal input terminal (LED4)
13	PWM2	External PWM dimming signal input terminal (LED2)	16	PWM3	External PWM dimming signal input terminal (LED3)
14	LSP	LED short circuit protection voltage setting terminal	15	LED_GND	GND terminal for LED

BD9261FP					
No.	Terminal	Function	No.	Terminal	Function
1	OVP	Over voltage protection detection terminal	28	FB	Error amplifier output terminal
2	LED_LV	LED feedback voltage setting terminal	27	SS	Connecting terminal for soft-start time setting capacitor
3	LED1	LED output 1	26	CP	Connecting terminal for filter setting capacitor
4	LED2	LED output 2	25	CS	DC/DC output current detection terminal
5	PWM1	External PWM dimming signal input terminal (LED1)	24	DCDC_GND	GND terminal for DC/DC converter
6	PWM2	External PWM dimming signal input terminal (LED2)	23	N	DC/DC switching output terminal
7	LSP	LED short circuit protection voltage setting terminal	22	VREF5V	5V regulator output terminal
8	LED_GND	GND terminal for LED	21	VCC	Power source terminal
9	PWM3	External PWM dimming signal input terminal (LED3)	20	STB	Enable terminal
10	PWM4	External PWM dimming signal input terminal (LED4)	19	UVLO	Low voltage malfunction prevention detection terminal
11	LED3	LED output 3	18	FAIL	Abnormality detection output terminal
12	LED4	LED output 4	17	SLOPE	Connecting terminal for Phase compensation resistance
13	VREF	Analog dimming DC voltage input terminal	16	RT	Connecting terminal for DC/DC switching frequency setting resistance
14	ISET	LED constant current setting resistance connecting terminal	15	AGND	GND terminal for analog part

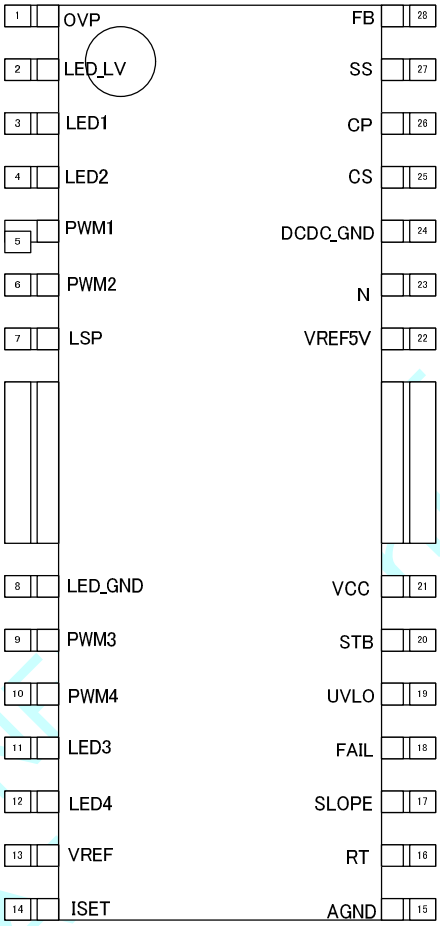
1.7 Block diagram



1.8 Pin location diagram

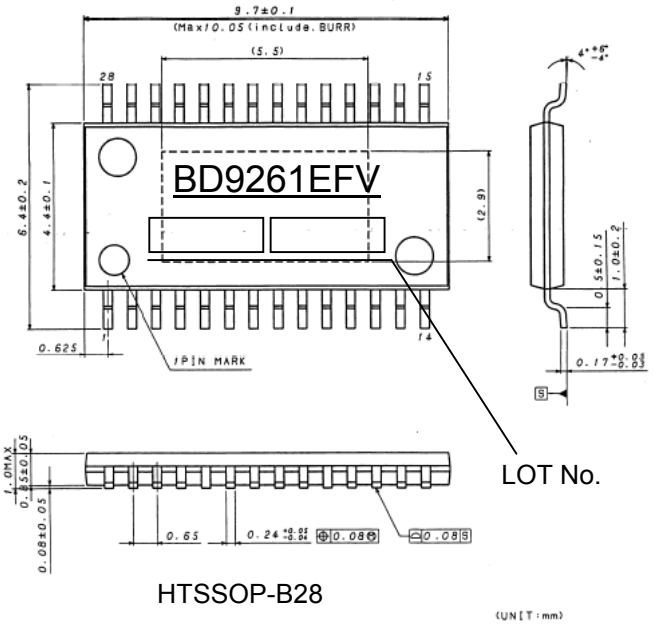


HTSSOP-B28

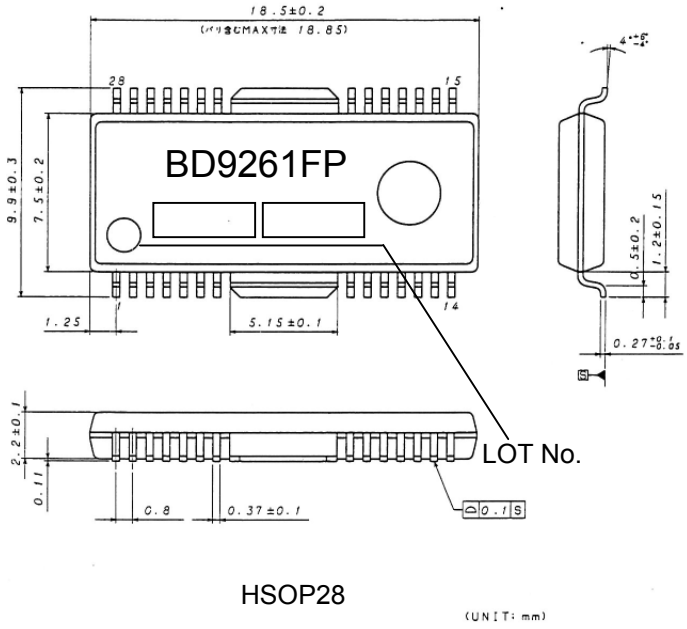


HSOP28

1.9 Package outline drawing



HTSSOP-B28



HSOP28

2 Understanding BD9261EFV・BD9261FP

2.1 Function of terminal

VREF5V (HTSSOP-B28:1PIN / HSOP28:22PIN)

5 V output terminal (TYP) used for DCDC converter driver, delivering 15 mA at maximum:
Use at a current higher than 15 mA may affect N terminal output pulse, which may result in malfunction. It will also cause heating of IC itself. Therefore it is recommended to set the load as small as possible.
Install an oscillation prevention ceramic capacitor (1.0 uF-10 uF) nearest to VREF5V between VREF5V-AGND terminals.

N (HTSSOP-B28:2PIN / HSOP28:23PIN)

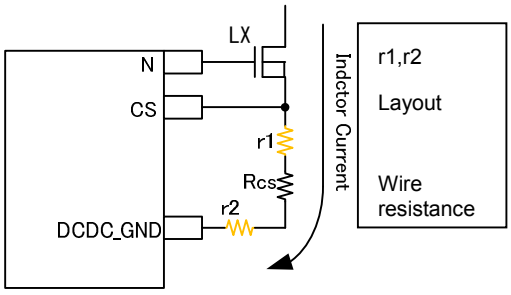
Gate drive output terminal of external NMOS of DC/DC converter with 0 – 5 V amplitudes:
Frequency can be set by a resistance connected to RT terminal. For details, see the explanation of <RT terminal>.
Gate drive signal output from N terminal becomes the source of noise, which may cause malfunction of IC due to cross talk if placed by the side of an analog line. It is recommended to avoid placing the output line especially by the side of CS, ISET, RT, OVP, LSP, LED_LV, FB, UVLO, etc. as far as possible when designing the board.

DCDC_GND (HTSSOP-B28:3PIN / HSOP28:24PIN)

Power GND terminal of output terminal, N Driver: it must be separated from AGND terminal and LED_GND terminal on the board and a wire as thick as possible must be used to reduce impedance.

CS (HTSSOP-B28:4PIN / HSOP28:25PIN)

Inductor current detection resistance connecting terminal of DC/DC current mode: it transforms the current flowing through the inductor into voltage by sense resistance R_{CS} connected to CS terminal, and this voltage is compared with that set in the error amplifier by current detection comparator to control DC/DC output voltage. R_{CS} also performs overvcurrent protection (OCP) and stops switching action when the voltage of CS terminal is 0.4 V (typ.) or higher.
R_{CS} resistance is affected by only a small wire resistance due to inductor current flowing through it. In consideration of print layout wiring, the resistance value R_{CS} becomes to be (R_{CS}+r1+r2), which is detected as overcurrent in some cases.
CS terminal should be therefore connected directly with R_{CS} to remove the influence of r1. The influence of r2 can also be decreased by connecting R_{CS} to DCDC_GND with a wire as thick and short as possible.
In addition, placing a line which causes a noise like that of N terminal or LX (beside NMOS-Drain) by the side of CS line may cause a noise on CS line, which may be wrongly detected by OCP.It is therefore recommended to place CS line apart from lines causing noise as far as possible and install a shield line if possible.



CP (HTSSOP-B28:4PIN／HSOP28:25PIN)

Terminal which sets the time from detection of abnormality until shutdown (Timer latch) : it performs constant current charge of 2.0 uA to the capacitor externally connected with CP terminal and shuts down when it exceeds 2.0 V. The external capacitor has an approximately 100 pF-1.0 uF capacitance.
CP charge time is set by the following equation:

$$T_{CP} = C_{CP} \times 10^{6} [\mathrm{sec}]$$

Here, Ccp = External capacitance of CP terminal [F]
Tcp = CP charge completion time

SS (HTSSOP-B28:6PIN／HSOP28:27PIN)

Terminal which sets soft-start time of DC/DC converter: it performs constant current charge of 2.0 uA to the external capacitor connected with SS terminal, which enables soft-start of DC/DC converter.

Since all the protection functions work when SS terminal voltage reaches 3.0 V (typ.) or higher, it must be set to bring stability to conditions such as DC/DC output voltage and LED constant current operation, etc. before the voltage of 3.0 V is detected.

SS terminal charge time is set by the following equation:

$$T_{SS} = (3.0 \times C_{SS}) / (2 \times 10^{-6}) [\mathrm{sec}]$$

Here, Css = External capacitance of SS terminal [F]

Tss = Soft-start completion time

FB (HTSSOP-B28:7PIN／HSOP28:28PIN)

Output terminal of the error amplifier of DC/DC converter which controls current mode: it detects the voltage of LED (1-6) terminals and controls inductor current so that the voltage of the LED terminal placed in the line with the highest Vf of LED should be 0.6 V (typ.). The voltage of other LED terminals is, as a result, higher by the variation of Vf. Phase compensation setting is separately described on Page 22.

A resistance and a capacitor need to be connected in series nearest to the terminal between FB and AGND.

The state in which all PWM signals are in LOW state brings high Impedance, keeping FB voltage. This action removes the time of charge to the specified voltage, which results in speed-up in DCDC conversion.

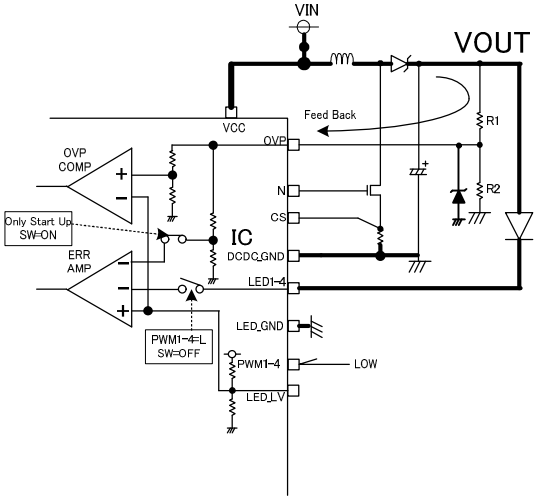
OVP (HTSSOP-B28:8PIN／HSOP28:1PIN)

OVP terminal is the input terminal of over voltage protection and short circuit protection for DC/DC output voltage, detecting over voltage at 1.63 V (typ.) or higher (when LED_LV is OPEN) and short circuit protection at 0.1 V (typ.) or lower.

At start (during SS Voltage<3.0V), OVP terminal acts as a feedback terminal, which enables increase and start of DCDC output up to the set voltage through the feed back of OVP terminal even when PWM is in LOW state.

As OVP feed back voltage and over voltage protection detection voltage use the voltage of LED_LV terminal as reference, they will be changed by changing the voltage of LED_LV terminal (as shown in the circuit diagram below).

Since the absolute maximum rating of OVP terminal is 7 V, OVP will be increased to VOUT if R2 comes off, which may cause damage. It is therefore recommended to connect a 5 V Zener diode with OVP terminal for protection.



Thus the values of resistance R1 and R2 connected to OVP are expressed in the following equation:

●Setting OVP feed back output voltage

$$R1 = (VOUT - 2 \times VLED\_LV) \times \frac{R2}{(2 \times VLED\_LV)} \quad [\Omega] \ldots (A)$$

Here, VLED_LV ＝ Set voltage of LED_LV terminal
(0.6 V when LED_LV = OPEN)
R1 and R2 are external resistance for setting OVP (as shown in the circuit diagram below)

Resistance R2 needs to be set at a negligible value (as a guide, 20 kΩ or lower) since OVP terminal has an input impedance of 650 kΩ (typ.).

●OVP detection voltage

OVP detection voltage is determined by the values R1 and R2 which have been determined by Equation (A).

$$VOUTth1 = \frac{19}{7} \times VLED\_LV \times \left(\frac{R1 + R2}{R2}\right) \quad [V] \ldots (B)$$

VOUTth1: Over voltage detection threshold voltage of DCDC output VOUT

●SCP detection voltage

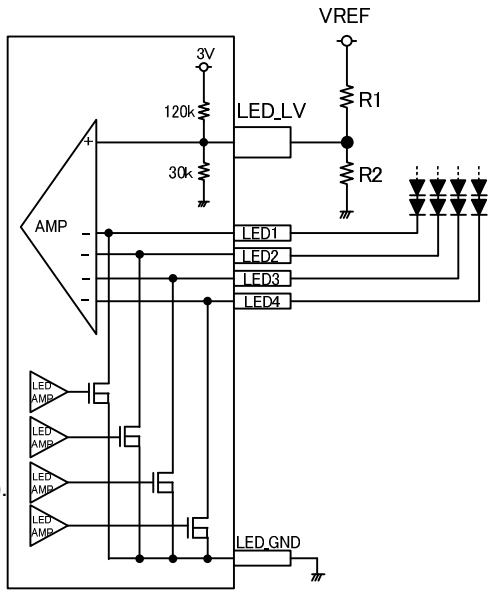
SCP detection voltage is determined by the values R1 and R2 which have been determined by Equation (A).

$$VOUTth2 = 0.1V \times \left(\frac{R1 + R2}{R2}\right) \quad [V] \ldots (C)$$

VOUTth1: Short circuit protection voltage threshold voltage of DCDC output VOUT

Example: Setting of R1 and R2 and calculation of over voltage/short circuit protection detection voltage when output voltage is set at 40.8 V

When LED_LV is set at OPEN and R2 is set at 10 kohm, Equation (A) gives:
R1 = (40.8 V－2×0.6 V)×10 k/(2×0.6 V) = 330 kohm
By Equation (B), over voltage detection voltage when R1 = 330 kohm and R2 = 10 kohm is given as follows:
VOUTth1 = 1 9/7×0.6 V×(330 k+10 k)/10 k = 55.37 V
Short circuit detection voltage is given by Equation (C) as follows:
VOUTth2 = 0.1 V × (330 k + 10 k)/10 k = 3.4 V



LED_LV (HTSSOP-B28:9PIN／HSOP28:2PIN)

Application of voltage on LED_LV terminal enables change of Feed Back voltage. When LED_LV terminal is in OPEN state, it is set at 0.6 V and the MAX value of LED current can be set up to 150 mA. Increase in the set voltage of LED_LV terminal increases MAX current value (upper limit: 400 mA). When output current is 150 mA or lower, decrease in the voltage of LED_LV terminal reduces heating.

The relation equation of LED_LV terminal voltage setting is:

$$VLED\_LV = 4.0 \times (ILED)[V]$$

Here, ILED is the maximum output current per 1 ch of LED terminal

VLED_LV: set voltage of LED terminal

An example of the setting is as follows:

Example: setting output current at 200 mA

Set voltage of LED_LV terminal = 4 × 200 mA = 0.8 V

Attention: Increase in LED_LV terminal voltage and LED current increases heating of IC.
Adequate consideration needs to be taken to thermal design in use.

Example: setting output current at 100 mA

Set voltage of LED_LV terminal = 4 × 100 mA = 0.4 V

Note that set voltage of LED_LV terminal cannot be set at 0.3 V or lower.

Attention: Though increase in LED_LV terminal voltage enables flow of peak current up to 400 mA max., the average of LED terminal current needs to not exceed 200 mA. (If 400mA flows, DUTY needs to be 50% or lower in use.)

LED1-4 (HTSSOP-B28:10・11・18・19PIN / HSOP28:3・4・11・12PIN)

LED constant current driver output terminal:

Setting of current value is adjustable by connection of a resistance with ISET terminal.

For details, see the explanation of <ISET / VREF> terminal.

When LED is in ON state, LED terminal voltage is 0.6 V (typ.) through DCDC conversion; when LED is in short mode or open mode, protection functions work.

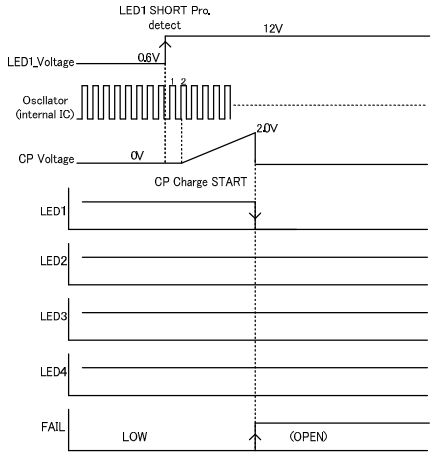
LED OPEN protection detection voltage・・・0.2 V (typ.)

LED SHORT protection detection voltage・・・9.0 V (typ.)・・・(Changeable by LSP terminal setting; For details, see the explanation of LSP terminal.)

Note that these protection functions stop when PWM terminal voltage is in LOW state.

LED SHORT protection function: When LED SHORT is detected, 4 pulses of inside oscillator are counted and CP charge is performed. After latch, the detected LED only is brought into OFF state and other LED drivers work normally.

By LED OPEN protection detection, all the system is brought into OFF after CP latch.



LED SHORT detection protection sequenc

Due to ripple of DCDC output voltage, LED current also may sustain ripple. It can be reduced by installation of a capacitor on LED terminal but Rise-Fall time of LED current increases. It is therefore recommended to prepare a dummy pattern to connect capacitance of approximately 0.01 uF.

PWM1-4 (HTSSOP-B28:12・13・16・17PIN / HSOP28:5・6・9・10PIN)

ON/OFF terminal of LED driver: it inputs PWM dimming signal directly to PWM terminal and change of DUTY enables dimming.

High/Low level of PWM terminal is shown as follows:

State	PWM voltage
LED ON state	PWM = 2.3 V to 5.0 V
LED OFF state	PWM = -0.3 V to 0.8 V

LSP (HTSSOP-B28:14PIN / HSOP28:7PIN)

Terminal which sets LED SHORT protection detection voltage: when LSP is in OPEN state, LED SHORT detection voltage is set at 9 V with LSP set at OPEN.

The relation between LSP terminal voltage and LED SHORT protection detection voltage is set as the following equation:

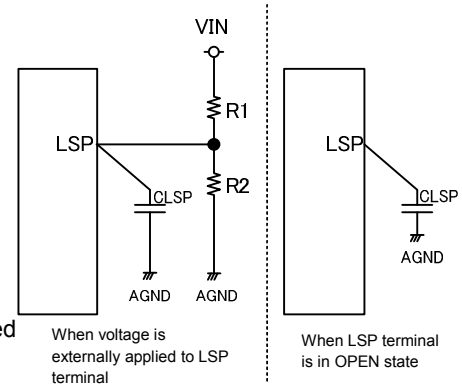
$$LED_{SHORT} = 10 \times VLSP[V]$$

Here, LED_{SHORT}: LED detection voltage

VLSP: LSP set voltage

Input voltage of LSP terminal needs to be set between 0.3 V - 3.5 V.

Since LSP terminal, which is a High Impedance terminal, is easily affected by noise, capacitance of 1000 pF or higher needs to be connected nearest to LSP and AGND terminals (even when unused) absolutely.



LED_GND(HTSSOP-B28:15PIN / HSOP28:8PIN)

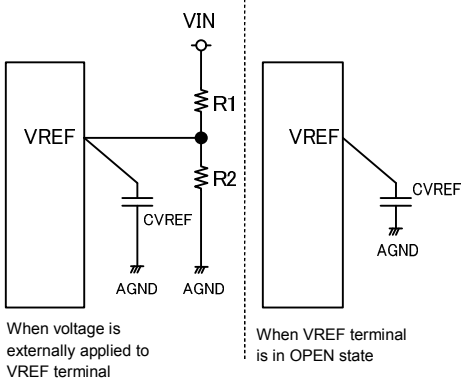
Power GND terminal of LED driver block: it should be placed separately from AGND terminal.

(See the example of layout of the explanation of AGND terminal.)

VREF(HTSSOP-B28:20PIN / HSOP28:13PIN)

Terminal for analog dimming, which can be set at 0.3 V - 1.5 V:

Output current ILED is in a proportional relationship to the voltage value to be input. Since VREF terminal, which is a High Impedance terminal, is easily affected by noise, capacitance of 1000 pF or higher needs to be connected nearest to LSP and AGND terminals (even when unused).



When voltage is applied on VREF terminal: the relationship between output current ILED and RSET resistance value **(ideal)**

$$I_{LED} = \frac{VREF}{R_{ISET}[k\Omega]} \times 2000[mA]$$

When VREF terminal is in OPEN state, VREF terminal voltage is 1.5 V.
Be careful that LED current accuracy is ±7%(at ILED=100mA,VREF=1.5V Input) accuracy when VREF terminal is used (that is, analog dimming is performed).

ISET(HTSSOP-B28:21PIN / HSOP28:14PIN)

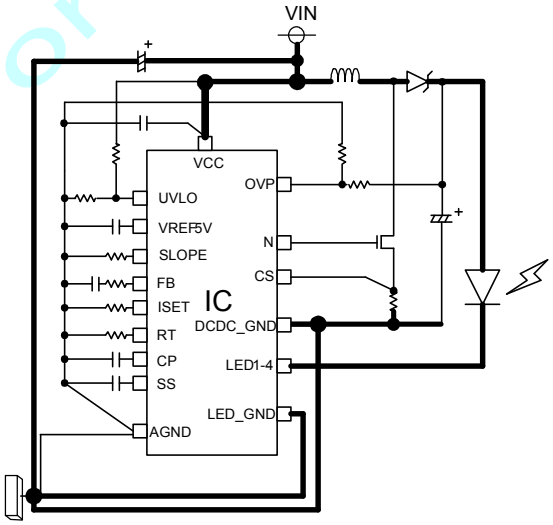
Resistance value to set output current; output current ILED varies inverse proportionally to resistance value.
The relationship among output current ILED, VREF input voltage and RSET resistance is described as follows.
When VREF terminal is in OPEN state: the relationship between output current ILED and RSET resistance value **(ideal)**

$$I_{LED} = \frac{1.5V}{R_{ISET}[k\Omega]} \times 2000[mA]$$

RSET resistance needs to be connected nearest to ISET and AGND terminals.
Output current is set at 150 mA ordinarily, and can be set at higher by increasing the voltage of LED_LV terminal. For details, see the explanation of <LED_LV terminal>.

AGND(HTSSOP-B28:22PIN / HSOP28:15PIN)

GND for analog system inside IC: it should be placed separately from DCDC_GND and LED_GND wherever possible. (Placing separately is recommended because short circuits of PGND and GND near GND PIN of the connector are hardly affected by switching noise.)
An example of GND wiring is as shown on the right. (Actual operation must be checked adequately with application.)



RT(HTSSOP-B28:23PIN／HSOP28:16PIN)

RT sets charge/discharge current determining frequency inside IC.

Only a resistance connected to RT determines saw tooth wave frequency inside IC.

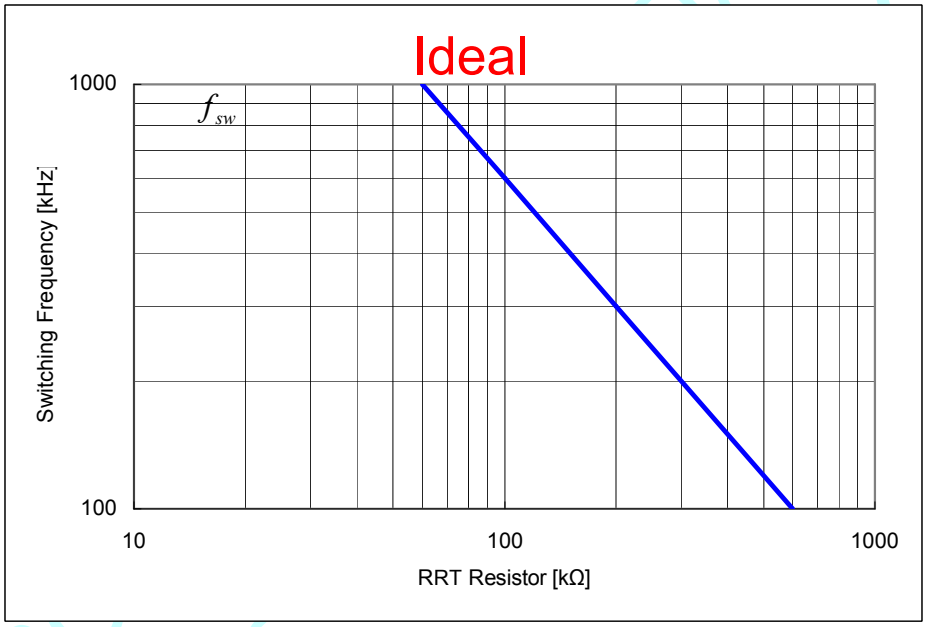
RT resistance needs to be connected nearest to RT and AGND terminals.

The relationship between drive frequency and RT resistance value **(ideal)**

$$R_{RT} = \frac{6 \times 10^{10}}{f_{SW}} [\Omega]$$

Where, f_{sw} = Oscillation frequency of DC/DC converter [Hz]

<Drive frequency（f_{SW}）constant setting (Reference)>



* This equation is an ideal equation in which correction factors are not applied.
Adequate verification with an actual set needs to be performed to set frequency precisely.

SLOPE(HTSSOP-B28:24PIN / HSOP28:17PIN)

SLOPE is a terminal to connect set resistance of compensation ramp wave which prevents subharmonic oscillation of DC/DC converter controlling current mode.

To prevent subharmonic oscillation, the slope of compensation ramp wave needs to be 1/2 times as large as the slope of the maximum descending slope at least. At this time, the value of external resistance R_{SLOPE} needs to satisfy the following relation equation:

$$R_{RT} \leq R_{SLOPE}[\Omega] \leq \frac{5.3 \times 10^{10} \times L}{R_{CS} \times (V_{OUT} - V_{IN})}$$

Compensation ramp wave is necessary when ON DUTY is 50 % or more. Resistance which sets slope needs to be connected nearest to SLOPE and AGND terminals.

FAIL(HTSSOP-B28:25PIN／HSOP28:18PIN)

FAIL signal output terminal (OPEN DRAIN); when an abnormality is detected, NMOS is brought into OPEN state.

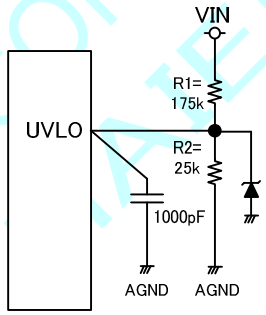
State	FAIL output
In ordinal cases	GND Level
When an abnormality is detected (After CP latch)	OPEN

UVLO(HTSSOP-B28:26PIN／HSOP28:19PIN)

UVLO terminal of the coil of step-up DC/DC converter and the power for external NMOSFET: at 2.55 V (typ.) or higher, IC starts step-up operation and stops at 2.45 V or lower (typ.). (It is not shutdown of IC.)

The power source level of FET needs to be set to the detection level of the IC described above by dividing the resistance. For reference of dividing resistance, setting 175 kΩ between VCC and UVLO and 25 kΩ between UVLO and GND allows start of step-up operation at 20.4 V or higher and stop of it at 19.6 V or lower. If any problem on the application causes noise on UVLO terminal which results in unstable operation of DC/DC converter, a capacitance of approximately 1000 pF needs to be connected between UVLO and AGND terminals.

As the absolute maximum rating of UVLO terminal is 7 V, UVLO is increased up to VIN if R2 comes off, which may cause damage. It is therefore recommended to connect a 5 V Zener diode to OVP terminal for protection.



STB(HTSSOP-B28:27PIN／HSOP28:20PIN)

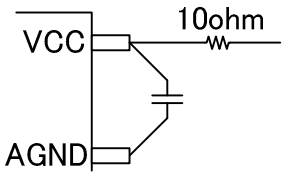
ON/OFF setting terminal for IC, which can be used to perform a reset at shutdown

* The voltage of STB terminal needs to be set at VCC voltage or lower and be input in the sequence of VCC → STB.
* Voltage input in STB terminal switches the state of IC (IC ON/OFF). Use between the 2 states (0.8 - 2.0V) needs to be avoided.

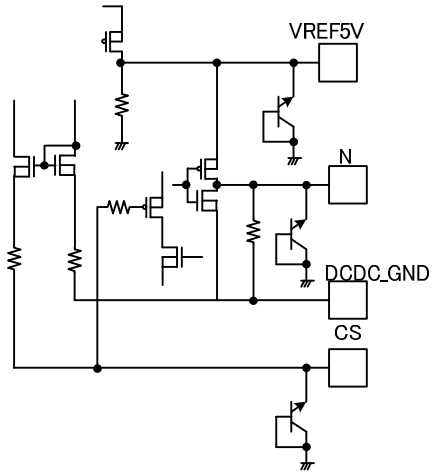
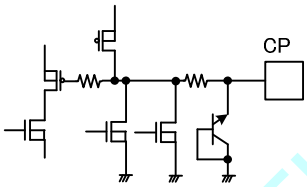
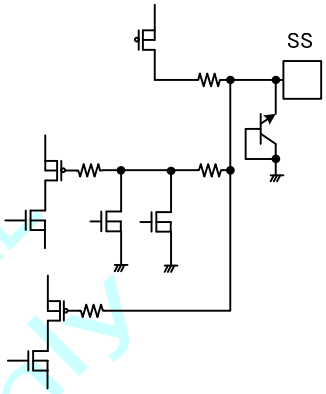
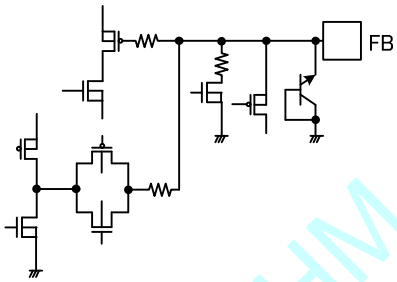
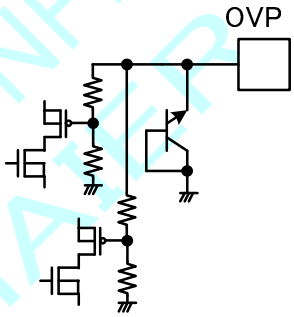
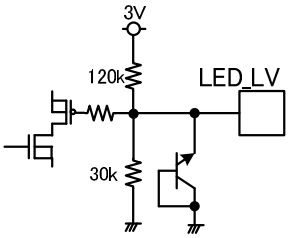
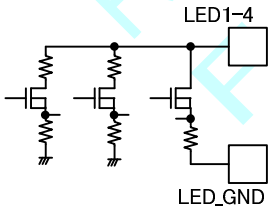
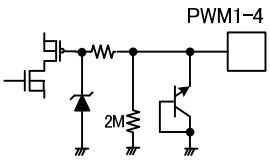
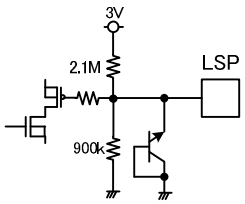
VCC(HTSSOP-B28:28PIN／HSOP28:21PIN)

Power source terminal of IC, which should be input in the range of 9 – 35 V; Operation starts when VCC is 7.0 V (TYP.) or higher and shuts down when VCC is 6.7 V (TYP.) or lower.

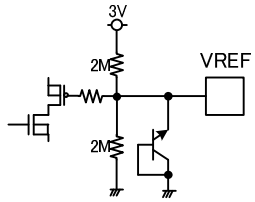
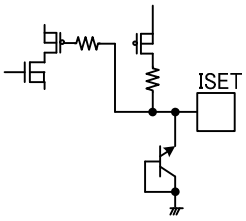
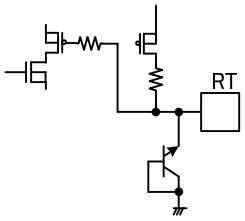
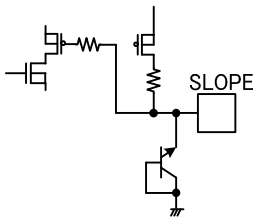
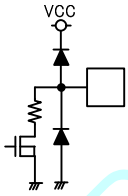
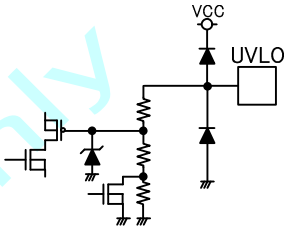
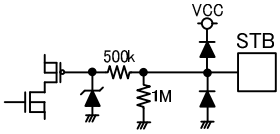
It is effective against surge to connect a ceramic capacitor of 1 uF or higher as near to VCC terminal as possible between VCC and AGND to remove noise, and it is more effective to connect a resistance of around 10 Ω additionally.



2.1 Internal equivalent circuit diagram (1/2)

VREF5V / N / DCDC_GND / CS	CP	SS
		
FB	**OVP**	**LED_LV**
		
LED1-4 / LED_GND	**PWM1-4**	**LSP**
		

Internal equivalent circuit diagram (2/2)

VREF	ISET	RT
		
SLOPE	**FAIL**	**UVLO**
		
STB		
		

3. APPLICATION OF BD9261EFV・BD9261FP

3.1 List of Threshold function (TYP. condition)

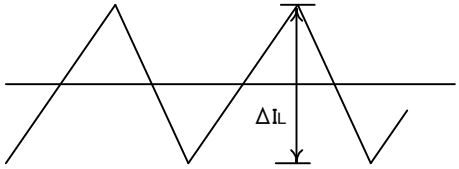
List of Threshold function	Function	Detection Point	Cancel Point	Type
STB	IC SYSTEMON/OFF	2.0V<VSTB	VSTB<0.8V	Hysteresis
PWM1-4	LED Current ON/OFF	VPWM1-4<2.3V	VPWM1-4<0.8V	Hysteresis
SS	Slow Start Function	VSS＜2.9V	VSS＞3.0V	Hysteresis
UVLO(VCC)	VCC Under Voltage Detection	VCC＜6.7V	VCC＞7.0V	Hysteresis
UVLO(VREF5V)	Under Voltage Detection	VREF5V＜4.2V	VREF5V＞4.5V	Hysteresis
UVLO(UVLO terminal)	VCC Under Voltage Detection	VUVLO＜2.45V	VUVLO＞2.55V	Hysteresis
OVP	DCDC Over Voltage Detection	VOVP＞1.63V(LED_LV=OPEN)	VOVP＜1.6V(LED_LV=OPEN)	Latch
SCP	DCDC Under Voltage Detection	VOVP<0.1V	VOVP>0.1V	Latch
OCP	FET Current Limit Function	VCS≧0.4V	VCS＜0.4V	-
LED OPEN Detection	LED Open Detection	VLED≦0.2V	VLED＞0.2V	Latch
LED Short Detection	LED Short Detection	VLED≧9.0V(Adjustable LSP)	VLED＜9.0V(Adjustable LSP)	Latch

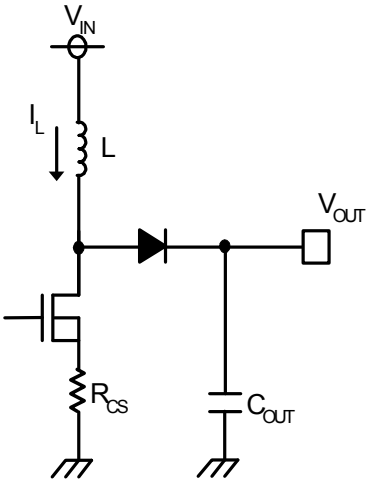
To clear latch type, drop STB to 'L' once and then set at 'H''

Protect Function	The Action of Hysterisys Type protection			
	DC/DC Convertor	LED Driver	Soft Start Function	FAIL State
UVLO(VCC)	STOP	STOP	RESET	OPEN
UVLO(VREF5V)	STOP	STOP	RESET	OPEN
UVLO(UVLO)	STOP	STOP	RESET	OPEN
TSD	STOP	STOP	RESET	OPEN
Protect Function	**The Action of Latch Type protection (Under CP Charge)**			
	DC/DC Convertor	**LED Driver**	**Soft Start Function**	**FAIL State**
OVP	STOP	Normal Action	Normal Action	LOW
SCP	STOP	Normal Action	Normal Action	LOW
OCP	Current Limit	Normal Action	Normal Action	LOW
LED Open Detection	Normal Action	Normal Action	Normal Action	LOW
LED Short Detection	Normal Action	Normal Action	Normal Action	LOW
Protect Function	**The Action of Latch Type protection (After CP Charge)**			
	DC/DC Convertor	**LED Driver**	**Soft Start Function**	**FAIL State**
OVP	STOP	STOP	RESET	OPEN
SCP	STOP	STOP	RESET	OPEN
OCP	STOP	STOP	RESET	OPEN
LED Open Detection	STOP	STOP	RESET	OPEN
LED Short Detection	Normal Action (at All Channel Latch->System OFF)	Stop detect Channel Only	Normal Action (at All Channel Latch->System OFF)	OPEN

Selecting external part

Selecting inductor L





The value of inductor has a great influence on input ripple current. As shown in Equation (1), as the inductor becomes large and switching frequency becomes high, the ripple current of an inductor ⊿IL becomes low.

$$\Delta IL = \frac{(V_{OUT} - V_{IN}) \times V_{IN}}{L \times V_{OUT} \times f_{SW}} [A] \quad \cdots\cdots \quad (1)$$

When the efficiency is expressed by Equation (2), input peak current will be given by Equation (3).

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \quad \cdots\cdots \quad (2)$$

$$IL_{MAX} = I_{IN} + \frac{\Delta IL}{2} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} + \frac{\Delta IL}{2} \quad \cdots\cdots \quad (3)$$

Here,

L: reactance value [H] V_{OUT}: DC/DC output voltage [V]

V_{IN}: input voltage [V]

I_{OUT}: output load current (total of LED current) [A]

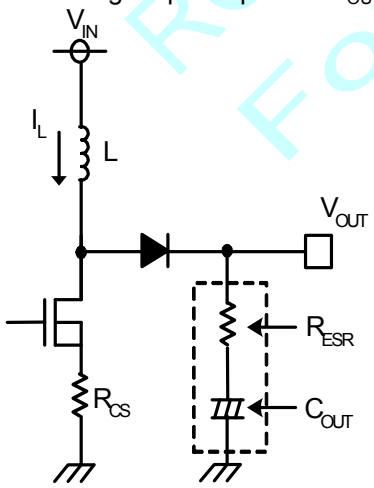
I_{IN}: input current [A] F_{SW}: oscillation frequency [Hz]

Generally, ⊿IL is set at around 30 – 50 % of output load current.

* Current exceeding the rated current value of inductor flown through the coil causes magnetic saturation, resulting in decrease in efficiency. Inductor needs to be selected to have such adequate margin that peak current does not exceed the rated current value of the inductor.

* To reduce inductor loss and improve efficiency, inductor with low resistance components (DCR, ACR) needs to be selected.

Selecting output capacitor C_{OUT}



Output capacitor needs to be selected in consideration of equivalent series resistance required to even the stable area of output voltage or ripple voltage. Be aware that set LED current may not be flown due to decrease in LED terminal voltage if output ripple voltage is high.

Output ripple voltage ⊿V_{OUT} is determined by Equation (4):

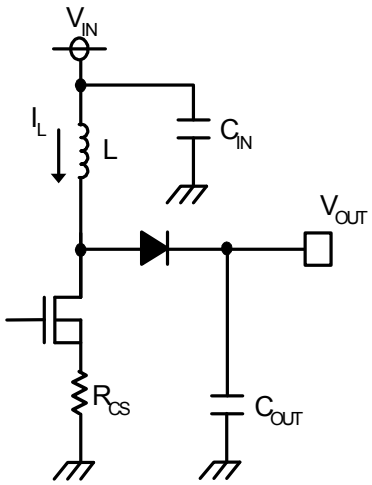
$$\Delta V_{OUT} = ILMAX \times R_{ESR} + \frac{1}{C_{OUT}} \times \frac{I_{OUT}}{\eta} \times \frac{1}{f_{SW}} [V] \quad \cdots\cdots \quad (4)$$

R_{ESR}: equivalent series resistance of C_{OUT}

* Rating of capacitor needs to be selected to have adequate margin against output voltage.

* To use an electrolytic capacitor, adequate margin against allowable current is also necessary. Be aware that current larger than set value flows transitionally in case that LED is provided with PWM dimming especially.

Selecting input capacitor C_{IN}



The input capacitor needs to be a low-ESR capacitor so large as is compatible with large ripple current to prevent large transitional voltage. Ripple current IRMS is given by Equation (5):

$$IRMS = I_{OUT} \times \frac{\sqrt{(V_{OUT} - V_{IN}) \times V_{IN}}}{V_{OUT}} [A] \quad \cdots\cdots (5)$$

Since it is highly dependent on the characteristics of the power source used to input, pattern of board wiring, and gate drain capacity of MOSFET, adequate verification needs to be performed at the operating temperature, in load range, and under MOSFET conditions.

Selecting switching MOSFET

Though there is no problem if the absolute maximum rating is the rated current of L or (withstand voltage of C_{OUT} + rectifying diode) VF or higher, one with small gate capacitance (injected charge) needs to be selected to achieve high-speed switching.

* One with over current protection setting or higher is recommended.
* Selection of one with small ON resistance results in high efficiency.

Selecting rectifying diode

A schottky barrier diode which has current ability higher than the rated current of L, reverse voltage larger than withstand voltage of C_{OUT}, and low forward voltage VF especially needs to be selected.

Selecting MOSFET for load switch and its soft-start

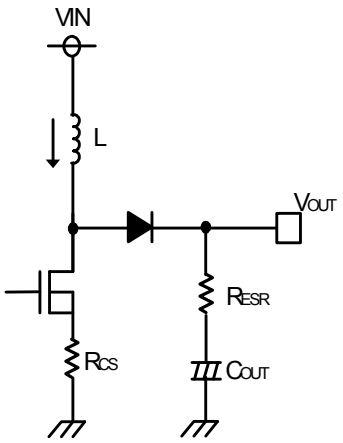
As a normal step-up DC/DC converter does not have a switch on the path from V_{IN} to V_{OUT}, output voltage is generated even though IC is OFF. To keep output voltage at 0 V until IC works, PMOSFET for load switch needs to be inserted between V_{IN} and the inductor. PMOSFET for the load switch of which gate-source withstand voltage and drain-source withstand voltage are both higher than V_{IN} needs to be selected.

To provide soft-start for the load switch, a capacitor must be inserted among gates and sources.

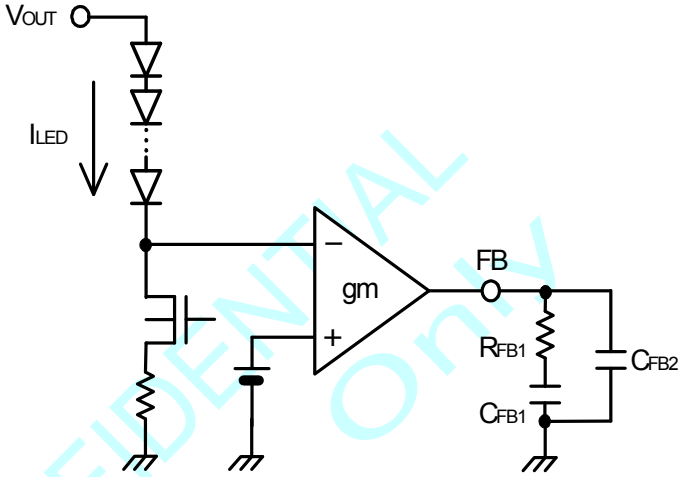
3.2 How to set phase compensation

DCDC converter application controlling current mode has each one pole (phase lag) f_p due to CR filter composed of output capacitor and output resistance (= LED current) and ZERO (phase lead) f_Z by output capacitor and ESR of the capacitor.

Moreover, step-up DC/DC converter has RHP ZERO f_{ZRHP} as another ZERO. Since RHP ZERO has a characteristic of phase lag (-90°) as pole does, cross-over frequency f_c needs to be set at RHP ZERO or lower.



Output part



Error amplifier

i. Determine Pole f_p and RHPZERO f_{ZRHP} of DC/DC converter:

$$f_p = \frac{I_{LED}}{2\pi \times V_{OUT} \times C_{OUT}} [Hz] \qquad f_{ZRHP} = \frac{V_{OUT} \times (1-D)^2}{2\pi \times L \times I_{LED}} [Hz]$$

Here, I_{LED} = total sum of LED current [A], $D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$

ii. Determine Phase compensation to be inserted into error amplifier (with f_c set at 1/5 of f_{ZRHP})

$$R_{FB1} = \frac{f_{RHZP} \times R_{CS} \times I_{LED}}{5 \times f_p \times gm \times V_{OUT} \times (1-D)} [\Omega] \qquad C_{FB1} = \frac{1}{2\pi \times R_{FB1} \times f_p} [F]$$

Here,

$$gm = 4.0 \times 10^{-4} [S]$$

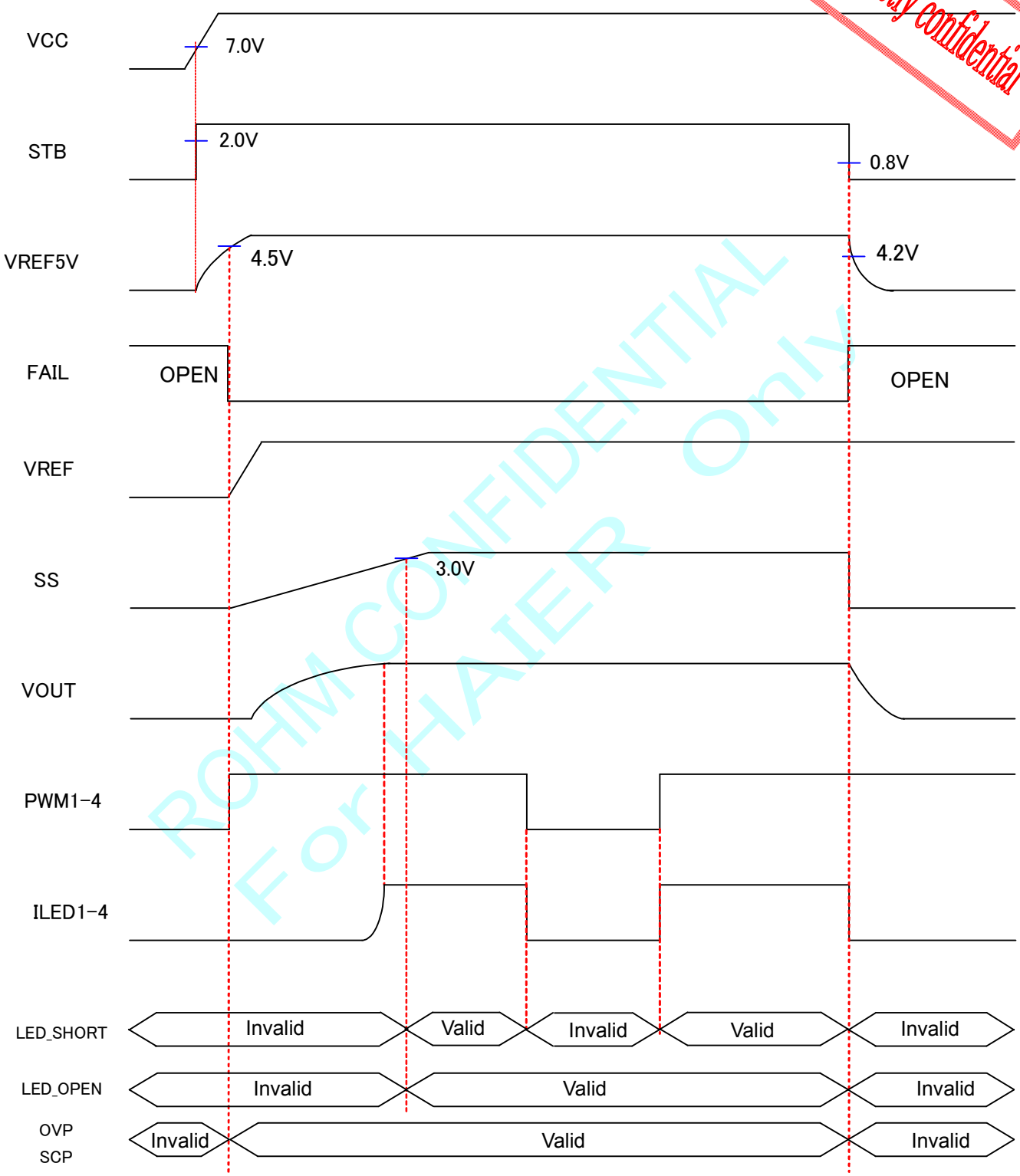
iii. Determine ZERO to compensate ESR (R_{ESR}) of C_{OUT} (electrolytic capacitor):

$$C_{FB2} = \frac{R_{ESR} \times C_{OUT}}{R_{FB1}} [F]$$

* When a ceramic capacitor (with R_{ESR} of the order of millimeters) is used to C_{OUT}, too, operation is stabilized by insertion of C_{FB2}.

Though increase in R_{FB1} and decrease in C_{FB1} are necessary to improve transient response, it needs to be adequately verified with an actual device in consideration of variation between external parts since phase margin is decreased.

3.3 Timing chart



Precautions in use

1.) This product is produced with strict quality control, but might be destroyed if used beyond its absolute maximum ratings including the range of applied voltage or operation temperature. Failure status such as short-circuit mode or open mode can not be estimated. If a special mode beyond the absolute maximum ratings is estimated, physical safety countermeasures like fuse needs to be provided.

2.) Connecting the power line to IC in reverse polarity (from that recommended) may cause damage to IC. For protection against damage caused by connection in reverse polarity, countermeasures, installation of a diode between external power source and IC power terminal, for example, needs to be taken.

3.) When this product is installed on a printed circuit board, attention needs to be paid to the orientation and position of IC. Wrong installation may cause damage to IC. Short circuit caused by problems like foreign particles entering between outputs or between an output and power GND also may cause damage.

4.) Since the back electromotive force of external coil causes regenerated current to return, countermeasures like installation of a capacitor between power source and GND as the path for regenerated current needs to be taken. The capacitance value must be determined after it is adequately verified that there is no problem in properties such that the capacity of electrolytic capacitor goes down at low temperatures. Thermal design needs to allow adequate margin in consideration of allowable loss (Pd) in actual operation state.

5.) The GND pin needs to be at the lowest potential in any operation state.

6.) Thermal design needs to be done with adequate margin in consideration of allowable loss (Pd) in actual operation state.

7.) When this product is installed on a printed circuit board, attention needs to be paid to the orientation and position of IC. Wrong installation may cause damage to IC. Short circuit caused by problems like foreign particles entering between outputs or between an output and power GND also may cause damage

8.) Use in a strong magnetic field may cause malfunction.

9.) Output Tr needs to not exceed the absolute maximum rating and ASO while using this IC. As CMOS IC and IC which has several power sources may undergo instant flow of rush current at turn-on, attention needs to be paid to the capacitance of power source coupling, power source, and the width and run length of GND wire pattern.

10.) This IC includes temperature protection circuit (TSD circuit). Temperature protection circuit (TSD circuit) strictly aims blockage of IC from thermal runaway, not protection or assurance of IC. Therefore use assuming continuous use and operation after this circuit is worked needs to not be done.

11.) As connection of a capacitor with a pin with low impedance at inspection of a set board may cause stress to IC, discharge needs to be performed every one process. Before a jig is connected to check a process, the power needs to be turned off absolutely. Before the jig is removed, as well, the power needs to be turned off.

12.) This IC is a monolithic IC which has P+ isolation for separation of elements and P board between elements.
A P-N junction is formed in this P layer and N layer of elements, composing various parasitic elements.
For example, a resistance and transistor are connected to a terminal as shown in the figure,
   - When GND>(Terminal A) in the resistance and when GND>(Terminal B) in the transistor (NPN), P-N junction operates as a parasitic diode.
   - When GND>(Terminal B) in the transistor (NPN), parasitic NPN transistor operates in N layer of other elements nearby the parasitic diode described before.

Parasitic elements are formed by the relation of potential inevitably in the structure of IC. Operation of parasitic elements can cause mutual interference among circuits , malfunction as well as damage. Therefore such use as will cause operation of parasitic elements like application of voltage on the input terminal lower than GND (P board) need to not be done.

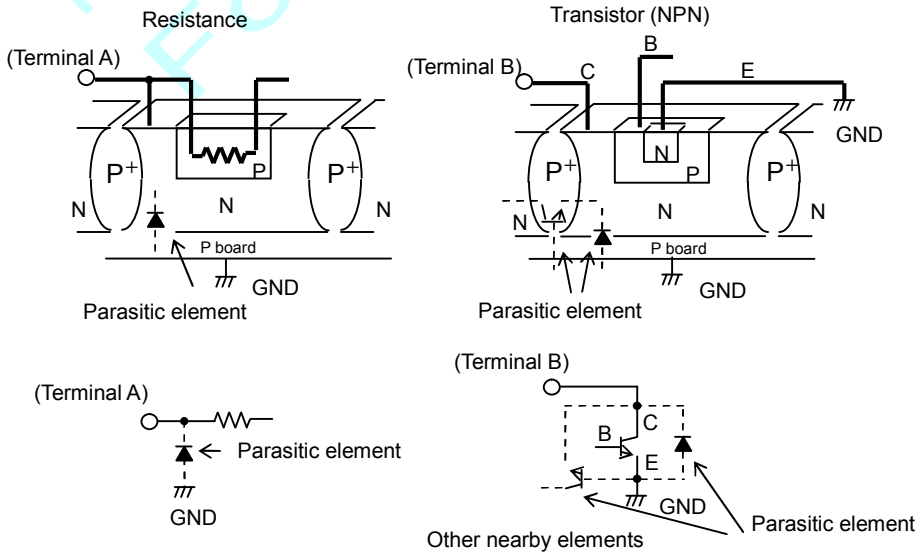


Figure: Example of simple structure of monolithic IC

5.RECORD OF REVISIONS

Revision No.	Date	Page	Description
1.0->2.0	JUL/28/2010	4	Oscillation frequency 600kHz±48kHz -> 600kHz±42kHz

Стандарт Электрон Связь

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