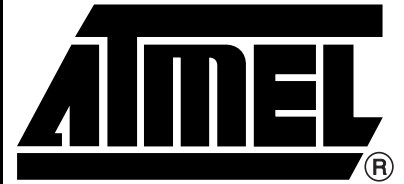
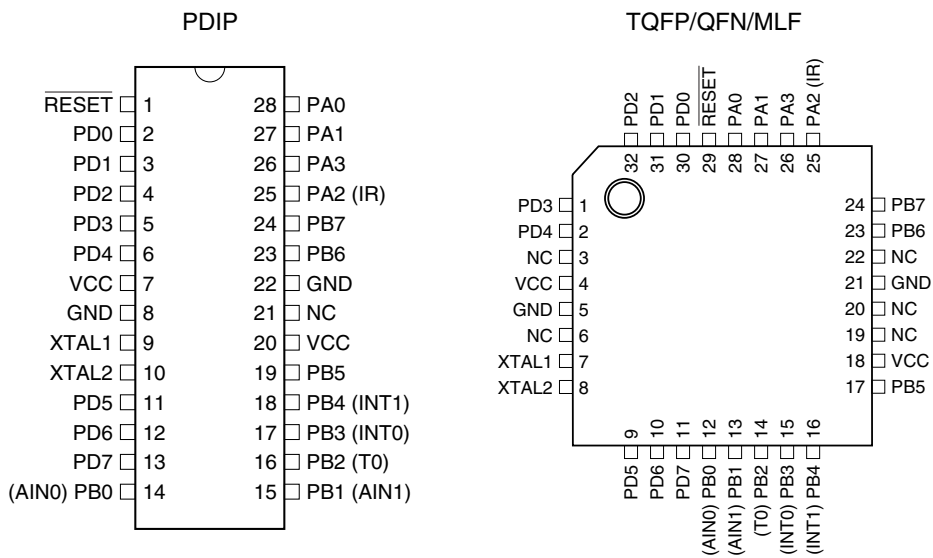


Features

- Utilizes the AVR[®] RISC Architecture
- AVR – High-performance and Low-power RISC Architecture
 - 90 Powerful Instructions – Most Single Clock Cycle Execution
 - 32 x 8 General-purpose Working Registers
 - Up to 4 MIPS Throughput at 4 MHz
- Nonvolatile Program Memory
 - 2K Bytes of Flash Program Memory
 - Endurance: 1,000 Write/Erase Cycles
 - Programming Lock for Flash Program Data Security
- Peripheral Features
 - Interrupt and Wake-up on Low-level Input
 - One 8-bit Timer/Counter with Separate Prescaler
 - On-chip Analog Comparator
 - Programmable Watchdog Timer with On-chip Oscillator
 - Built-in High-current LED Driver with Programmable Modulation
- Special Microcontroller Features
 - Low-power Idle and Power-down Modes
 - External and Internal Interrupt Sources
 - Power-on Reset Circuit with Programmable Start-up Time
 - Internal Calibrated RC Oscillator
- Power Consumption at 1 MHz, 2V, 25°C
 - Active: 3.0 mA
 - Idle Mode: 1.2 mA
 - Power-down Mode: <1 μA
- I/O and Packages
 - 11 Programmable I/O Lines, 8 Input Lines and a High-current LED Driver
 - 28-lead PDIP, 32-lead TQFP, and 32-pad MLF
- Operating Voltages
 - V_{CC}: 1.8V - 5.5V for the ATtiny28V
 - V_{CC}: 2.7V - 5.5V for the ATtiny28L
- Speed Grades
 - 0 - 1.2 MHz for the ATtiny28V
 - 0 - 4 MHz For the ATtiny28L

Pin Configurations



8-bit AVR[®]
Microcontroller
with 2K Bytes of
Flash

ATtiny28L
ATtiny28V

Summary

Rev. 1062FS-AVR-07/06



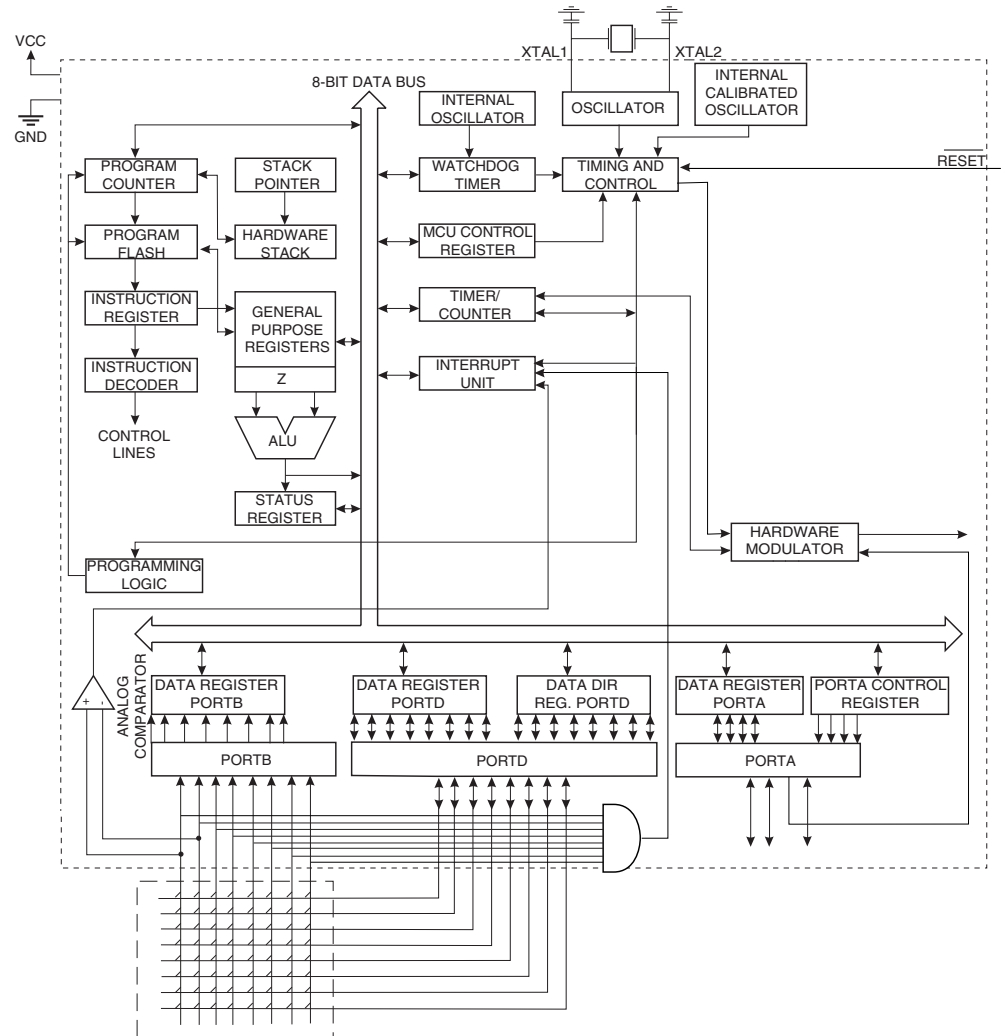
Note: This is a summary document. A complete document is available on our Web site at www.atmel.com.

Description

The ATtiny28 is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny28 achieves throughputs approaching 1 MIPS per MHz, allowing the system designer to optimize power consumption versus processing speed. The AVR core combines a rich instruction set with 32 general-purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

Block Diagram

Figure 1. The ATtiny28 Block Diagram



The ATtiny28 provides the following features: 2K bytes of Flash, 11 general-purpose I/O lines, 8 input lines, a high-current LED driver, 32 general-purpose working registers, an 8-bit timer/counter, internal and external interrupts, programmable Watchdog Timer with internal oscillator and 2 software-selectable power-saving modes. The Idle Mode stops the CPU while allowing the timer/counter and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset. The wake-up or inter-

rupt on low-level input feature enables the ATtiny28 to be highly responsive to external events, still featuring the lowest power consumption while in the power-down modes.

The device is manufactured using Atmel's high-density, nonvolatile memory technology. By combining an enhanced RISC 8-bit CPU with Flash on a monolithic chip, the Atmel ATtiny28 is a powerful microcontroller that provides a highly flexible and cost-effective solution to many embedded control applications. The ATtiny28 AVR is supported with a full suite of program and system development tools including: macro assemblers, program debugger/simulators, in-circuit emulators and evaluation kits.

Pin Descriptions

VCC	Supply voltage pin.
GND	Ground pin.
Port A (PA3..PA0)	Port A is a 4-bit I/O port. PA2 is output-only and can be used as a high-current LED driver. At $V_{CC} = 2.0V$, the PA2 output buffer can sink 25 mA. PA3, PA1 and PA0 are bi-directional I/O pins with internal pull-ups (selected for each bit). The port pins are tri-stated when a reset condition becomes active, even if the clock is not running.
Port B (PB7..PB0)	Port B is an 8-bit input port with internal pull-ups (selected for all Port B pins). Port B pins that are externally pulled low will source current if the pull-ups are activated. Port B also serves the functions of various special features of the ATtiny28 as listed on page 27. If any of the special features are enabled, the pull-up(s) on the corresponding pin(s) is automatically disabled. The port pins are tri-stated when a reset condition becomes active, even if the clock is not running.
Port D (PD7..PD0)	Port D is an 8-bit I/O port. Port pins can provide internal pull-up resistors (selected for each bit). The port pins are tri-stated when a reset condition becomes active, even if the clock is not running.
XTAL1	Input to the inverting oscillator amplifier and input to the internal clock operating circuit.
XTAL2	Output from the inverting oscillator amplifier.
$\overline{\text{RESET}}$	Reset input. An external reset is generated by a low level on the $\overline{\text{RESET}}$ pin. Reset pulses longer than 50 ns will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset.



Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
\$3F	SREG	I	T	H	S	V	N	Z	C	page 6
\$3E	Reserved									
...	Reserved									
\$20	Reserved									
\$1F	Reserved									
\$1E	Reserved									
\$1D	Reserved									
\$1C	Reserved									
\$1B	PORTA	-	-	-	-	PORTA3	PORTA2	PORTA1	PORTA0	page 32
\$1A	PACR	-	-	-	-	DDA3	PA2HC	DDA1	DDA0	page 32
\$19	PINA	-	-	-	-	PINA3	-	PINA1	PINA0	page 32
\$18	Reserved									
\$17	Reserved									
\$16	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	page 32
\$15	Reserved									
\$14	Reserved									
\$13	Reserved									
\$12	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	page 33
\$11	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	page 33
\$10	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	page 33
\$0F	Reserved									
\$0E	Reserved									
\$0D	Reserved									
\$0C	Reserved									
\$0B	Reserved									
\$0A	Reserved									
\$09	Reserved									
\$08	ACSR	ACD	-	ACO	ACI	ACIE	-	ACIS1	ACIS0	page 44
\$07	MCUCS	PLUPB	-	SE	SM	WDRF	-	EXTRF	PORF	page 19
\$06	ICR	INT1	INT0	LLIE	TOIE0	ISC11	ISC10	ISC01	ISC00	page 22
\$05	IFR	INTF1	INTF0	-	TOV0	-	-	-	-	page 23
\$04	TCCR0	FOV0	-	-	OOM01	OOM00	CS02	CS01	CS00	page 35
\$03	TCNT0	Timer/Counter0 (8-bit)								page 36
\$02	MODCR	ONTIM4	ONTIM3	ONTIM2	ONTIM1	ONTIM0	MCONF2	MCONF1	MCONF0	page 43
\$01	WDTCR	-	-	-	WDTOE	WDE	WDP2	WDP1	WDP0	page 37
\$00	OSCCAL	Oscillator Calibration Register								page 9

- Notes:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
 2. Some of the status flags are cleared by writing a logical "1" to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers \$00 to \$1F only.

Instruction Set Summary

Mnemonic	Operands	Description	Operation	Flags	# Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add Two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry Two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
SUB	Rd, Rr	Subtract Two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry Two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \cdot Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd \cdot K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd \vee Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \vee K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	$Rd \leftarrow \text{NOT } Rd$	Z,C,N,V	1
NEG	Rd	Two's Complement	$Rd \leftarrow \text{NOT } Rd + 1$	Z,C,N,V,H	1
SBR	Rd, K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V	1
CBR	Rd, K	Clear Bit(s) in Register	$Rd \leftarrow Rd \cdot (\text{NOT } K)$	Z,N,V	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \cdot Rd$	Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow \text{NOT } Rd$	Z,N,V	1
SER	Rd	Set Register	$Rd \leftarrow \text{NOT } \text{NOT } Rd$	None	1
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
RCALL	k	Relative Subroutine Call	$PC \leftarrow PC + k + 1$	None	3
RET		Subroutine Return	$PC \leftarrow \text{STACK}$	None	4
RETI		Interrupt Return	$PC \leftarrow \text{STACK}$	I	4
CPSE	Rd, Rr	Compare, Skip if Equal	if $(Rd = Rr)$ $PC \leftarrow PC + 2$ or 3	None	1/2
CP	Rd, Rr	Compare	$Rd - Rr$	Z,N,V,C,H	1
CPC	Rd, Rr	Compare with Carry	$Rd - Rr - C$	Z,N,V,C,H	1
CPI	Rd, K	Compare Register with Immediate	$Rd - K$	Z,N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if $(Rr(b) = 0)$ $PC \leftarrow PC + 2$ or 3	None	1/2
SBRS	Rr, b	Skip if Bit in Register is Set	if $(Rr(b) = 1)$ $PC \leftarrow PC + 2$ or 3	None	1/2
SBIC	P, b	Skip if Bit in I/O Register Cleared	if $(P(b) = 0)$ $PC \leftarrow PC + 2$ or 3	None	1/2
SBIS	P, b	Skip if Bit in I/O Register is Set	if $(P(b) = 1)$ $PC \leftarrow PC + 2$ or 3	None	1/2
BRBS	s, k	Branch if Status Flag Set	if $(SREG(s) = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if $(SREG(s) = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BREQ	k	Branch if Equal	if $(Z = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRNE	k	Branch if Not Equal	if $(Z = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRCS	k	Branch if Carry Set	if $(C = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRCC	k	Branch if Carry Cleared	if $(C = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRSH	k	Branch if Same or Higher	if $(C = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRLO	k	Branch if Lower	if $(C = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRMI	k	Branch if Minus	if $(N = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRPL	k	Branch if Plus	if $(N = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if $(N \oplus V = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRLT	k	Branch if Less than Zero, Signed	if $(N \oplus V = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRHS	k	Branch if Half-carry Flag Set	if $(H = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRHC	k	Branch if Half-carry Flag Cleared	if $(H = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRTS	k	Branch if T-flag Set	if $(T = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRTC	k	Branch if T-flag Cleared	if $(T = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if $(V = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if $(V = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRIE	k	Branch if Interrupt Enabled	if $(I = 1)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRID	k	Branch if Interrupt Disabled	if $(I = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2

Instruction Set Summary (Continued)

Mnemonic	Operands	Description	Operation	Flags	# Clocks
DATA TRANSFER INSTRUCTIONS					
LD	Rd, Z	Load Register Indirect	$Rd \leftarrow (Z)$	None	2
ST	Z, Rr	Store Register Indirect	$(Z) \leftarrow Rr$	None	2
MOV	Rd, Rr	Move between Registers	$Rd \leftarrow Rr$	None	1
LDI	Rd, K	Load Immediate	$Rd \leftarrow K$	None	1
IN	Rd, P	In Port	$Rd \leftarrow P$	None	1
OUT	P, Rr	Out Port	$P \leftarrow Rr$	None	1
LPM		Load Program Memory	$R0 \leftarrow (Z)$	None	3
BIT AND BIT-TEST INSTRUCTIONS					
SBI	P, b	Set Bit in I/O Register	$I/O(P,b) \leftarrow 1$	None	2
CBI	P, b	Clear Bit in I/O Register	$I/O(P,b) \leftarrow 0$	None	2
LSL	Rd	Logical Shift Left	$Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$	Z,C,N,V	1
LSR	Rd	Logical Shift Right	$Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$	Z,C,N,V	1
ROL	Rd	Rotate Left through Carry	$Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$	Z,C,N,V	1
ROR	Rd	Rotate Right through Carry	$Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	$Rd(n) \leftarrow Rd(n+1), n = 0..6$	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	$Rd(3..0) \leftarrow Rd(7..4), Rd(7..4) \leftarrow Rd(3..0)$	None	1
BSET	s	Flag Set	$SREG(s) \leftarrow 1$	SREG(s)	1
BCLR	s	Flag Clear	$SREG(s) \leftarrow 0$	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	$T \leftarrow Rr(b)$	T	1
BLD	Rd, b	Bit Load from T to Register	$Rd(b) \leftarrow T$	None	1
SEC		Set Carry	$C \leftarrow 1$	C	1
CLC		Clear Carry	$C \leftarrow 0$	C	1
SEN		Set Negative Flag	$N \leftarrow 1$	N	1
CLN		Clear Negative Flag	$N \leftarrow 0$	N	1
SEZ		Set Zero Flag	$Z \leftarrow 1$	Z	1
CLZ		Clear Zero Flag	$Z \leftarrow 0$	Z	1
SEI		Global Interrupt Enable	$I \leftarrow 1$	I	1
CLI		Global Interrupt Disable	$I \leftarrow 0$	I	1
SES		Set Signed Test Flag	$S \leftarrow 1$	S	1
CLS		Clear Signed Test Flag	$S \leftarrow 0$	S	1
SEV		Set Two's Complement Overflow	$V \leftarrow 1$	V	1
CLV		Clear Two's Complement Overflow	$V \leftarrow 0$	V	1
SET		Set T in SREG	$T \leftarrow 1$	T	1
CLT		Clear T in SREG	$T \leftarrow 0$	T	1
SEH		Set Half-carry Flag in SREG	$H \leftarrow 1$	H	1
CLH		Clear Half-carry Flag in SREG	$H \leftarrow 0$	H	1
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1

Ordering Information

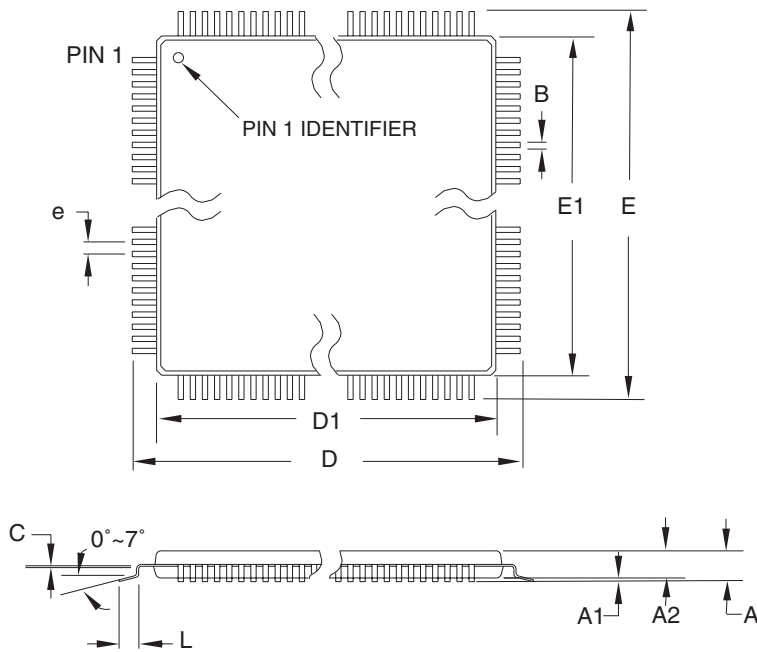
Speed (MHz)	Power Supply (Volts)	Ordering Code	Package ⁽¹⁾	Operation Range
4	2.7 - 5.5	ATtiny28L-4AC	32A	Commercial (0°C to 70°C)
		ATtiny28L-4PC	28P3	
		ATtiny28L-4MC	32M1-A	
		ATtiny28L-4AI	32A	Industrial (-40°C to 85°C)
		ATtiny28L-4AU ⁽²⁾	32A	
		ATtiny28L-4PI	28P3	
ATtiny28L-4PU ⁽²⁾	28P3			
ATtiny28L-4MI	32M1-A			
ATtiny28L-4MU ⁽²⁾	32M1-A			
1.2	1.8 - 5.5	ATtiny28V-1AC	32A	Commercial (0°C to 70°C)
		ATtiny28V-1PC	28P3	
		ATtiny28V-1MC	32M1-A	
		ATtiny28V-1AI	32A	Industrial (-40°C to 85°C)
		ATtiny28V-1AU ⁽²⁾	32A	
		ATtiny28V-1PI	28P3	
ATtiny28V-1PU ⁽²⁾	28P3			
ATtiny28V-1MI	32M1-A			
ATtiny28V-1MU ⁽²⁾	32M1-A			

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. Pb-free packaging alternative, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

Package Type	
32A	32-lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)
28P3	28-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
32M1-A	32-pad, 5x5x1.0 body, Lead Pitch 0.50mm, Quad Flat No-lead/Micro Lead Frame Package (QFN/MLF)

Packaging Information

32A



COMMON DIMENSIONS
(Unit of Measure = mm)

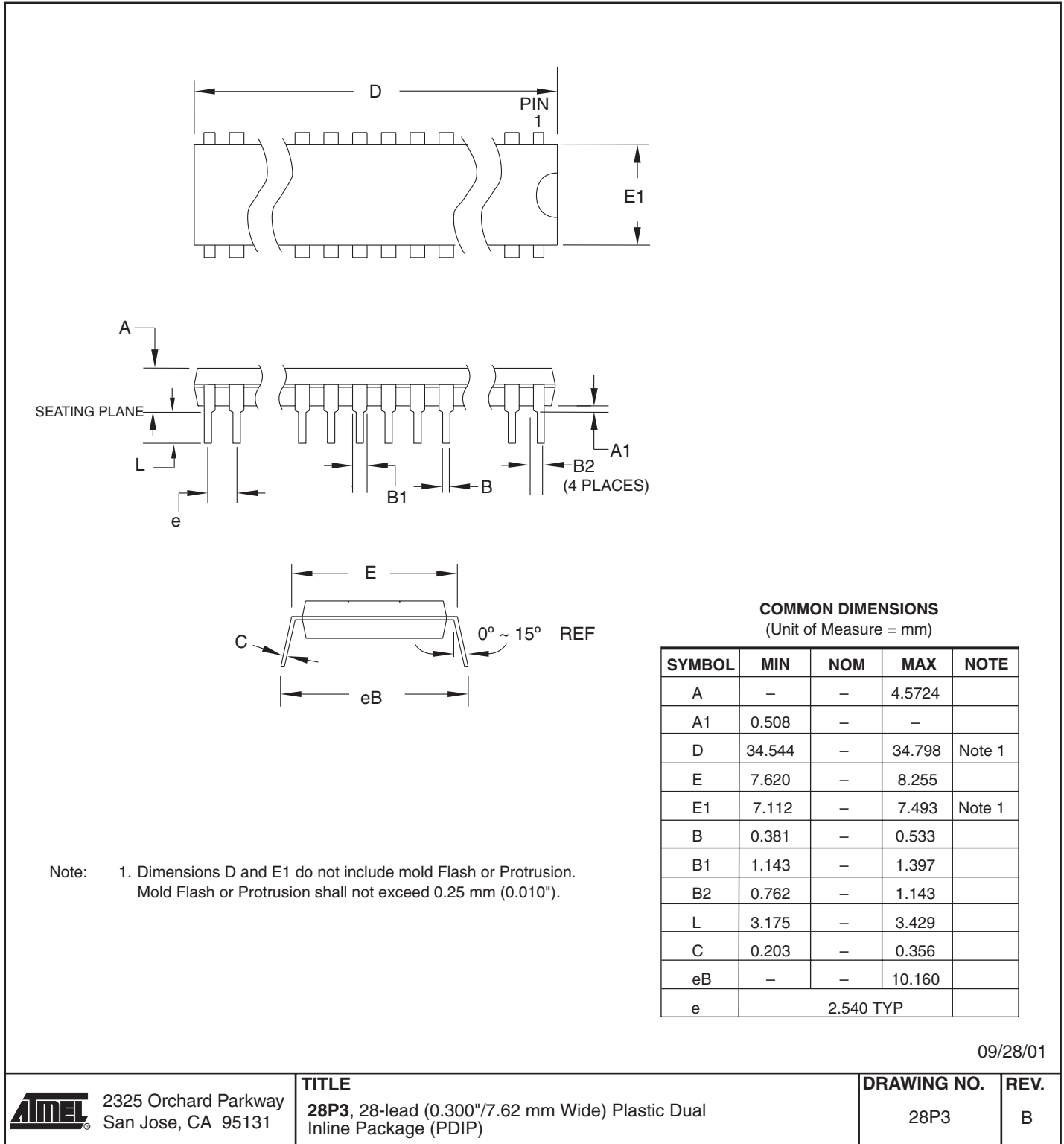
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	8.75	9.00	9.25	
D1	6.90	7.00	7.10	Note 2
E	8.75	9.00	9.25	
E1	6.90	7.00	7.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-026, Variation ABA.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
 3. Lead coplanarity is 0.10 mm maximum.

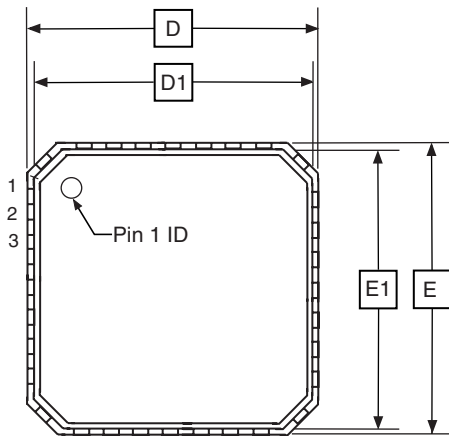
10/5/2001

2325 Orchard Parkway San Jose, CA 95131	TITLE	DRAWING NO.	REV.
	32A , 32-lead, 7 x 7 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	32A	B

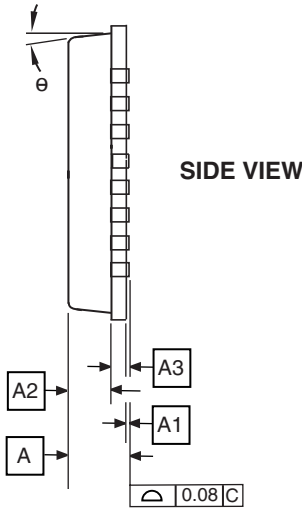
28P3



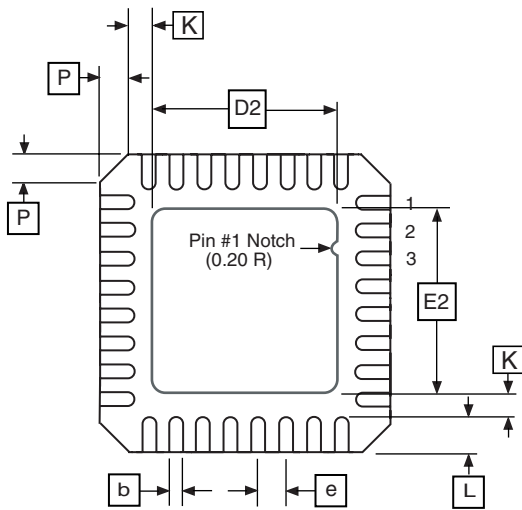
32M1-A



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	-	0.02	0.05	
A2	-	0.65	1.00	
A3	0.20 REF			
b	0.18	0.23	0.30	
D	4.90	5.00	5.10	
D1	4.70	4.75	4.80	
D2	2.95	3.10	3.25	
E	4.90	5.00	5.10	
E1	4.70	4.75	4.80	
E2	2.95	3.10	3.25	
e	0.50 BSC			
L	0.30	0.40	0.50	
P	-	-	0.60	
θ	-	-	12°	
K	0.20	-	-	

Note: JEDEC Standard MO-220, Fig. 2 (Anvil Singulation), VHHD-2.

5/25/06



2325 Orchard Parkway
San Jose, CA 95131

TITLE

32M1-A, 32-pad, 5 x 5 x 1.0 mm Body, Lead Pitch 0.50 mm,
3.10 mm Exposed Pad, Micro Lead Frame Package (MLF)

DRAWING NO.

32M1-A

REV.

E

Errata

All revisions

No known errata.

Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

Rev – 01/06G

1. Updated chapter layout.
2. Updated "Ordering Information" on page 7.

Rev – 01/06G

1. Updated description for "Port A" on page 25.
2. Added note 6 in "DC Characteristics" on page 54.
3. Updated "Ordering Information" on page 7.
4. Added "Errata" on page 11.

Rev – 03/05F

1. Updated "Electrical Characteristics" on page 54.
2. MLF-package alternative changed to "Quad Flat No-Lead/Micro Lead Frame Package QFN/MLF".
3. Updated "Ordering Information" on page 7.



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