

FEATURES

- 16-Bit 250ksps ADCs in MSOP Package
- Single 5V Supply
- Low Supply Current: 850µA (Typ)
- Auto Shutdown Reduces Supply Current to 2µA at 1ksps
- True Differential Inputs
- 1-Channel (LTC1864) or 2-Channel (LTC1865) Versions
- SPI/MICROWIRE™ Compatible Serial I/O
- 16-Bit Upgrade to 12-Bit LTC1286/LTC1298
- Pin Compatible with 12-Bit LTC1860/LTC1861
- Guaranteed Operation to +125°C (MSOP Package)

APPLICATIONS

- High Speed Data Acquisition
- Portable or Compact Instrumentation
- Low Power Battery-Operated Instrumentation
- Isolated and/or Remote Data Acquisition

LT, LT, LTC and LTM are registered trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners.

DESCRIPTION

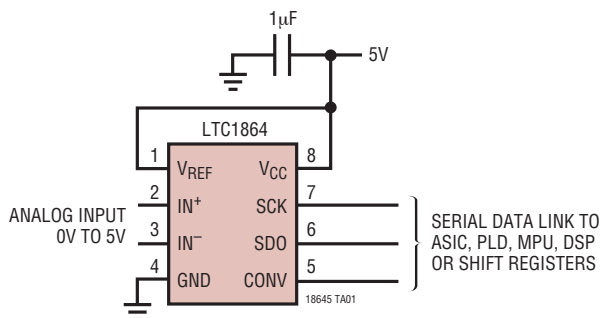
The LTC®1864/LTC1865 are 16-bit A/D converters that are offered in MSOP and SO-8 packages and operate on a single 5V supply. At 250ksps, the supply current is only 850µA. The supply current drops at lower speeds because the LTC1864/LTC1865 automatically power down between conversions. These 16-bit switched capacitor successive approximation ADCs include sample-and-holds. The LTC1864 has a differential analog input with an adjustable reference pin. The LTC1865 offers a software-selectable 2-channel MUX and an adjustable reference pin on the MSOP version.

The 3-wire, serial I/O, small MSOP or SO-8 package and extremely high sample rate-to-power ratio make these ADCs ideal choices for compact, low power, high speed systems.

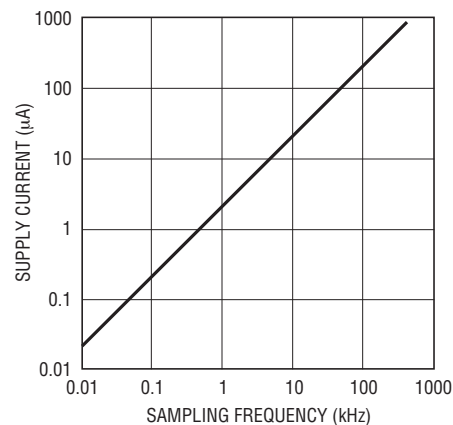
These ADCs can be used in ratiometric applications or with external references. The high impedance analog inputs and the ability to operate with reduced spans down to 1V full scale, allow direct connection to signal sources in many applications, eliminating the need for external gain stages.

TYPICAL APPLICATION

Single 5V Supply, 250ksps, 16-Bit Sampling ADC



Supply Current vs Sampling Frequency



LTC1864/LTC1865

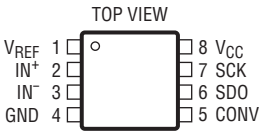
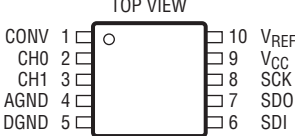
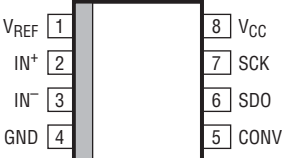
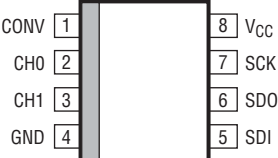
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) 7V
 Ground Voltage Difference
 AGND, DGND LTC1865 MSOP Package $\pm 0.3V$
 Analog Input (GND – 0.3V) to ($V_{CC} + 0.3V$)
 Digital Input (GND – 0.3V) to 7V
 Digital Output (GND – 0.3V) to ($V_{CC} + 0.3V$)
 Power Dissipation 400mW

Operating Temperature Range
 LTC1864C/LTC1865C/
 LTC1864AC/LTC1865AC 0°C to 70°C
 LTC1864I/LTC1865I/
 LTC1864AI/LTC1865AI –40°C to 85°C
 LTC1864H/LTC1865H
 LTC1864AH/LTC1865AH –40°C to 125°C
 Storage Temperature Range –65°C to 150°C
 Lead Temperature (Soldering, 10 sec) 300°C

PIN CONFIGURATION

LTC1864  MS8 PACKAGE 8-LEAD PLASTIC MSOP $T_{JMAX} = 150^{\circ}C, \theta_{JA} = 210^{\circ}C/W$	LTC1865  MS PACKAGE 10-LEAD PLASTIC MSOP $T_{JMAX} = 150^{\circ}C, \theta_{JA} = 210^{\circ}C/W$
LTC1864  S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}C, \theta_{JA} = 175^{\circ}C/W$	LTC1865  S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}C, \theta_{JA} = 175^{\circ}C/W$

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1864CMS8#PBF	LTC1864CMS8#TRPBF	LTHQ	8-Lead Plastic MSOP	0°C to 70°C
LTC1864IMS8#PBF	LTC1864IMS8#TRPBF	LTHQ	8-Lead Plastic MSOP	–40°C to 85°C
LTC1864HMS8#PBF	LTC1864HMS8#TRPBF	LTHQ	8-Lead Plastic MSOP	–40°C to 125°C
LTC1864ACMS8#PBF	LTC1864ACMS8#TRPBF	LTHQ	8-Lead Plastic MSOP	0°C to 70°C
LTC1864AIMS8#PBF	LTC1864AIMS8#TRPBF	LTHQ	8-Lead Plastic MSOP	–40°C to 85°C
LTC1864AHMS8#PBF	LTC1864AHMS8#TRPBF	LTHQ	8-Lead Plastic MSOP	–40°C to 125°C
LTC1864CS8#PBF	LTC1864CS8#TRPBF	1864	8-Lead Plastic SO	0°C to 70°C
LTC1864IS8#PBF	LTC1864IS8#TRPBF	1864I	8-Lead Plastic SO	–40°C to 85°C
LTC1864ACS8#PBF	LTC1864ACS8#TRPBF	1864A	8-Lead Plastic SO	0°C to 70°C
LTC1864AIS8#PBF	LTC1864AIS8#TRPBF	1864AI	8-Lead Plastic SO	–40°C to 85°C
LTC1865CMS#PBF	LTC1865CMS#TRPBF	LTHS	10-Lead Plastic MSOP	0°C to 70°C
LTC1865IMS#PBF	LTC1865IMS#TRPBF	LTHS	10-Lead Plastic MSOP	–40°C to 85°C

18645fb

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1865HMS#PBF	LTC1865HMS#TRPBF	LTHS	10-Lead Plastic MSOP	–40°C to 125°C
LTC1865ACMS#PBF	LTC1865ACMS#TRPBF	LTHS	10-Lead Plastic MSOP	0°C to 70°C
LTC1865AIMS#PBF	LTC1865AIMS#TRPBF	LTHS	10-Lead Plastic MSOP	–40°C to 85°C
LTC1865AHMS#PBF	LTC1865AHMS#TRPBF	LTHS	10-Lead Plastic MSOP	–40°C to 125°C
LTC1865CS8#PBF	LTC1865CS8#TRPBF	1865	8-Lead Plastic SO	0°C to 70°C
LTC1865IS8#PBF	LTC1865IS8#TRPBF	1865I	8-Lead Plastic SO	–40°C to 85°C
LTC1865ACS8#PBF	LTC1865ACS8#TRPBF	1865A	8-Lead Plastic SO	0°C to 70°C
LTC1865AIS8#PBF	LTC1865AIS8#TRPBF	1865AI	8-Lead Plastic SO	–40°C to 85°C
LEAD BASED FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1864CMS8	LTC1864CMS8#TR	LTHQ	8-Lead Plastic MSOP	0°C to 70°C
LTC1864IMS8	LTC1864IMS8#TR	LTHQ	8-Lead Plastic MSOP	–40°C to 85°C
LTC1864HMS8	LTC1864HMS8#TR	LTHQ	8-Lead Plastic MSOP	–40°C to 125°C
LTC1864ACMS8	LTC1864ACMS8#TR	LTHQ	8-Lead Plastic MSOP	0°C to 70°C
LTC1864AIMS8	LTC1864AIMS8#TR	LTHQ	8-Lead Plastic MSOP	–40°C to 85°C
LTC1864AHMS8	LTC1864AHMS8#TR	LTHQ	8-Lead Plastic MSOP	–40°C to 125°C
LTC1864CS8	LTC1864CS8#TR	1864	8-Lead Plastic SO	0°C to 70°C
LTC1864IS8	LTC1864IS8#TR	1864I	8-Lead Plastic SO	–40°C to 85°C
LTC1864ACS8	LTC1864ACS8#TR	1864A	8-Lead Plastic SO	0°C to 70°C
LTC1684AIS8	LTC1684AIS8#TR	1864AI	8-Lead Plastic SO	–40°C to 85°C
LTC1865CMS	LTC1865CMS#TR	LTHS	10-Lead Plastic MSOP	0°C to 70°C
LTC1865IMS	LTC1865IMS#TR	LTHS	10-Lead Plastic MSOP	–40°C to 85°C
LTC1865HMS	LTC1865HMS#TR	LTHS	10-Lead Plastic MSOP	–40°C to 125°C
LTC1865ACMS	LTC1865ACMS#TR	LTHS	10-Lead Plastic MSOP	0°C to 70°C
LTC1865AIMS	LTC1865AIMS#TR	LTHS	10-Lead Plastic MSOP	–40°C to 85°C
LTC1865AHMS	LTC1865AHMS#TR	LTHS	10-Lead Plastic MSOP	–40°C to 125°C
LTC1865CS8	LTC1865CS8#TR	1865	8-Lead Plastic SO	0°C to 70°C
LTC1865IS8	LTC1865IS8#TR	1865I	8-Lead Plastic SO	–40°C to 85°C
LTC1865ACS8	LTC1865ACS8#TR	1865A	8-Lead Plastic SO	0°C to 70°C
LTC1865AIS8	LTC1865AIS8#TR	1865AI	8-Lead Plastic SO	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

LTC1864/LTC1865

CONVERTER AND MULTIPLEXER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{CC} = 5\text{V}$, $V_{REF} = 5\text{V}$, $f_{SCK} = f_{SCK}(\text{MAX})$ as defined in Recommended Operating Conditions, unless otherwise noted.

PARAMETER	CONDITIONS		LTC1864/LTC1865			LTC1864A/LTC1865A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		●	16			16			Bits
No Missing Codes Resolution		●	14			15			Bits
INL	(Note 3) H-Grade (Note 3)	● ●			± 8 ± 8.5			± 6 ± 6.5	LSB LSB
Transition Noise				1.1			1.1		LSB_{RMS}
Gain Error		●			± 20			± 20	mV
Offset Error	LTC1864 SO-8 and MSOP, LTC1865 MSOP LTC1865 SO-8	● ●		± 2 ± 3	± 5 ± 7		± 2 ± 3	± 5 ± 7	mV mV
Input Differential Voltage Range	$V_{IN} = IN^+ - IN^-$	●	0		V_{REF}	0		V_{REF}	V
Absolute Input Range	IN^+ Input IN^- Input		-0.05 -0.05		$V_{CC} + 0.05$ $V_{CC}/2$	-0.05 -0.05		$V_{CC} + 0.05$ $V_{CC}/2$	V V
V_{REF} Input Range	LTC1864 SO-8 and MSOP, LTC1865 MSOP		1		V_{CC}	1		V_{CC}	V
Analog Input Leakage Current	(Note 4)	●			± 1			± 1	μA
C_{IN} Input Capacitance	In Sample Mode During Conversion			12 5			12 5		pF pF

DYNAMIC ACCURACY

$T_A = 25^\circ\text{C}$. $V_{CC} = 5\text{V}$, $V_{REF} = 5\text{V}$, $f_{\text{SAMPLE}} = 250\text{kHz}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LTC1864/LTC1865			UNITS
			MIN	TYP	MAX	
SNR	Signal-to-Noise Ratio			87		dB
$S/(N + D)$	Signal-to-Noise Plus Distortion Ratio	10kHz Input Signal		83		dB
		100kHz Input Signal		76		dB
THD	Total Harmonic Distortion Up to 5th Harmonic	10kHz Input Signal		88		dB
		100kHz Input Signal		77		dB
	Full Power Bandwidth			20		MHz
	Full Linear Bandwidth	$S/(N+D) \geq 75\text{dB}$		125		kHz

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25^\circ\text{C}$. $V_{CC} = 5\text{V}$, $V_{REF} = 5\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LTC1864/LTC1865			UNITS
			MIN	TYP	MAX	
V_{IH}	High Level Input Voltage	$V_{CC} = 5.25\text{V}$	●	2.4		V
V_{IL}	Low Level Input Voltage	$V_{CC} = 4.75\text{V}$	●		0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●		2.5	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0\text{V}$	●		-2.5	μA
V_{OH}	High Level Output Voltage	$V_{CC} = 4.75\text{V}$, $I_O = 10\mu\text{A}$ $V_{CC} = 4.75\text{V}$, $I_O = 360\mu\text{A}$	● ●	4.5 2.4	4.74 4.72	V V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.75\text{V}$, $I_O = 1.6\text{mA}$	●		0.4	V
I_{OZ}	Hi-Z Output Leakage	$CONV = V_{CC}$	●		± 3	μA
I_{SOURCE}	Output Source Current	$V_{OUT} = 0\text{V}$		-25		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$		20		mA
I_{REF}	Reference Current (LTC1864 SO-8 and MSOP, LTC1865 MSOP)	$CONV = V_{CC}$ $f_{SMPL} = f_{SMPL(MAX)}$	● ●	0.001 0.05	3 0.1	μA mA
I_{CC}	Supply Current	$CONV = V_{CC}$ After Conversion $CONV = V_{CC}$ After Conversion, H-Grade $f_{SMPL} = f_{SMPL(MAX)}$	● ● ●	0.001 0.001 0.85	3 5 1.3	μA μA mA
P_D	Power Dissipation	$f_{SMPL} = f_{SMPL(MAX)}$		4.25		mW

LTC1864/LTC1865

RECOMMENDED OPERATING CONDITIONS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25^\circ\text{C}$.

SYMBOL	PARAMETER	CONDITIONS	LTC1864/LTC1865			UNITS
			MIN	TYP	MAX	
V_{CC}	Supply Voltage		4.75		5.25	V
f_{SCK}	Clock Frequency	H-Grade ● ●			20 16.7	MHz MHz
t_{CYC}	Total Cycle Time		$16 \cdot SCK + t_{CONV}$			μs
t_{SMPL}	Analog Input Sampling Time	LTC1864 (Note 5) LTC1865 (Note 5)	16 14			SCK SCK
t_{suCONV}	Setup Time CONV↓ Before First SCK↑ (See Figure 1)	H-Grade	60 65	30 30		ns ns
t_{hDI}	Hold Time SDI After SCK↑	LTC1865	15			ns
t_{suDI}	Setup Time SSDI Stable Before SCK↑	LTC1865	15			ns
t_{WHCLK}	SCK High Time	$f_{SCK} = f_{SCK(MAX)}$	40%			$1/f_{SCK}$
t_{WLCLK}	SCK Low Time	$f_{SCK} = f_{SCK(MAX)}$	40%			$1/f_{SCK}$
t_{WHCONV}	CONV High Time Between Data Transfer Cycles	(Note 5)	t_{CONV}			μs
t_{WLCONV}	CONV Low Time During Data Transfer	(Note 5)	16			SCK
t_{hCONV}	Hold Time CONV Low After Last SCK↑			13		ns

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25^\circ\text{C}$. $V_{CC} = 5\text{V}$, $V_{REF} = 5\text{V}$, $f_{SCK} = f_{SCK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1864/LTC1865			UNITS
				MIN	TYP	MAX	
t_{CONV}	Conversion Time (See Figure 1)	H-Grade	● ●		2.75 2.75	3.2 3.3	μs μs
$f_{SMPL(MAX)}$	Maximum Sampling Frequency	H-Grade	● ●	250 234			kHz kHz
t_{dDO}	Delay Time, $SCK\downarrow$ to SDO Data Valid	$C_{LOAD} = 20\text{pF}$ $C_{LOAD} = 20\text{pF}$ $C_{LOAD} = 20\text{pF}$, H-Grade	● ● ●		15	20 25 30	ns ns ns
t_{dis}	Delay Time, $CONV\uparrow$ to SDO Hi-Z	H-Grade	● ●		30 30	60 65	ns ns
t_{en}	Delay Time, $CONV\downarrow$ to SDO Enabled	$C_{LOAD} = 20\text{pF}$ $C_{LOAD} = 20\text{pF}$, H-Grade	● ●		30 30	60 65	ns ns
t_{hDO}	Time Output Data Remains Valid After $SCK\downarrow$	$C_{LOAD} = 20\text{pF}$	●	5	10		ns
t_r	SDO Rise Time	$C_{LOAD} = 20\text{pF}$			8		ns
t_f	SDO Fall Time	$C_{LOAD} = 20\text{pF}$			4		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

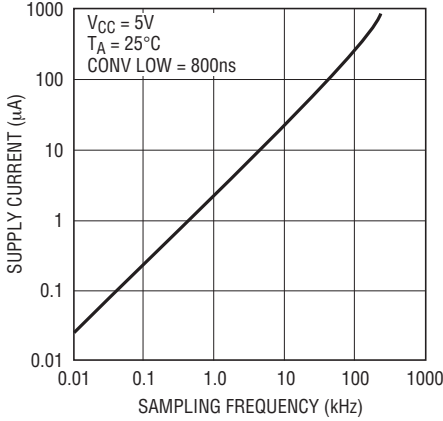
Note 3: Integral nonlinearity is defined as deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 4: Channel leakage current is measured while the part is in sample mode.

Note 5: Guaranteed by design, not subject to test.

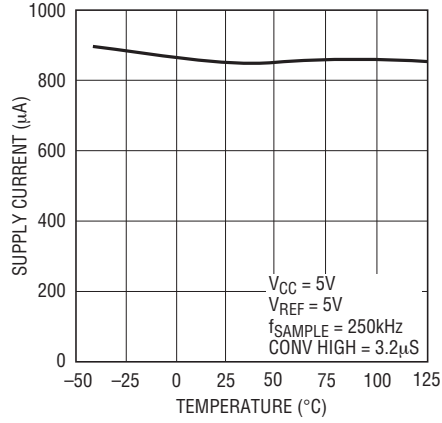
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Sampling Frequency



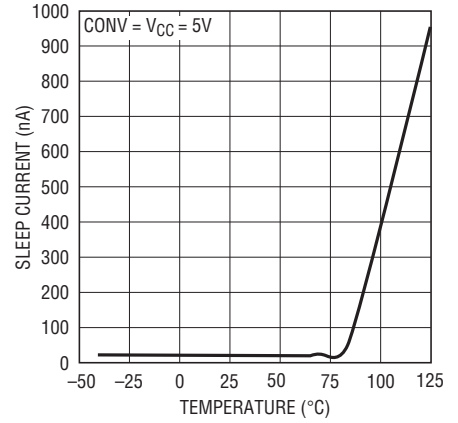
18645 G01

Supply Current vs Temperature



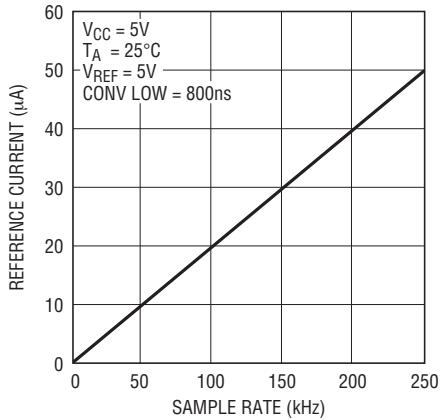
18645 G02

Sleep Current vs Temperature



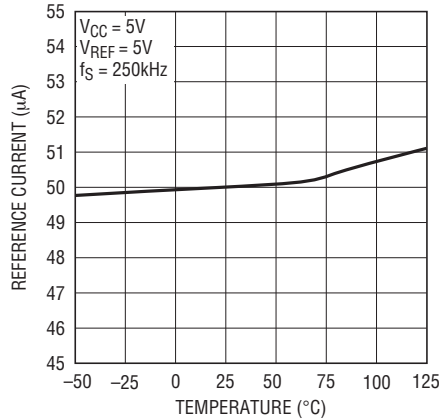
18645 G03

Reference Current vs Sampling Rate



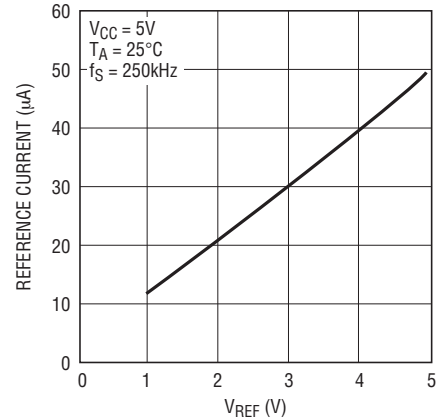
18645 G04

Reference Current vs Temperature



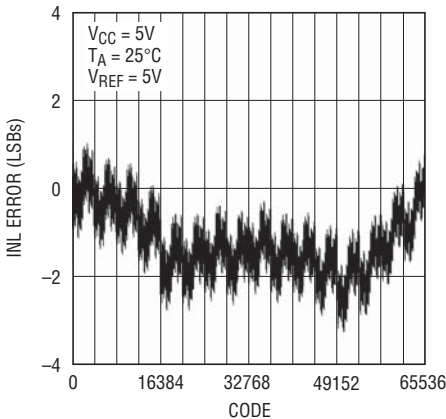
18645 G05

Reference Current vs Reference Voltage



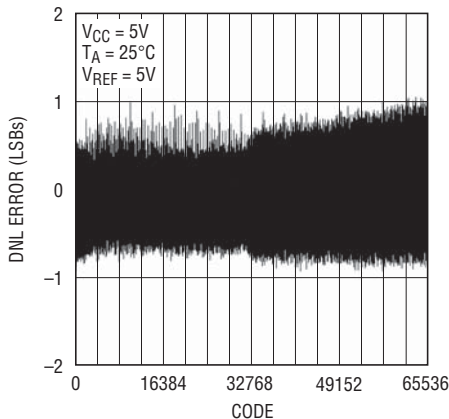
18645 G06

Typical INL Curve



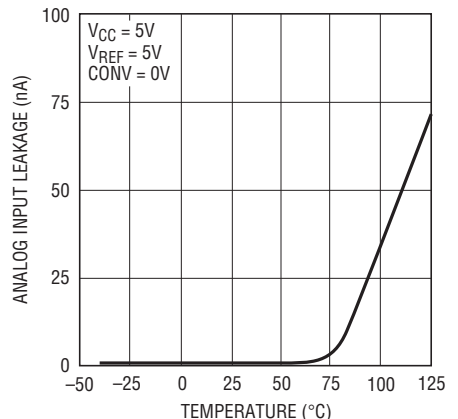
18645 G07

Typical DNL Curve



18645 G08

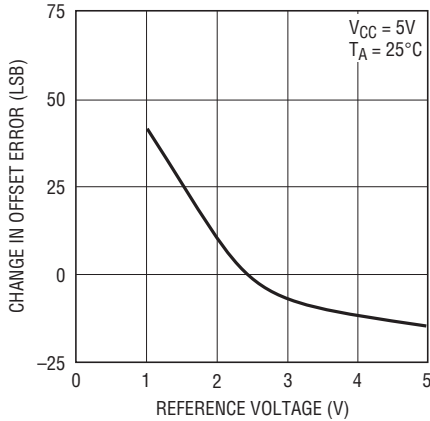
Analog Input Leakage Current vs Temperature



18645 G09

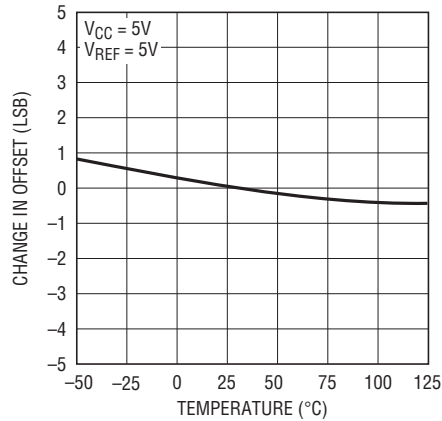
TYPICAL PERFORMANCE CHARACTERISTICS

Change in Offset Error vs Reference Voltage



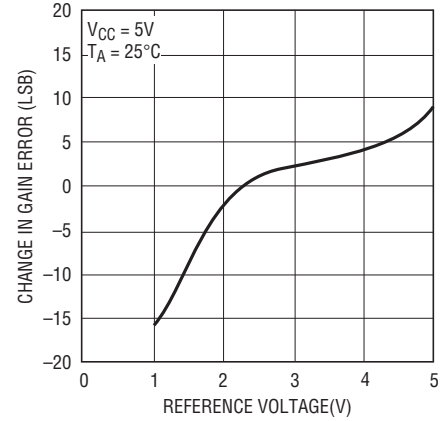
18645 G10

Change in Offset vs Temperature



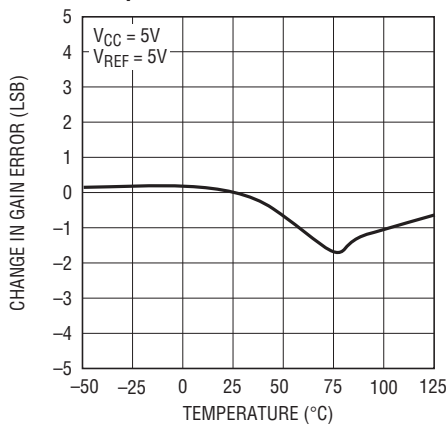
18645 G11

Change in Gain Error vs Reference Voltage



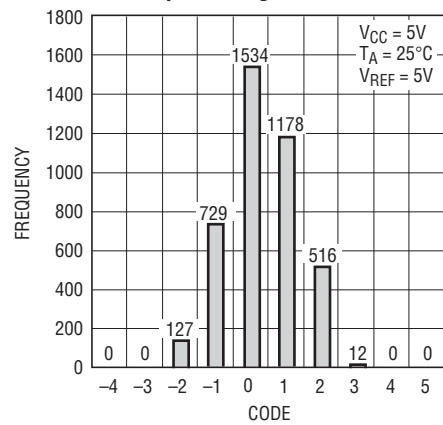
18645 G12

Change in Gain Error vs Temperature



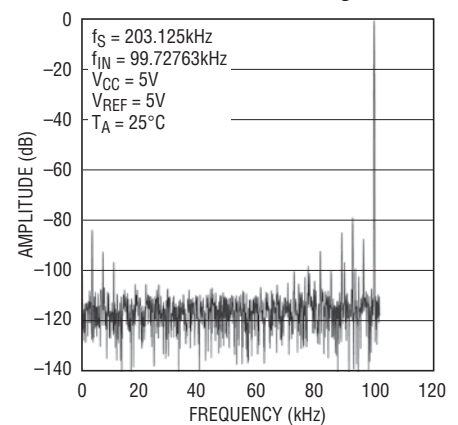
18645 G13

Histogram of 4096 Conversions of a DC Input Voltage



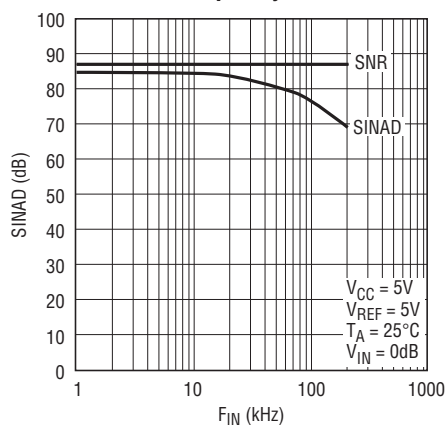
18645 G14

4096 Point FFT Nonaveraged



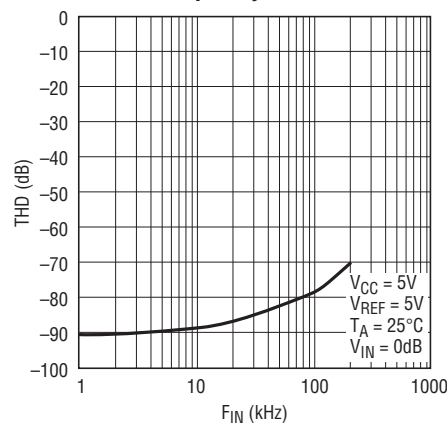
18645 G15

SINAD vs Frequency



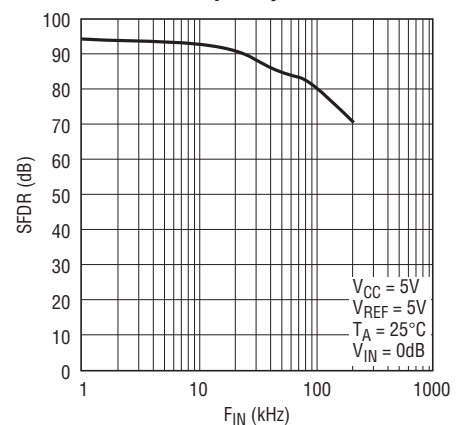
18645 G16

THD vs Frequency



18645 G17

SFDR vs Frequency



18645 G18

PIN FUNCTIONS

LTC1864

V_{REF} (Pin 1): Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to GND.

IN⁺, IN⁻ (Pins 2, 3): Analog Inputs. These inputs must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

CONV (Pin 5): Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part

powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

SDO (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this pin.

SCK (Pin 7): Shift Clock Input. This clock synchronizes the serial data transfer.

V_{CC} (Pin 8): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

LTC1865 (MSOP Package)

CONV (Pin 1): Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

CH0, CH1 (Pins 2, 3): Analog Inputs. These inputs must be free of noise with respect to AGND.

AGND (Pin 4): Analog Ground. AGND should be tied directly to an analog ground plane.

DGND (Pin 5): Digital Ground. DGND should be tied directly to an analog ground plane.

SDI (Pin 6): Digital Data Input. The A/D configuration word is shifted into this input.

SDO (Pin 7): Digital Data Output. The A/D conversion result is shifted out of this output.

SCK (Pin 8): Shift Clock Input. This clock synchronizes the serial data transfer.

V_{CC} (Pin 9): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

V_{REF} (Pin 10): Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to AGND.

LTC1865 (SO-8 Package)

CONV (Pin 1): Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

CH0, CH1 (Pins 2, 3): Analog Inputs. These inputs must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

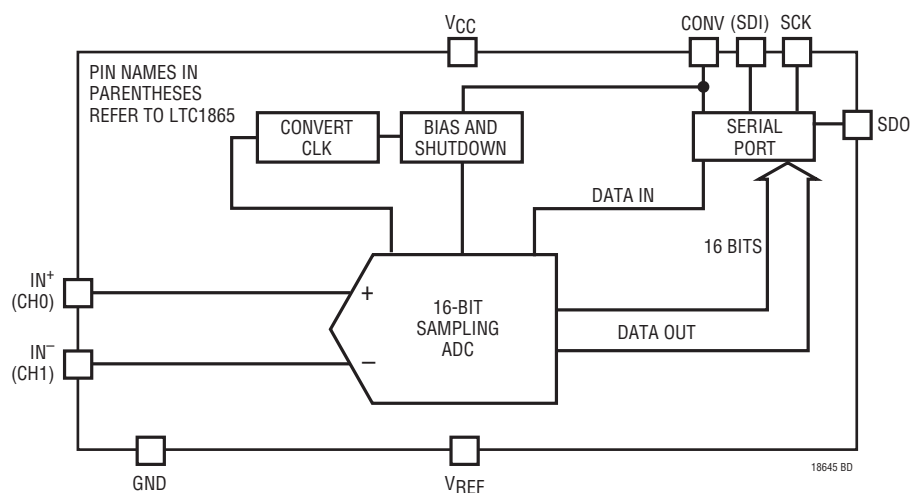
SDI (Pin 5): Digital Data Input. The A/D configuration word is shifted into this input.

SDO (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

SCK (Pin 7): Shift Clock Input. This clock synchronizes the serial data transfer.

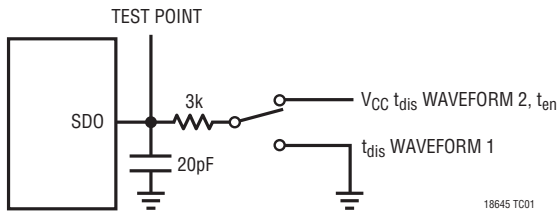
V_{CC} (Pin 8): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane. V_{REF} is tied internally to this pin.

FUNCTIONAL BLOCK DIAGRAM



TEST CIRCUITS

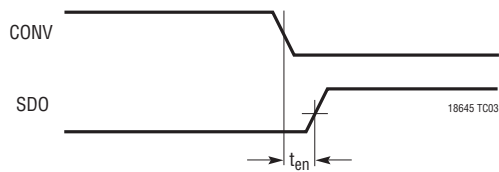
Load Circuit for t_{dDO} , t_r , t_f , t_{dis} and t_{en}



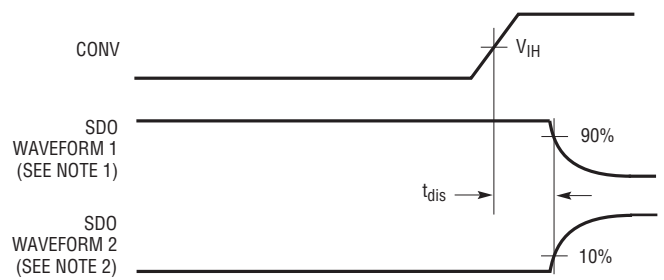
Voltage Waveforms for SDO Rise and Fall Times, t_r , t_f



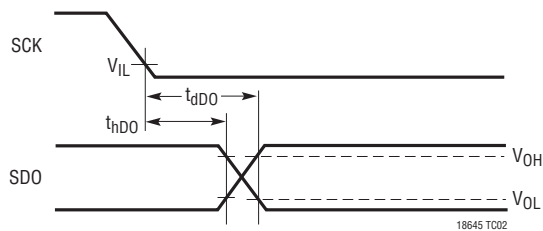
Voltage Waveforms for t_{en}



Voltage Waveforms for t_{dis}



Voltage Waveforms for SDO Delay Times, t_{dDO} and t_{hDO}



APPLICATIONS INFORMATION

LTC1864 OPERATION

Operating Sequence

The LTC1864 conversion cycle begins with the rising edge of CONV. After a period equal to t_{CONV} , the conversion is finished. If CONV is left high after this time, the LTC1864 goes into sleep mode drawing only leakage current. On the falling edge of CONV, the LTC1864 goes into sample mode and SDO is enabled. SCK synchronizes the data transfer with each bit being transmitted from SDO on the falling edge of SCK. The receiving system should capture the data from SDO on the rising edge of SCK. After completing the data transfer, if further SCK clocks are applied with CONV low, SDO will output zeros indefinitely. See Figure 1.

Analog Inputs

The LTC1864 has a unipolar differential analog input. The converter will measure the voltage between the “IN+” and “IN-” inputs. A zero code will occur when IN^+ minus IN^- equals zero. Full scale occurs when IN^+ minus IN^- equals V_{REF} minus 1LSB. See Figure 2. Both the “IN+” and “IN-” inputs are sampled at the same time, so common mode noise on the inputs is rejected by the ADC. If “IN-” is grounded and V_{REF} is tied to V_{CC} , a rail-to-rail input span will result on “IN+” as shown in Figure 3.

Reference Input

The voltage on the reference input of the LTC1864 defines the full-scale range of the A/D converter. The LTC1864 can operate with reference voltages from V_{CC} to 1V.

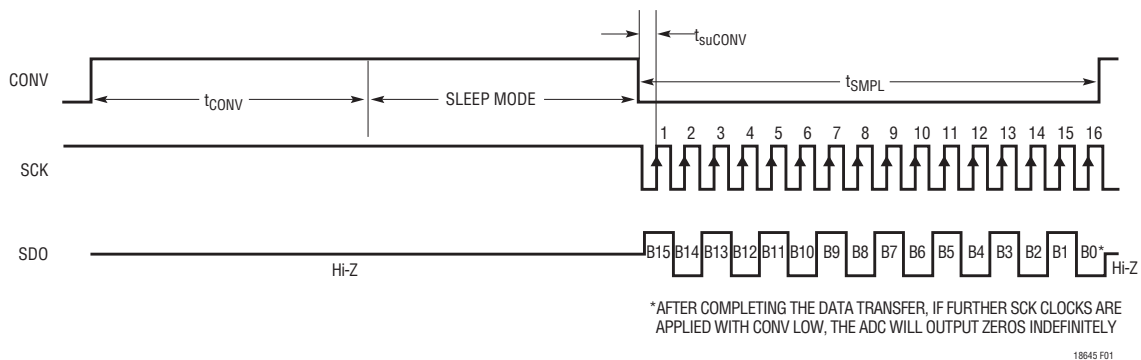


Figure 1. LTC1864 Operating Sequence

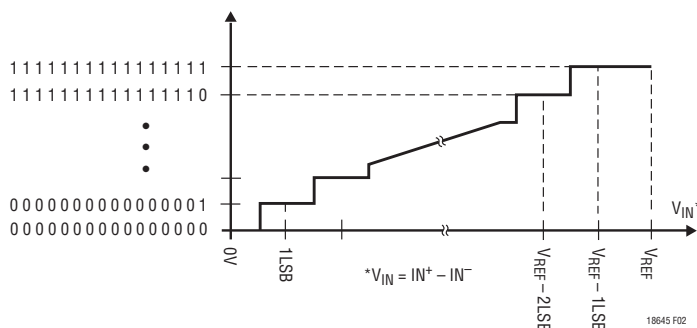


Figure 2. LTC1864 Transfer Curve

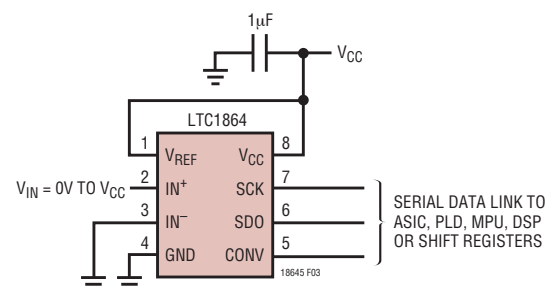


Figure 3. LTC1864 with Rail-to-Rail Input Span

APPLICATIONS INFORMATION

LTC1865 OPERATION

Operating Sequence

The LTC1865 conversion cycle begins with the rising edge of CONV. After a period equal to t_{CONV} , the conversion is finished. If CONV is left high after this time, the LTC1865 goes into sleep mode drawing only leakage current. The LTC1865's 2-bit data word is clocked into the SDI input on the rising edge of SCK after CONV goes low. Additional inputs on the SDI pin are then ignored until the next CONV cycle. The shift clock (SCK) synchronizes the data transfer with each bit being transmitted on the falling SCK edge and captured on the rising SCK edge in both transmitting and receiving systems. The data is transmitted and received simultaneously (full duplex). After completing the data transfer, if further SCK clocks are applied with CONV low, SDO will output zeros indefinitely. See Figure 4.

Analog Inputs

The two bits of the input word (SDI) assign the MUX configuration for the next requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the "+" and "-" signs in the selected row of the following table. In

single-ended mode, all input channels are measured with respect to GND. A zero code will occur when the "+" input minus the "-" input equals zero. Full scale occurs when the "+" input minus the "-" input equals V_{REF} minus 1LSB. See Figure 5. Both the "+" and "-" inputs are sampled at the same time so common mode noise is rejected. The input span in the SO-8 package is fixed at $V_{\text{REF}} = V_{\text{CC}}$. If the "-" input in differential mode is grounded, a rail-to-rail input span will result on the "+" input.

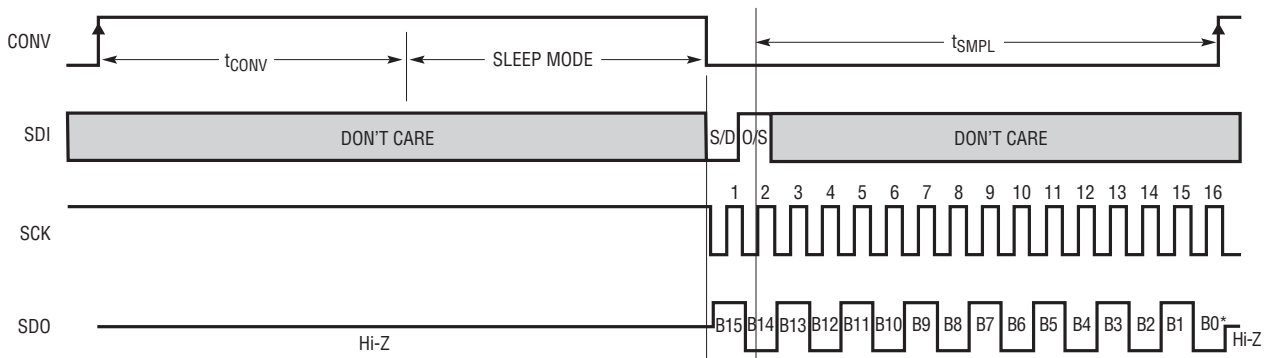
Reference Input

The reference input of the LTC1865 SO-8 package is internally tied to V_{CC} . The span of the A/D converter is therefore equal to V_{CC} . The voltage on the reference input of the LTC1865 MSOP package defines the span of the A/D converter. The LTC1865 MSOP package can operate with reference voltages from 1V to V_{CC} .

Table 1. Multiplexer Channel Selection

	MUX ADDRESS		CHANNEL #		GND
	SGL/DIFF	ODD/SIGN	0	1	
SINGLE-ENDED MUX MODE	1	0	+	—	—
	1	1		+	—
DIFFERENTIAL MUX MODE	0	0	+	—	—
	0	1	—	+	—

18645 TBL1



*AFTER COMPLETING THE DATA TRANSFER, IF FURTHER SCK CLOCKS ARE APPLIED WITH CONV LOW, THE ADC WILL OUTPUT ZEROS INDEFINITELY

Figure 4. LTC1865 Operating Sequence

18645 F04

APPLICATIONS INFORMATION

GENERAL ANALOG CONSIDERATIONS

Grounding

The LTC1864/LTC1865 should be used with an analog ground plane and single point grounding techniques. Do not use wire wrapping techniques to breadboard and evaluate the device. To achieve the optimum performance, use a printed circuit board. The ground pins (AGND and DGND for the LTC1865 MSOP package and GND for the LTC1864 and LTC1865 SO-8 package) should be tied directly to the analog ground plane with minimum lead length.

Bypassing

For good performance, the V_{CC} and V_{REF} pins must be free of noise and ripple. Any changes in the V_{CC}/V_{REF} voltage with respect to ground during the conversion cycle can

induce errors or noise in the output code. Bypass the V_{CC} and V_{REF} pins directly to the analog ground plane with a minimum of 1 μ F tantalum. Keep the bypass capacitor leads as short as possible.

Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1864/LTC1865 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem if source resistances are less than 200 Ω or high speed op amps are used (e.g., the LT[®]1211, LT1469, LT1807, LT1810, LT1630, LT1226 or LT1215). But if large source resistances are used, or if slow settling op amps drive the inputs, take care to ensure the transients caused by the current spikes settle completely before the conversion begins.

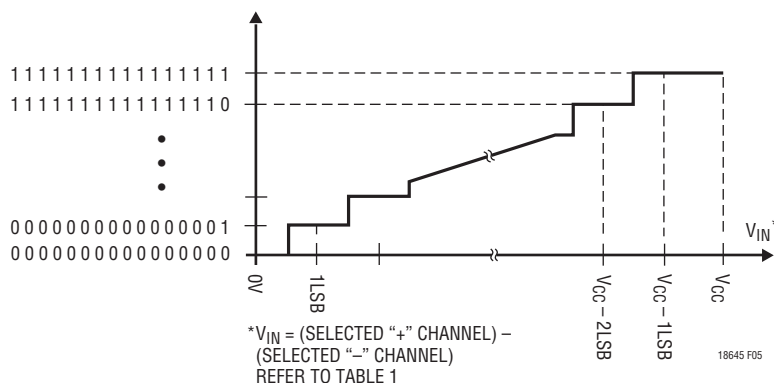


Figure 5. LTC1865 Transfer Curve

15V 5V_{LOG}

U1 LT1021-5

U2 OPT

U3 LTC1864CMTS8

U4 74HC595ADT

U5 74HC595ADT

U6 74HC163AD

U7 74HC163AD

U8 74AC14

U9 74AC00

U10 LC71799

U13A 74AC32

U13C 74AC32

U13D 74AC32

U13E 74AC32

U13F 74AC32

U13G 74AC32

U13H 74AC32

U13I 74AC32

U13J 74AC32

U13K 74AC32

U13L 74AC32

U13M 74AC32

U13N 74AC32

U13O 74AC32

U13P 74AC32

U13Q 74AC32

U13R 74AC32

U13S 74AC32

U13T 74AC32

U13U 74AC32

U13V 74AC32

U13W 74AC32

U13X 74AC32

U13Y 74AC32

U13Z 74AC32

U13AA 74AC32

U13AB 74AC32

U13AC 74AC32

U13AD 74AC32

U13AE 74AC32

U13AF 74AC32

U13AG 74AC32

U13AH 74AC32

U13AI 74AC32

U13AJ 74AC32

U13AK 74AC32

U13AL 74AC32

U13AM 74AC32

U13AN 74AC32

U13AO 74AC32

U13AP 74AC32

U13AQ 74AC32

U13AR 74AC32

U13AS 74AC32

U13AT 74AC32

U13AU 74AC32

U13AV 74AC32

U13AW 74AC32

U13AX 74AC32

U13AY 74AC32

U13AZ 74AC32

U13BA 74AC32

U13BB 74AC32

U13BC 74AC32

U13BD 74AC32

U13BE 74AC32

U13BF 74AC32

U13BG 74AC32

U13BH 74AC32

U13BI 74AC32

U13BJ 74AC32

U13BK 74AC32

U13BL 74AC32

U13BM 74AC32

U13BN 74AC32

U13BO 74AC32

U13BP 74AC32

U13BQ 74AC32

U13BR 74AC32

U13BS 74AC32

U13BT 74AC32

U13BU 74AC32

U13BV 74AC32

U13BW 74AC32

U13BX 74AC32

U13BY 74AC32

U13BZ 74AC32

U13CA 74AC32

U13CB 74AC32

U13CC 74AC32

U13CD 74AC32

U13CE 74AC32

U13CF 74AC32

U13CG 74AC32

U13CH 74AC32

U13CI 74AC32

U13CJ 74AC32

U13CK 74AC32

U13CL 74AC32

U13CM 74AC32

U13CN 74AC32

U13CO 74AC32

U13CP 74AC32

U13CQ 74AC32

U13CR 74AC32

U13CS 74AC32

U13CT 74AC32

U13CU 74AC32

U13CV 74AC32

U13CW 74AC32

U13CX 74AC32

U13CY 74AC32

U13CZ 74AC32

U13DA 74AC32

U13DB 74AC32

U13DC 74AC32

U13DD 74AC32

U13DE 74AC32

U13DF 74AC32

U13DG 74AC32

U13DH 74AC32

U13DI 74AC32

U13DJ 74AC32

U13DK 74AC32

U13DL 74AC32

U13DM 74AC32

U13DN 74AC32

U13DO 74AC32

U13DP 74AC32

U13DQ 74AC32

U13DR 74AC32

U13DS 74AC32

U13DT 74AC32

U13DU 74AC32

U13DV 74AC32

U13DW 74AC32

U13DX 74AC32

U13DY 74AC32

U13DZ 74AC32

U13EA 74AC32

U13EB 74AC32

U13EC 74AC32

U13ED 74AC32

U13EE 74AC32

U13EF 74AC32

U13EG 74AC32

U13EH 74AC32

U13EI 74AC32

U13EJ 74AC32

U13EK 74AC32

U13EL 74AC32

U13EM 74AC32

U13EN 74AC32

U13EO 74AC32

U13EP 74AC32

U13EQ 74AC32

U13ER 74AC32

U13ES 74AC32

U13ET 74AC32

U13EU 74AC32

U13EV 74AC32

U13EW 74AC32

U13EX 74AC32

U13EY 74AC32

U13EZ 74AC32

U13FA 74AC32

U13FB 74AC32

U13FC 74AC32

U13FD 74AC32

U13FE 74AC32

U13FF 74AC32

U13FG 74AC32

U13FH 74AC32

U13FI 74AC32

U13FJ 74AC32

U13FK 74AC32

U13FL 74AC32

U13FM 74AC32

U13FN 74AC32

U13FO 74AC32

U13FP 74AC32

U13FQ 74AC32

U13FR 74AC32

U13FS 74AC32

U13FT 74AC32

U13FU 74AC32

U13FV 74AC32

U13FW 74AC32

U13FX 74AC32

U13FY 74AC32

U13FZ 74AC32

U13GA 74AC32

U13GB 74AC32

U13GC 74AC32

U13GD 74AC32

U13GE 74AC32

U13GF 74AC32

U13GG 74AC32

U13GH 74AC32

U13GI 74AC32

U13GJ 74AC32

U13GK 74AC32

U13GL 74AC32

U13GM 74AC32

U13GN 74AC32

U13GO 74AC32

U13GP 74AC32

U13GQ 74AC32

U13GR 74AC32

U13GS 74AC32

U13GT 74AC32

U13GU 74AC32

U13GV 74AC32

U13GW 74AC32

U13GX 74AC32

U13GY 74AC32

U13GZ 74AC32

U13HA 74AC32

U13HB 74AC32

U13HC 74AC32

U13HD 74AC32

U13HE 74AC32

U13HF 74AC32

U13HG 74AC32

U13HH 74AC32

U13HI 74AC32

U13HJ 74AC32

U13HK 74AC32

U13HL 74AC32

U13HM 74AC32

U13HN 74AC32

U13HO 74AC32

U13HP 74AC32

U13HQ 74AC32

U13HR 74AC32

U13HS 74AC32

U13HT 74AC32

U13HU 74AC32

U13HV 74AC32

U13HW

NOTES: UNLESS OTHERWISE SPECIFIED
INSTALL SHUNTS ON JP1, JP3-JP7 PIN 1 AND PIN2;
ON JP8 AND JP9 PIN 2 AND PIN 4, PIN 3 AND PIN 5.



APPLICATIONS INFORMATION

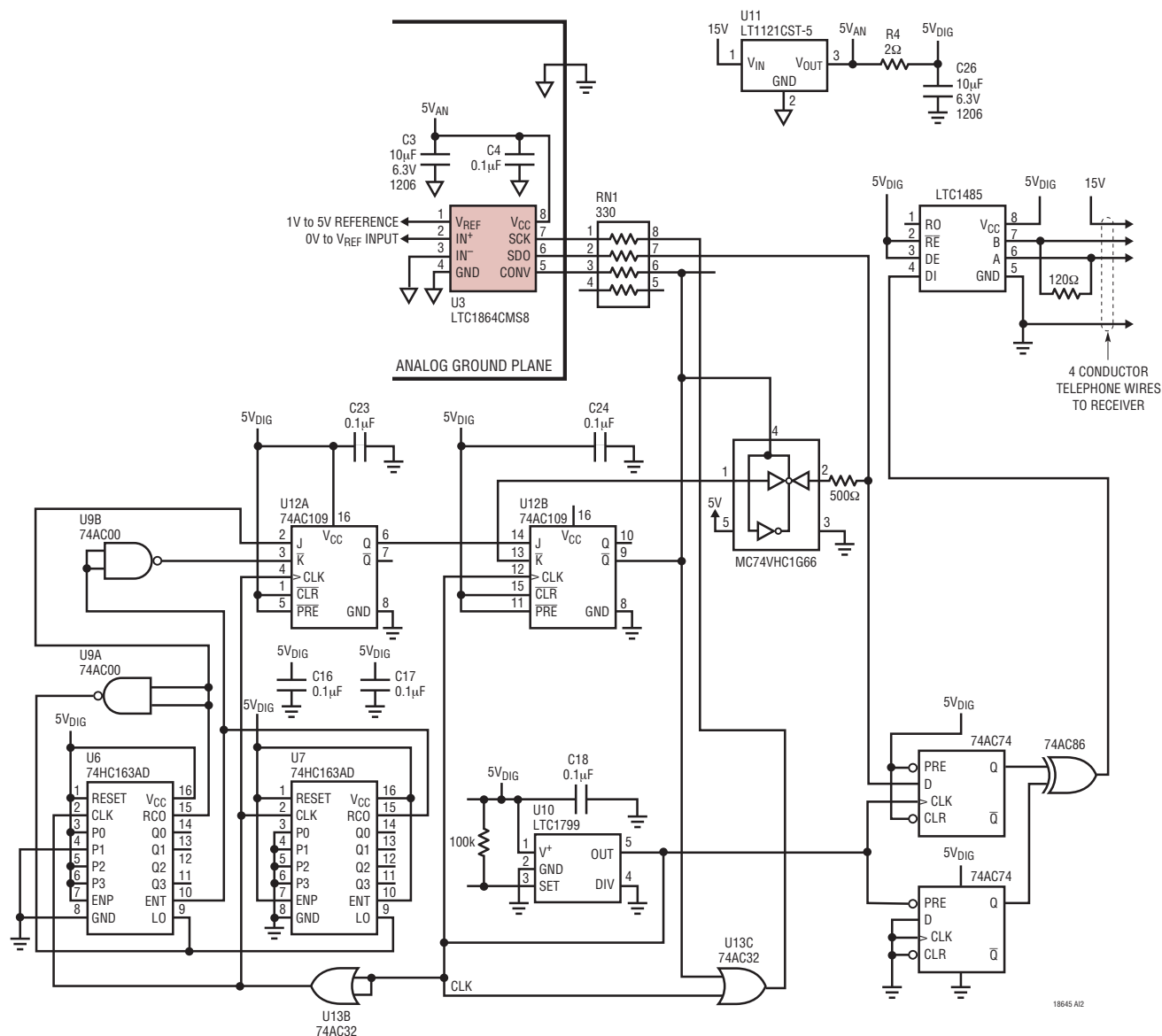


Figure 6. LTC1864 Manchester Transmitter

APPLICATIONS INFORMATION

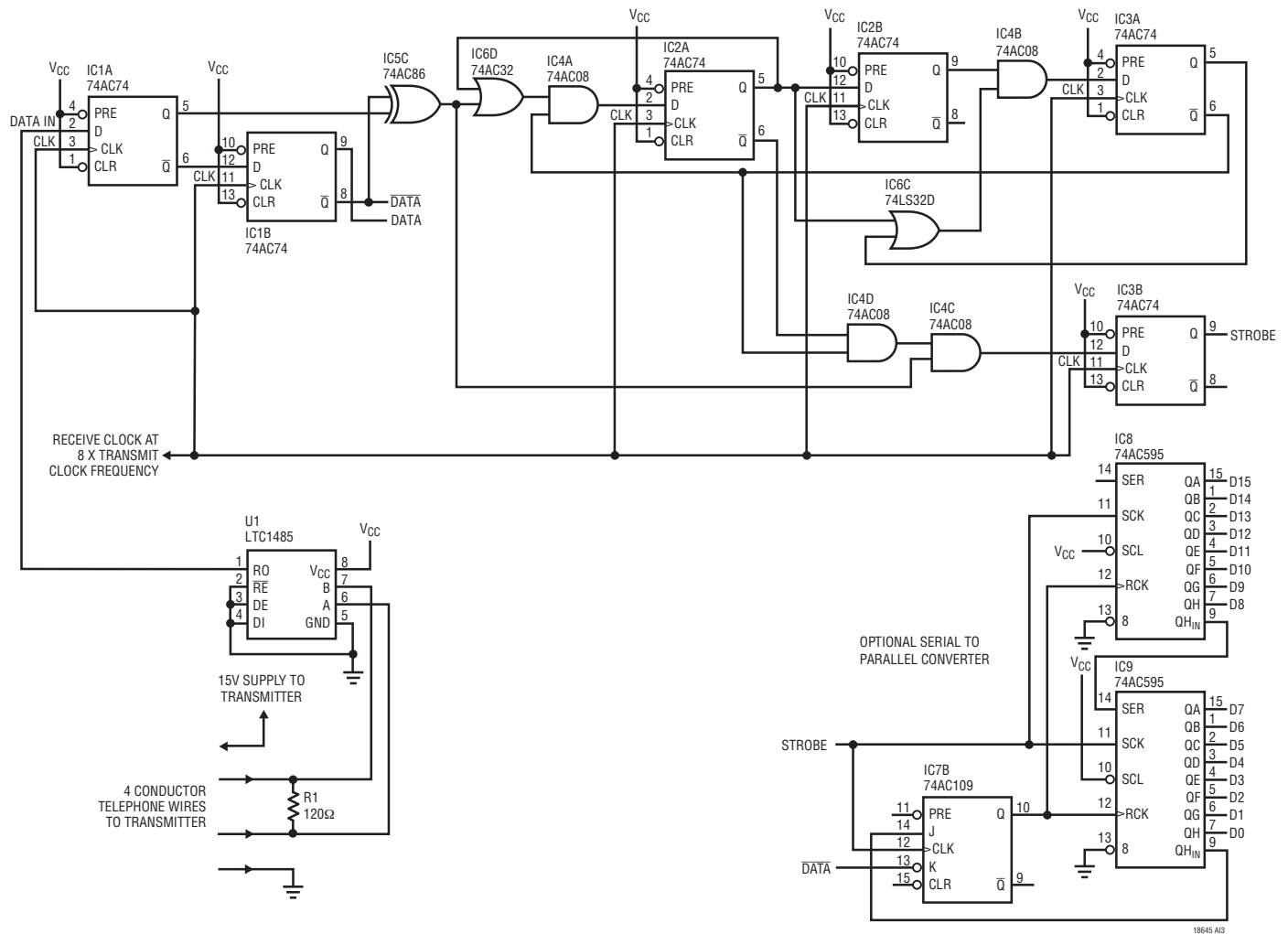


Figure 7. LTC1864 Manchester Receiver

APPLICATIONS INFORMATION

Transmit LTC1864 Data Over Modular Telephone Wire Using Simple Transmitter/Receiver

Figure 6 shows a simple Manchester encoder and differential transmitter suitable for use with the LTC1864. This circuit allows transmission of data over inexpensive telephone wire. This is useful for measuring a remote sensor, particularly when the cost of preserving the analog signal over a long distance is high.

Manchester encoding is a clock signal that is modulated by exclusive ORing with the data signal. The resulting signal contains both clock and data information and has an average duty cycle of 50%, that also allows transformer coupling. In practice, generating a Manchester encoded signal with an XOR gate will often produce glitches due to the skew between data and clock transitions. The D flip-flops in this encoder retime the clock and data such that the respective edges are closely aligned, effectively suppressing glitches. The retimed data and clock are then XORed to produce the Manchester encoded data, which is interfaced to telephone wire with an LTC1485 RS485 transceiver.

In order to synchronize to incoming data, the receiver needs a sequence to indicate the start of a data word. The transmitter schematic shows logic that will produce 31

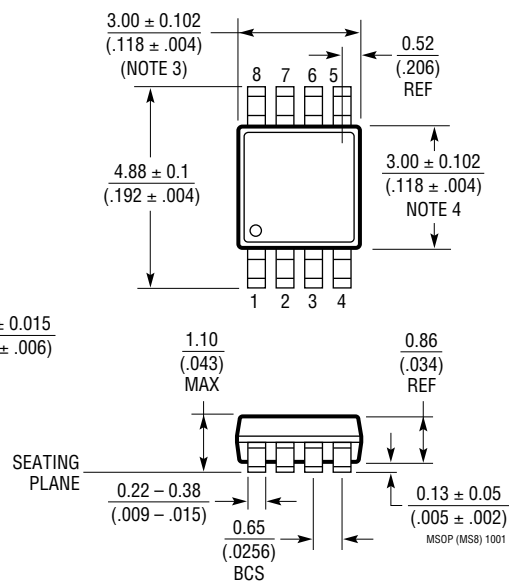
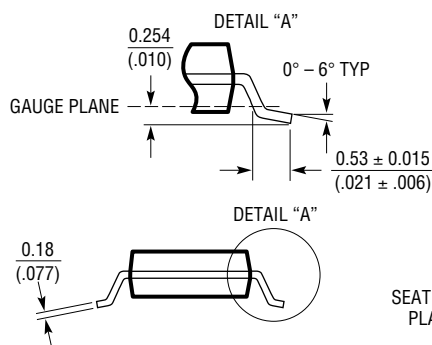
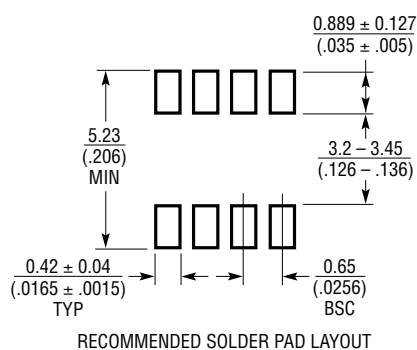
zeros, a start bit, followed by the 16 data bits (one sample every 48 clock cycles) at a clock frequency of 1MHz set by the LTC1799 oscillator. Sending at least 18 zeros before each start bit ensures that if synchronization is lost, the receiver can resynchronize to a start bit under all conditions. The serial to parallel converter shown in Figure 7 requires 18 zeros to avoid triggering on data bits.

The Manchester receiver shown in Figure 7 was adopted from Xilinx application note 17-30 and would typically be implemented in an FPGA. The decoder clock frequency is nominally 8 times the transmit clock frequency and is very tolerant of frequency errors. The outputs of the decoder are data and a strobe that indicates a valid data bit. The data can be deserialized using shift registers as shown. The start bit resets the J-K/flip-flop on its way into the first shift register. When it appears at the QH_{IN} output of the second shift register, it sets the flip-flop that loads the parallel data into the output register.

With AC family CMOS logic at 5V the receiver clock frequency is limited to 20MHz; the corresponding transmitter clock frequency is 2.5MHz. If the receiver is implemented in an FPGA that can be clocked at 160MHz, the LTC1864 can be clocked at its rated clock frequency of 20MHz.

PACKAGE DESCRIPTION

MS8 Package
8-Lead Plastic MSOP
 (Reference LTC DWG # 05-08-1660)

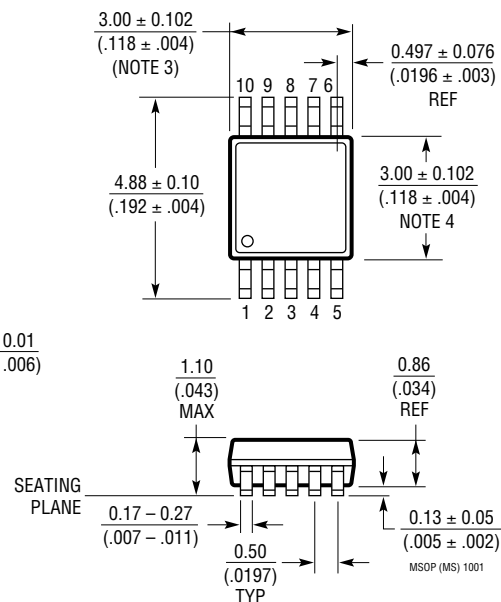
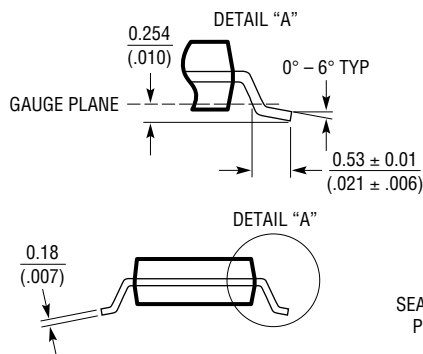
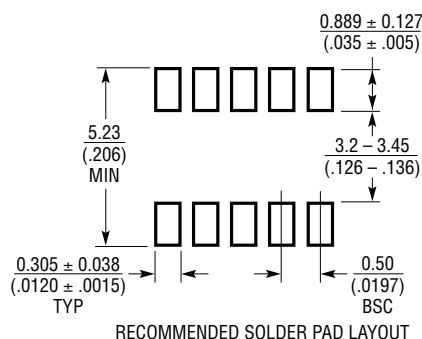


NOTE:

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

MS Package
10-Lead Plastic MSOP
 (Reference LTC DWG # 05-08-1661)

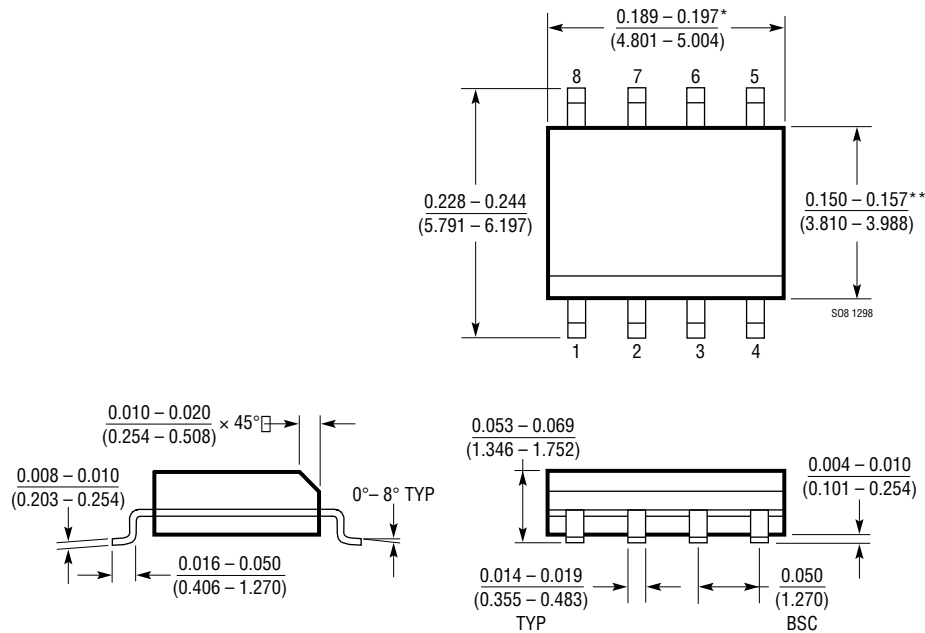


NOTE:

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm ($.006$) PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm ($.006$) PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm ($.004$) MAX

PACKAGE DESCRIPTION

S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



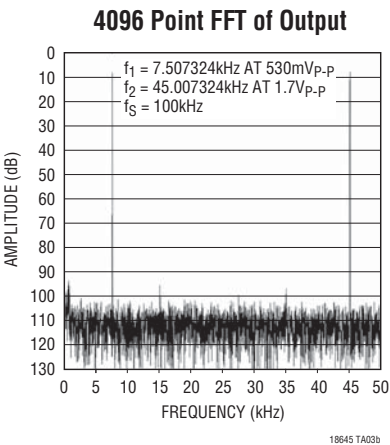
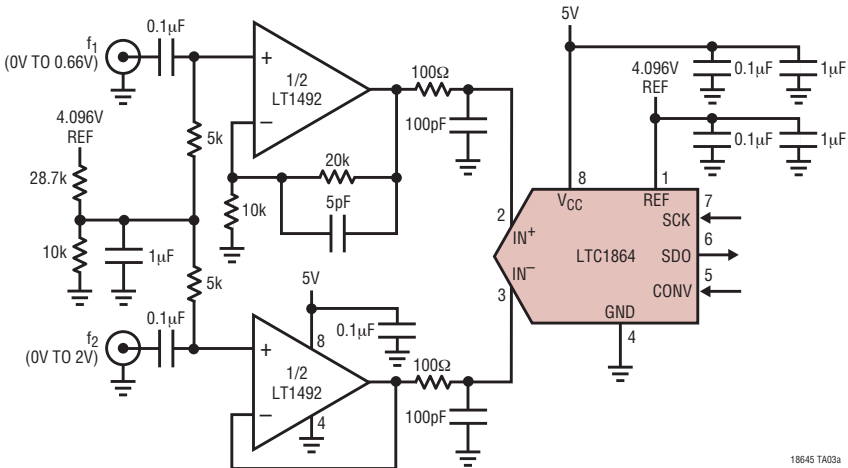
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

LTC1864/LTC1865

TYPICAL APPLICATION

Sample Two Channels Simultaneously with a Single Input ADC



RELATED PARTS

PART NUMBER	SAMPLE RATE	POWER DISSIPATION	DESCRIPTION
14-Bit Serial I/O ADCs			
LTC1417	400ksps	20mW	16-Pin SSOP, Unipolar or Bipolar, Reference, 5V or ±5V
LTC1418	200ksps	15mW	Serial/Parallel I/O, Internal Reference, 5V or ±5V
16-Bit Serial I/O ADCs			
LTC1609	200ksps	65mW	Configurable Bipolar or Unipolar Input Ranges, 5V
References			
LT1460	Micropower Precision Series Reference		Bandgap, 130µA Supply Current, 10ppm/°C, Available in SOT-23
LT1790	Micropower Low Dropout Reference		60µA Supply Current, 10ppm/°C, SOT-23
Op Amps			
LT1468/LT1469	Single/Dual 90MHz, 16-Bit Accurate Op Amps		22V/µs Slew Rate, 75µV/125µV Offset
LT1806/LT1807	Single/Dual 325MHz Low Noise Op Amps		140V/µs Slew Rate, 3.5nV/√Hz Noise, −80dBc Distortion
LT1809/LT1810	Single/Dual 180MHz Low Distortion Op Amps		350V/µs Slew Rate, −90dBc Distortion at 5MHz



**Стандарт
Электрон
Связь**

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург,
Промышленная ул, дом № 19, литера Н,
помещение 100-Н Офис 331