

**MAXIM**

# Lowest Power 3.0GHz ECL/PECL Differential Data and Clock D Flip-Flop

## General Description

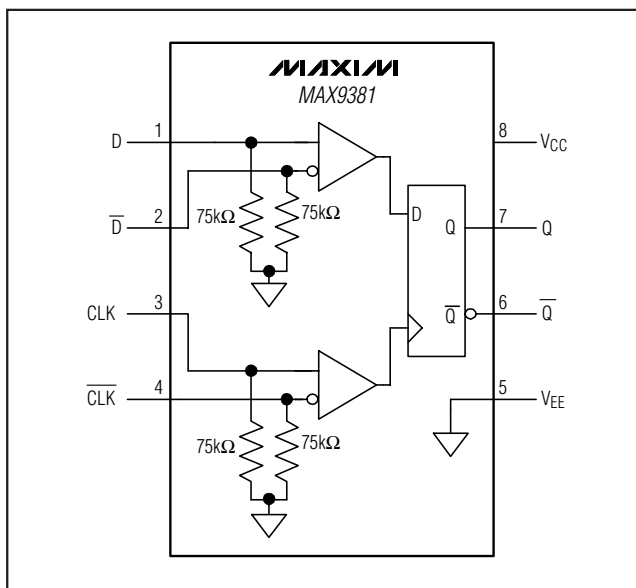
The MAX9381 differential data, differential clock D flip-flop is pin compatible with the ON Semiconductor MC100EP52, with the added benefit of a wider supply-voltage range from 2.25V to 5.5V and 25% lower supply current. Data enters the master part of the flip-flop when the clock is low and is transferred to the outputs upon a positive transition of the clock. Interchanging the clock inputs allows the part to be used as a negative edge-triggered device. The MAX9381 utilizes input clamping circuits that ensure the stability of the outputs when the inputs are left open or at  $V_{EE}$ .

The MAX9381 is offered in an 8-pin SO package and the smaller 8-pin  $\mu$ MAX package.

## Applications

Precision Clock and Data Distribution  
Central Office  
DSLAM  
DLC  
Base Station  
ATE

## Functional Diagram



## Features

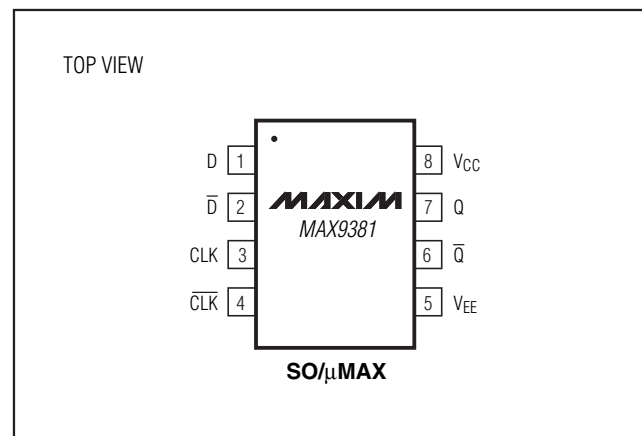
- ◆ 3.0GHz Guaranteed Operating Clock Frequency
- ◆ 0.2psRMS Added Random Jitter
- ◆ 328ps Typical Propagation Delay
- ◆ PECL Operation from  $V_{CC} = 2.25V$  to  $5.5V$  with  $V_{EE} = 0V$
- ◆ ECL Operation from  $V_{EE} = -2.25V$  to  $-5.5V$  with  $V_{CC} = 0V$
- ◆ Input Safety Clamps Ensure Output Stability when Inputs are Open or at  $V_{EE}$
- ◆  $\pm 2kV$  ESD Protection (Human Body Model)

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9381ESA	-40°C to +85°C	8 SO
MAX9381EUA*	-40°C to +85°C	8 $\mu$ MAX

\*Future product—contact factory for availability.

## Pin Configuration

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## ABSOLUTE MAXIMUM RATINGS

V <sub>CC</sub> - V <sub>EE</sub> .....	-0.3V to +6.0V
Input Voltage (D, $\bar{D}$ , CLK, $\bar{CLK}$ ) .....	(V <sub>EE</sub> - 0.3V) to (V <sub>CC</sub> + 0.3V)
Differential Input Voltage .....	Smaller of IV <sub>CC</sub> - V <sub>EEI</sub> or 3.0V
Output Current (Q, $\bar{Q}$ )	
Continuous .....	50mA
Surge .....	100mA
Junction-to-Ambient Thermal Resistance in Still Air	
8-Pin $\mu$ MAX .....	+221°C/W
8-Pin SO .....	+170°C/W
Maximum Continuous Power Dissipation	
8-Pin $\mu$ MAX (derate 4.5mW/°C above +70°C) .....	362mW
8-Pin SO (derate 5.9mW/°C above +70°C) .....	471mW

Junction-to-Ambient Thermal Resistance with 500LFPM Airflow	
8-Pin $\mu$ MAX .....	+155°C/W
8-Pin SO .....	+99°C/W
Junction-to-Case Thermal Resistance	
8-Pin $\mu$ MAX .....	+39°C/W
8-Pin SO .....	+40°C/W
Operating Temperature Range .....	-40°C to +85°C
Junction Temperature .....	+150°C
Storage Temperature Range .....	-65°C to +150°C
ESD Protection	
Human Body Model .....	±2kV
Soldering Temperature (10s) .....	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> - V<sub>EE</sub> = 2.25V to 5.5V (T<sub>A</sub> = +25°C to +85°C), V<sub>CC</sub> - V<sub>EE</sub> = 2.375V to 5.5V (T<sub>A</sub> = -40°C to +25°C), outputs terminated with 50 $\Omega$   $\pm$ 1% to V<sub>CC</sub> - 2.0V, unless otherwise noted. Typical values are at V<sub>CC</sub> - V<sub>EE</sub> = 3.3V, V<sub>IHD</sub> = V<sub>CC</sub> - 1.0V, V<sub>ILD</sub> = V<sub>CC</sub> - 1.5V, unless otherwise noted.) (Notes 1, 2, and 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
<b>INPUTS (D, <math>\bar{D}</math>, CLK, <math>\bar{CLK}</math>)</b>												
Differential Input High Voltage	V <sub>IHD</sub>	Figure 1	V <sub>EE</sub> + 1.2	V <sub>CC</sub>	V <sub>EE</sub> + 1.2	V <sub>CC</sub>	V <sub>EE</sub> + 1.2	V <sub>CC</sub>	V <sub>EE</sub> + 1.2	V <sub>CC</sub>	V	
Differential Input Low Voltage	V <sub>ILD</sub>	Figure 1	V <sub>EE</sub>	V <sub>CC</sub> - 0.15	V <sub>EE</sub>	V <sub>CC</sub> - 0.15	V <sub>EE</sub>	V <sub>CC</sub> - 0.15	V <sub>EE</sub>	V <sub>CC</sub> - 0.15	V	
Differential Input Voltage	V <sub>ID</sub>	Figure 1	V <sub>CC</sub> - V <sub>EE</sub> < 3.0V	V <sub>CC</sub> - V <sub>EE</sub>	0.15	V <sub>CC</sub> - V <sub>EE</sub>	0.15	V <sub>CC</sub> - V <sub>EE</sub>	0.15	V <sub>CC</sub> - V <sub>EE</sub>	V	
			V <sub>CC</sub> - V <sub>EE</sub> $\geq$ 3.0V	3.0	0.15	3.0	0.15	3.0	0.15	3.0	V	
Single-Ended Input Current	I <sub>IH</sub> , I <sub>IL</sub>	D, $\bar{D}$ , CLK, or $\bar{CLK}$ = V <sub>IHD</sub> or V <sub>ILD</sub>	-10	+200	-10	+200	-10	+200	-10	+200	$\mu$ A	
<b>OUTPUTS (Q, <math>\bar{Q}</math>)</b>												
Output High Voltage	V <sub>OH</sub>	Figure 1	V <sub>CC</sub> - 1.145	V <sub>CC</sub> - 0.895	V <sub>CC</sub> - 1.145	V <sub>CC</sub> - 0.895	V <sub>CC</sub> - 1.145	V <sub>CC</sub> - 0.895	V <sub>CC</sub> - 1.145	V <sub>CC</sub> - 0.895	V	
Output Low Voltage	V <sub>OL</sub>	Figure 1	V <sub>CC</sub> - 1.945	V <sub>CC</sub> - 1.695	V <sub>CC</sub> - 1.945	V <sub>CC</sub> - 1.695	V <sub>CC</sub> - 1.945	V <sub>CC</sub> - 1.695	V <sub>CC</sub> - 1.945	V <sub>CC</sub> - 1.695	V	
Differential Output Voltage	V <sub>OD</sub>	V <sub>OH</sub> - V <sub>OL</sub> , Figure 1	550		550		550		550		mV	
<b>POWER SUPPLY</b>												
Power-Supply Current (Note 4)	I <sub>EE</sub>		17	35	20	35	22	35	22	35	mA	

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## AC ELECTRICAL CHARACTERISTICS

( $V_{CC} - V_{EE} = 2.25V$  to  $5.5V$  ( $T_A = +25^{\circ}C$  to  $+85^{\circ}C$ ),  $V_{CC} - V_{EE} = 2.375V$  to  $5.5V$  ( $T_A = -40^{\circ}C$  to  $+25^{\circ}C$ ), outputs terminated with  $50\Omega \pm 1\%$  to  $V_{CC} - 2.0V$ ,  $f_{CLK} \leq 3.0GHz$ , input transition time =  $125ps$  (20% to 80%),  $V_{IHD} = V_{EE} + 1.2V$  to  $V_{CC}$ ,  $V_{ILD} = V_{EE}$  to  $V_{CC} - 0.15V$ ,  $V_{IHD} - V_{ILD} = 0.15V$  to smaller of  $|V_{CC} - V_{EE}|$  or  $3V$ , unless otherwise noted. Typical values are at  $V_{CC} - V_{EE} = 3.3V$ ,  $V_{IHD} = V_{CC} - 1.0V$ ,  $V_{ILD} = V_{CC} - 1.5V$ , unless otherwise noted.) (Notes 1, 5)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay CLK, $\overline{CLK}$ to Q, $\overline{Q}$	$t_{PHL}$ $t_{PLH}$	Figure 2			370		328	405			490	ps
Maximum Clock Frequency	$f_{CLKMAX}$	$V_{OD} \geq 300mV$	3.0			3.0			3.0			GHz
Setup Time	$t_S$	Figure 2	100			100			100			ps
Hold Time	$t_H$	Figure 2	50			50			50			ps
Added Random Jitter (Note 6)	$t_{RJ}$			0.2	0.8		0.2	0.8		0.2	0.8	ps (RMS)
Differential Output Rise/Fall Time	$t_{R}/t_{F}$	20% to 80%, Figure 2	70	120	170	80	120	180	90	120	200	ps

**Note 1:** Measurements are made with the device in thermal equilibrium.

**Note 2:** Current into a pin is defined as positive. Current out of a pin is defined as negative.

**Note 3:** DC parameters are production tested at  $+25^{\circ}C$ . DC limits are guaranteed by design and characterization over the full operating temperature range.

**Note 4:** All pins floating except  $V_{CC}$  and  $V_{EE}$ .

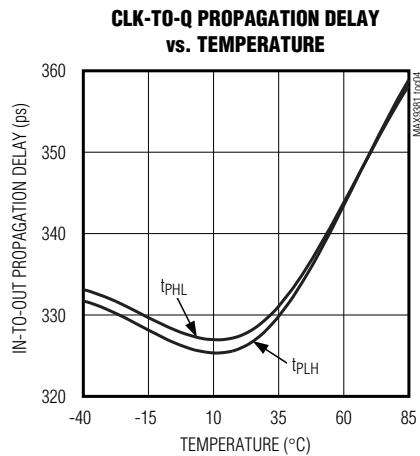
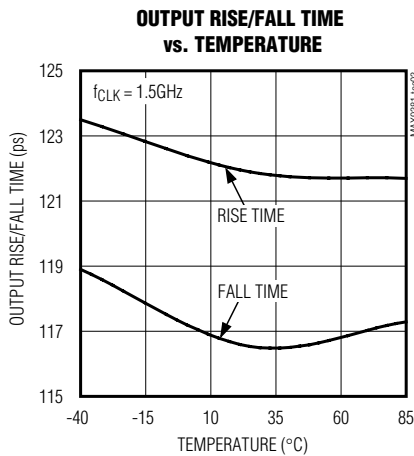
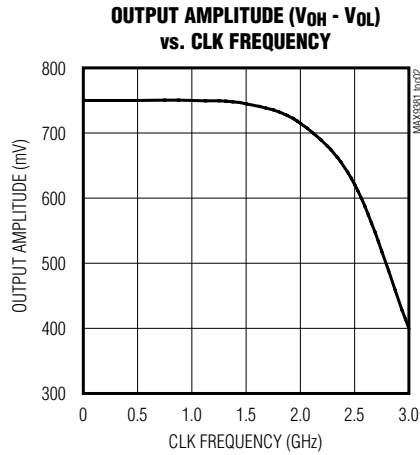
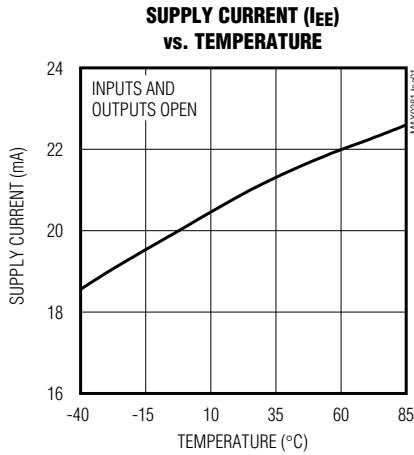
**Note 5:** Guaranteed by design and characterization, and are not production tested. Limits are set to  $\pm 6$  sigma.

**Note 6:** Device jitter added to the input clock.

# Lowest Power 3.0GHz ECL/PECL Differential Data and Clock D Flip-Flop

## Typical Operating Characteristics

( $V_{CC} - V_{EE} = 3.3V$ , outputs loaded with  $50\Omega \pm 1\%$  to  $V_{CC} - 2V$ ,  $V_{IH} = V_{CC} - 1V$ ,  $V_{IL} = V_{CC} - 1.5V$ ,  $f_{CLK} = 3GHz$ ,  $f_D = f_{CLK}/2$  input transition time = 125ps (20% to 80%), unless otherwise noted.)



# Lowest Power 3.0GHz ECL/PECL Differential Data and Clock D Flip-Flop

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## Pin Description

PIN	NAME	FUNCTION
1	D	Noninverting D Input to the Flip-Flop. Internally pulled down with a 75kΩ resistor to V <sub>EE</sub> .
2	$\overline{D}$	Inverting D Input to the Flip-Flop. Internally pulled down with a 75kΩ resistor to V <sub>EE</sub> .
3	CLK	Noninverting Clock Input to the Flip-Flop. Internally pulled down with a 75kΩ resistor to V <sub>EE</sub> .
4	$\overline{CLK}$	Inverting Clock Input to the Flip-Flop. Internally pulled down with a 75kΩ resistor to V <sub>EE</sub> .
5	V <sub>EE</sub>	Negative Supply
6	$\overline{Q}$	Inverting Q Output from the Flip-Flop. Terminate with a 50Ω resistor to V <sub>CC</sub> - 2V or equivalent.
7	Q	Noninverting Q Output from the Flip-Flop. Terminate with a 50Ω resistor to V <sub>CC</sub> - 2V or equivalent.
8	V <sub>CC</sub>	Positive Supply. Bypass from V <sub>CC</sub> to V <sub>EE</sub> with 0.1μF and 0.01μF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.

## Detailed Description

The MAX9381 D flip-flop transfers the logic level at the D input to the Q output on a rising edge transition of the clock, provided the minimum setup and hold times are met. By interchanging the CLK and  $\overline{CLK}$  inputs, the flip-flop functions as a falling-edge triggered flip-flop.

The input signals (D,  $\overline{D}$  and CLK,  $\overline{CLK}$ ) are differential and have a maximum differential input voltage of 3.0V or V<sub>CC</sub> - V<sub>EE</sub>, whichever is less. To ensure that the outputs remain stable when the inputs are left open, each of the inputs is driven low by a 75kΩ bias resistor connected to V<sub>EE</sub>. If the D and  $\overline{D}$  inputs are left open or at V<sub>EE</sub>, the output is guaranteed to be a differential low on the next low-to-high transition of the clock. If the CLK and  $\overline{CLK}$  inputs are left open or at V<sub>EE</sub>, the outputs remain unchanged (Table 1). Terminate the outputs (Q,  $\overline{Q}$ ) through 50Ω to V<sub>CC</sub> - 2V or an equivalent Thevenin termination (see the *Output Termination* section).

## ECL/PECL Operation

Output levels are referenced to V<sub>CC</sub> and are considered PECL or ECL, depending on the level of the V<sub>CC</sub>

Table 1. Truth Table\*

D, $\overline{D}$	CLK, $\overline{CLK}$	Q, $\overline{Q}$
L	↑	L
H	↑	H
Open or V <sub>EE</sub>	↑	L
X	Open or V <sub>EE</sub>	No change

\*Where logic states are differential, ↑ is a low-to-high transition and X signifies a don't care state.

supply. With V<sub>CC</sub> connected to a positive supply and V<sub>EE</sub> connected to GND, the outputs are PECL. The outputs are ECL when V<sub>CC</sub> is connected to GND and V<sub>EE</sub> is connected to a negative supply.

## Applications Information

### T Flip-Flop

The MAX9381 can be configured as a T flip-flop by connecting Q to  $\overline{D}$  and  $\overline{Q}$  to D. This configuration provides an output at half the frequency of the clock. The maximum operating frequency is determined by the sum of the setup time, the propagation delay of the

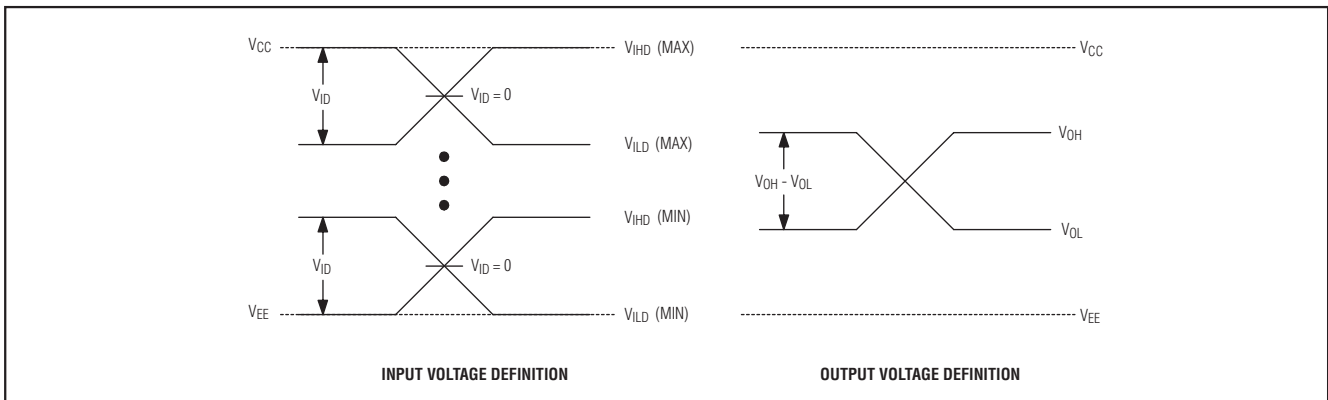


Figure 1. Input and Output Voltage Definitions

# Lowest Power 3.0GHz ECL/PECL Differential Data and Clock D Flip-Flop

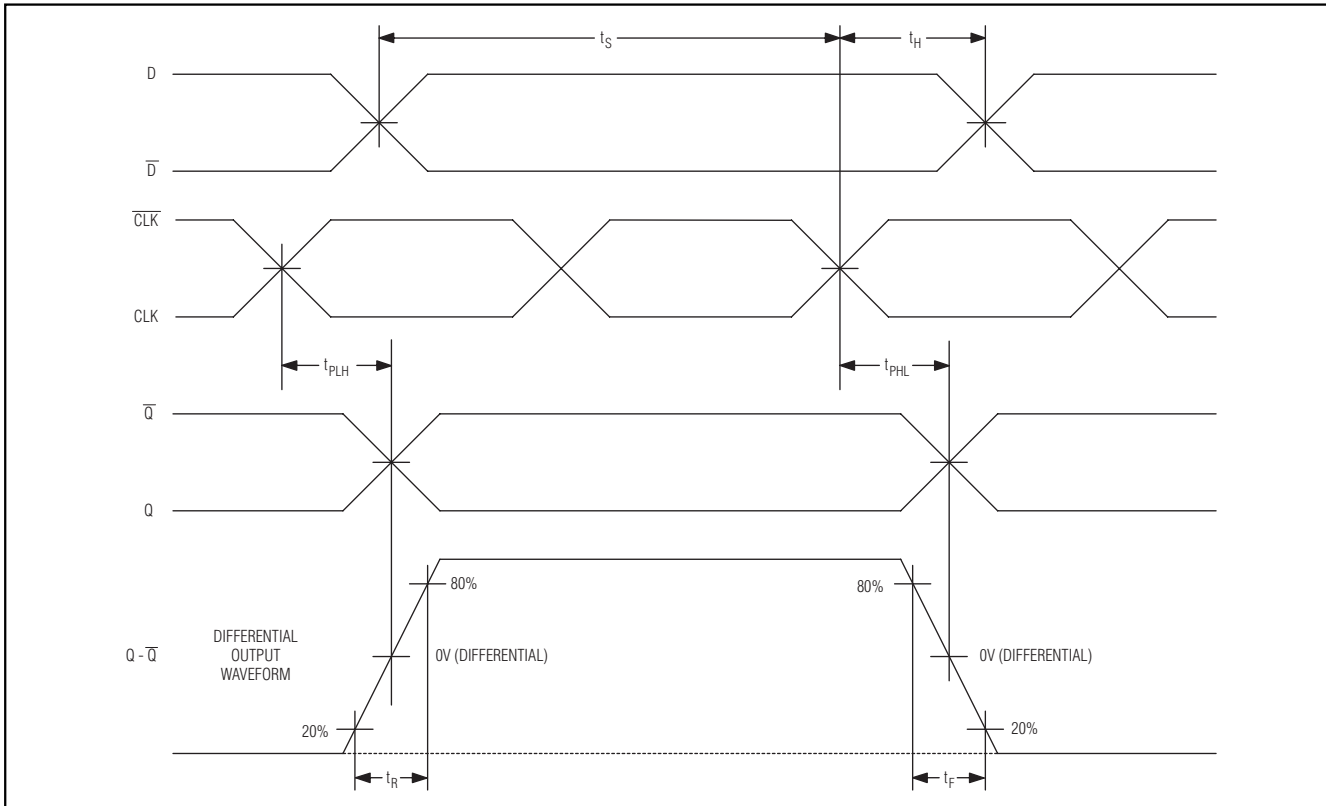


Figure 2. CLK-to-Q Propagation Delay and Transition Timing Diagram

device and any added delay by circuit board traces. The minimum supply voltage is 2.375V and is determined by input and output voltage range.

### Output Termination

Terminate the outputs through  $50\Omega$  to  $V_{CC} - 2V$  or use equivalent Thevenin terminations. Terminate each Q and  $\bar{Q}$  outputs with identical termination on each for the lowest output distortion. When a single-ended signal is taken from the differential output, terminate both Q and  $\bar{Q}$ .

Ensure that output currents do not exceed the current limits as specified in the *Absolute Maximum Ratings* table. Under all operating conditions, the device's total thermal limits should be observed.

### Power-Supply Bypassing

Bypass  $V_{CC}$  to  $V_{EE}$  with high-frequency surface-mount ceramic  $0.1\mu F$  and  $0.01\mu F$  capacitors. Place the capacitors as close to the device as possible with the  $0.01\mu F$  capacitor closest to the device pins.

Use multiple vias when connecting the bypass capacitors to ground. This reduces trace inductance, which lowers power-supply bounce when drawing high transient currents.

### Circuit Board Traces

Circuit board trace layout is very important to maintain the signal integrity of high-speed differential signals. Maintaining integrity is accomplished in part by reducing signal reflections and skew, and increasing common-mode noise immunity.

Signal reflections are caused by discontinuities in the  $50\Omega$  characteristic impedance of the traces. Avoid discontinuities by maintaining the distance between differential traces, not using sharp corners, or using vias. Maintaining distance between the traces also increases common-mode noise immunity. Reducing signal skew is accomplished by matching the electrical length of the differential traces.

### Chip Information

TRANSISTOR COUNT: 375

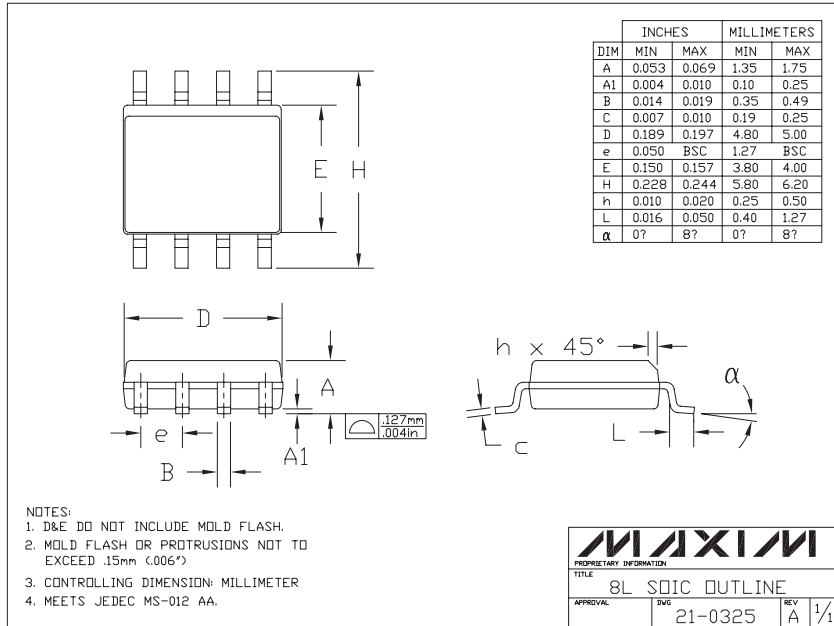
PROCESS: Bipolar

# Lowest Power 3.0GHz ECL/PECL Differential Data and Clock D Flip-Flop

## Package Information

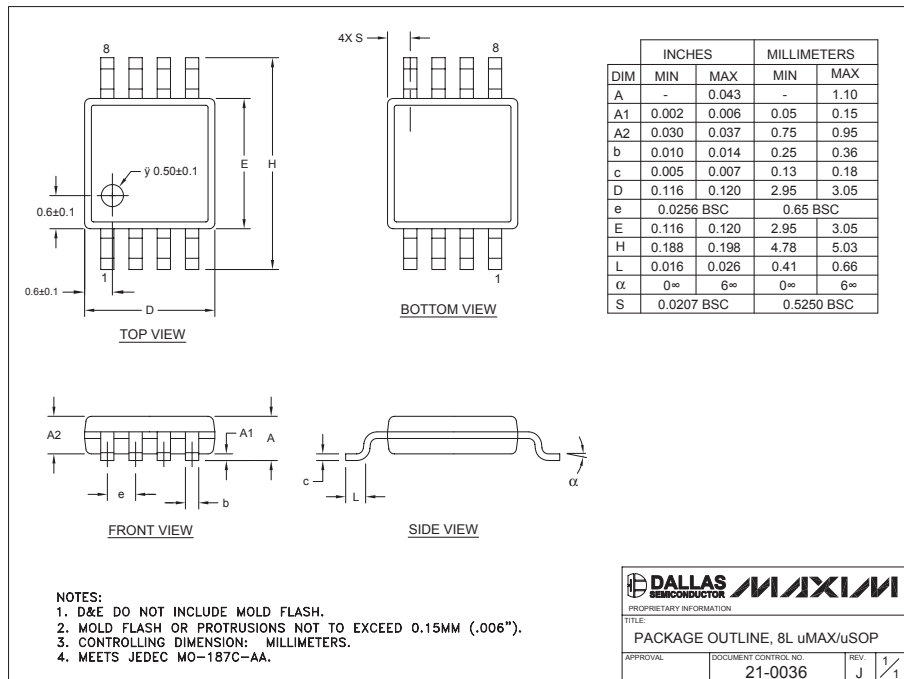
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

MAX9381



8LUCDF-3x3EFS

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 PROPRIETARY INFORMATION  
 TITLE: 8L SOIC OUTLINE  
 APPROVAL: [ ] DWG: 21-0325 REV: A 1/1



8LUMAXDFPS

**DALLAS SEMICONDUCTOR** **MAXIM**  
 PROPRIETARY INFORMATION  
 TITLE: PACKAGE OUTLINE, 8L uMAX/uSOP  
 APPROVAL: [ ] DOCUMENT CONTROL NO.: 21-0036 REV: J 1/1

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