

## Description

The DPS1113 is part of a family of power switches optimized for USB Power Delivery and other hot-swap applications. Through the analog interface, exception status is reported and several functions can be programmed: current limit, overvoltage protection (OVP), and output voltage ramping up. The device implements the fast role-swap function, which complies with the USB Power Delivery Specification Release 3.0, V1.0a requirement.

This device operates between 4.5V and 5.5V and offers fast short-circuit response time to ensure system robustness. The integrated port-discharge function allows the voltage levels at the input and output ports to be discharged to meet the requirements of the USB Power Delivery Specification. Comprehensive fault detection and recovery mechanisms are provisioned to enable applications, which are subjected to heavy capacitive loads and the risk of short circuit. These mechanisms include reverse voltage & current blocking, input OVP, output overcurrent, short-circuit protection and overtemperature shut-down. In addition, the rise time of output voltage can be adjusted to minimize in-rush current and to ensure system stability. Before any exception condition is notified via the low-active FAULTB signal, deglitch of 7ms is applied to prevent false triggering.

The DPS1113 is housed in the low-profile and space-saving V-QFN4040-17 package, which is manufactured with environmental-friendly material.

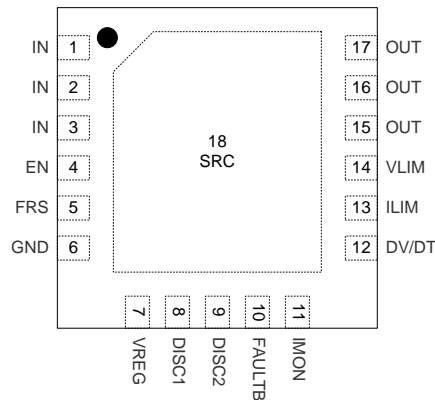
## Features

- Operating Voltage Range: 4.5V to 5.5V
- 1-Channel Power Switch with Integrated Adjustable Current & Voltage Limits
- Ability to Discharge the Input and Output Ports Either Individually or Simultaneously via the Two External Control Pins
- Fast Short-Circuit Response Time at 2 $\mu$ s
- Comprehensive Built-in Fault Detection and Recovery Mechanisms like Input Undervoltage Lock-out, Reverse Voltage & Current Blocking, Thermal Shut-down, Overcurrent and Short-Circuit Protection
- $R_{DS(ON)}$  of Embedded MOSFET at 30m $\Omega$
- Adjustable DV/DT Control at Start-up
- Fault Reporting (FAULTB) with Blanking Time at 7ms Typical
- Fast Role Swap Supported
- UL Recognized, File No. E322375
- IEC60950-1 CB Scheme Certified
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3),compliant.  
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.  
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds

## Pin Assignments

(Top View)

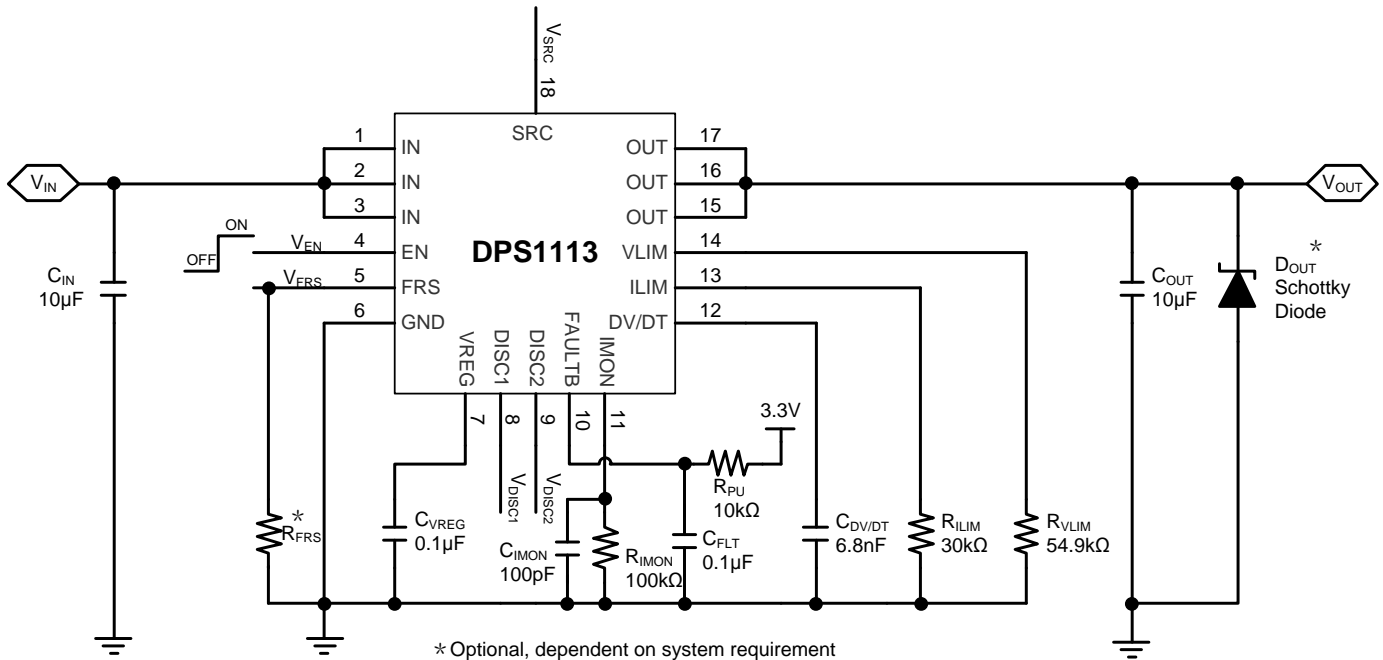


V-QFN4040-17

## Applications

- Notebook & Desktop & AIO PCs, Servers, and Tablets
- Docking Stations, Universal & Multimedia Hubs
- FPTVs, PC Monitors
- Set-Top-Boxes, Residential Gateways, Storage Devices

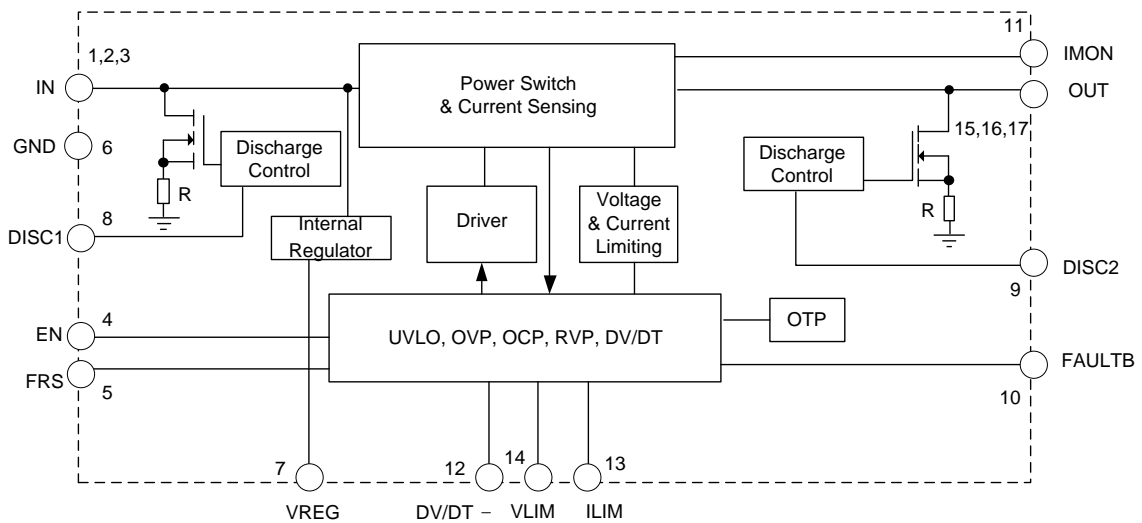
## Typical Application Circuit



## Pin Descriptions

Pin Number	Pin Name	Type	Function
1, 2, 3	IN	P	Power Supply and Input Port.
4	EN	I	Enable Input. Active high. '0' = Device OFF; '1' = Device ON. This pin must not be left floating.
5	FRS	I	Fast Role Swap Control. This pin enables the Fast Role Swap sequence defined in the USB Power Delivery Specification Release 3.0, V1.0a.
6	GND	GND	Device Ground.
7	VREG	I/O	Voltage Regulator. A 0.1µF is recommended between this pin and GND.
8	DISC1	I	IN Port Discharge Control. '1' = port voltage to be discharged; '0' = disabled.
9	DISC2	I	OUT Port Discharge Control. '1' = port voltage to be discharged; '0' = disabled.
10	FAULTB	O	Fault Status Indicator. An external pull-up resistor is required. This active-low pin must be tied to GND when not used.
11	IMON	O	Current Monitor. A 100pF capacitor and a resistor connected in parallel between this pin and GND creates a positive average voltage proportional to the current flowing through the device. This pin can be left floating if current monitoring is not required.
12	DV/DT	I/O	Ramp-up Control. A capacitor between this pin and GND sets the ramp-up rate.
13	ILIM	I/O	Current Limit Setting. A resistor between this pin and GND sets the overcurrent limit of the OUT port.
14	VLIM	I/O	Voltage Limit Setting. A resistor between this pin and GND sets the overvoltage limit of the IN port.
15, 16, 17	OUT	O	Output Port.
18 (Exposed Pad)	SRC	I/O	Common Source. The exposed pad of the V-QFN4040-17 package must not be connected to any signal.

**Functional Block Diagram**



**Absolute Maximum Ratings** (@  $T_A = +25^\circ\text{C}$ , unless otherwise specified) (Note 4)

Symbol	Parameter	Rating	Unit
$V_{IN}$	Voltage Range of Power IN Pin	-0.3 to 7	V
$V_{OUT}$	Voltage Range of OUT Pin	-0.3 to 30	V
$V_{EN}$	Voltage Range of EN Pin	-0.3 to 30	V
$V_{I/O}$	Voltage Range of Other Pins (FRS, VREG, DISC1, DISC2, FAULTB, IMON, DV/DT, ILIM, VLIM)	-0.3 to 6	V
$I_{OUT}$	Load Current Range	5	A
$T_J$	Operating Junction Temperature	-40 to +125	$^\circ\text{C}$
$T_L$	Lead Temperature	+260	$^\circ\text{C}$
$T_{ST}$	Storage Temperature	-65 to +150	$^\circ\text{C}$
ESD	Human Body Model (HBM), JESD22-A114	2	kV
	Charge Device Model (CDM)	1	

**Thermal Characteristics** (@  $T_A = +25^\circ\text{C}$ , unless otherwise specified) (Note 5)

Symbol	Parameter	Rating	Unit
$P_D$	Power Dissipation	1.7	W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	58.5	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	12.3	$^\circ\text{C}/\text{W}$

Notes: 4. These are stress ratings only. Operation outside the absolute maximum ratings can cause device failure. Operation at the absolute maximum rating for extended periods can reduce device reliability.  
5. Device mounted on FR-4 substrate PC board, 2oz copper, with 1" x 1" copper pad layout.

**Recommended Operating Conditions** (@  $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
$V_{IN}$	Input Supply Voltage	4.5	5.5	V
$V_{OUT}$	Output Voltage	0	24	V
$I_{OUT}$	Output Load Current	0	3.5	A
$C_{IN}$	Input Capacitance	10	—	$\mu\text{F}$
$C_{OUT}$	Output Capacitance	1	100	$\mu\text{F}$
$V_{EN}$	Input Voltage on EN Pin	0	5.5	V
$V_{FRS}, V_{DISC1}, V_{DISC2}$	Input Voltage on FRS, DISC1, DISC2 Pins	0	5.5	V
$R_{VLIM}$	VLIM Resistance	51	56	k $\Omega$
$R_{ILIM}$	ILIM Resistance	27	200	k $\Omega$

**Electrical Characteristics** (@  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 4.5\text{V}$  to  $5.5\text{V}$ ,  $C_{IN} = C_{OUT} = 10\mu\text{F}$ ,  $V_{EN} = 3.3\text{V}$ ,  $V_{FRS} = 0\text{V}$ ,  $C_{DV/DT} = 1\text{nF}$ ,  $R_{VLIM} = 54.9\text{k}\Omega$ ,  $R_{ILIM} = 27\text{k}\Omega$ , unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ.	Max	Unit
<b>Bias Supply</b>						
$V_{REG}$	Regulated Voltage	$V_{IN} = 5\text{V}$	—	4.9	—	V
$V_{UVLO}$	$V_{IN}$ Undervoltage Lock-out Threshold	$V_{IN}$ Rising	3.2	3.6	4.0	V
$V_{UVHY}$	$V_{IN}$ Undervoltage Lock-out Threshold Hysteresis	$V_{IN}$ Falling	—	250	—	mV
$I_{SHDN}$	Shut-down Current (Disabled)	$V_{IN} = 5\text{V}$ , $V_{EN} = 0\text{V}$	—	—	5	$\mu\text{A}$
$I_Q$	Quiescent Current (Enabled)	$V_{IN} = 5\text{V}$ , No Load	—	1.2	1.6	mA
<b>MOSFET</b>						
$R_{DS(ON)}$	Switch ON Resistance	$V_{IN} = 5\text{V}$	—	29	33	m $\Omega$
$I_{LKGSRC}$	OUT Leakage Current in OFF State, Sourcing	$V_{EN} = 0\text{V}$ , $V_{OUT} = 0\text{V}$	—	—	1	$\mu\text{A}$
$I_{LKGSNK}$	OUT Leakage Current in OFF State, Sinking	$V_{IN} = 3.3\text{V}$ , $V_{EN} = 0\text{V}$ , $V_{OUT} = 5\text{V}$	—	—	15	$\mu\text{A}$
<b>Enable Control</b>						
$V_{ENL}$	EN Threshold Voltage Low	$V_{EN}$ Falling	—	—	0.4	V
$V_{ENH}$	EN Threshold Voltage High	$V_{EN}$ Rising	1.4	—	—	
$I_{EN}$	EN Input Leakage Current	$V_{IN} = 5\text{V}$ , $V_{EN} = 5\text{V}$	—	—	5	$\mu\text{A}$
<b>Output Ramping Control</b>						
$I_{DV/DT}$	DV/DT Sourcing Current	$V_{DV/DT} = 0\text{V}$	—	1	—	$\mu\text{A}$
$G_{DV/DT}$	DV/DT to OUT Gain	$\Delta V_{OUT} / \Delta V_{DV/DT}$ , Guaranteed by Design	—	12	—	V/V

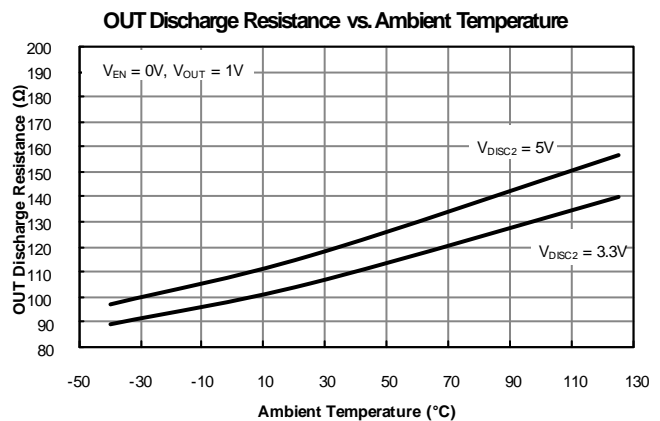
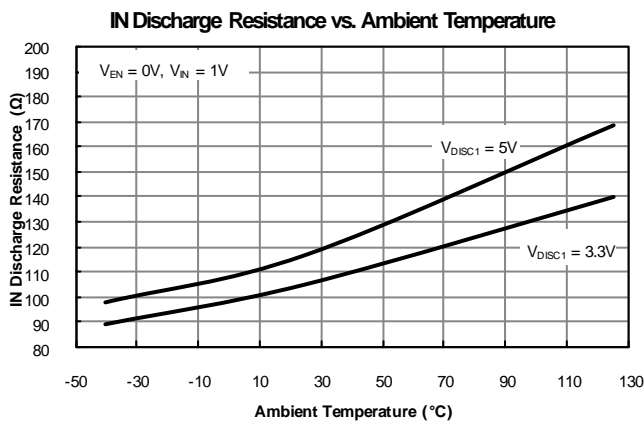
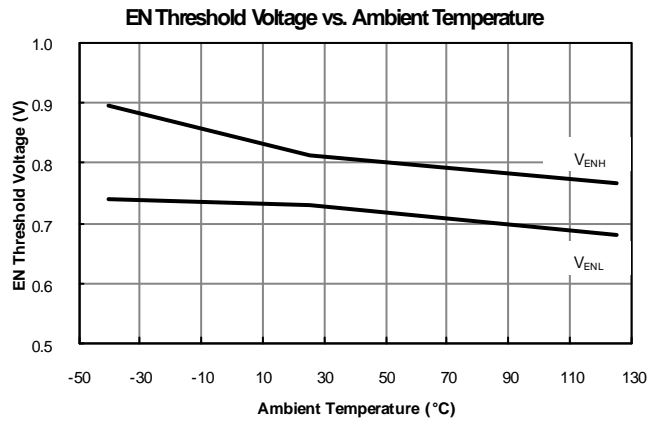
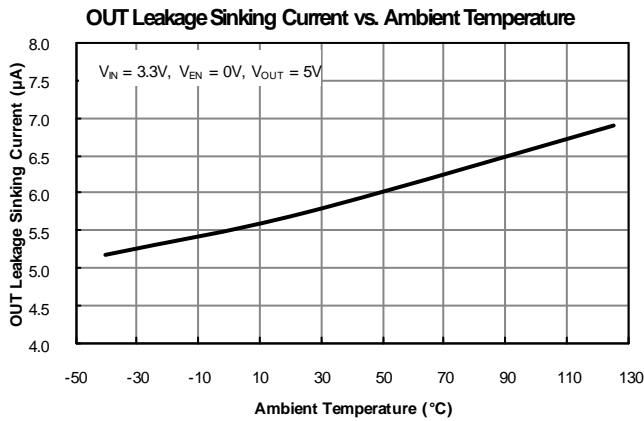
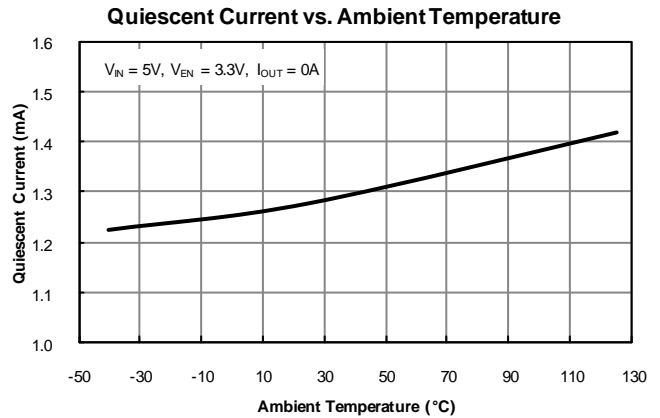
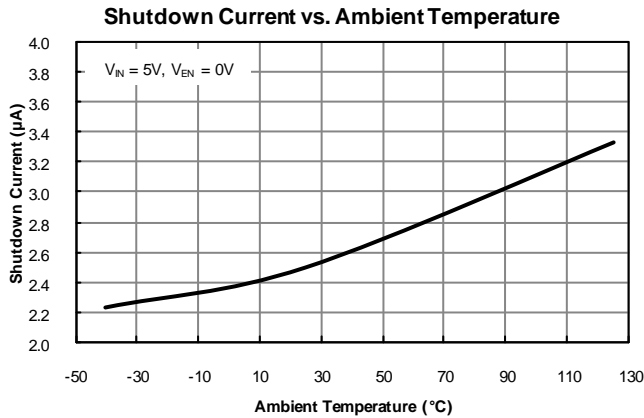
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Symbol	Parameter	Condition	Min	Typ.	Max	Unit
<b>Output Timing</b>						
$t_{DON}$	Output Turn-ON Delay Time	$V_{IN} = 5\text{V}$ , $C_{OUT} = 1\mu\text{F}$ , $V_{EN} = 0\text{V}$ to $3.3\text{V}$	—	0.2	—	ms
$t_R$	Output Turn-ON Rise Time	$V_{IN} = 5\text{V}$ , $C_{OUT} = 1\mu\text{F}$ , $V_{EN} = 0\text{V}$ to $3.3\text{V}$	—	0.3	—	ms
$t_{DOFF}$	Output Turn-OFF Delay Time	$V_{IN} = 5\text{V}$ , $C_{OUT} = 1\mu\text{F}$ , $V_{EN} = 3.3\text{V}$ to $0\text{V}$	—	1	—	$\mu\text{s}$
$t_F$	Output Turn-OFF Fall Time	$V_{IN} = 5\text{V}$ , $C_{OUT} = 1\mu\text{F}$ , $V_{EN} = 3.3\text{V}$ to $0\text{V}$	—	10	—	$\mu\text{s}$
<b>Fast Role Swap (FRS) Control and Timing</b>						
$V_{FRSL}$	FRS Threshold Voltage Low	$V_{FRS}$ Falling	—	—	0.4	V
$V_{FRSH}$	FRS Threshold Voltage High	$V_{FRS}$ Rising	1.4	—	—	V
$I_{FRS}$	FRS Input Leakage Current	$V_{IN} = 5\text{V}$ , $V_{FRS} = 5\text{V}$	—	—	7	$\mu\text{A}$
$t_{FRS\_ON}$	FRS ON Time	$V_{IN} = 5\text{V}$ , a Single Positive Pulse Width on FRS and $V_{FRSH} = 3.3\text{V}$ , Guaranteed by Design	600	—	—	$\mu\text{s}$
$t_{DON\_FRS}$	Output Turn-ON Delay Time with FRS	$V_{IN} = 5\text{V}$ , $C_{OUT} = 1\mu\text{F}$ , $V_{FRS} = 3.3\text{V}$ to $0\text{V}$ , 50% Falling Edge of $V_{FRS}$ to 90% Rising Edge of $V_{OUT}$ , Guaranteed by Design	—	—	60	$\mu\text{s}$
<b>Discharge Control on IN and OUT Ports</b>						
$R_{DISC1} / R_{DISC2}$	IN / OUT Discharge Resistance	$V_{DISC1} = 5\text{V}$ , $V_{DISC2} = 5\text{V}$	—	105	—	$\Omega$
		$V_{DISC1} = 3.3\text{V}$ , $V_{DISC2} = 3.3\text{V}$	—	115	—	$\Omega$
$V_{DISC1L} / V_{DISC2L}$	DISC1 / DISC2 Threshold Voltage Low	$V_{DISC1} / V_{DISC2}$ Falling	—	—	0.4	V
$V_{DISC1H} / V_{DISC2H}$	DISC1 / DISC2 Threshold Voltage High	$V_{DISC1} / V_{DISC2}$ Rising	1.4	—	—	V
<b>Overcurrent Protection (OCP)</b>						
$V_{ILIM}$	ILIM Bias Voltage	$R_{ILIM} = 50\text{k}\Omega$	—	1	—	V
$I_{LIM}$	Current Limit, 1A	$R_{ILIM} = 100\text{k}\Omega$	0.9	1.05	1.2	A
	Current Limit, 2A	$R_{ILIM} = 50\text{k}\Omega$	1.8	2	2.2	
	Current Limit, 3A	$R_{ILIM} = 33.3\text{k}\Omega$	2.76	3	3.24	
$I_{FASTRIP}$	Fast-Trip Threshold	Guaranteed by Design	—	$1.125 \times I_{LIM} + 1.8$	—	A
<b>Current Monitoring Output</b>						
$V_{IMON}$	Current Monitoring Output Voltage	—	—	—	4.5	V
$G_{IMON}$	IMON to OUT Current Gain	$I_{IMON} / I_{OUT}$	—	10	—	$\mu\text{A}/\text{A}$
<b>OVP</b>						
$I_{VLIM}$	VLIM Sourcing Current	$V_{IN} = 5\text{V}$ , $R_{V_{LIM}} = 54.9\text{k}\Omega$	—	10	—	$\mu\text{A}$
$V_{OVPRTH}$	Input Overvoltage Threshold, Rising	$R_{V_{LIM}} = 54.9\text{k}\Omega$ , $V_{IN}$ Rising	—	6	—	V
$V_{OVPFTH}$	Input Overvoltage Threshold, Falling	$R_{V_{LIM}} = 54.9\text{k}\Omega$ , $V_{IN}$ Falling	—	5.5	—	

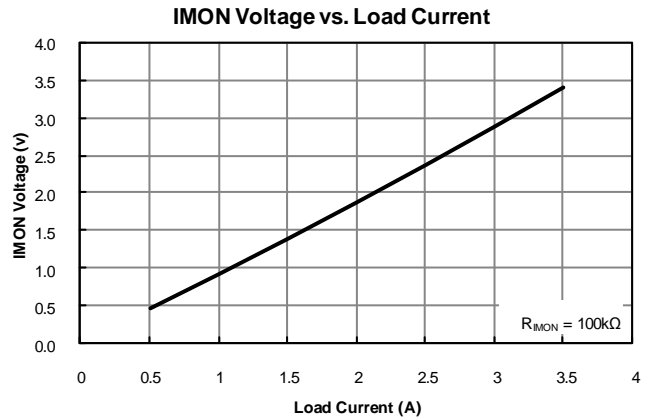
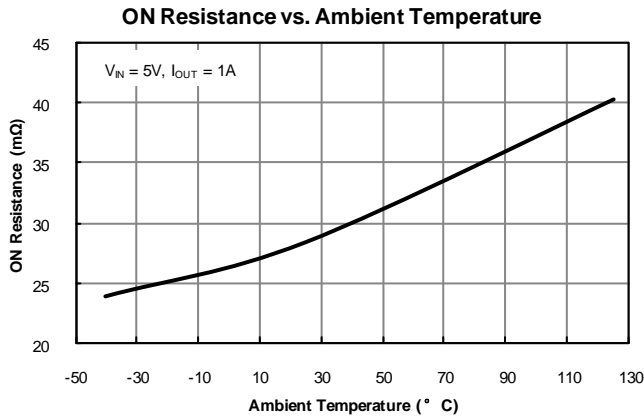
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Symbol	Parameter	Condition	Min	Typ.	Max	Unit
<b>Reverse-voltage Protection (RVP)</b>						
$V_{RVPFTH}$	$V_{IN} - V_{OUT}$ Threshold Entering into Reverse Protection	$V_{IN} - V_{OUT}$ Falling	—	-30	—	mV
$V_{RVPRTH}$	$V_{IN} - V_{OUT}$ Threshold Exiting from Reverse Protection	$V_{IN} - V_{OUT}$ Rising	—	0	—	
$t_{RVPTD}$	Reverse Protection Response Time	—	—	2	—	$\mu\text{s}$
<b>Fault Flag (FAULTB): Active-Low</b>						
$R_{FAULTB}$	FAULTB Pull-down Resistor	$V_{IN} = 7\text{V}$ , $R_{VLIM} = 54.9\text{k}\Omega$ , $I_{FAULTB} = 10\text{mA}$ Sinking	—	25	—	$\Omega$
$I_{LKGFAULTB}$	FAULTB Leakage Current	$V_{IN} = 5\text{V}$ , $R_{VLIM} = 54.9\text{k}\Omega$ , $V_{FAULTB} = 5\text{V}$	—	—	1	$\mu\text{A}$
$t_{BLANKFAULTB}$	FAULTB Blanking Time	$V_{IN} = 5\text{V}$ , $R_{VLIM} = 54.9\text{k}\Omega$ , $V_{FAULTB} = 5\text{V}$	—	7	—	ms
<b>Thermal Shut-Down</b>						
$T_{SHDN}$	Thermal Shut-down Threshold	—	—	+155	—	$^\circ\text{C}$
$T_{HYS}$	Thermal Shut-down Hysteresis	—	—	+20	—	

**Performance Characteristics** (@  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $C_{IN} = C_{OUT} = 10\mu\text{F}$ ,  $V_{EN} = 3.3\text{V}$ ,  $V_{FRS} = 0\text{V}$ ,  $C_{DV/DT} = 1\text{nF}$ ,  $R_{LIM} = 54.9\text{k}\Omega$ ,  $R_{LIM} = 27\text{k}\Omega$ , unless otherwise specified.)

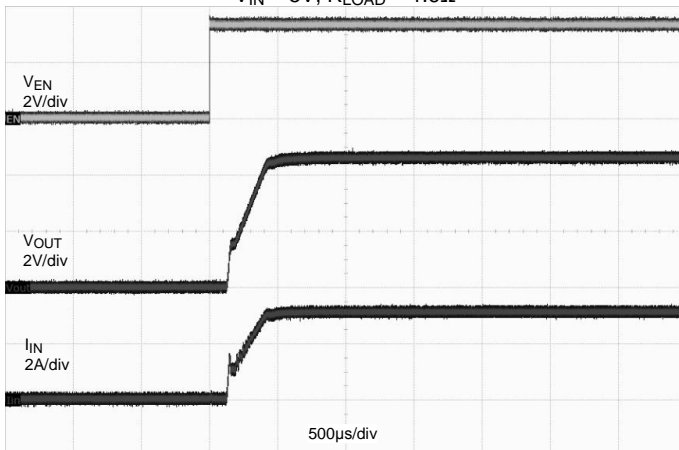


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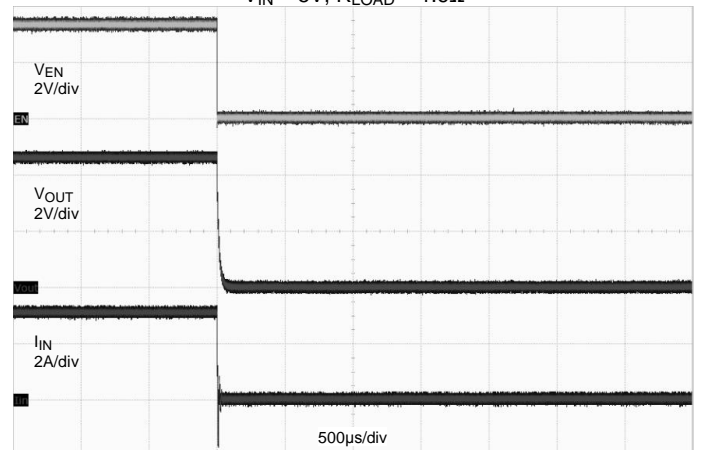
**EN Turn ON with a 1.6Ω Load**

$V_{IN} = 5\text{V}$ ,  $R_{LOAD} = 1.6\Omega$



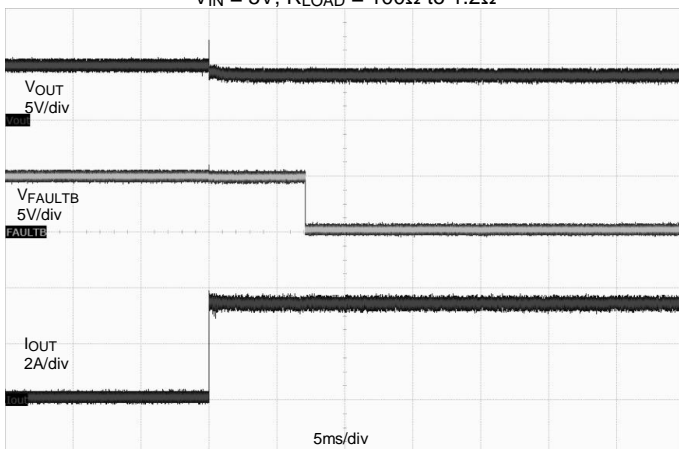
**EN Turn OFF with a 1.6Ω Load**

$V_{IN} = 5\text{V}$ ,  $R_{LOAD} = 1.6\Omega$



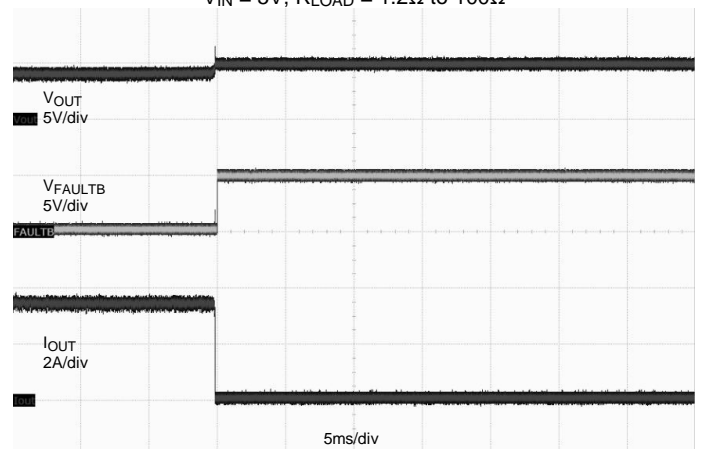
**Overcurrent Protection**

$V_{IN} = 5\text{V}$ ,  $R_{LOAD} = 100\Omega$  to  $1.2\Omega$



**Overcurrent Recovery**

$V_{IN} = 5\text{V}$ ,  $R_{LOAD} = 1.2\Omega$  to  $100\Omega$

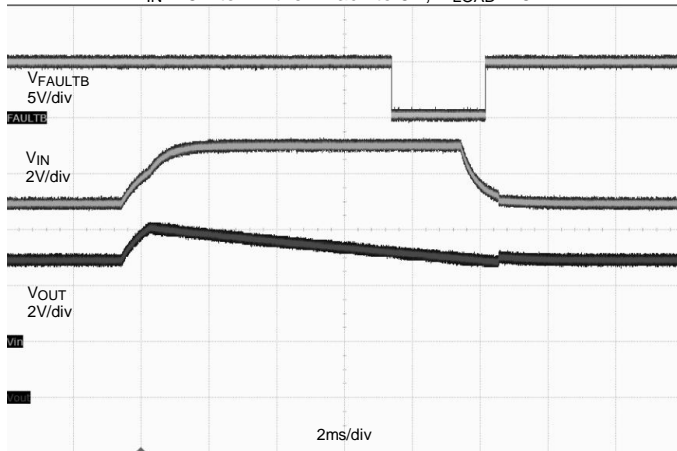




**Performance Characteristics** (@  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $C_{IN} = C_{OUT} = 10\mu\text{F}$ ,  $V_{EN} = 3.3\text{V}$ ,  $V_{FRS} = 0\text{V}$ ,  $C_{DV/DT} = 1\text{nF}$ ,  $R_{LIM} = 54.9\text{k}\Omega$ ,  $R_{LIM} = 27\text{k}\Omega$ , unless otherwise specified.) (Cont.)

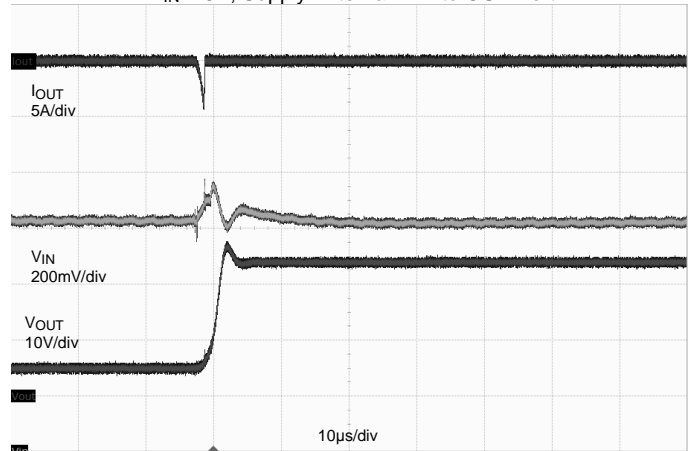
**Input OVP and Recovery**

$V_{IN} = 5\text{V}$  to  $7\text{V}$  then Back to  $5\text{V}$ ,  $R_{LOAD} = 5\text{k}\Omega$



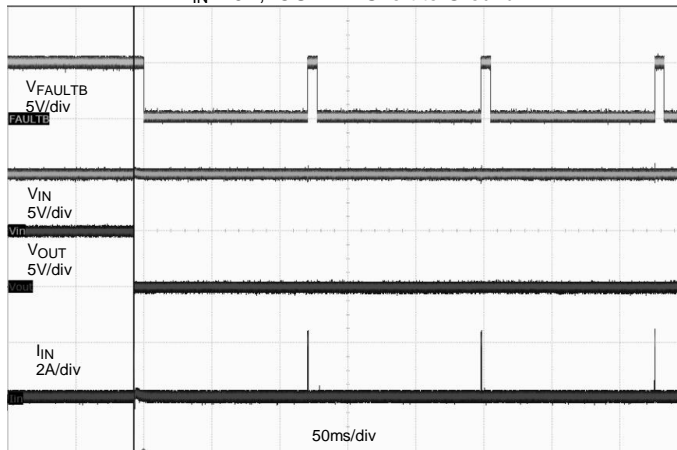
**Reverse Voltage Response**

$V_{IN} = 5\text{V}$ , Supply External  $24\text{V}$  to OUT Port



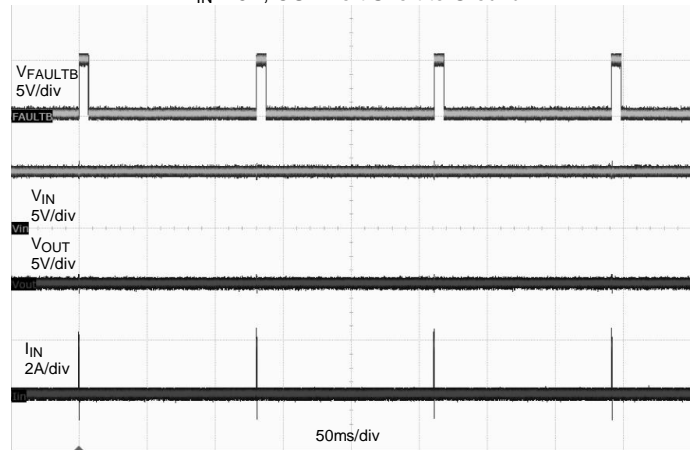
**Short Circuit Protection Auto Retry**

$V_{IN} = 5\text{V}$ , OUT Pin Short to Ground



**OUT Always Short to Ground at 5V**

$V_{IN} = 5\text{V}$ , OUT Port Short to Ground



## Application Information

### General Description

The DPS1113 is a 1-channel power switch designed to meet the input and output voltage/current requirements that are common with many hot-pluggable serial interfaces found in computing and consumer electronics equipment. For example, DPS1113 is compatible with the USB Power Delivery Specification Release 3.0, V1.0a and many popular USB Type-C™ applications.

### Start-up Time

An external capacitor connected from the DV/DT pin to GND defines the slew rate of the output voltage at power-on in the following equation.

$$dV_{OUT} / dt = (I_{DV/DT} / C_{DV/DT}) \times G_{DV/DT}$$

Where:

- $dV_{OUT} / dt$  is the desired output slew rate in V/ms
- $I_{DV/DT}$  is in  $\mu A$  and it is  $1\mu A$  typical
- $C_{DV/DT}$  is the ramp-up control setting capacitor in nF
- $G_{DV/DT}$  is the gain of DV/DT to OUT and  $G_{DV/DT} = 12$

The total ramp time  $t_{DV/DT}$  of  $V_{OUT}$  increasing from 0 to  $V_{IN}$  can be calculated using the following equation.

$$t_{DV/DT} = 8.3 \times 10^{-2} \times V_{IN} \times C_{DV/DT}$$

Where:

- $t_{DV/DT}$  is the total ramp time in ms
- $V_{IN}$  is in volts
- $C_{DV/DT}$  is nF

Choosing a proper value for the capacitor  $C_{DV/DT}$  ensures the device is turned ON with the preset ramp up imposed over the output voltage. The regulated output voltage ramp or the limited current setting limits the in-rush current at power up.

### Input Overvoltage Protection (OVP)

The voltage at the IN port is monitored continuously. The built-in OVP fault-handling mechanism triggers when the voltage at the IN port is larger than the  $V_{OVPRTH}$  value. The internal power MOSFET turns OFF to protect the downstream connected equipment. The  $V_{OVPRTH}$  value is determined by the following equation.

$$V_{OVPRTH} = 0.1 \times R_{VLIM} + 0.5$$

Where:

- $V_{OVPRTH}$  is in volts
- $R_{VLIM}$  is k $\Omega$
- $51k\Omega \leq R_{VLIM} \leq 56k\Omega$

### Reverse-Voltage Protection (RVP)

The difference in voltage ( $V_{IN} - V_{OUT}$ ) between the IN and OUT ports is monitored continuously. Once the voltage difference drops below the  $V_{RVPFTH}$  level, the device immediately turns OFF the internal power MOSFET to prevent the current flowing from the opposite direction. When the reverse-voltage condition is no longer valid, that is ( $V_{IN} - V_{OUT}$ ) becomes greater than the  $V_{RVPFTH}$  level, the internal power MOSFET must be turned ON.

### Overtemperature Protection (OTP)

During overload conditions, the output voltage drops with the limited current  $I_{LIM}$ , which results in the increasing junction temperature  $T_J$  with the increased power consumption on device. When  $T_J$  reaches the thermal shutdown threshold  $T_{SHDN}$ , the internal power MOSFET turns OFF. The internal MOSFET turns ON again once the condition [ $T_J < (T_{SHDN} - T_{HYS})$ ] occurs.

## Application Information (Cont.)

### Overcurrent Protection (OCP)

The output current is monitored continuously. Whenever the output current  $I_{OUT}$  is larger than the  $I_{LIM}$  value by over  $2\mu s$ , the embedded-OCP fault-handling mechanism triggers. This action results in the output current clamping at the  $I_{LIM}$  value hundreds of microseconds later and in the voltage dropping at the OUT port.  $R_{ILIM}$  sets the  $I_{LIM}$  value.

$$I_{LIM} = 100 / R_{ILIM}$$

Where:

- $I_{LIM}$  is in amperes,
- $R_{ILIM}$  is  $k\Omega$
- $27k\Omega \leq R_{ILIM} \leq 200k\Omega$

$R_{ILIM} (k\Omega)$	$I_{LIM} (A)$		
	Min	Typ.	Max
200	0.50	0.55	0.7
100	0.90	1.05	1.20
66.7	1.35	1.50	1.65
50	1.80	2.00	2.20
40	2.25	2.50	2.75
33.3	2.76	3.00	3.24
28.6	3.22	3.50	3.78

### Short-Circuit Protection (SCP)

There are two behaviors to protect device under short-circuit conditions. The first is fast-trip current detection. When the output current exceeds the fast-trip threshold  $I_{FASTRIP}$ , the device switches OFF the internal MOSFET.

$$I_{FASTRIP} = 1.125 \times I_{LIM} + 1.8$$

Where:

- $I_{FASTRIP}$  is in amperes
- $I_{LIM}$  is in amperes

The other behavior is low-output voltage detection. During heavy overload or short-circuit conditions, the output current is limited to  $I_{LIM}$ , and the output voltage would drop quickly. When the output voltage drop exceeds the capability of MOSFET, the power switch turns OFF. The device is operating in auto-retry mode, and the cycle time is approximately 128ms.

### Adjustable Current Monitoring Output (IMON)

A 100pF capacitor and a resistor  $R_{IMON}$  connected in parallel between the IMON pin and GND generates an average current-monitor output voltage  $V_{IMON}$ , which is proportional to the load current flowing through the device.

$$V_{IMON} = 10^{-3} \times G_{IMON} \times R_{IMON} \times I_{OUT}$$

Where:

- $G_{IMON}$  is the ratio of the IMON to the load current in  $\mu A/A$  and  $G_{IMON} = 10$
- $V_{IMON}$  is in volts
- $R_{IMON}$  is  $k\Omega$
- $I_{OUT}$  is in amperes

The resistor  $R_{IMON}$  ensures that the voltage at the IMON pin is less than 4.5V under the maximum load current  $I_{LIM}$ . For example if  $R_{IMON}$  is 100k $\Omega$ , there is a 1V output on IMON pin at 1A load, and  $V_{IMON} = 3V$  at 3A load. Connecting this IMON pin to an analog-to-digital converter (ADC) can help monitor the current information of a system.

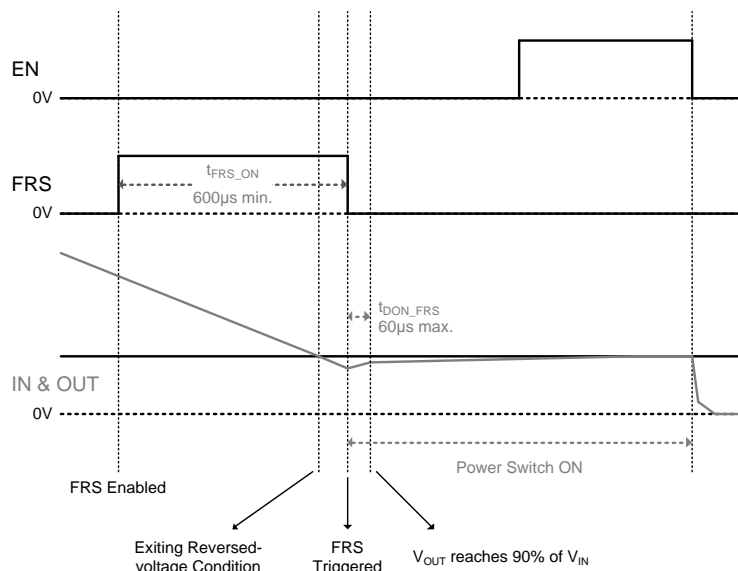
### Fault Response

An external pull-up resistor is required. The device generates a warning flag whenever one of the following fault conditions becomes valid: input overvoltage, reverse voltage, overtemperature, short circuit, overcurrent, and ILIM pin short to ground. After a de-glitch time out of 7ms, the low-active FAULTB signal must be asserted. The FAULTB signal must remain at *low*, and the internal power MOSFET remains OFF until the device exits from the exception status.

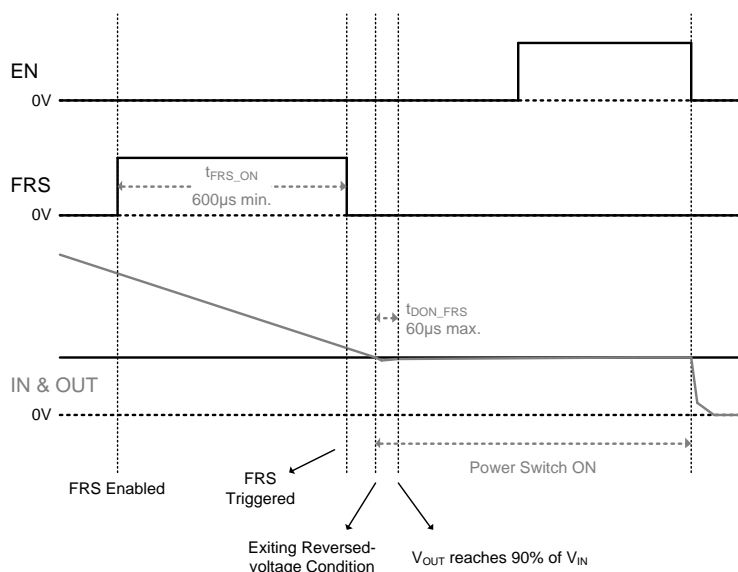
**Application Information** (Cont.)

**Support of Fast Role Swap (FRS)**

The DPS1113 supports the Fast Role Swap (FRS) operation. This operation allows the system to change its role from a power consumer to a power provider within the time limit defined in the USB Power Delivery Specification Release 3.0 V1.0a. Regardless of the voltage level at the EN pin, the relevant FRS control circuit inside the device enables at the rising edge of any positive pulse appearing at the FRS pin. When the pulse width ( $t_{FRS\_ON}$ ) is found to be larger than  $600\mu s$ , the internal power MOSFET must be turned ON within  $60\mu s$  from the falling edge of the pulse in the absence of the reverse-voltage condition. At the end of the  $60\mu s$ , the voltage level at the OUT port must be  $90\%$  of the voltage level at the IN port. Thereafter, while a subsequent rising edge at the EN pin must always be ignored, the occurrence of a falling edge disables the device. After the device shuts down, it will not resume proper operation until a rising edge appears at either the EN pin or the FRS pin.



**Figure 1. FRS Control Sequence for Fast Role Swap, Power Switch ON at Falling Edge of FRS Signal after Exiting RVP Condition**



**Figure 2. FRS Control Sequence for Fast Role Swap, Power Switch ON when Exiting RVP Condition after FRS is Triggered (Falling Edge)**

## Application Information (Cont.)

### Discharge Function

To facilitate the various applications envisioned by the system designers, the input or output port can be discharged via two external controls: DISC1, DISC2. The internal discharge resistor at each port is approximately 100Ω. The discharge paths are OFF by default with an internal 1MΩ pull-down resistor between DISC1 (or DISC2) and GND. The settings are shown in the following table.

DISC1	DISC2	Description
0	0	Discharge function disabled
0	1	OUT port is being discharged until the pin DISC2 is pulled <i>low</i>
1	0	IN port is being discharged until the pin DISC1 is pulled <i>low</i>
1	1	Both IN and OUT ports are discharged simultaneously

### Schottky Diode for Protection of Current Surge

When a cable is hot plugged in/out of the USB Type-C connector behind where the OUT port of the DPS1113 is connected, a large ground current can be seen at the OUT port of the DPS1113. When the far end of a connected cable is short to ground for whatever reason, the OUT port of the DPS1113 can also detect a large ground current. With the Schottky diode, SBR3U40P1, populated as close as possible to the USB Type-C connector, no ground current can go through the DPS1113 to cause false operation.

### Printed Circuit Board (PCB) Layout Consideration

- Place the input/output capacitors  $C_{IN}$  and  $C_{OUT}$  as close as possible to the IN and OUT pins.
- The power traces ( $V_{IN}$  trace and the  $V_{OUT}$  trace), including the power ground, is kept direct, short and wide.
- Place the resistors and capacitors ( $R_{VLIM}$ ,  $R_{ILIM}$ ,  $R_{IMON}$ ,  $C_{IMON}$ ,  $C_{DV/DT}$  and  $C_{VREG}$ ) near the device pins.
- Connect the signal ground to the GND pin, and keep a single connection from GND pin to the power ground behind the input or output capacitors.
- For better power dissipation, via holes are recommended to connect the exposed pad's landing area to a large copper polygon on the other side of the printed circuit board. The copper polygons and exposed pad of SRC (common source nodes of internal power MOSFET) must not be connected to any of the signal and power grounds on the PCB.

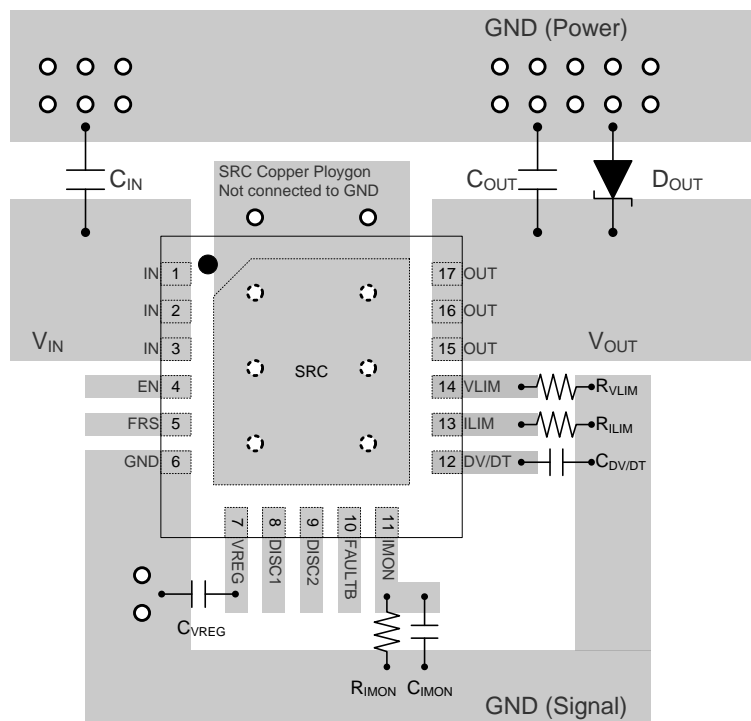
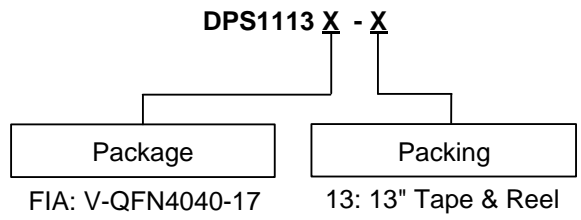


Figure 3. Suggested PCB Layout

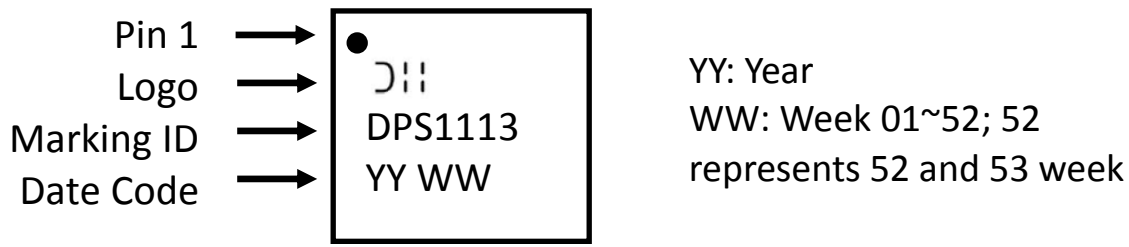
**Ordering Information** (Note 6)



Part Number	Marking ID	Reel Size (inches)	Tape Width (mm)	13" Tape and Reel	
				Quantity	Part Number Suffix
DPS1113FIA-13	DPS1113	13	12	4,000/Tape & Reel	-13

Note: 6. For packaging details, refer to <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

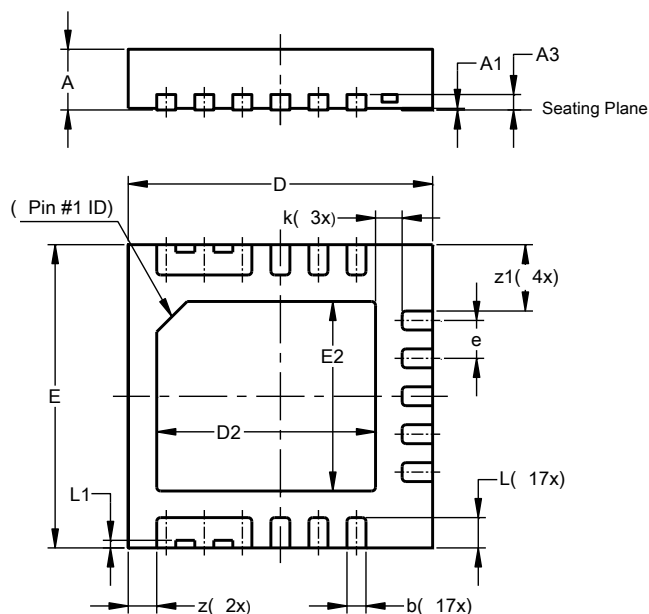
**Marking Information**



## Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

V-QFN4040-17

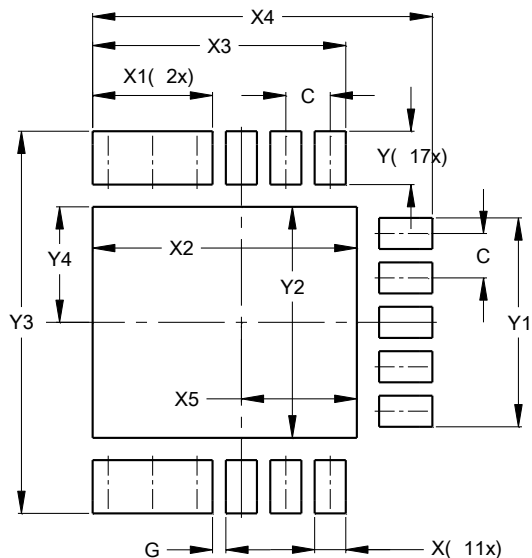


V-QFN4040-17			
Dim	Min	Max	Typ
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	-	-	0.203
b	0.20	0.30	0.25
D	3.95	4.05	4.00
D2	2.775	2.975	2.875
E	3.95	4.05	4.00
E2	2.40	2.60	2.50
e	0.50 BSC		
k	-	-	0.35
L1	-	-	0.10
L	0.35	0.45	0.40
z	-	-	0.38
z1	-	-	0.88
All Dimensions in mm			

## Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

V-QFN4040-17



Dimensions	Value (in mm)
C	0.500
G	0.150
X	0.350
X1	1.350
X2	2.975
X3	2.850
X4	3.825
X5	1.300
Y	0.600
Y1	2.350
Y2	2.600
Y3	4.300
Y4	1.300

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### Наши контакты:

**Телефон:** +7 812 627 14 35

**Электронная почта:** [sales@st-electron.ru](mailto:sales@st-electron.ru)

**Адрес:** 198099, Санкт-Петербург,  
Промышленная ул, дом № 19, литера Н,  
помещение 100-Н Офис 331