

MC74AC652, MC74ACT652

Octal Transceiver/Register with 3-State Outputs (Non-Inverting)

The MC74AC/ACT652 consists of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CAB or CBA). The four fundamental data handling functions available are illustrated in Figures 1 to 4.

- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data Transfers
- Choice of True and Inverting Data Paths
- 3-State Outputs
- 300 mil Slim Dual-in-Line Package
- Outputs Source/Sink 24 mA
- 'ACT652 Has TTL Compatible Inputs
- **These devices are available in Pb-free package(s). Specifications herein apply to both standard and Pb-free devices. Please see our website at www.onsemi.com for specific Pb-free orderable part numbers, or contact your local ON Semiconductor sales office or representative.**

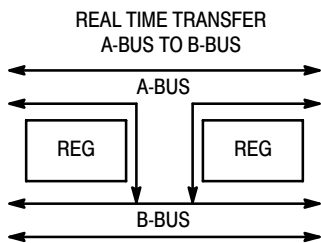


Figure 1.

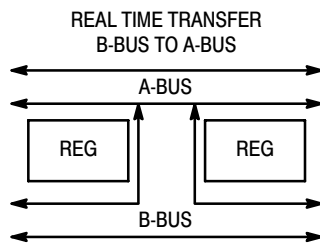


Figure 2.

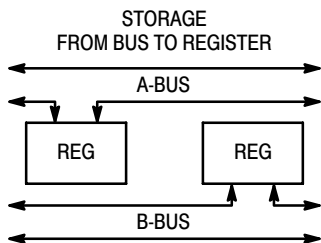


Figure 3.

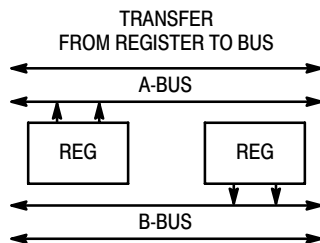
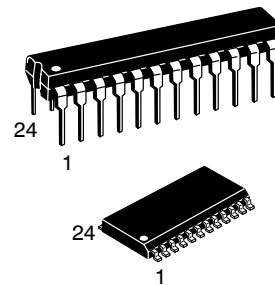


Figure 4.



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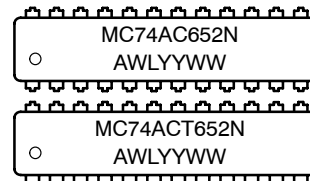


PDIP-24
N SUFFIX
CASE 724

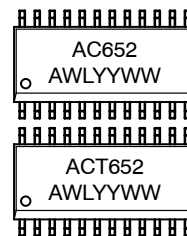
SO-24
DW SUFFIX
CASE 751E

MARKING DIAGRAMS

PDIP-24



SO-24

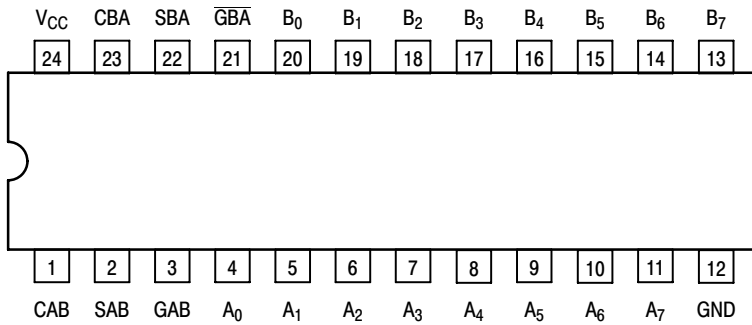


A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74AC652N	PDIP-24	15 Units/Rail
MC74ACT652N	PDIP-24	15 Units/Rail
MC74AC652DW	SOIC-24	30 Units/Rail
MC74AC652DWR	SOIC-24	1000 Tape & Reel
MC74ACT652DW	SOIC-24	30 Units/Rail
MC74ACT652DWR2	SOIC-24	1000 Tape & Reel

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PIN ASSIGNMENT

PIN	FUNCTION
A ₀ -A ₇	Data Register A Inputs Data Register A Outputs
B ₀ -B ₇	Data Register B Inputs Data Register B Outputs
CAB, CBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
GAB, GBA	Output Enable Inputs

Figure 5. Pinout: 24-Lead Plastic Package (Top View)

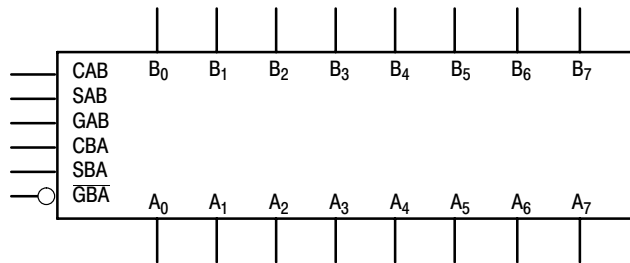
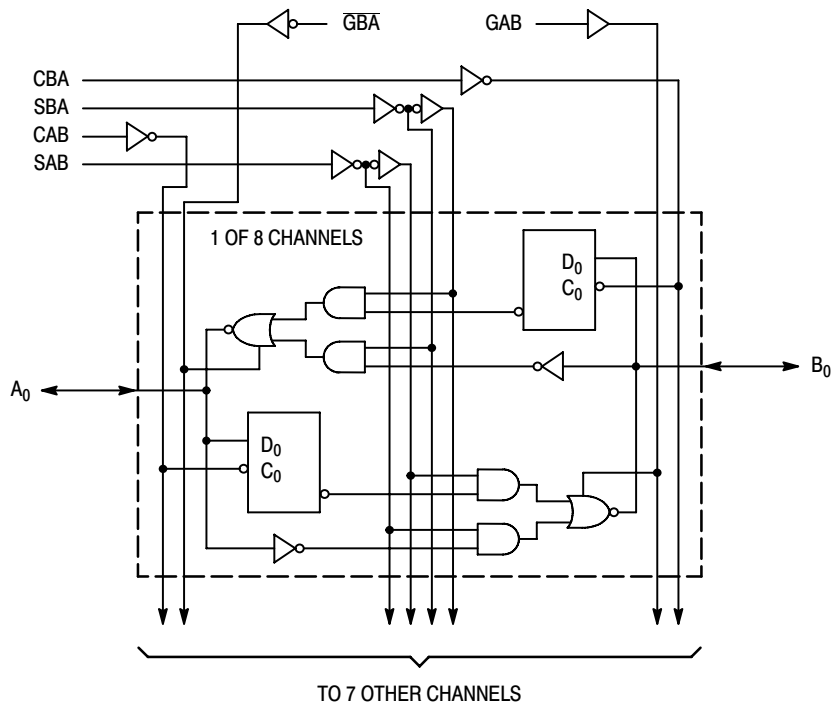


Figure 6. Logic Symbol



NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 7. Logic Diagram

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FUNCTION TABLE

Inputs						Data I/O*		Operation or Function
GAB	$\overline{\text{GBA}}$	CAB	CBA	SAB	SBA	A ₀ – A ₇	B ₀ – B ₇	
L	H	H or L	H or L	X	X	Input	Input	Isolation Store A and B Data
L	H	↑	↑	X	X			
X	H	↑	H or L	X	X	Input	Unspecified* Output	Store A, Hold B Store A in Both Registers
H	H	↑	↑	X**	X			
L	X	H or L	↑	X	X	Unspecified* Output	Input	Hold A, Store B Store B in Both Registers
L	L	↑	↑	X	X**			
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus Stored B Data to A Bus
L	L	X	H or L	X	H			
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus Stored A Data to B Bus
H	H	H or L	X	H	X			
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

*The data output functions may be enabled or disabled by various signals at the $\overline{\text{GBA}}$ and GAB inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

**Select control = L: clocks can occur simultaneously.

H = HIGH Voltage Level; L = LOW Voltage Level; X = Immaterial; ↑ = LOW-to-HIGH Transition

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	–0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	–0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Sink/Source Current, per Pin	±50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	±50	mA
T _{stg}	Storage Temperature	–65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
V _{CC}	Supply Voltage	'AC	2.0	5.0	6.0	V
		'ACT	4.5	5.0	5.5	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Ref. to GND)	0	–	V _{CC}	V	
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	–	150	–	ns/V
		V _{CC} @ 4.5 V	–	40	–	
		V _{CC} @ 5.5 V	–	25	–	
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	–	10	–	ns/V
		V _{CC} @ 5.5 V	–	8.0	–	
T _J	Junction Temperature (PDIP)	–	–	140	°C	
T _A	Operating Ambient Temperature Range	–40	25	85	°C	
I _{OH}	Output Current — HIGH	–	–	–24	mA	
I _{OL}	Output Current — LOW	–	–	24	mA	

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.

2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC	Unit	Conditions
			T _A = +25°C		T _A = -40°C to +85°C		
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = - 50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0	-	2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} - 12 mA I _{OH} - 24 mA - 24 mA
		4.5	-	3.86	3.76		
		5.5	-	4.86	4.76		
V _{OL}	Minimum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0	-	0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
		4.5	-	0.36	0.44		
		5.5	-	0.36	0.44		
I _{IN}	Maximum Input Leakage Current	5.5	-	±0.1	±1.0	μA	V _I = V _{CC} , GND
I _{OZT}	Maximum 3-State Current	5.5	-	±0.6	±6.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5	-	-	75	mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5	-	-	-75	mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	-	8.0	80	μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one input loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V.

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AC CHARACTERISTICS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Unit
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Min	Max	Min	Max	
t _{PLH}	Propagation Delay CPBA or CPAB to A _n or B _n	3.0	4.0	17.0	3.0	19.0	ns
		5.0	2.5	12.0	2.0	14.0	
t _{PHL}	Propagation Delay CPBA or CPAB to A _n or B _n	3.0	3.0	14.5	2.5	16.5	ns
		5.0	2.0	10.5	1.5	12.0	
t _{PLH}	Propagation Delay A or B to B _n or A _n	3.0	3.0	14.0	2.5	16.0	ns
		5.0	2.0	9.5	1.5	11.0	
t _{PHL}	Propagation Delay A or B to B _n or A _n	3.0	2.5	13.0	2.0	15.0	ns
		5.0	1.5	9.0	1.0	10.5	
t _{PLH}	Propagation Delay SBA or SAB to A _n or B _n	3.0	3.0	14.0	2.5	16.0	ns
		5.0	2.5	10.0	2.0	11.5	
t _{PHL}	Propagation Delay SBA or SAB to A _n or B _n	3.0	2.5	13.5	2.0	15.5	ns
		5.0	2.0	10.0	1.5	11.5	
t _{PZH}	Output Enable Time OEBA to A _n	3.0	2.5	12.0	2.0	13.5	ns
		5.0	1.5	9.0	1.0	10.0	
t _{PZL}	Output Enable Time OEBA to A _n	3.0	2.5	12.0	2.0	14.0	ns
		5.0	1.5	9.0	1.0	10.5	
t _{PHZ}	Output Disable Time OEBA to A _n	3.0	3.0	13.0	2.5	14.0	ns
		5.0	2.0	11.0	1.5	12.0	
t _{PLZ}	Output Disable Time OEBA to A _n	3.0	2.5	12.5	2.0	14.0	ns
		5.0	2.0	10.5	1.5	12.0	

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

MC74AC652, MC74ACT652

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Unit	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4		V	I _{OUT} = - 50 μA
		5.5	5.49	5.4	5.4			
		4.5	-	3.86	3.76		V	*V _{IN} = V _{IL} or V _{IH} - 24 mA I _{OH} - 24 mA
		5.5	-	4.86	4.76			
V _{OL}	Minimum Low Level Output Voltage	4.5	0.001	0.1	0.1		V	I _{OUT} = - 50 μA
		5.5	0.001	0.1	0.1			
		4.5	-	0.36	0.44		V	*V _{IN} = V _{IL} or V _{IH} - 24 mA I _{OH} - 24 mA
		5.5	-	0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5	-	±0.1	±1.0		μA	V _I = V _{CC} , GND
ΔI _{CC}	Additional Max. I _{CC} /Input	5.5	0.6	-	1.5		mA	V _I = V _{CC} - 2.1 V
I _{OZT}	Maximum 3-State Current	5.5	-	±0.6	±6.0		μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5	-	-	75		mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5	-	-	-75		mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	-	8.0	80		μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one input loaded at a time.

MC74AC652, MC74ACT652

AC CHARACTERISTICS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT		Unit
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Min	Max	Min	Max	
t _{PLH}	Propagation Delay CPBA or CPAB to A _n or B _n	5.0	4.0	14.5	3.5	16.5	ns
t _{PHL}	Propagation Delay CPBA or CPAB to A _n or B _n	5.0	3.5	14.5	3.0	16.5	ns
t _{PLH}	Propagation Delay A or B to B _n or A _n	5.0	2.5	11.5	2.0	13.0	ns
t _{PHL}	Propagation Delay A or B to B _n or A _n	5.0	2.5	11.5	2.0	13.0	ns
t _{PLH}	Propagation Delay SBA or SAB to A _n or B _n	5.0	2.5	12.0	2.0	13.5	ns
t _{PHL}	Propagation Delay SBA or SAB to A _n or B _n	5.0	3.0	12.0	2.5	13.5	ns
t _{PZH}	Output Enable Time OEBA to A _n	5.0	2.0	11.5	1.5	13.0	ns
t _{PZL}	Output Enable Time OEBA to A _n	5.0	2.5	11.5	2.0	13.0	ns
t _{PHZ}	Output Disable Time OEBA to A _n	5.0	3.0	13.0	2.5	14.0	ns
t _{PLZ}	Output Disable Time OEBA to A _n	5.0	2.5	12.5	2.0	14.0	ns
t _{PZH}	Output Enable time OEAB to B _n	5.0	2.5	12.0	2.0	13.5	ns
t _{PZL}	Output Enable Time OEAB to B _n	5.0	2.5	12.0	2.0	13.5	ns
t _{PHZ}	Output Enable Time OEAB to B _n	5.0	3.5	13.5	3.0	14.5	ns
t _{PLZ}	Output Enable Time OEAB to B _n	5.0	3.0	13.5	2.5	15.0	ns
t _s	Setup Time, HIGH or LOW A _n or B _n to CPBA or CPAB	5.0	7.0	-	8.0	-	ns
t _h	Hold Time, HIGH or LOW A _n or B _n to CPBA or CPAB	5.0	2.5	-	2.5	-	ns
t _w	CPAB, CPBA Pulse Width HIGH or LOW	5.0	6.0	-	7.0	-	ns

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

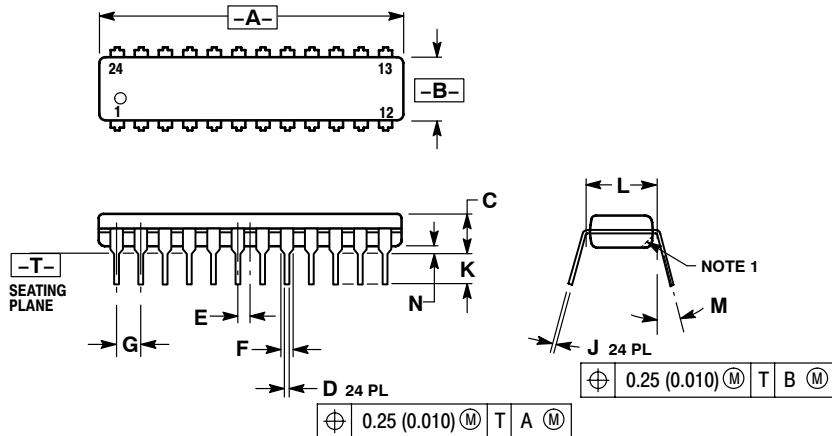
CAPACITANCE

Symbol	Parameter	74ACT Typ	Unit	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{I/O}	Input/Output Capacitance	15	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	60.0	pF	V _{CC} = 5.0 V

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PACKAGE DIMENSIONS

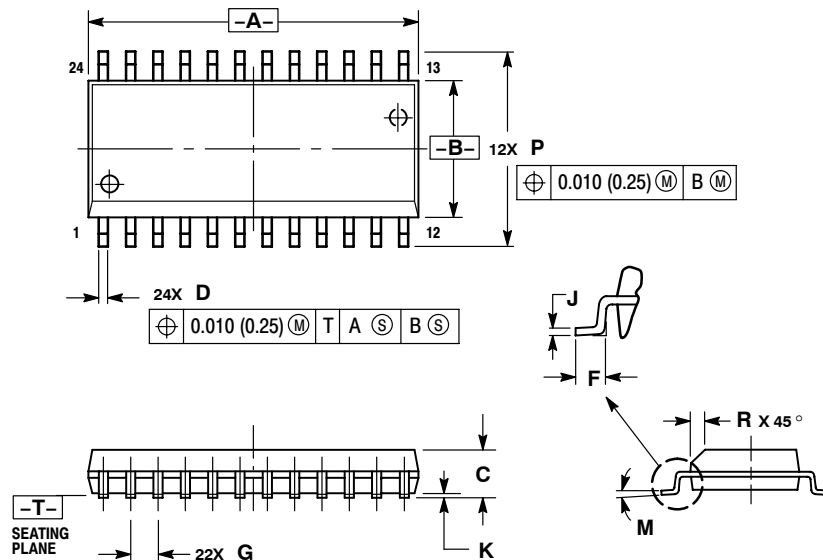
PDIP-24 N SUFFIX 24 PIN PLASTIC DIP PACKAGE CASE 724-03 ISSUE D



- NOTES:
 1. CHAMFERED CONTOUR OPTIONAL.
 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 4. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.230	1.265	31.25	32.13
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.020	0.38	0.51
E	0.050 BSC		1.27 BSC	
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
J	0.007	0.012	0.18	0.30
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0° 15°		0° 15°	
N	0.020	0.040	0.51	1.01

SO-24 DW SUFFIX 24 PIN PLASTIC SOIC PACKAGE CASE 751E-04 ISSUE E



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0° 8°		0° 8°	
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

Notes

Notes

Notes

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