Spread Spectrum Frequency Timing Generator

Features

- **Maximized EMI suppression using Cypress's Spread Spectrum technology**
- **Generates a spread spectrum copy of the provided input**
- **Integrated loop filter components**
- **Operates with a 5V supply**
- **Low power CMOS design**
- **Available in 8-pin SOIC (Small Outline Integrated Circuit)**

Overview

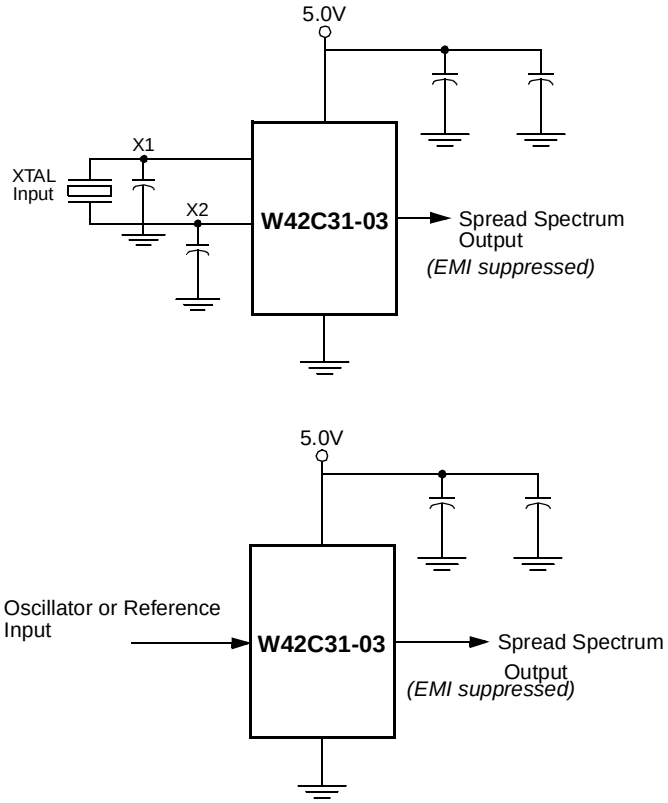
The W42C31-03 incorporates the latest advances in PLL spread spectrum frequency synthesizer techniques. By frequency modulating the output with a low-frequency carrier, EMI is greatly reduced. Use of this technology allows systems to pass increasingly difficult EMI testing without resorting to costly shielding or redesign.

In a system, not only is EMI reduced in the various clock lines, but also in all signals which are synchronized to the clock. Therefore, the benefits of using this technology increase with the number of address and data lines in the system. The Simplified Block Diagram shows a simple implementation.

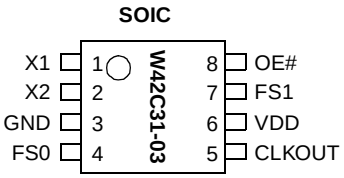
Table 1. Frequency Spread Selection

W42C31-03		Oscillator Input Frequency (MHz)	XTAL Input Frequency (MHz)	Output Frequency (MHz)
FS1	FS0			
0	0	10 to 20	10 to 20	f_{IN} ±1.875%
0	1	10 to 20	10 to 20	f_{IN} ±1.0%
1	0	20 to 33	20 to 25	f_{IN} ±1.875%
1	1	20 to 33	20 to 25	f_{IN} –2.0%

Simplified Block Diagram



Pin Configuration



Pin Definitions

Pin Name	Pin No.	Pin Type	Pin Description
CLKOUT	5	O	***Output Modulated Frequency***: Frequency modulated copy of the unmodulated input clock
X1	1	I	***Crystal Connection or External Reference Frequency Input:*** This pin has dual functions. It may either be connected to an external crystal, or to an external reference clock.
X2	2	I	***Crystal Connection:*** If using an external reference, this pin must be left unconnected.
OE#	8	I	***Output Enable (Active LOW):*** This pin three-states the output when HIGH. It has an internal pull-down resistor.
FS0	4	I	***Frequency Selection Bit 0:*** This pin selects the frequency spreading characteristics. Refer to *Table 1*. This pin has a pull-up resistor.
FS1	7	I	***Frequency Selection Bit 1:*** This pin selects the frequency range. Refer to *Table 1*. This pin has a pull-up resistor.
VDD	6	P	***Power Connection:*** Connected to 5V power supply.
GND	3	G	***Ground Connection:*** This should be connected to the common ground plane.

Functional Description

The W42C31-03 uses a phase-locked loop (PLL) to frequency modulate an input clock. The result is an output clock whose frequency is slowly swept over a narrow band near the input signal. The basic circuit topology is shown in *Figure 1*. An on-chip crystal driver causes the crystal to oscillate at its fundamental. The resulting reference signal is divided by Q and fed to the phase detector. A signal from the VCO is divided by P and fed back to the phase detector also. The PLL will force the frequency of the VCO output signal to change until the divided output signal and the divided reference signal match at the phase detector input. The output frequency is then equal to the ratio of P/Q times the reference frequency. The unique feature of the Spread Spectrum Clock Generator is that a modulating waveform is superimposed at the input to the VCO. This causes the VCO output to be slowly swept across a predetermined frequency band.

Because the modulating frequency is typically 1000 times slower than the fundamental clock, the spread spectrum process has little impact on system performance.

Frequency Selection With SSFTG

In Spread Spectrum Frequency Timing Generation, EMI reduction depends on the shape, modulation percentage, and frequency of the modulating waveform. While the shape and frequency of the modulating waveform are fixed, the modulation percentage may be varied.

Using frequency select bits (FS1:0 pins), various spreading percentages can be chosen (see *Table 1*).

A larger spreading percentage improves EMI reduction. However, large spread percentages may either exceed system maximum frequency ratings or lower the average frequency to a point where performance is affected. For these reasons, spreading percentages between ±0.5% and ±2.5% are most common.

The W42C31 features the ability to select from various spread spectrum characteristics. Selections specific to the W42C31-03 are shown in *Table 1*. Other spreading characteristics are available (see separate data sheets) or can be created with a custom mask.

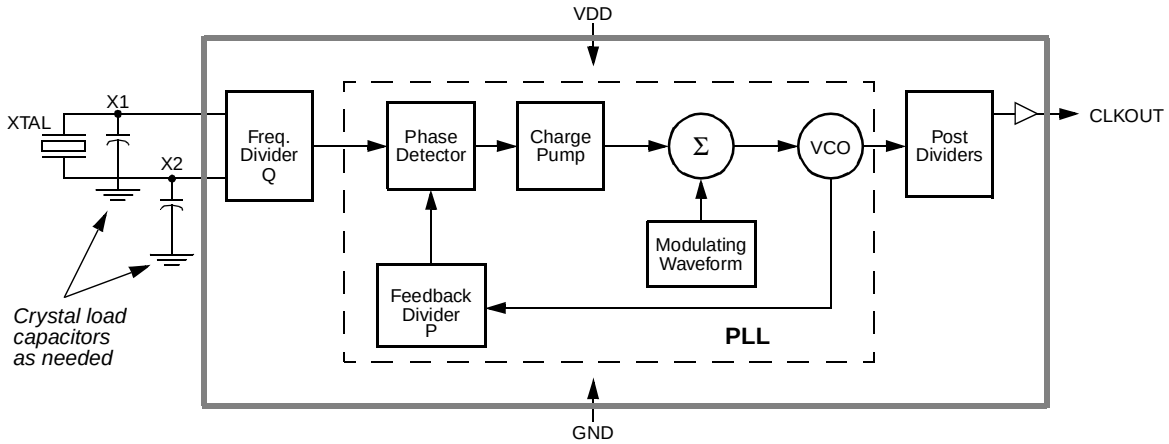


Figure 1. System Block Diagram

Spread Spectrum Frequency Timing Generation

The benefits of using Spread Spectrum Frequency Timing Generation are depicted in *Figure 2*. An EMI emission profile of a clock harmonic is shown.

Contrast the typical clock EMI with the Cypress Spread Spectrum Frequency Timing Generation EMI. Notice the spike in the typical clock. This spike can make systems fail quasi-peak EMI testing. The FCC and other regulatory agencies test for peak emissions. With spread spectrum enabled, the peak energy is much lower (at least 8 dB) because the energy is spread out across a wider bandwidth.

Modulating Waveform

The shape of the modulating waveform is critical to EMI reduction. The modulation scheme used to accomplish the maximum reduction in EMI is shown in *Figure 3*. The period of the modulation is shown as a percentage of the period length along the X axis. The amount that the frequency is varied is shown along the Y axis, also shown as a percentage of the total frequency spread.

Cypress frequency selection tables express the modulation percentage in two ways. The first method displays the spreading frequency band as a percent of the programmed average output frequency, symmetric about the programmed average frequency. This method is always shown using the expression $f_{Center} \pm X_{MOD}\%$ in the frequency spread selection table.

The second approach is to specify the maximum operating frequency and the spreading band as a percentage of this frequency. The output signal is swept from the lower edge of the band to the maximum frequency. The expression for this approach is $f_{MAX} - X_{MOD}\%$. Whenever this expression is used, Cypress has taken care to ensure that f_{MAX} will never be exceeded. This is important in applications where the clock drives components with tight maximum clock speed specifications.

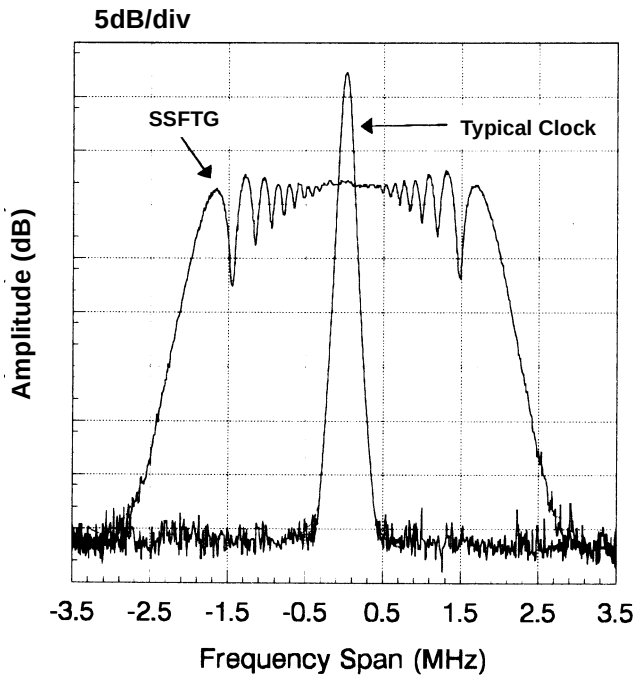


Figure 2. Typical Clock and SSFTG Comparison

OE# Pin

An internal pull-down resistor defaults the chip into a mode in which all outputs are active. If OE# goes HIGH, all outputs are three-stated. The chip will not prevent short cycles in a transition from three-state to enabled.

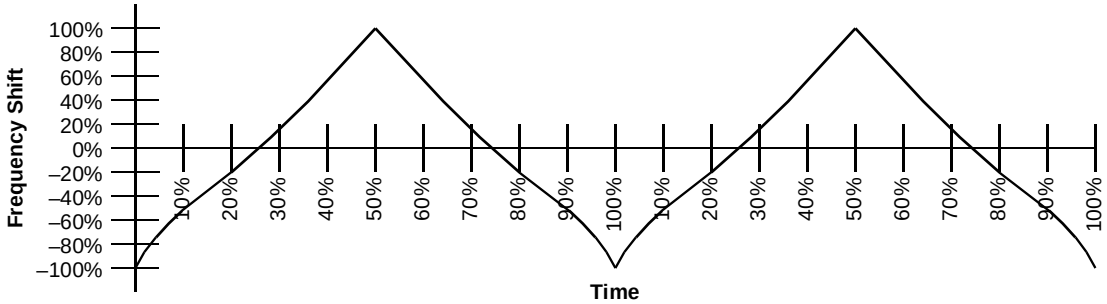


Figure 3. Modulation Waveform Profile

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
P_D	Power Dissipation	0.5	W

DC Electrical Characteristics: 0°C < T_A < 70°C, V_{DD} = 5V ±10%

Parameter	Description	Test Condition	Min	Typ	Max	Unit
I_{DD}	Supply Current			18	32	mA
t_{ON}	Power Up Time	First locked clock cycle after Power Good			5	ms
V_{IL}	Input Low Voltage				$0.15V_{DD}$	V
V_{IH}	Input High Voltage		$0.7V_{DD}$			V
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Output High Voltage		2.5			V
I_{IL}	Input Low Current	Note 1			–100	µA
I_{IH}	Input High Current	Note 1			10	µA
I_{OL}	Output Low Current	@ 0.4V, V_{DD} = 5V		24		mA
I_{OH}	Output High Current	@ 2.4V, V_{DD} = 5V		24		mA
C_I	Input Capacitance	All pins except X1, X2			7	pF
C_L	Load Capacitance (as seen by XTAL)	Pins X1, X2[2]		17		pF
R_P	Input Pull-Up Resistor			500		kΩ
Z_{OUT}	Clock Output Impedance			20		Ω

AC Electrical Characteristics: T_A = 0°C to +70°C, V_{DD} = 5V±10%

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
f_{IN}	Input Frequency	Input Clock	10		33	MHz
f_{OUT}	Output Frequency		10		33	MHz
t_R	Output Rise Time	V_{DD}, 15-pF load 0.8–2.4		2	5	ns
t_F	Output Fall Time	V_{DD}, 15-pF load 2.4–0.8		2	5	ns
t_{OD}	Output Duty Cycle	15-pF load	45		55	%
t_{ID}	Input Duty Cycle		40		60	%
t_{JCYC}	Jitter, Cycle-to-Cycle				300	ps
	Harmonic Reduction		8			dB

Notes:

1. Inputs FS1:0 have a pull-up resistor; Input OE# has a pull-down resistor.
2. Pins X1 and X2 each have a 34-pF capacitance. When used with a XTAL, the two capacitors combined load the crystal with 17 pF. If driving X1 with a reference clock signal, the load capacitance will be 34 pF (typical).

Application Information

Recommended Circuit Configuration

For optimum performance in system applications the power supply decoupling scheme shown in *Figure 4* should be used.

V_{DD} decoupling is important to both reduce phase jitter and EMI radiation. The 0.1-µF decoupling capacitor should be placed as close to the V_{DD} pin as possible, otherwise the increased trace inductance will negate its decoupling capability.

The 10-µF decoupling capacitor shown should be a tantalum type. For further EMI protection, the V_{DD} connection can be made via a ferrite bead, as shown.

The 6-pF XTAL load capacitors can be used to raise the integrated 17-pF capacitance up to a total load of 20 pF on the crystal.

Recommended Board Layout

Figure 5 shows a recommended 2-layer board layout.

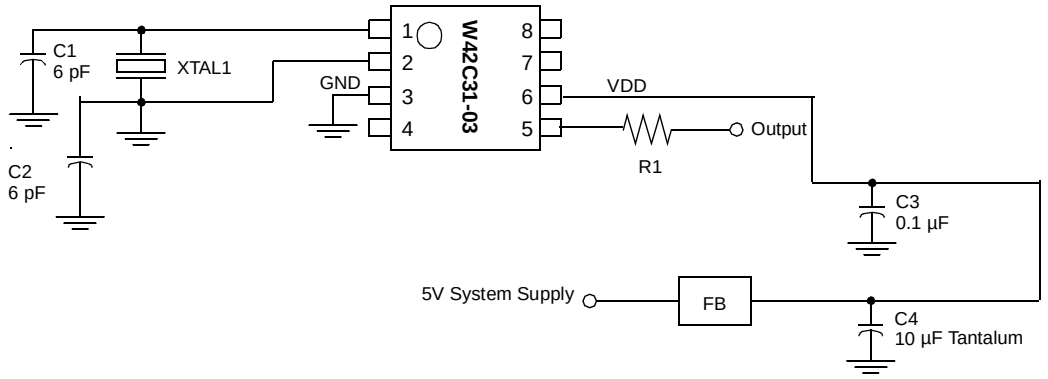


Figure 4. Recommended Circuit Configuration

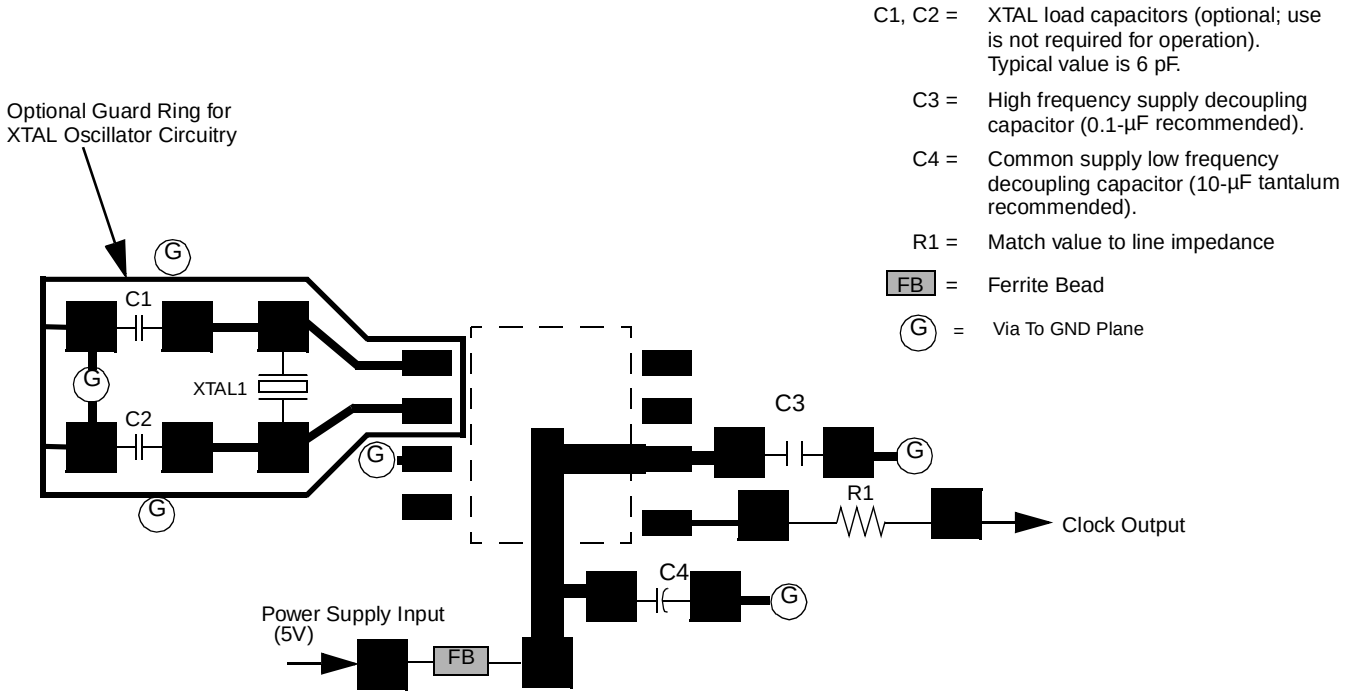


Figure 5. Recommended Board Layout (2-Layer Board)

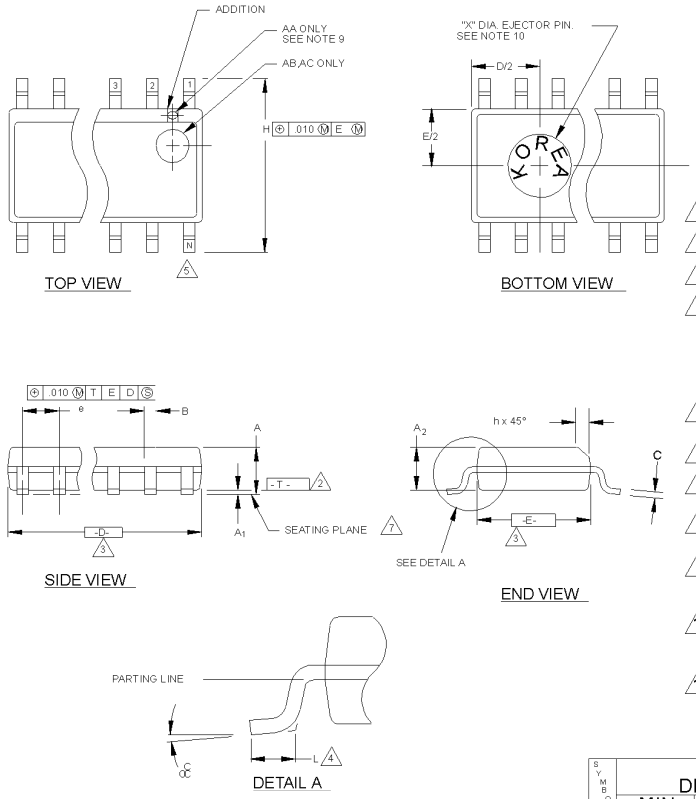
Ordering Information

Ordering Code	Freq. Mask Code	Package Name	Package Type
W42C31	03	G	8-pin Plastic SOIC (150-mil)

Document #: 38-00802

Package Diagram

8-Pin Small Outline Integrated Circuit (SOIC, 150-mil)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .015.
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. THE APPEARANCE OF PIN #1 I.D ON THE 8 LD IS OPTIONAL, ROUND TYPE ON SINGLE LEADFRAME AND RECTANGULAR TYPE ON MATRIX LEADFRAME.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPEND ON ASSEMBLY LOCATION.
11. CONTROLLING DIMENSION: INCHES.

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARI-ATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	.061	.064	.068		AA	.189	.194	.196	8
A_1	.004	.006	.0098		AB	.337	.342	.344	14
A_2	.055	.058	.061		AC	.386	.391	.393	16
B	.0138	.016	.0192						
C	.0075	.008	.0098						
D	SEE VARIATIONS			3					
E	.150	.155	.157						
e	.050 BSC								
H	.230	.236	.244						
h	.010	.013	.016						
L	.016	.025	.035						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	.085	.093	.100						

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARI-ATIONS	3 D			5 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	1.55	1.63	1.73		AA	4.80	4.93	4.98	8
A_1	0.127	0.15	0.25		AB	8.58	8.69	8.74	14
A_2	1.40	1.47	1.55		AC	9.80	9.93	9.98	16
B	0.35	0.41	0.49						
C	0.19	0.20	0.25						
D	SEE VARIATIONS			3					
E	3.81	3.94	3.99						
e	1.27 BSC								
H	5.84	5.99	6.20						
h	0.25	0.33	0.41						
L	0.41	0.64	0.89						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
X	2.16	2.36	2.54						

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